17-V Input, 6-A, Synchronous Step-Down DC-DC Voltage Converter

Features

- Ultra-low $R_{DS(ON)}$ 18-mΩ and 15-mΩ MOSFETs
- 200-kHz to 1.6-MHz Adjustable Switching Frequency
- Integrated PLL to Synchronize with External Clock
- Adjustable UVLO Voltage and Hysteresis
- Under-voltage and Over-voltage Power Good Output
- Adjustable Soft-Start and Sequencing
- Full-Current Range Low-dropout Operation
- Hiccup Current Limit
- 0.6-V (TPP206080) / 0.8-V (TPP206081) 1% Internal Voltage Reference
- 14-Pin QFN3.5X3.5-14 with Exposed Pad Package
- −40°C to 125°C Ambient Temperature Range

Applications

- 5-V, 12-V Industrial Power Application
- High-Density Point-of-Load Regulation
- Telecom & Communication Equipment Power Applications

Description

The TPP20608x is a series of 17-V, 6-A output, synchronous, step-down, switch-mode converters with integrated power MOSFETs.

The TPP20608x series employs current mode control supporting simple external compensation and flexible component selection. With the integrated phase-locked loop, the TPP20608x series can synchronize with external clock source with wide frequency selection, optimized for efficiency, physical dimensions, and electromagnetic interference (EMI).

Protection and diagnostics features protect the device as well as the system power supply. By using open-drain power-good output, the system is able to distinguish if the output supply is within the target voltage range. Soft-start features, which control the output ramping, can be set independently by an external resistor or to sequencing/tracking mode. Current-limit and over-temperature protection improve system-level robustness.

Typical Application Circuit

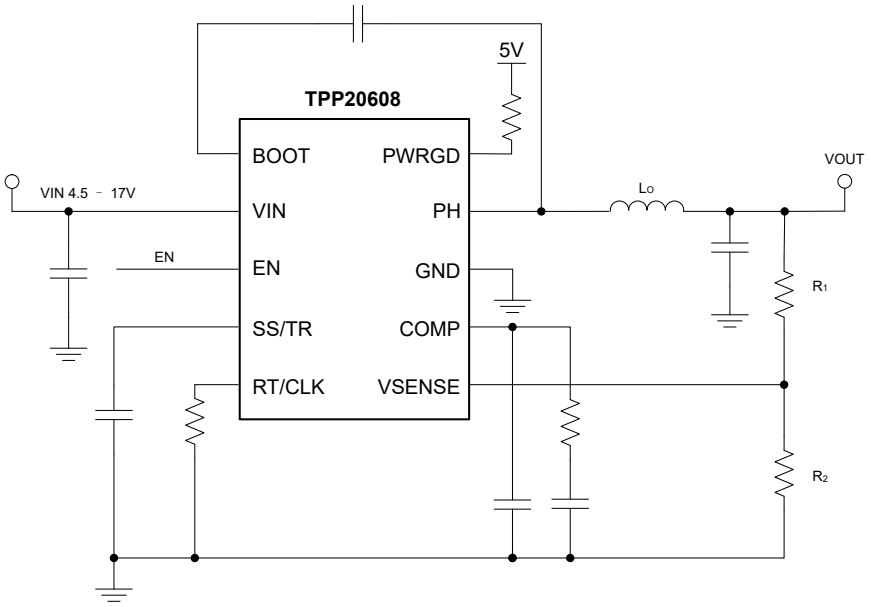


Table of Contents

Revision History

Date	Revision	Notes
2022-11-28	Rev.A.0	Initial revision.
2023-04-24	Rev.A.1	Updated TPP206081 reference voltage and minor fix.
2023-11-07	Rev.A.2	Misc. update on package and reel infomation

Pin Configuration and Functions

TPP20608
QFN3.5X3.5-14 Package
Top View

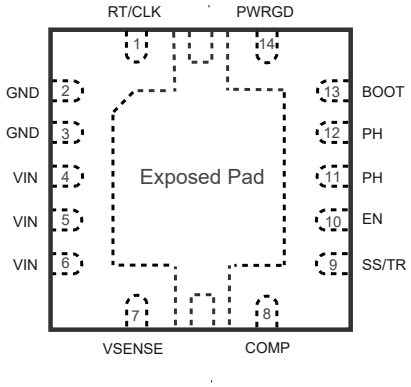


Table 1. Pin Functions: TPP36208

Pin	Name	I/O	Description
BOOT	13		Bootstrap capacitor between BOOT and PH. Recommend using a 0.1-μF ceramic capacitor with a 10-V or higher voltage rating.
COMP	8		Error amplifier output and input to the PWM comparator. Connect the frequency compensation network to this pin.
EN	10		Device enable pin with internal pull-up current source. Threshold can be increased via external resistors.
GND	2, 3		Device ground pin.
PH	11, 12		Switching node.
PWRGD	14		Open-drain power-good output.
RT/CLK	1		Frequency selection and external clock input. When using it as frequency setting mode, an external connected resistor sets the switching frequency; When using it as clock synchronization input, the input is a high impedance clock input for internal PLL.
SS/TR	9		Soft-start and tracking input. When using the soft-start mode, an external capacitor connected to this pin sets output ramping time; When using track/sequence mode, the voltage on this pin overrides the internal voltage reference thus setting the output voltage.
VIN	4, 5, 6		Supply voltage with 4.5-V to 17-V operating range.
VSENSE	7		Feedback input, connected to the internal inverting input of gm error amplifier.
Exposed Pad	15		Device exposed pad must be connected to GND with heat sink area for thermal dissipation.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{IN}	Supply Voltage	−0.3	20	V
PH	Switching Node Voltage	−1	20	V
PH 5-ns Transient	Switching Node Voltage	−4	20	V
PH 10-ns Transient	Switching Node Voltage	−3	20	V
BOOT-PH	Bootstrap Voltage	−0.3	6.5	V
VSENSE	Feedback Voltage	−0.3	3	V
COMP	Compensation	−0.3	3	V
EN	Enable Input	−0.3	6	V
PWRGD	Power Good	−0.3	6	V
SS/TR		−0.3	3	V
RT/CLK		−0.3	6	V
T_J	Maximum Junction Temperature		150	°C
T_A	Operating Junction Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 300 mV beyond the power supply, the input current should be limited to less than 10 mA.
(3) A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
V_{IN}	Input Voltage	4.5		17	V
I_{OUT}	Output Current			6	A
T_J	Operating Junction Temperature	−40		150	℃

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
QFN3.5X3.5-14	30.8	39.1	°C/W

Electrical Characteristics

All test condition is at V_{IN} = 4.5 V to 17 V, T_j = −40°C to +125°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Power Supply						
V_{IN}	Operating Voltage Range		4.5		17	V
$V_{(UVLO)}$	Internal Undervoltage Lockout Threshold	Rising Threshold		4	4.5	V
$V_{(UVLO,hys)}$				150		mV
I_Q	Quiescent Supply Current	EN = 5 V, T_A = 25 °C, $V_{(VSENSE)}$ = 0.81 V, TPP206080		1.1	1.7	mA
I_{QSD}	Shut-down Supply Current	EN = 0 V, T_A = 25 °C		2	5	μA
VSENSE Voltage						
$V_{(VSENSE)}$	VSENSE Voltage	TPP206080	0.594	0.6	0.606	V
		TPP206081	0.792	0.8	0.808	V
MOSFFET						
H_{SRDSON}	HS Switching on Resistance	VIN = 12 V, BOOT − SW = 6 V		18	32	mΩ
L_{SRDSON}	LS Switching on Resistance	VIN = 12 V		15	28	mΩ
Current Limit						
$I_{Limit-HS}$	High-side Switch Current Limit Threshold		8	11	14	A
$I_{Limit-LS-source}$	Low-side Switch Sourcing Current Limit Threshold		6.5	10	15	A
$I_{Limit-LS-sink}$	Low-side Switch Sinking Current Limit Threshold		2	3	4	A
$N_{Hiccup-deg}$	Number of Clock Cycle for Hiccup Deglitch			512		Cycles
$N_{Hiccup-prot}$	Number of Clock Cycle for Hiccup Protection			16384		Cycles
Error Amplifier						
$I_{(SENSE)}$	Input Current			1		nA
g_m	Error Amplifier Transconductance	−2 μA < I_{COMP} < 2 μA, V_{COMP} = 1 V		1300		μMhos
ADC	Error Amplifier Gain	$V_{(FB)}$ = 0.8 V		86		V/V
$I_{(COMP)}$	Error Amplifier Output Current Capability	$V_{(COMP)}$ = 1 V , 100mV overdrive		±130		μA
$g_{COMP-SW}$	COMP to SW Current Transconductance			16		A/V

Parameter		Conditions	Min	Typ	Max	Unit
Thermal Shutdown						
T_{SD}	Thermal Shut-down Temperature			175		°C
T_{HYS}	Thermal Hysteresis			15		°C
Power Good (PWRGD)						
$V_{th(UV\text{-}falling)}$	Output Undervoltage Falling Threshold			92		%
$V_{th(UV\text{-}rising)}$	Output Undervoltage Rising Threshold			94		%
$V_{th(OV\text{-}falling)}$	Output Overvoltage Falling Threshold			106		%
$V_{th(OV\text{-}rising)}$	Output Overvoltage Rising Threshold			104		%
$I_{lkg(PWRGD)}$	PWRGD Leakage Current(1)	$V_{(PWRGD)}$ = 5.5 V		30	100	nA
$R_{dson(PWRGD)}$	PWRGD on-resistance	$I_{(PWRGD)}$ = 3 mA , VFB < 0.79 V		30		Ω
$V_{(minVIN,PWRGD)}$	Minimal VIN for Defined Output	$V_{(PWRGD)}$ < 0.5 V , $I_{(PWRGD)}$ = 100 μA		1.8	2.4	V
Soft Start and Tracking (SS/TR)						
$I_{(SS/TR)}$	Soft-start Charging Current	$V_{(SS/TR)}$ = 0.4V		2.3		μA
$\Delta V_{(SS/TR)}$	SS/TR to FB Matching Error	$V_{(SS/TR)}$ = 0.4V		20		mV
$I_{(SS/TR),disch}$	Max SS/TR Discharge Current	$V_{(FB)}$ = 0 V, $V_{(SS/TR)}$ = 0.4V		1300		μA
$V_{(SS/TR),\ disch}$	SS/TR Discharge Voltage	$V_{(FB)}$ = 0 V		30		mV
$V_{(SS/TR),\ th}$	SS/TR to Reference Cross-over Threshold			1.16		V
LOGIC						
V_{EN_rising}	EN Rising Threshold Voltage			1.21	1.26	V
$V_{EN\_falling}$	EN Falling Threshold Voltage		1.1	1.17		V
I_{EN}	EN threshold + 50 mV			−4.6		μA
	EN threshold − 50 mV		−0.58	−1.2	−1.8	μA
$I_{EN,hys}$	EN Hysteresis		−2.2	−3.4	−4.5	μA
$V_{th(RT/CLK),rising}$	RT/CLK Rising Threshold			1.55	2	V
$V_{th(RT/CLK),falling}$	RT/CLK Falling Threshold		0.8	1.2		V
Timing Characteristics						
t_{OCP}	Over-current Protection Delay			60		ns
$t_{d,EN}$	Enable COMP Delay			540		μs
$t_{CLK,min}$	Minimal CLK Input Pulse Width			15		ns
$t_{d,CLK}$	RT/CLK falling edge to SW rising edge delay	f_{SW} = 500 kHz		55		ns

Parameter		Conditions	Min	Typ	Max	Unit
f_{SW}	Switching Frequency	RT = 240 kΩ	160	200	240	kHz
		RT = 100 kΩ	400	480	560	kHz
		RT = 29 kΩ	1440	1600	1760	kHz
	Switching frequency using RT mode (1)		100		1600	kHz
	Switching frequency using CLK mode		160		1600	kHz
D_{max}	Maximum dutycycle	TPP20608x supports maximum full-on		100%		
t_{PLL}	PLL lock in time	f_{SW} = 500 kHz		78		μs

(1) Guranteed by design.

Typical Performance Characteristics

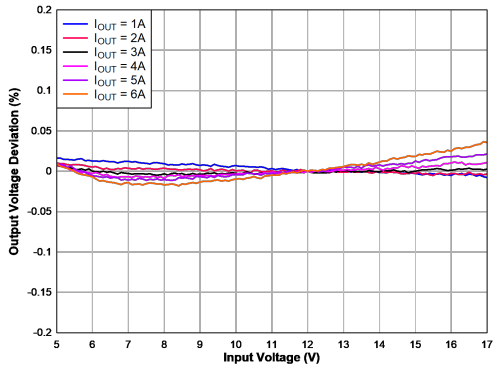


Figure 1. Line Regulation

$V_{(OUT)}$ = 3.3 V, $f_{(SW)}$ = 500 kHz T_A = 25 °C

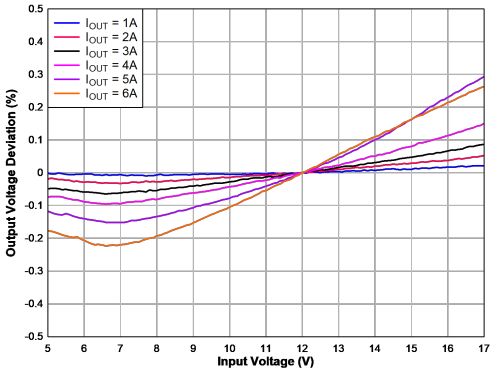


Figure 2. Load Regulation

$V_{(OUT)}$ = 3.3 V, $f_{(SW)}$ = 1600 kHz T_A = 25 °C,

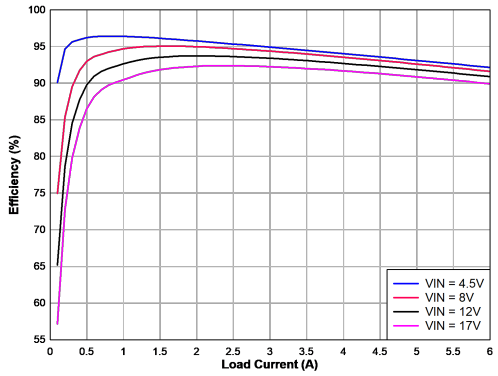


Figure 3. Efficiency vs Load Current

$V_{(OUT)}$ = 3.3 V, $F_{(SW)}$ = 500 kHz

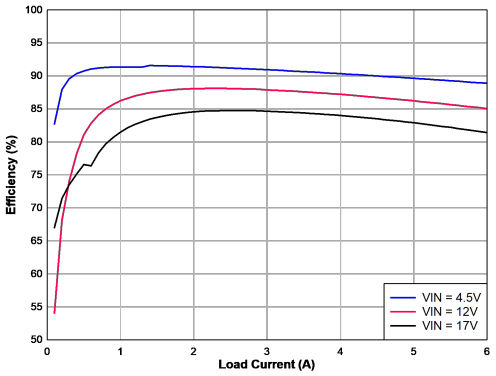


Figure 4. On-Resistance vs Temperature

$V_{(OUT)}$ = 3.3 V, $F_{(SW)}$ = 1600 kHz

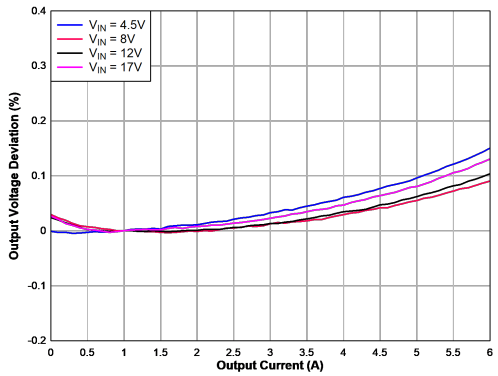


Figure 5. Load Regulation

$V_{(OUT)}$ = 3.3 V, $F_{(SW)}$ = 500 kHz

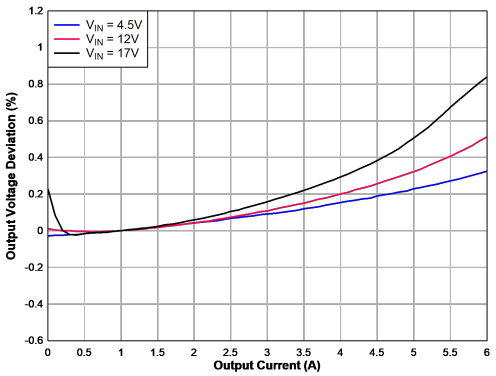


Figure 6. Load Regulation

$V_{(OUT)}$ = 3.3 V, $F_{(SW)}$ = 1600 kHz

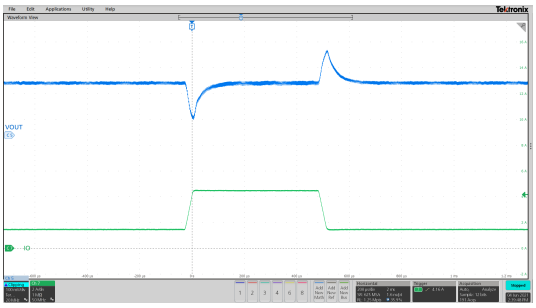


Figure 7. Load transient

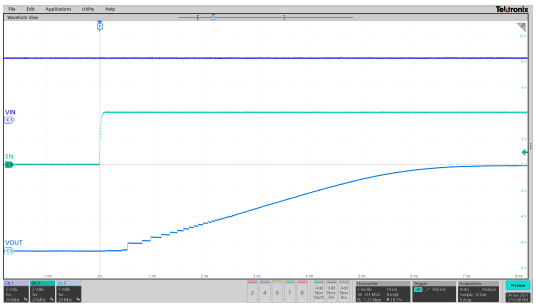


Figure 8. Start up with EN

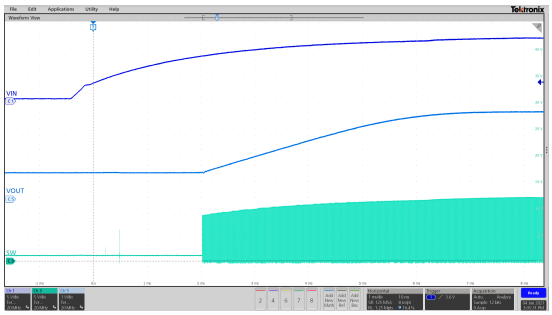


Figure 9. Pre-bias start up

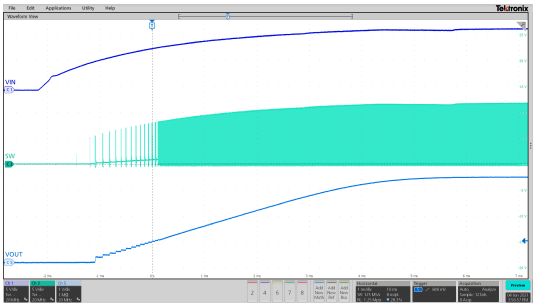


Figure 10. Start up with supply ramp

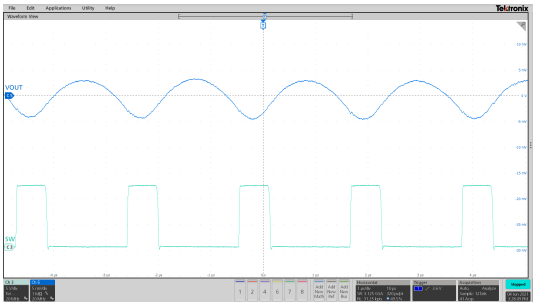


Figure 11. Switching Transient

Detailed Description

Overview

The TPP20608x series device is a family of 17-V 6-A synchronous buck converter with integrated power MOSFETs. The device employs peak-current-mode control mechanism to improve transient performance as well as line and load regulations. The low-Rdson MOSFETs are designed to optimize low output voltage applications with current up to 6 A.

The device supports both external and internal switching frequency settings via RT/PLL pin. The switching frequency ranges from 200 kHz to 1.6 MHz. Using an external resistor, the device can set the switching frequency. It can also switch to an external clock using PLL mode when a clock signal is detected on RT/PLL.

The device supports a wide range of output voltage as low as 0.6 V (TPP206080) / 0.8 V (TPP206081). The device supports 100% duty cycle operation with the integrated boot-recharge feature. When the boot capacitor voltage is below the required voltage threshold, the device will automatically recharge the boot capacitor by turning on the low-side transistor for a short period.

Integrated SS/TR feature provides programmable Soft Start via an external capacitor and supplies sequencing by tracking external voltage.

The device also provides diagnostics and protection against output voltage, overload, and over-temperature scenarios. It also has open-drain power good indicator PWRGD if the VSENSE pin voltage is within the desired range.

Functional Block Diagram

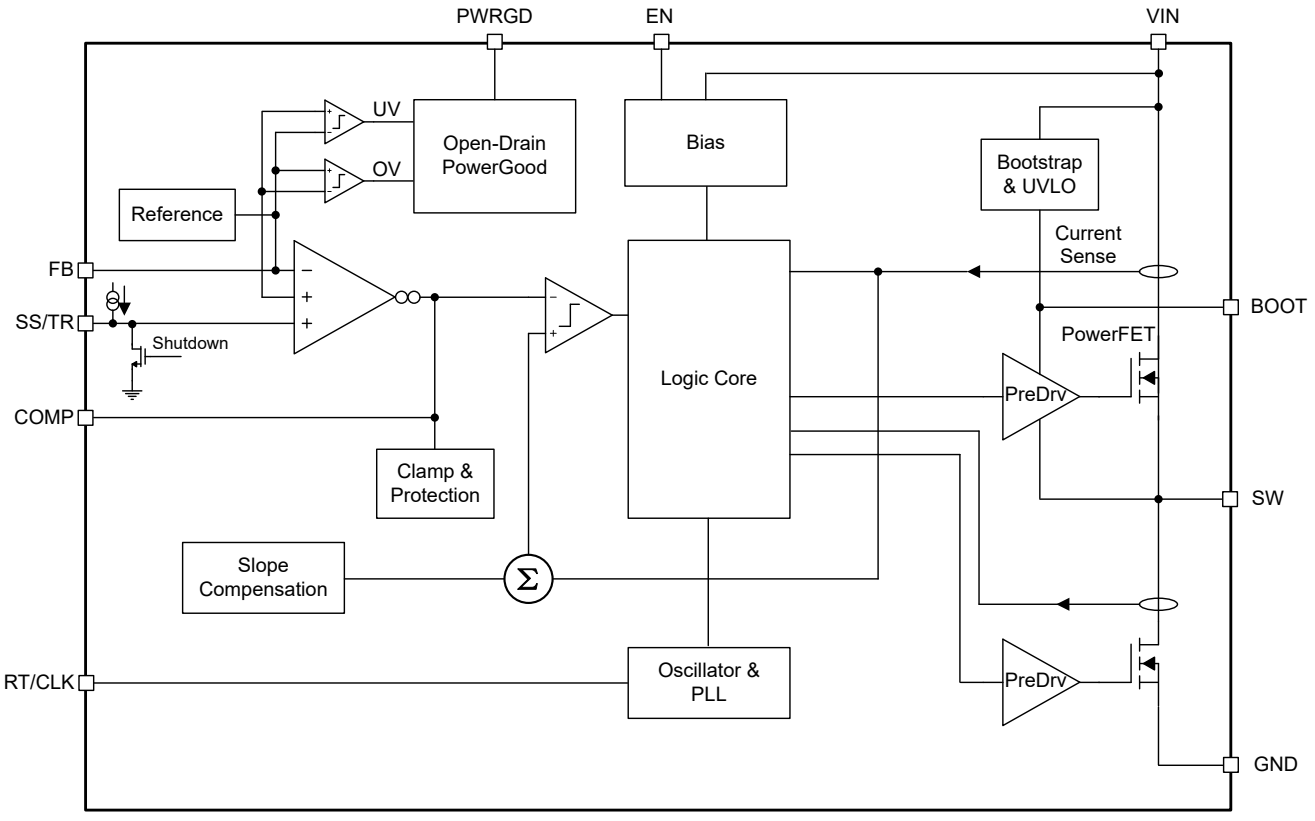


Figure 12. Functional Block Diagram

Feature Description

Fixed Frequency Peak Current Mode Control

The TPP20608x employs peak current mode control with adjustable switching frequency. The feedback voltage is sensed through VSENSE pin to compare with internal voltage reference by an error amplifier. The output of the error amplifier is compared by PWM comparator with internal voltage ramp and controls power switch. Internal oscillator controls the frequency of switching high-side MOSFET.

The high-side switching current is sensed internally as part of the voltage ramp. Once the PWM comparator detects peak switching current reaches the threshold level set by COMP voltage, the high-side MOSFET is switched off and the low-side MOSFET is switched on. During light-load operation, the device will enter forced-PWM mode with the same switching frequency.

The transconductance error amplifier converts the error voltage between VSENSE pin voltage and internal voltage, whichever lower of the soft-start voltage or internal voltage reference V_{REF}, to current with transconductance gm of 1300 μMhos during normal operation conditions. It is recommended to connect compensation network between COMP and GND pin to ensure stability across all working ranges. The details are discussed in the application chapter.

Setting Output Voltage

The precision internal voltage reference produces a 0.6-V voltage reference (TPP206080) and 0.8-V voltage reference (TPP206081) with ±1% tolerance across operating temperature and voltage ranges. The resistor divider from output voltage to FB pin sets the output voltage.

$$R_H = R_L \times \left(\frac{V_{OUT} - V_{FB}}{V_{FB}} \right) \quad (1)$$

Soft-Start with Pre-Biased Capability

The device uses SS node to implement a programmable soft-start feature by controlling ramping up reference voltage. The reference voltage will be the lower of internal reference voltage and SS voltage. The timing of soft-start is programmable via external capacitor connected to SS node.

An internal constant-current source of 2.3 μA charges up the external SS/TR capacitor to an internally clamped 2.7V. The timing can be calculated as below equation, measured from 10% to 90%. Reference voltage is 0.6V for TPP206080 and 0.8V for TPP206081.

$$T_{SS} = \frac{V_{REF} \times C_{SS} \times (90\% - 10\%)}{I_{SS}} \quad (2)$$

To ensure proper start-up, the device will discharge SS/TR voltage upon powering up if SS/TR voltage is above 54 mV. During any case the device stops switching, such as undervoltage lockout (UVLO), EN pulled low or over temperature protection, the device will discharge SS/TR below 54mV before switching.

The device also supports using SS/TR input for tracking as well as power supply sequencing. Sequencing needs to be carefully designed to ensure the system is able to recover from any fault.

RT/CLK

The device supports wide switching frequency from 200kHz to 1600kHz. The frequency is programmable via resistor connected between RT/CLK and GND. The switching frequency will affect solution size, efficiency, and minimal duty cycle. It is suggested that all factors taken care of when selecting switching frequency. The resistor can be calculated via equation

$$R_{RT}(k\Omega) = 48000 \cdot f_{SW}^{-0.997} - 2 \quad (3)$$

The device switching clock supports external clock sources for synchronization. Once a square wave is applied at the RT/CLK pin, the rising edge of SW synchronizes to the falling edge of RT/CLK. It is also suggested to connect a frequency set resistor to RT/CLK pin in case external clock source is not available.

The first rising edge of RT/CLK sets the device from free-running frequency mode to synchronization mode. The internal 0.5V voltage source is removed and the RT/CLK is set to high impedance mode. It takes 78μs to lock on external clock frequency; When external clock source stops, the device will switch back to free running frequency mode with frequency set by external resistor. During the transition, the device frequency will stay at 70kHz and then switch to the free-running frequency.

Protection

Undervoltage Lockout (UVLO)

The device has undervoltage lockout feature with default rising threshold of 4V. It can be adjusted by using EN pin with external resistors. A weak current source of 1.2 μA pulls up the EN pin to internal voltage rail. Another 3.4-μA hysteresis current source provides hysteresis voltage between rising and falling threshold. The resistor values can be calculated via below equations.

$V_{SYS_UVLO_H}$is the desired system level undervoltage protection rising threshold voltage, $V_{SYS_UVLO_L}$is the desired system level undervoltage protection falling threshold voltage. RUVLOH and RUVLOL are depicted in Figure 13.

$$R_{UVLOH} = \frac{V_{SYS\_UVLO\_H} \cdot \frac{V_{EN\_rising}}{V_{EN\_falling}} - V_{SYS\_UVLO\_L}}{I_{EN} \cdot \left(1 - \frac{V_{EN\_rising}}{V_{EN\_falling}}\right) + I_{EN,hys}} \quad (4)$$

$$R_{UVLOL} = \frac{R_{UVLOH} \cdot V_{EN\_falling}}{V_{SYS\_UVLO\_L} - V_{EN\_falling} + R_{UVLOH} \cdot \left(I_{EN} + I_{EN,hys}\right)} \quad (5)$$

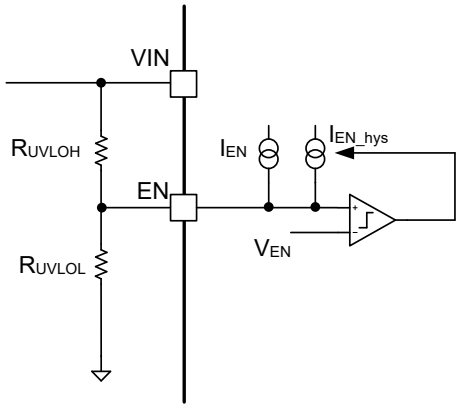


Figure 13.

Over-Current Protection

The device employs peak current mode control by controlling the peak current of internal high-side power transistor. The high side transistor current is converted to a voltage signal and compared to COMP pin. When the peak switching current is above the threshold set by COMP voltage, the device turns off high-side power transistor.

When the device is in over current scenario, the output voltage is pulled low and device will increase switching current threshold until it reaches the internal current limit threshold. Once the switching current is above the threshold, the device will turn off the transistor as current limit. Delay needs to be taken in to account that may cause the peak inductor current slightly higher than open-loop current limit.

Once the over current load is removed, the device will resume normal operation in the following cycle.

Power Good

The device uses an open-drain output PWRGD to signal if the output voltage is operating within the boundaries. If the FB voltage is within the 94% and 104% of internal reference voltage, the PWRGD pull-down will be disabled and pulled up by

externally resistor. The external pull up voltage source is recommended to be less than 5.5V with a 1kΩ resistor. If FB voltage is lower than 92% or greater than 106% of internal reference voltage, the PWRGD will be pulled low.

If UVLO, over temperature protection or EN going low, the PWRGD will also be pulled low. When supply voltage is below 2.4V, the PWRGD may not be at any defined state.

Over-Voltage Protection

The device stops high-side FET switching when it detects FB voltage above the over voltage protection (OVP) rising threshold (106% of internal reference voltage). When the voltage falls below the falling threshold (104% of internal reference voltage), it resumes switching high-side FET. With the OVP feature, the device can minimize voltage overshoot during load transient with low output capacitance.

Over-Temperature Shutdown

When the devices sense the junction temperature above the internal rising threshold of 175°C, the device stops high-side FET switching. Once the device junction temperature falls below falling threshold 165°C, the device restart the device with power up sequence.

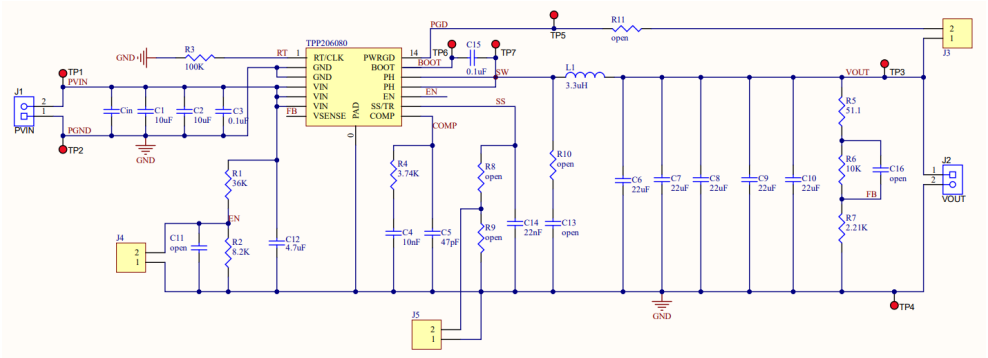
The device will discharge the SS/TR to GND as part of power up sequence. Care must be taken that the SS/TR is able to be pulled low to avoid deadlock scenario that may prevent the device re-start.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

As an easy-to-use step-down voltage regulator, also known as a buck regulator, the TPP20608x series usually converts a higher input voltage to the desired output voltage set by the VSENSE resistor divider. The maximum output current is 6 A. The below section depicts a simplified design flow of circuitry for the TPP20608x series. In most 12-V systems, lower voltage rail such as 3.3 V is a typical need for microcontrollers, I/Os, and other low-voltage components. The below application lists the typical schematic for a 3.3-V buck regulator.



This application describes detailed information about the design of a switching regulator and a few parameters must be known to start the design process. These parameters are typically determined at the system level. For this application, begin with the known parameters listed in Table 2.

Table 2. Application Parameter Selection

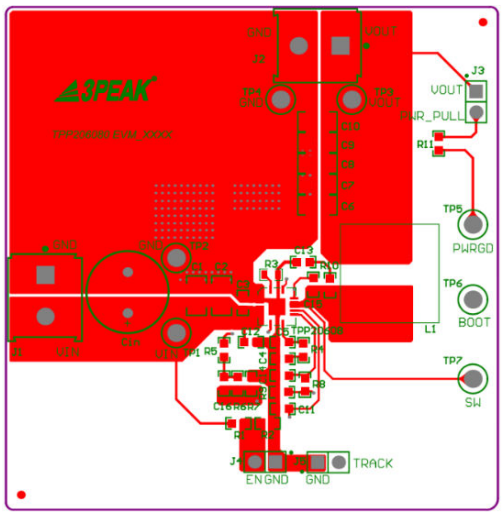
Design Parameter	Example Value
Output Voltage	3.3 V
Output Current	6 A
Input Voltage	12 V nominal, 8 V to 17 V
Output Voltage Ripple	22 mV p-p
Start Input Voltage (rising VIN)	6.366 V
Stop Input Voltage (falling VIN)	6.082 V
Switching Frequency	480 kHz

Layout

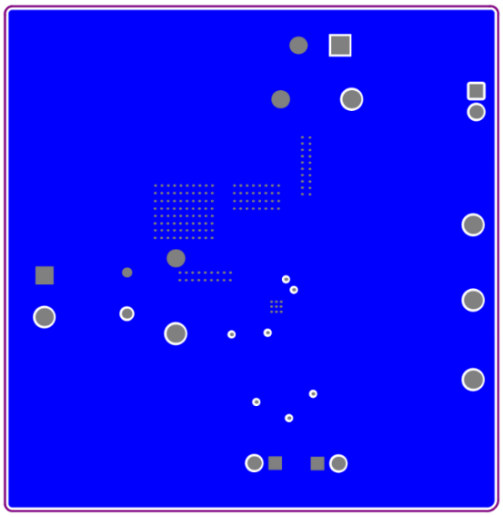
Layout Guideline

- The VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric, and the bypass capacitor should also be located as close as possible to the IC PIN.
- It is needed to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the ground connections.
- Because of the switching node PH, the output inductor should be located close to the PH pins, and the area of the PCB conductor is minimized to prevent excessive capacitive coupling.
- The RT/CLK pin is sensitive to noise so the RT resistor must be located as close as possible to the IC pin.

Layout Recommendations

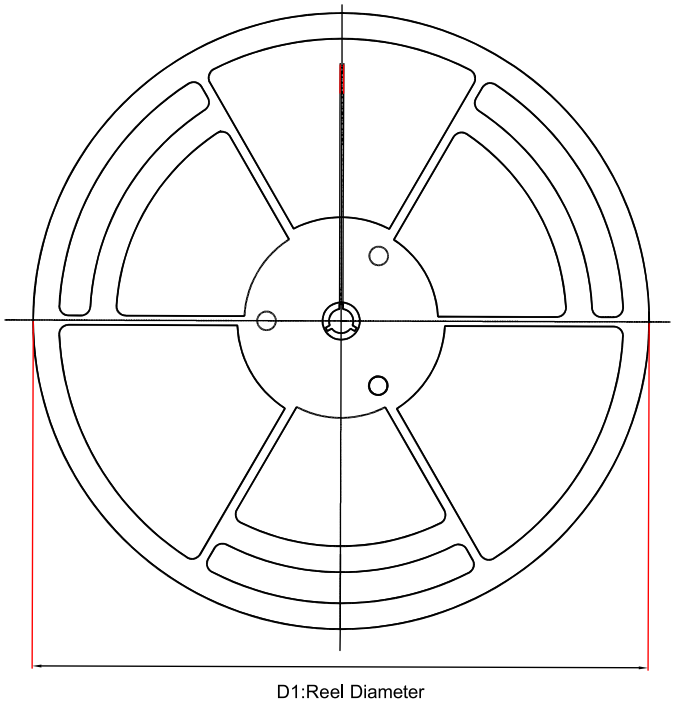


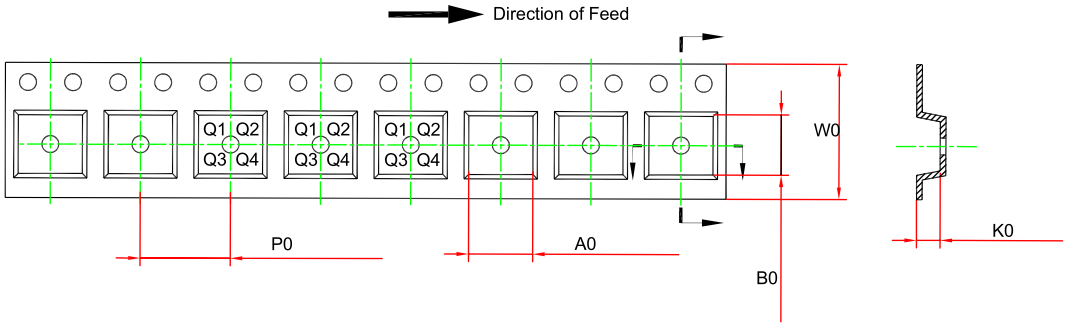
Top Layer



Bottom Layer

Tape and Reel Information



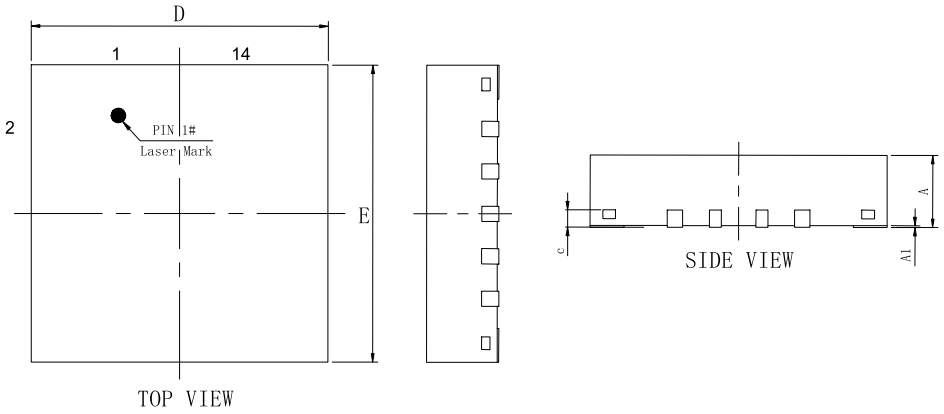


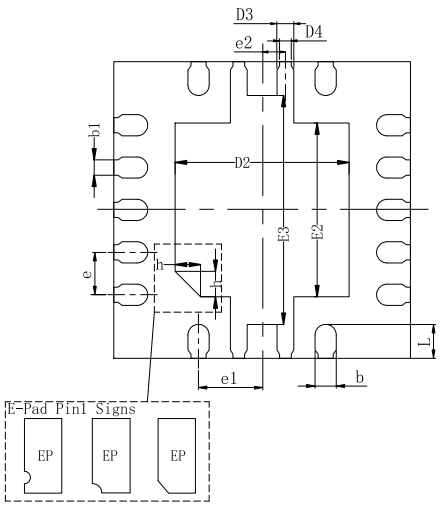
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPP206080-QFMR-S	QFN3.5X3.5-14	330	17.6	3.75	3.75	1.0	8	12	Q1
TPP206081-QFMR-S	QFN3.5X3.5-14	330	17.6	3.75	3.75	1.0	8	12	Q1
TPP206080-QFMR	QFN3.5X3.5-14	330	17.6	3.75	3.75	1.0	8	12	Q1
TPP206081-QFMR	QFN3.5X3.5-14	330	17.6	3.75	3.75	1.0	8	12	Q1

Package Outline Dimensions

QFN3.5X3.5-14

Package Outline Dimensions QFM(QFN3.5X3.5-14-A)





BOTTOM VIEW

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.850	0.950	0.033	0.039
A1	0.000	0.050	0.000	0.002
b	0.200	0.300	0.008	0.012
b1	0.180 REF		0.007 REF	
c	0.203 REF		0.008 REF	
D	3.400	3.600	0.134	0.142
D2	1.950	2.150	0.077	0.085
D3	0.100	0.300	0.004	0.012
D4	0.040	0.240	0.002	0.009
E	3.400	3.600	0.134	0.142
E2	1.950	2.150	0.077	0.085
E3	2.600	2.800	0.102	0.110
e	0.500 BSC		0.020 BSC	
e1	0.750 BSC		0.030 BSC	
e2	0.275 BSC		0.011 BSC	
L	0.350	0.450	0.014	0.018
h	0.250	0.350	0.010	0.014

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPP206080-QFMR-S	−40 to 125°C	QFN3.5X3.5-14	2680	3	Tape and Reel, 4000	Green
TPP206081-QFMR-S	−40 to 125°C	QFN3.5X3.5-14	2681	3	Tape and Reel, 4000	Green
TPP206080-QFMR	−40 to 125°C	QFN3.5X3.5-14	2680	3	Tape and Reel, 4000	Green
TPP206081-QFMR	−40 to 125°C	QFN3.5X3.5-14	2681	3	Tape and Reel, 4000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

IMPORTANT NOTICE AND DISCLAIMER

Trademarks. Any of the 思瑞浦 or 3PEAK trade names, trademarks, graphic marks, and domain names(“Trademarks”) contained in this document/material are the property of 3PEAK. You may NOT reproduce, modify, publish, transmit or distribute any Trademark without the prior written consent of 3PEAK.

Performance Information. Performance tests or performance range contained in this document/material are results of design simulation or actual tests conducted under designated testing environment. Any differences in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

Forward-Looking Statements. The information in this document/material may contain forward-looking statements, except for statements or descriptions of historical facts. These forward-looking statements are based upon our current understanding of our industry, management philosophy and certain assumptions and speculative calculations. These forward-looking statements are subject to risks and uncertainties and our actual results may differ. Please do not rely solely on the above information to make your business decisions.

Disclaimer. 3PEAK provides technical and reliability data (including data sheets), design resources (including reference designs), application or other design recommendations, networking tools, security information and other resources "As Is". 3PEAK makes no warranty as to the absence of defects, and makes no warranties of any kind, express or implied, including, without limitation, implied warranties as to merchantability, fitness for a particular purpose or non-infringement of any third-party’s intellectual property rights.

This page intentionally left blank