170-V, 0.5-A Asynchronous Buck Converter with Rectifier Diode

Features

- 16-V to 170-V Input Voltage Range
- Selectable 12-V, 15-V, and 18-V Output Voltages
- Programmable Output Voltage from 3.3 V to 26 V
- 0.5-A Output Current Capability
- High-Voltage Startup
- High Efficiency with PFM Mode at Light Loads
- 12-ms Soft Startup Time
- 100-kHz Switching Frequency
- VDD Under-voltage Protection
- Over Load Protection
- Output Short-circuit Protection
- Cycle-by-cycle Current Limit
- Operating Temperature Range from −40°C to +150°C
- Available in the SOP8 Package

Applications

- PoE
- E-Bike
- E-Tools
- Scotter
- Solar Energy

Description

The TPP15053 is a wide input range, non-synchronous DC-DC buck converter that uses peak current mode control. The TPP15053 integrates a 170-V, 1.3-Ω power MOSFET with 1.5-A peak current limit having up to 0.5-A output current capability.

The TPP15053 has a high-voltage startup circuitry to enable the device from high input voltage directly. The TPP15053 has a built-in 12-ms soft-start time to minimize the inrush current during startup. In the moderate to heavy load condition, the TPP15053 works in PWM mode at 100-kHz switching frequency. In the light load condition, the TPP15053 enters PFM mode to reduce the switching loss and improve the efficiency. The TPP15053 also has spread spectrum switching frequency dithering to reduce the EMI.

The TPP15053 features a cycle-by-cycle current limit in over-load conditions. Furthermore, when the output voltage is 10% below the regulation target and the current limit is touched for 128 switching cycles, or the output is short to ground, the TPP15053 enters hiccup mode and stops PWM switching for 65 ms. After hiccup times out, the TPP15053 restarts the soft startup.

The TPP15053 is available in the SOP8 package.

Typical Application Circuit

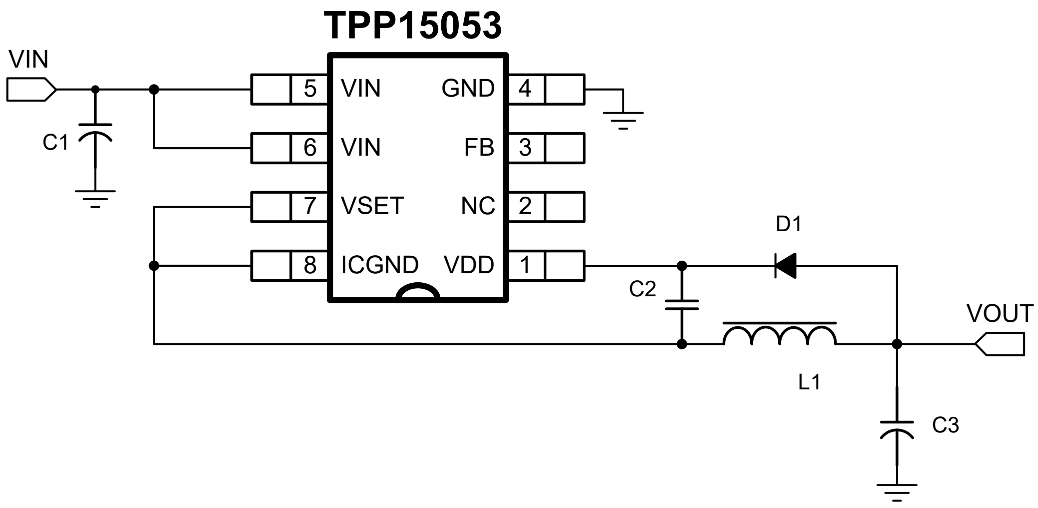


Table of Contents

Product Family Table

Order Number	Feature	Package
TPP15053	Buck Converter	SOP8

Revision History

Date	Revision	Notes
2026-05-12	Rev.A.0	Initial release

Pin Configuration and Functions

TPP15053
SOP8 Package
Top View

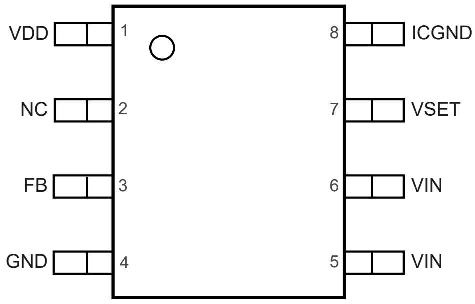


Table 1. Pin Functions: TPP15053

Pin		I/O/P	Description
No.	Name		
1	VDD	P	Power supply for the internal control circuitry
2	NC	-	No connection
3	FB	I	The feedback input of the output voltage when using an external feedback resistor divider. When using internal fixed output setting, leave the FB pin floating or connect it to the ICGND pin.
4	GND	GND	Ground of the output voltage
5,6	VIN	I	Drain of the switch MOSFET
7	VSET	P	Output voltage setting pin. Leave the VSET pin floating to select the fixed 12-V output voltage. Connect the VSET pin to the ICGND pin to select the fixed 15-V output voltage. Connect a 51-kΩ resistor between the VSET pin and the ICGND pin to select the fixed 18-V output voltage. Connect a 150-kΩ between the VSET pin and the ICGND pin to set the output voltage by an external resistor divider.
8	ICGND	O	Source of the switch MOSFET. It is also the ground of the internal control circuitry.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Voltage Range at Terminals (refer to the ICGND pin)	VIN	−0.3	180	V
	VDD	−0.3	26	V
	VSET, FB	−0.3	6	V
	GND	−200	1.5	V
T_J	Maximum Junction Temperature	−40	150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
V_{HBM}	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	2000	V
V_{CDM}	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
V_{IN}	Power Supply	16		170	V
V_{OUT}	Output Voltage	3.3		26	V
C_{OUT}	Effective Capacitance for Output	220	470	1000	μF
L	Inductor	47	220	470	μH
T_J	Junction Temperature Range	–40		125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JB}	$\theta_{JC(TOP)}$	Unit
SOP8	109.0	80.3	54.1	°C/W

Electrical Characteristics

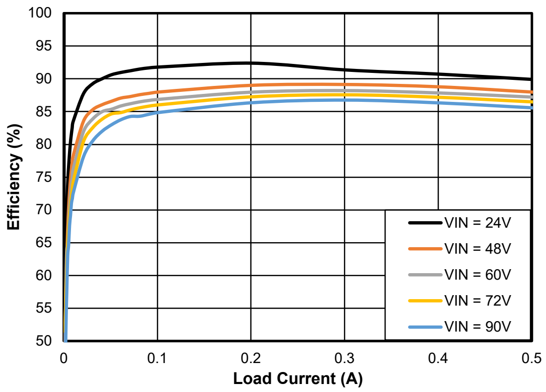
All test conditions: V_{IN} = 48 V, V_{DD} = 12 V, T_J = −40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIN Supply Voltage and Current						
V_{IN}	IC Supply Voltage Range		16		170	V
I_{HVC}	High Voltage Operating Quiescent Current	V_{DD} = 0 V, V_{IN} = 150 V		4		mA
I_{HVSD}	High Voltage Shutdown Current	V_{DD} = 18 V, V_{IN} = 150 V		6		μA
VDD Regulator						
V_{DD}	VDD Voltage Range	After startup	6.5		21	V
I_{DD}	Quiescent Current	Switching mode		0.9		mA
V_{DD_C}	VDD Internal Charging Termination Voltage			9.5		V
V_{DD_UVLO}	VDD UVLO Rising Threshold		7.5	8	8.5	V
$V_{DD\_UVLO\_HYS}$	VDD UVLO Hysteresis			2		V
V_{DD_CLMP}	VDD Clamp Voltage	I_{DD_CLMP} = 10 mA	21	22.5	24	V
I_{DD_CLMP}	VDD Sinking Current at Clamp Voltage		8	10		mA
Reference Voltage						
V_{REF}	Reference Voltage at the REF Pin	T_J = −40°C - 125°C	0.965	1.01	1.045	V
Power MOSFET Switch						
R_{DSON_N}	N-channel 180-V MOSFET on-Resistance			1.3		Ω
I_{LIM}	Peak Current Limit	T_A = 25°C	1	1.5	2.0	A
I_{SW_LKG}	N-channel MOSFET Leakage Current	V_{DD} = 5 V, V_{IN} = 150 V		6		μA
Rectifier Diode						
V_{BR}	Breakdown Voltage	I_R = 5 μA	200			V
V_F	Forward Voltage	I_F = 500 mA		1	1.5	V
I_F	Maximum Average Forward Rectified Current		0.5			A
Soft Start						
t_{SS}	Soft Startup Time			12		ms
Hiccup Time						
t_{HICCUP}	Hiccup Delay Time			65		ms
Switching Frequency						

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SW}	Switching Frequency		75	100	125	kHz
Δf_{DITHER}	Switching Frequency Dithering			±6%		
t_{MIN_OFF}	Minimum OFF Time			500		ns
t_{MIN_ON}	Minimum ON Time			500		ns
Thermal Protection						
T_{SD}	Thermal Shutdown Protection Threshold	T_J rising		175		ºC
T_{SD_HYS}	Thermal Shutdown Hysteresis	T_J falling below T_{SD}		25		ºC

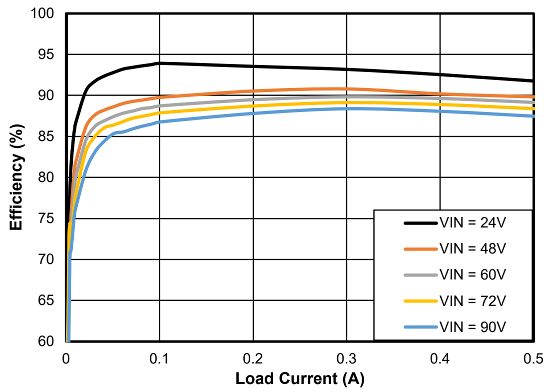
Typical Performance Characteristics

All test conditions: V_{IN} = 48 V, V_{DD} = 12 V, T_A = +25°C, unless otherwise noted.



V_{OUT} = 12 V

Figure 1. Efficiency vs. Load Current



V_{OUT} = 15 V

Figure 2. Efficiency vs. Load Current

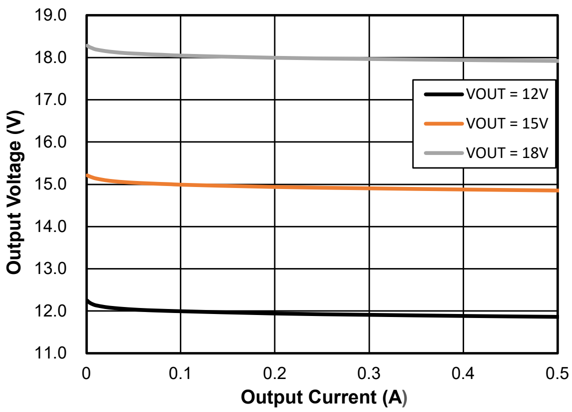


Figure 3. Output Voltage vs. Load Current

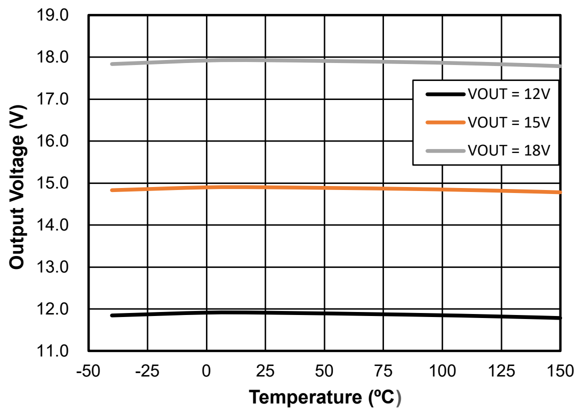


Figure 4. Output Voltage vs. Temperature

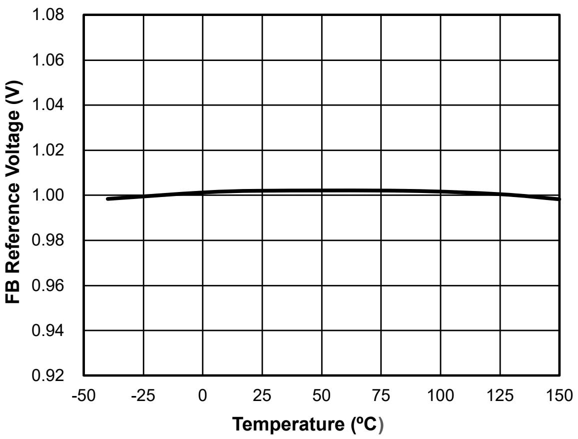


Figure 5. FB Reference Voltage vs. Temperature

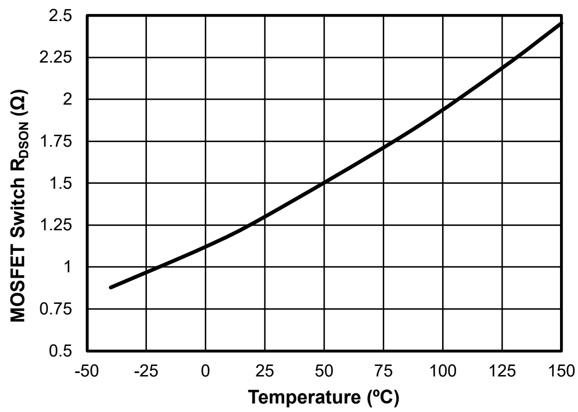


Figure 6. R_{DSON} vs. Temperature

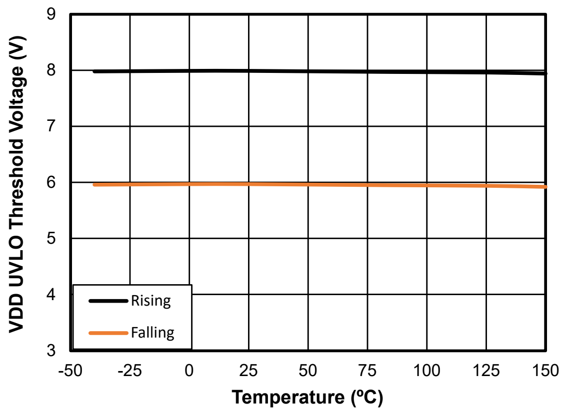


Figure 7. VDD UVLO vs. Temperature

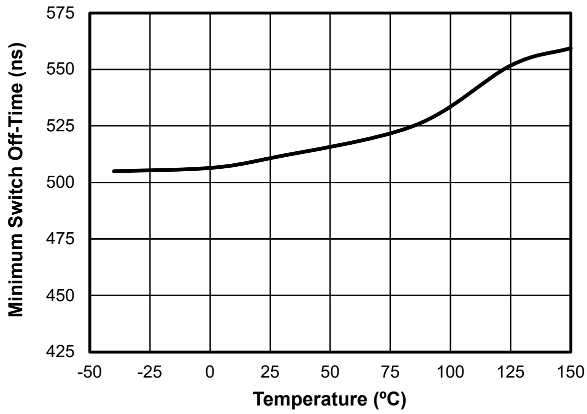


Figure 8. Minimum OFF Time vs. Temperature

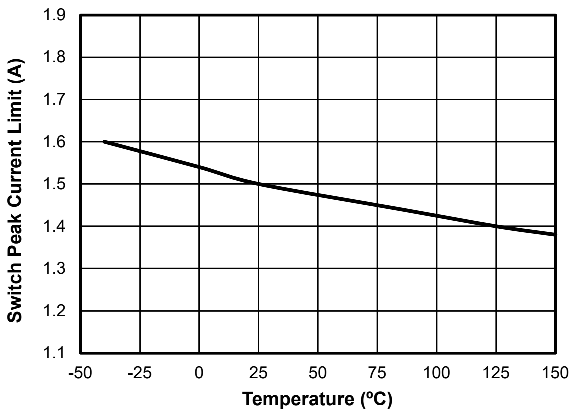


Figure 9. Current Limit vs. Temperature

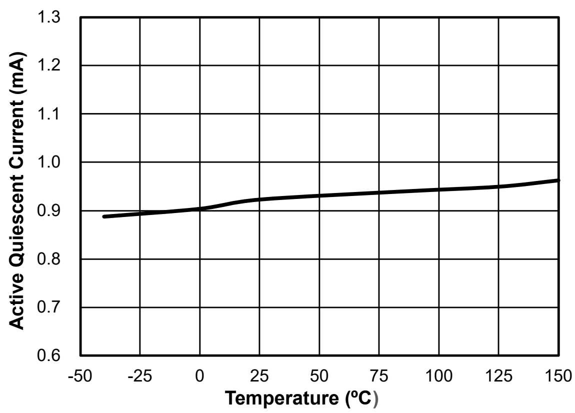


Figure 10. Quiescent Current vs. Temperature

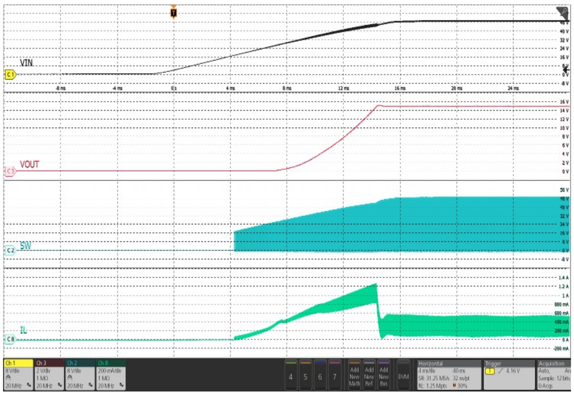
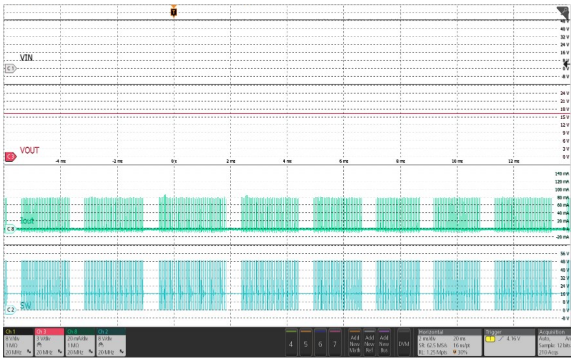


Figure 11. Startup Waveform

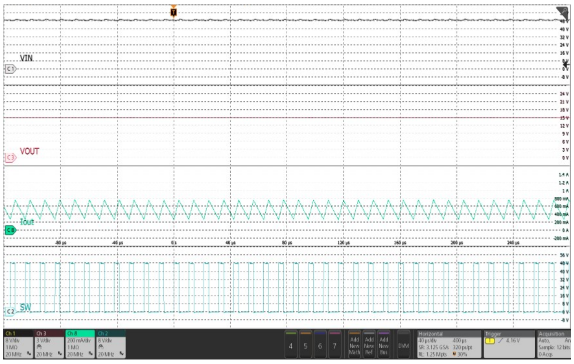


V_{IN} = 48 V, V_{OUT} = 15 V, I_{OUT} = 0.7 mA

Figure 12. Switching Waveform in Hiccup Mode

V_{IN} = 48 V, V_{OUT} = 15 V, I_{OUT} = 100 mA

Figure 13. Switching Waveform in DCM Mode



V_{IN} = 48 V, V_{OUT} = 15 V, I_{OUT} = 500 mA

Figure 14. Switching Waveform in CCM Mode

Detailed Description

Overview

The TPP15053 is a wide input range, asynchronous DC-DC buck converter that uses peak current mode control. The TPP15053 integrates a 170-V, 1.3-Ω power MOSFET with 1.5-A peak current limit having up to 0.5-A output current capability.

The TPP15053 has a high-voltage startup circuitry to enable the device from high input voltage directly. The TPP15053 has a built-in 12-ms soft-start time to minimize the inrush current during startup. In the moderate to heavy load condition, the TPP15053 works in PWM mode at 100-kHz switching frequency. In the light load condition, the TPP15053 enters PFM mode to reduce the switching loss and improve efficiency. The TPP15053 also has spread spectrum switching frequency dithering to reduce the EMI.

Functional Block Diagram

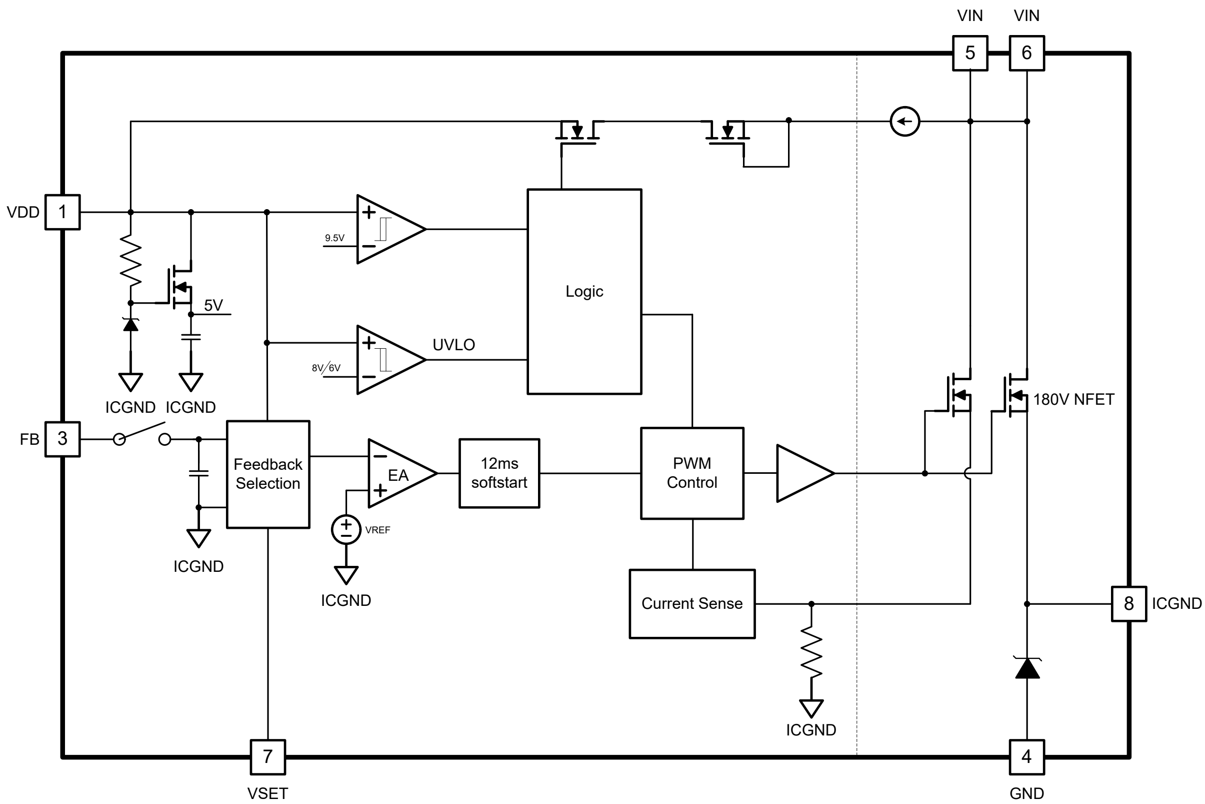


Figure 15. Functional Block Diagram

Feature Description

High Voltage Startup and VDD UVLO

The TPP15053 integrates a high-voltage startup circuitry. When the VIN pin is applied with a voltage above 16 V, an internal current source starts charging the capacitor at the VDD pin to 9.5 V. When the VDD voltage is above the UVLO threshold of the 8 V, the device starts switching. The power switch between the VIN pin and the ICGND pin is turned on and the current goes from the VIN pin to the ICGND pin.

When the VDD voltage is below 6 V, the TPP15053 is disabled.

Soft Startup

The TPP15053 has a built-in 12-ms soft start time. When the PWM switching starts, the output of the internal error amplifier increases slowly. The current of the power switch is limited to eliminate the inrush current during startup. During the soft startup, the hiccup mode is disabled. Once the output voltage is above 95% of the regulation voltage or a 32-ms timer for soft startup times out, the hiccup mode is enabled.

PWM mode and PFM Mode

In heavy load, the TPP15053 works in PWM mode. The switching frequency is fixed at 100 kHz. As the load decreases, the PWM switching operation goes from CCM mode to DCM mode.

At the light load, the PWM duty cycle goes to a minimum on-time limit as the load current decreases. The TPP15053 enters PFM mode. The switching frequency gradually changes from 100 kHz to 35 kHz to regulate the output voltage. When the switching frequency reaches 35 kHz but the load current continues decreasing, the output voltage goes above the regulation voltage. To regulate the output voltage, the TPP15053 goes into hiccup mode and stops switching for 500 µs. After a 500-µs hiccup, the TPP15053 resumes switching without a soft start.

Output Voltage Setting

The TPP15053 has preset 12-V, 15-V, and 18-V output voltage settings inside by connecting different resistances between the VSET pin and the ICGND pin, as shown in Table 2.

Table 2. VOUT Setting by VSET Pin

VSET Connection	VOUT
VSET floating	12 V
VSET connected to ICGND	15 V
51-kΩ resistance between VSET and ICGND	18 V
150-kΩ resistance between VSET and ICGND	Adjustable VOUT set by an external resistor divider between VOUT and ICGND

When using an external resistor divider to set the output voltage, it is recommended using a resistor with a value less than 5 kΩ as the bottom resistor R_B between the FB pin and the ICGND pin. The upper resistor R_U between the FB pin and the output can be calculated by Equation 1.

$$R_U = \left(\frac{V_{OUT} + V_F}{V_{REF}} - 1\right) \times R_B \qquad (1)$$

Where

- V_F is the forward voltage of the rectifier diode.
- V_{REF} is the internal reference voltage.

Dummy Load

A minimum load is needed to prevent the output voltage from running away to high voltage when the load current is too small. When the system is powered by the TPP15053, which may consume very small power in some conditions, like standby mode, a dummy load is needed. However, a large dummy load increases the power loss in the system standby condition. It is recommended using a 15-kΩ resistor at the output as the minimum load.

Output Overload Protection

After startup, when the output voltage is below the regulation voltage, the output of the internal error amplifier goes up to the high limit and the switch current hits the limit. When the output voltage is below 90% of the target regulation voltage and the current limit is reached for 128 switching cycles, the TPP15053 enters hiccup mode and stops switching for 65 ms. After a 65-ms hiccup period, the TPP15053 restarts the soft startup. If the output voltage rises above 90% of the target regulation voltage within the 128 switching cycles, the overload timer resets.

Cycle-by-cycle Current Limit Protection

When the current through the power switch trips 1.5 A, the power switch is turned off immediately. The power switch is kept off until the next switching cycle.

Output Short-circuit Protection

When the output short-circuit happens, the current through the power switch goes up above the cycle-by-cycle limit because the inductor current continues to increase within the minimum on-time period of each cycle. When the TPP15053 detects the current through the power switch more than 2.2 A (50% higher than the limit), the TPP15053 goes into hiccup mode and stop switching for 65 ms. After a 65-ms hiccup period, the TPP15053 restarts soft start.

Thermal Shutdown Protection

A thermal shutdown is implemented to prevent damages due to excessive heat and power dissipation. Typically, the thermal shutdown happens at a junction temperature of 175°C. When the thermal shutdown is triggered, the device stops switching until the junction temperature falls below typically 150°C, then the device starts switching again.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPP15053 is designed for outputting voltage from high input voltage up to 170 V. It adopts a peak current control scheme to achieve a fast transient response.

Typical Application

48-V input to 15-V output buck converter.

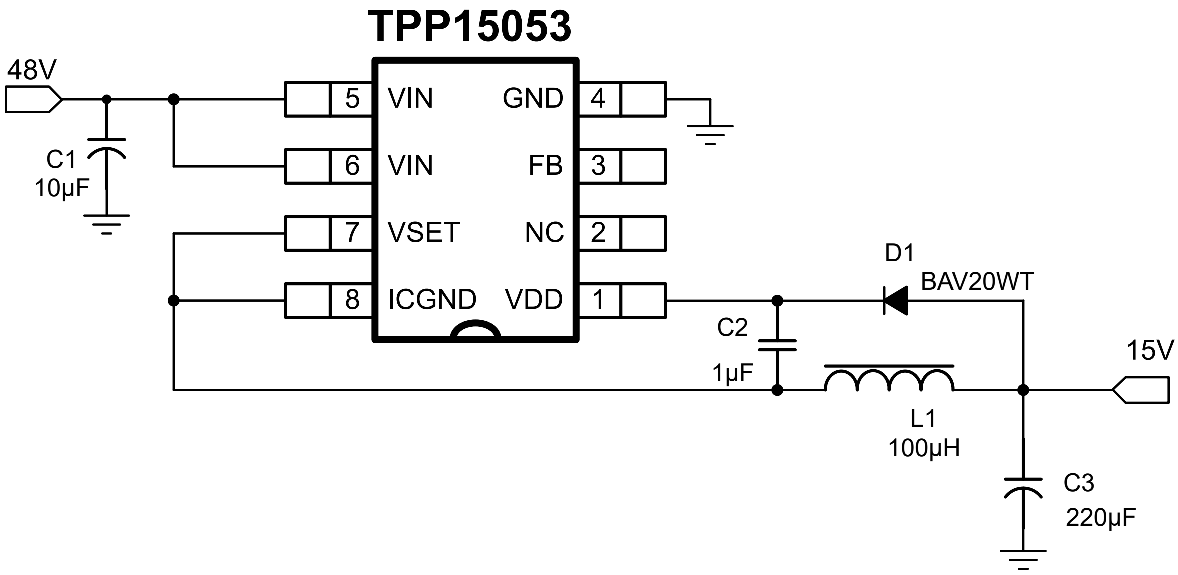


Figure 16. TPP15053 48-V to 15-V Buck Converter Application Circuit

Application Examples

48-V input to 5-V output buck converter with the external voltage setting resistor divider.

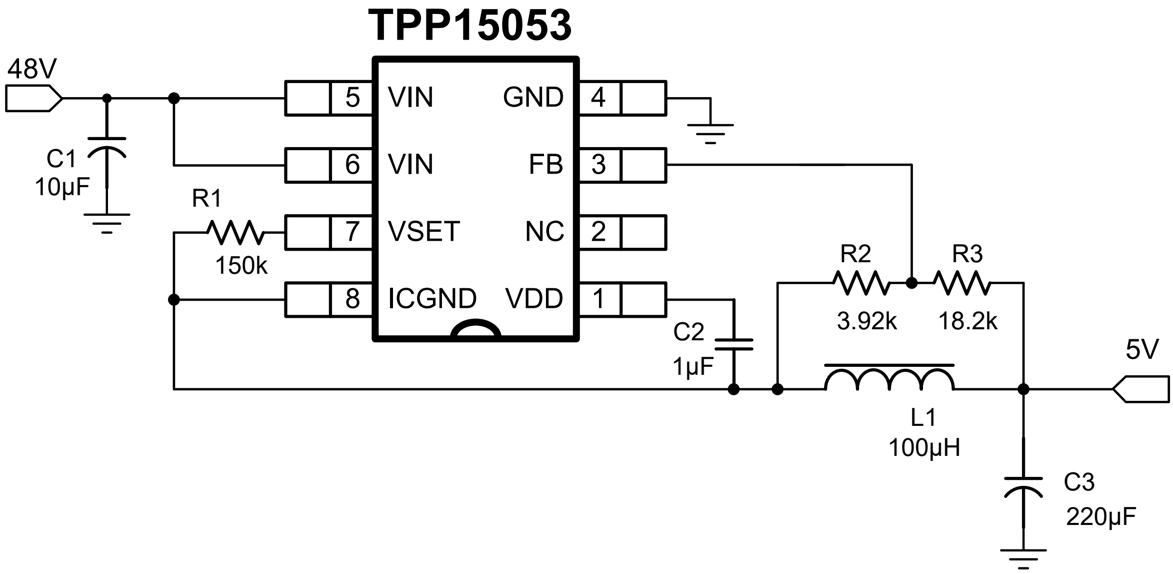


Figure 17. TPP15053 48-V to 5-V Buck Converter Application Circuit

Layout

Layout Guideline

PCB layout is very critical for the performance of a DC to DC converter, especially for loop stability, EMI, and thermal performance. A good PCB layout with less parasitic inductance and capacitance results in a stable output voltage with less switching noise.

- Place the input bypass capacitor as close as possible to the VIN pin and the ground. Use short and wide trace to connect the input capacitor and the VIN pin. Care should be taken to minimize the loop area formed by the input bypass capacitor connections, the VIN pins, the ICGND pin and the ground connections.
- Since the ICGND connection is the swithing node, the inductor should be located as close as possible to the ICGND pin. The area of the switching node connection area must be kept small to minimize the EMI and the capacitive coupling between the ICGND node and the output.
- Use a low ESR ceramic capacitor as the boot capacitor between the VDD pin and the ICGND pin. The boot capacitor must also be located close to the VDD pin.
- When using an external resistor divider to set the output voltage, place the resistor divider as close as possible to the FB pin. The node of the center tap of the resistor divider and the FB pin must be kept far away from the ground plane to minimize the parasitic capacitance between the FB pin and ground.

Layout Example

Figure 18 and Figure 19 are two examples of PCB layout when using the TPP15053. For adjustable output voltage configuration, the node of the center tap of the feedback resistor divider and the FB pin must be kept far away from the ground plane to minimize the parasitic capacitance between the FB pin and ground.

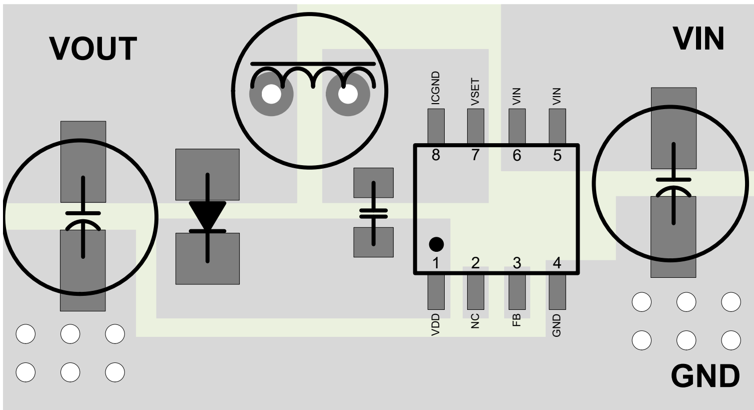


Figure 18. PCB Layout Example for 15-V Fixed Output

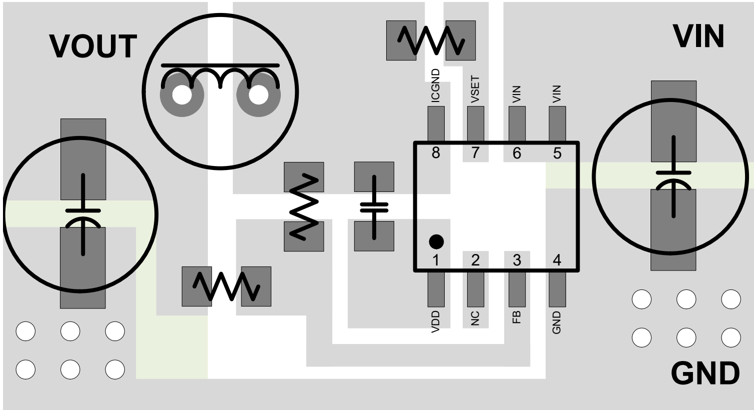
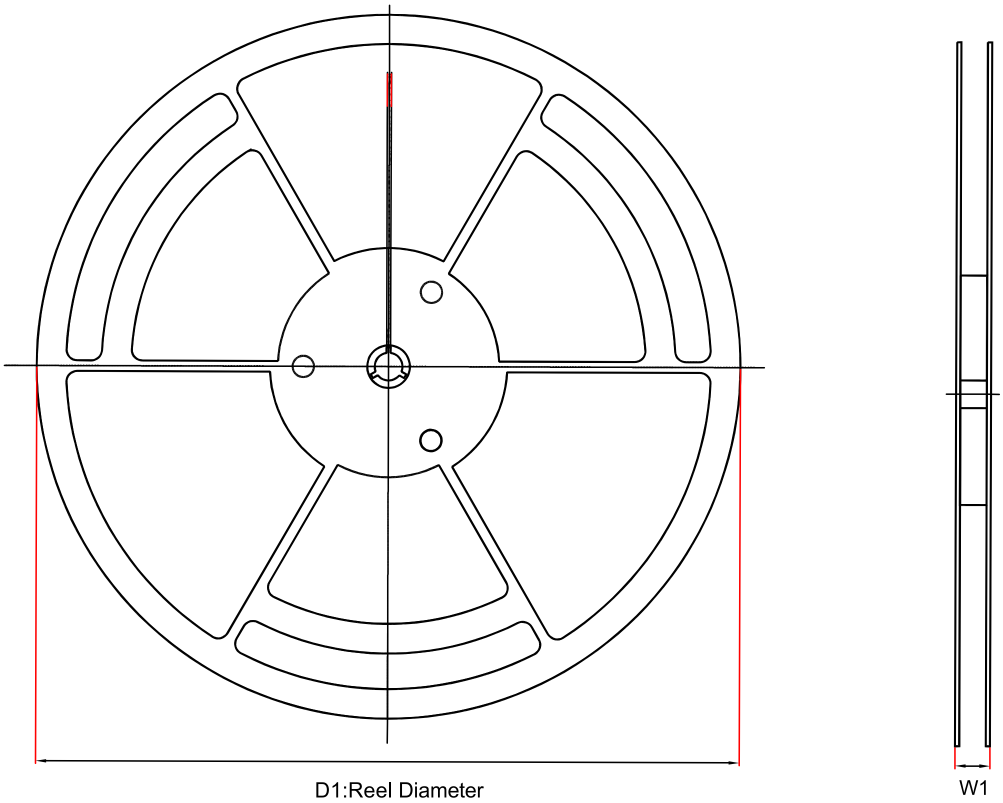
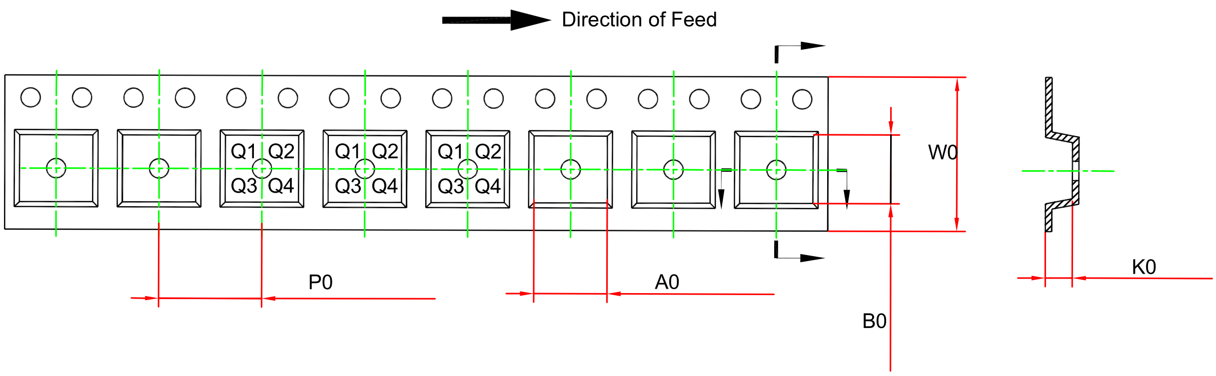


Figure 19. PCB Layout Example for Adjustable Output

Tape and Reel Information



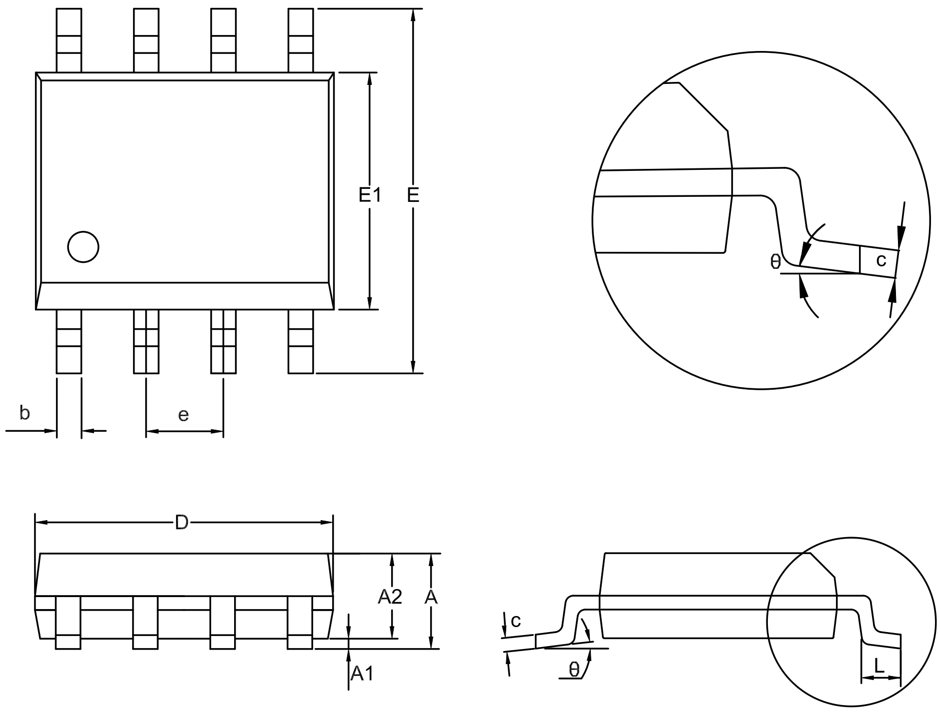


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPP15053-SO1R-C	SOP8	330	17.6	6.5	5.4	2	8	12	Q1

Package Outline Dimensions

SOP8

Package Outline Dimensions SO1(SOP-8-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.550	0.049	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.000	0.016	0.039
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPP15053-SO1R-C	−40 to 125°C	SOP8	15053	MSL3	Tape & Reel, 4000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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