2.8-V to 6-V Vin, 6-A Synchronous Step-down Regulator

Features

- High Efficiency at Light Loads with Pulse Skipping
- Ultra-low $R_{DS(ON)}$ 8-mΩ Highside and 8-mΩ Lowside MOSFETs
- Adjustable Switching Frequency
- Integrated PLL to Synchronize with External Clock
- Adjustable UVLO Voltage and Hysteresis
- Under-voltage and Over-voltage Power Good Output
- Adjustable Soft-start and Sequencing
- Low-dropout Operation at Light Loads
- Cycle-by-cycle Current Limit
- 0.6-V 1% Internal Voltage Reference
- 16-Pin QFN3X3-16 with Exposed Pad Package
- –40°C to 125°C Ambient Temperature Range

Applications

- Point-of-load Regulators
- Communication and Networking Devices
- Personal Electronics, Personal Healthcare

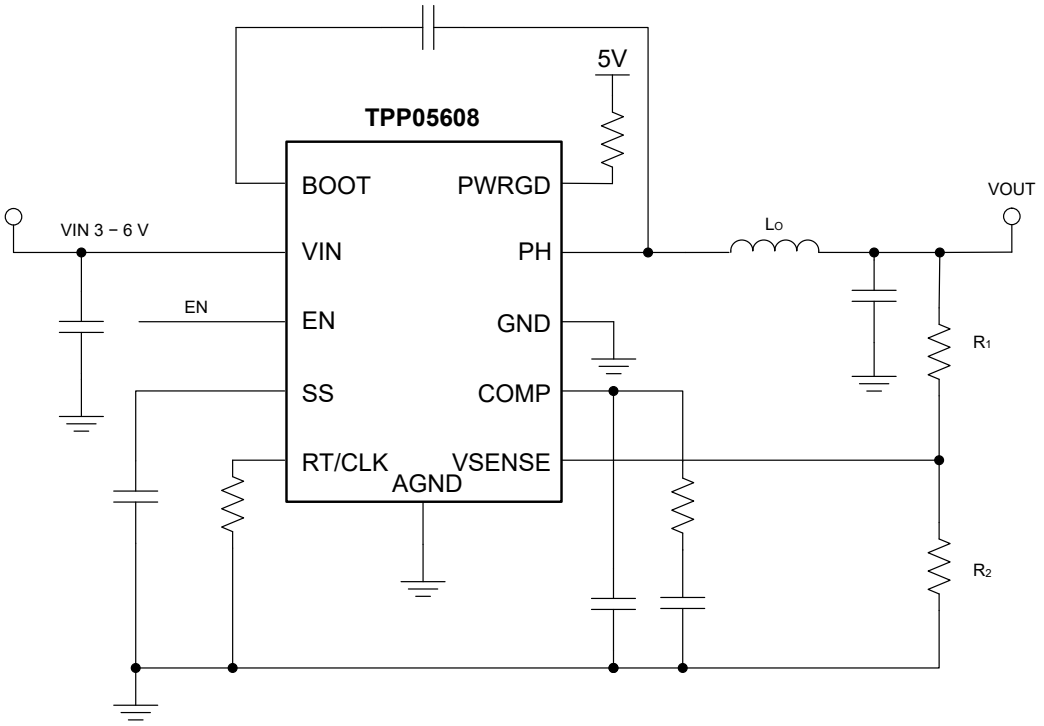
Description

The TPP05608 is a 6-V 6-A synchronous step-down converter with integrated power FETs.

The TPP05608 employs current-mode topology to support various applications. With a wide range of switching frequency support, the device can reduce the inductor size. The high precision reference provides output voltage with <1% accuracy over temperature, which is especially useful for low-voltage loads.

The TPP05608 has various diagnostics and protections such as undervoltage lock-out (UVLO), power good, current limit, and thermal shutdown.

Typical Application Circuit



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Product Family Table

Order Number	Package
TPP056080-QFMR	QFN3X3-16

Revision History

Date	Revision	Notes
2021-07-19	Rev.Pre.0	Initial version
2022-08-15	Rev.A.0	Released

Pin Configuration and Functions

TPP05608
QFN3X3-16 Package
Top View

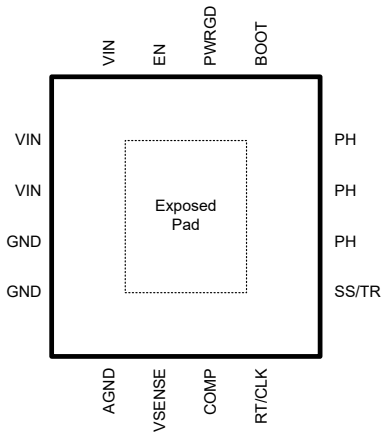


Table 1. Pin Functions

Pin		I/O	Description
No.	Name		
1, 2, 16	VIN	I	Power supply voltage input pin. Connect VIN to GND with a 1-μF or greater capacitor.
3, 4	GND	–	Ground
5	AGND	–	Analog ground
6	VSENSE	I	Voltage feedback sense input, connected to internal negative node of error amplifier.
7	COMP	–	Error amplifier output
8	RT/CLK	I	Frequency selection and external clock input. When using it as frequency setting mode, an external connected resistor sets switching frequency; When using it as clock synchronization input, the input is a high impedance clock input for internal PLL.
9	SS/TR	I	Soft-start and tracking input. When using the soft-start mode, an external capacitor connected to this pin sets output ramping time; When using track/sequence mode, the voltage on this pin overrides the internal voltage reference thus sets the output voltage.
10, 11, 12	PH	O	Switching node
13	BOOT	I	Bootstrap capacitor between BOOT and PH, recommend using a 0.1-μF ceramic capacitor with 10-V or higher voltage rating.
14	PWRGD	P	Open-drain power good output
15	EN	I	Device enable pin with internal pull-up current source. Threshold can be increased via external resistors

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
EN, VIN, RT/CLK, PWRGD	Input voltage	–0.3	6.5	V
COMP, SS/TR, VSENSE		–0.3	3	V
BOOT-PH	Output voltage		6.5	V
PH		–0.7	6.5	
PH (20-ns transient)		–2	10	
PH (5-ns transient)		–4	12	
I_{EN}, I_{RT_CLK}	Source current		100	µA
I_{COMP}, I_{SS}	Sink current		100	µA
I_{PWRGD}			10	mA
T_J	Operating junction temperature	–40	150	°C
T_{STG}	Storage Temperature Range	–65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
V_{IN}	Input Voltage	2.9		6	V
T_J	Operating Junction Temperature	–40		150	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
QFN3X3-16	45	50	°C/W

Electrical Characteristics

All test condition is at T_A = –40 °C to 125 °C . V_{IN} = 3 V to 6 V, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage and Current						
V_{UVLO_Rising}	UVLO Rising Threshold		2.54	2.61	2.68	V
$V_{UVLO\_Falling}$	UVLO Falling Threshold		2.4	2.48	2.68	V
I_D	Shutdown supply current	EN = 0 V, 25°C, 2.9 V ≤ VIN ≤ 6 V		1		μA
I_Q	Operating non-switching supply current	VSENSE = 0.6 V, VIN = 5 V, 25°C, f_{SW} = 500 kHz		800	1300	μA
Enable and Under Voltage Lock Out						
$V_{TH(EN\_Rising)}$	Rising Edge		1.21	1.27	1.32	V
$V_{TH(EN\_Falling)}$	Falling Edge		1.11	1.17	1.23	V
I_{EN_H}	EN = H		–2.8	–3.6	–4.4	μA
I_{EN_L}	EN = L		–0.5	–0.7	–1	μA
Voltage Reference						
V_{REF}	Voltage Reference	2.9 V ≤ VIN ≤ 6 V, –40°C < T_J < 150°C	594	600	606	mV
Output Stage						
$R_{DS(ON)\_HS}$	High-side switch on-resistance	BOOT-PH = 5 V		8		mΩ
		BOOT-PH = 2.95 V		10		
$R_{DS(ON)\_LS}$	Low-side switch on-resistance	VIN = 5 V		8		
		VIN = 2.95 V		10		
$t_{ON(min)}$	Minimum ON-time	I_{OUT} = 3 A		90		ns
		I_{OUT} = 0 A		100		
$t_{OFF(min)}$ (1)	Minimum OFF-time	BOOT - PH = 3 V, I_{OUT} = 3 A		70		ns
R_{CHG}	BOOT Charge Resistance	VIN = 6 V, BOOT-PH = 6 V		6		Ω
V_{BOOT_UV}	BOOT UVLO Threshold			2.2		V
Error Amplifier						
I_{EA_IN}	EA input current			7		nA
g_m	Error amplifier transconductance	–5 μA < $I_{(COMP)}$ < 5 μA	200	220	240	μS
$I_{EA\_OUT\_SRC}$	Error amplifier output source current	$V_{(COMP)}$ = 1 V 100-mV overdrive	22	30	40	μA
$I_{EA\_OUT\_SINK}$	Error amplifier output sink current	$V_{(COMP)}$ = 1 V –100-mV overdrive	22	30	40	μA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
g_{SW}	Transconductance from COMP to switching current			20		μS
Current Limit						
I_{LIMIT_HS}	F_{SW} = 500 kHz			11		A
$N_{DEGLITCH}$	Over current deglitch cycle count			512		Cycles
N_{HICCUP}	Hiccup cycles			16512		Cycles
I_{LIMIT_LSSRC}	Low-side sourcing current threshold			8		A
V_{LIMIT_LSNEG}	Low-side FET negative current threshold			3.2		A
Thermal Protection						
T_{SD}	Thermal shutdown threshold			175		°C
V_{HYS}	Thermal shutdown hysteresis			12		°C
Timing						
f_{SW}	Switching frequency range		200		1600	kHz
	RT clock frequency	R_T = 82.5 kΩ	450	500	550	kHz
$t_{CLK(min)}$	Minimum CLK pulse width			75		ns
V_{RT}	RT/CLK Voltage	R_T = 82.5 kΩ		0.5		V
V_{CLK_H}	RT/CLK High Threshold			1.5	1.8	V
V_{CLK_L}	RT/CLK Low Threshold		0.7	0.95		V
t_{RT_DELAY}	RT/CLK falling edge to PH rising edge delay	f_{SW} = 500 kHz		55		ns
t_{PLL_Lock}	PLL lock-in time			200		μs
Soft-start and Tracking						
I_{SS}	Soft-start charge current	$V_{(SS/TR)}$ < 0.15 V		41.5		μA
		$V_{(SS/TR)}$ > 0.15 V		2.2		
$V_{SS\_MATCHING}$	SS/TR to VSENSE matching	V_{IN} = 3.3 V		60		mV
$V_{SS\_CROSSOVER}$	SS/TR to reference crossover			120		mV
I_{SS_DISCHG}	SS/TR discharge current	V_{SS}= 0.4 V, VSENSE = 0 V, V_{IN}= 2.8-6V		1200		μA
V_{SS_DISCHG}	SS/TR discharge voltage, over load condition	VSENSE = 0 V		4.5		mV
POWERGOOD						
$V_{TH\_OVP\_RISING}$	Over voltage protection VSENSE rising threshold	Percentage of VREF		108		%
$V_{TH\_OVP\_FALLING}$	Over voltage protection VSENSE falling threshold	Percentage of VREF		106		%

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{TH\_UVP\_RISING}$	Under voltage protection VSENSE rising threshold	Percentage of VREF		93		%
$V_{TH\_UVP\_FALLING}$	Under voltage protection VSENSE falling threshold	Percentage of VREF		91		%
I_{LKG_PWRGD}	Output high leakage	VSENSE = V_{REF}, $V_{(PWRGD)}$ = 5.5 V		5		nA
R_{PWRGD}	PWRGD on-resistance	V_{IN} = 5 V		5.5	10	Ω
V_{PWRGD_LOW}	PWRGD low	$I_{(PWRGD)}$= 3 mA			0.1	V
$V_{IN\_PWRGD\_MIN}$	Minimum VIN for valid output	$V_{(PWRGD)}$ < 0.5 V, $I_{(PWRGD)}$ = 100 μA		0.85	1.15	V

1. Guranteed by design

Typical Performance Characteristics

All test condition: V_{IN} =5 V, V_A = 25°C, unless otherwise noted.

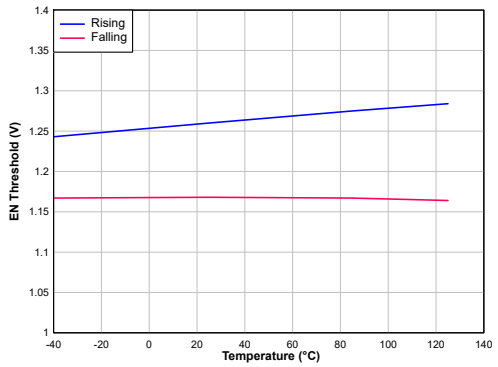


Figure 1. EN Threshold vs. Junction Temperature

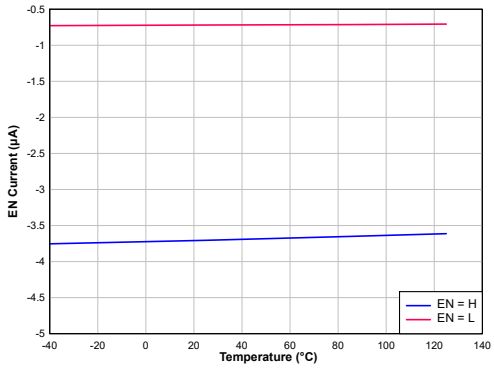


Figure 2. EN Current vs. Junction Temperature

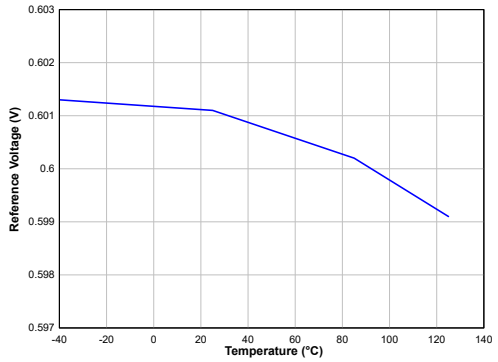


Figure 3. Reference Voltage vs. Junction Temperature

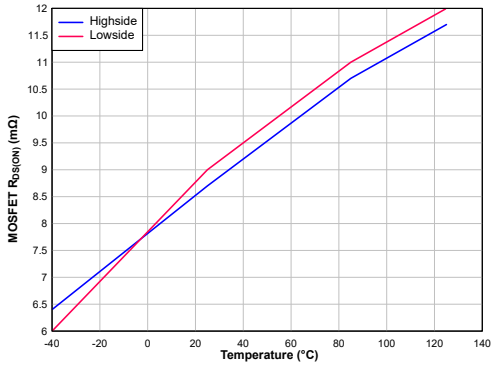


Figure 4. MOSFET On-resistance vs. Junction Temperature

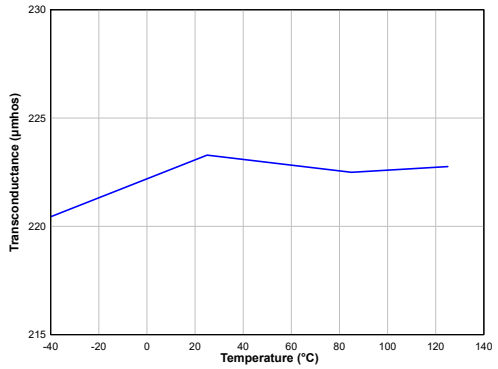


Figure 5. Transconductance vs. Junction Temperature

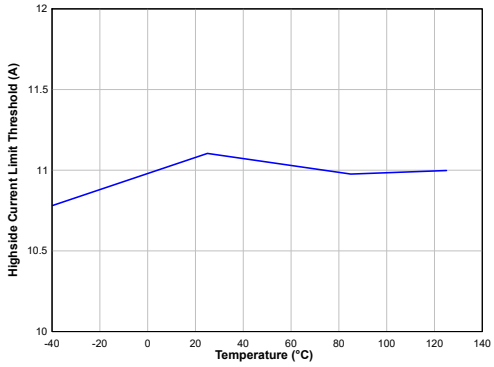
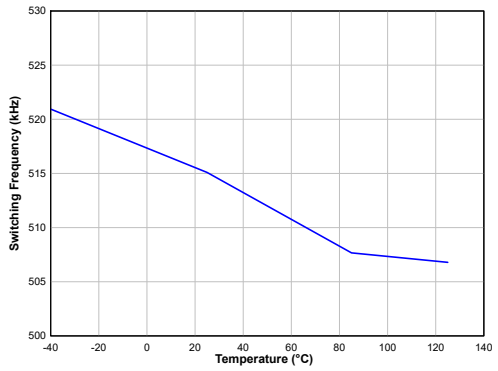


Figure 6. High-side Current Limit Threshold vs. Junction Temperature



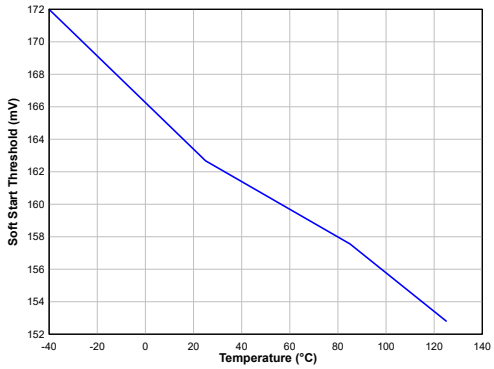


Figure 7. Soft-start Voltage Threshold vs. Junction Temperature

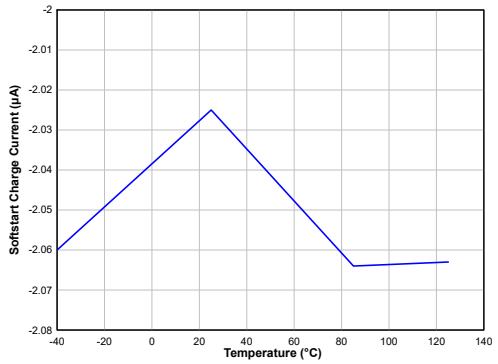


Figure 8. Soft-start Charge Current vs. Junction Temprature

$V_{SS/TR}$> 0.15 V

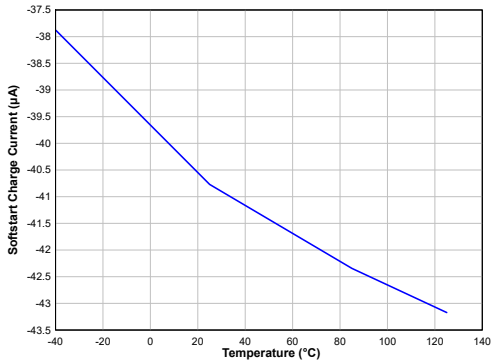


Figure 9. Soft-start Charge Current vs. Junction Temperature

$V_{SS/TR}$< 0.15 V

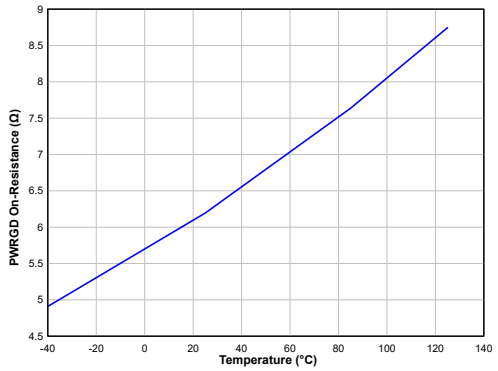


Figure 10. PWRGD $RD_{S(ON)}$ vs. Junction Temperature

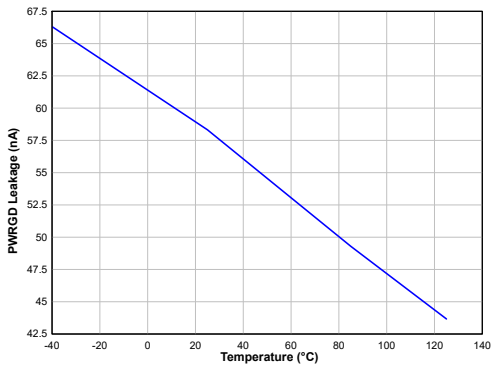


Figure 11. PWRGD Leakage vs. Junction Temperature

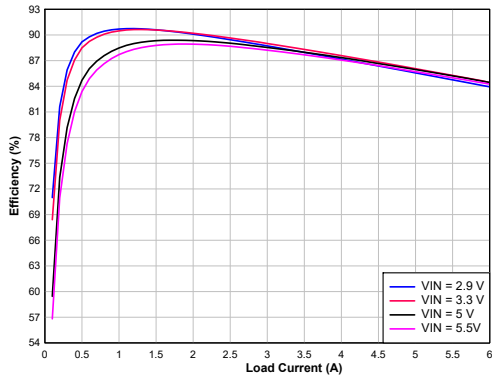


Figure 12. Efficiency vs. Load Current

f_{SW}= 500 kHz

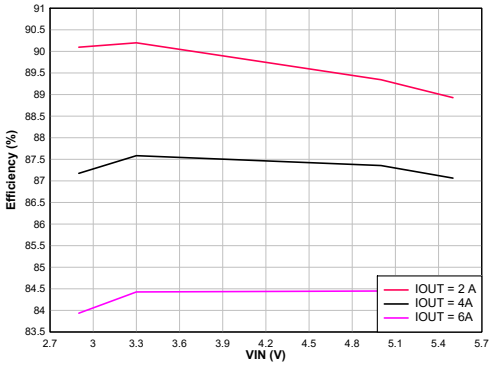


Figure 13. Efficiency vs. Supply Voltage

f_{SW}= 500 kHz

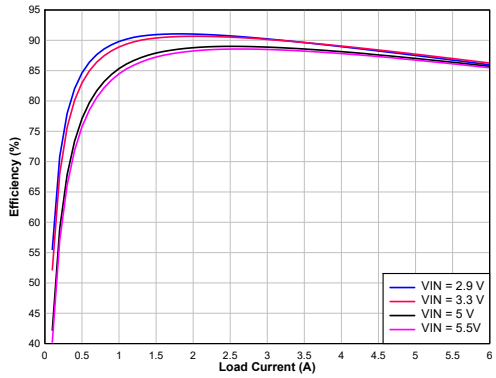


Figure 14. Efficiency vs. Load Current

f_{SW}= 200 kHz

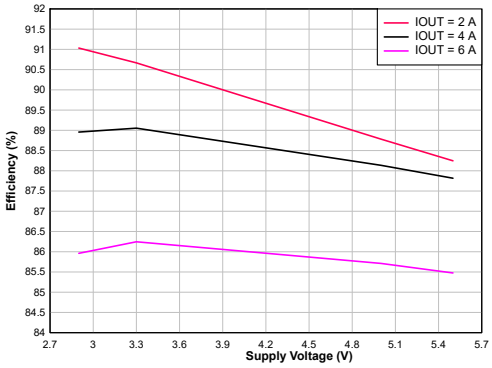


Figure 15. Efficiency vs. Supply Voltage

f_{SW}= 200 kHz

Detailed Description

Overview

The TPP05608 is a 6-V, 6-A, synchronous step-down converter with integrated N-channel MOSFETs as power stage. The device employs peak current mode control mechanism with constant frequency, supporting from 200kHz to 2000kHz switching frequency.

The TPP05608 has enable input EN with internal pull-up current source. The EN threshold can be adjusted by external resistors. The device also support external PWM input with integrated phase-locked-loop (PLL). The RT/CLK pin can be used to synchronize switching frequency with external clock source.

The device has high efficiency switching power stage with ultra-low on-resistance. The device also integrates boot recharge diode with bootstrap under-voltage lock out. The device supports high dutycycle close to 100% considering boot recharge cycles.

The TPP05608 has high-precision 0.6-V reference with 1% precision. The output voltage could be as low as 0.6V. The device also has output voltage monitor and open-drain power good output for output over voltage and under voltage monitoring.

SS/TR provides soft-start setting and input tracking feature to set reference voltage accordingly. The device also supports cycle-by-cycle current limit and hiccup protection for over current scenarios.

Functional Block Diagram

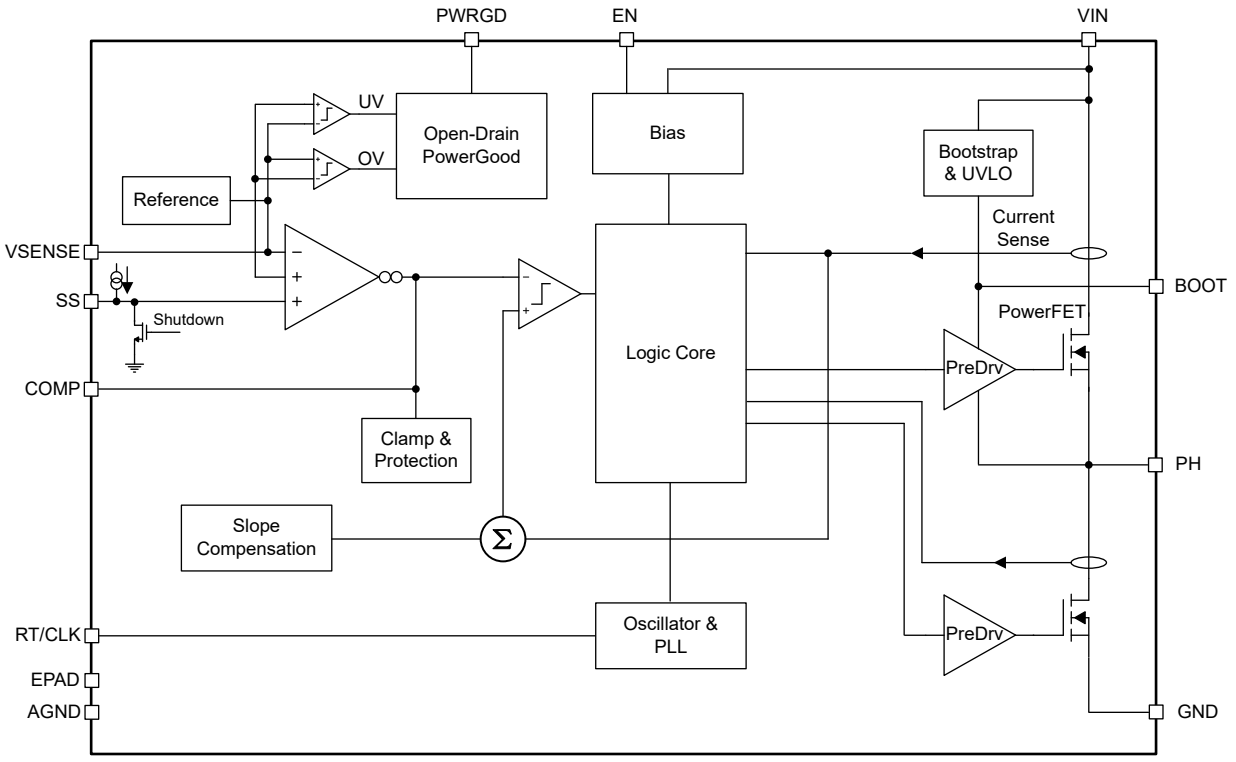


Figure 16. Functional Block Diagram

Feature Description

Current Mode Control

The TPP05608 employs peak current mode control with adjustable switching frequency. The feedback voltage is sensed through VSENSE pin to compare with internal voltage reference by an error amplifier. The output of the error amplifier is compared by PWM comparator with internal voltage ramp and controls power switch. Internal oscillator controls the frequency of switching high-side MOSFET.

The high-side switching current is sensed internally as part of the voltage ramp. Once the PWM comparator detects peak switching current reaches the threshold level set by COMP voltage, the high-side MOSFET is switched off and the low-side MOSFET is switched on. During light-load operation, the device will enter forced-PWM mode with the same switching frequency.

The transconductance error amplifier converts the error voltage between VSENSE pin voltage and internal voltage, whichever lower of the soft-start voltage or internal voltage reference V_{REF}, to current with transconductance gm of 1300 μMhos during normal operation conditions. It is recommended to connect compensation network between COMP and GND pin to ensure stability across all working ranges. The details are discussed in the application chapter.

Setting Output Voltage

The precision internal voltage reference produces a 0.6-V voltage reference with ±1% tolerance across operating temperature and voltage ranges. The resistor divider from output voltage to FB pin sets the output voltage.

$$R_H = R_L \times \left(\frac{V_{OUT} - V_{FB}}{V_{FB}}\right) \quad (1)$$

Soft-Start with Pre-Biased Capability

The device uses SS node to implement a programmable soft-start feature by controlling ramping up reference voltage. The reference voltage will be the lower of internal reference voltage and SS voltage. The timing of soft-start is programmable via external capacitor connected to SS node.

An internal constant-current source of 2.3 μA charges up the external SS/TR capacitor to an internally clamped 2.7V. The timing can be calculated as below equation, measured from 10% to 90%. Reference voltage is 0.6V.

To ensure proper start-up, the device will discharge SS/TR voltage upon powering up if SS/TR voltage is above 54 mV. During any case the device stops switching, such as undervoltage lockout (UVLO), EN pulled low or over temperature protection, the device will discharge SS/TR below 54mV before switching.The device also supports using SS/TR input for tracking as well as power supply sequencing. Sequencing needs to be carefully designed to ensure the system is able to recover from any fault.

$$T_{SS} = \frac{V_{REF} \times C_{SS} \times (90\% - 10\%)}{I_{SS}} \quad (2)$$

RT/CLK

The device supports wide switching frequency from 100kHz to 2000kHz. The frequency is programmable via resistor connected between RT/CLK and GND. The switching frequency will affect solution size, efficiency, and minimal duty cycle. It is suggested that all factors taken care of when selecting switching frequency. The resistor can be calculated via equation .

$$f = \frac{k}{R_{RT}} \quad (3)$$

The device switching clock supports external clock sources for synchronization. Once a square wave is applied at the RT/CLK pin, the rising edge of SW synchronizes to the falling edge of RT/CLK. It is also suggested to connect a frequency set resistor to RT/CLK pin in case external clock source is not available.

The first rising edge of RT/CLK sets the device from free-running frequency mode to synchronization mode. The internal 0.5V voltage source is removed and the RT/CLK is set to high impedance mode. It takes 78μs to lock on external clock frequency; When external clock source stops, the device will switch back to free running frequency mode with frequency set by external resistor. During the transition, the device frequency will stay at 70kHz and then switch to the free-running frequency.

Protection

The device has undervoltage lockout feature with default rising threshold of 4V. It can be adjusted by using EN pin with external resistors. A weak current source of 1.2 μA pulls up the EN pin to internal voltage rail. Another 3.4-μA hysteresis current source provides hysteresis voltage between rising and falling threshold. The resistor values can be calculated via below equations.

$V_{SYS_UVLO_H}$is the desired system level undervoltage protection rising threshold voltage, $V_{SYS_UVLO_L}$is the desired system level undervoltage protection falling threshold voltage. RUVLOH and RUVLOL are depicted in Figure 16.

$$R_H = \frac{V_{START}\left(\frac{V_{EN\_FALLING}}{V_{EN\_RISING}}\right) - V_{STOP}}{I_P\left(1 - \frac{V_{EN\_FALLING}}{V_{EN\_RISING}}\right) + I_H} \quad (4)$$

$$R_L = \frac{R_H \cdot V_{EN\_FALLING}}{V_{STOP} - V_{EN\_FALLING} + R_H \cdot (I_P + I_H)} \quad (5)$$

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

Typical Application

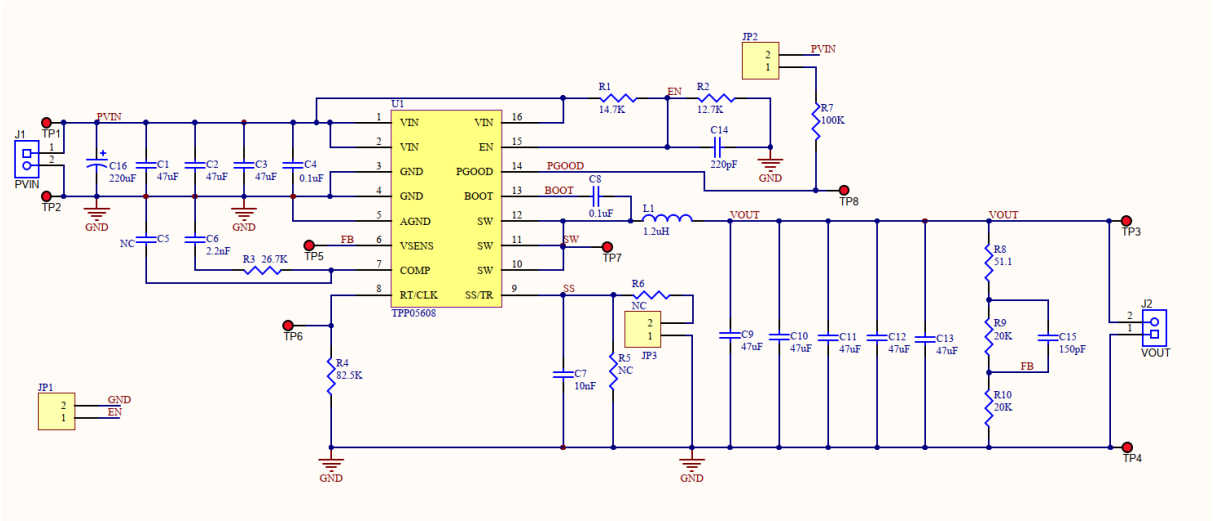


Figure 17. Typical Application Circuit

C4, C8	0.1 µF	Capacitor, ceramic, 50 V, X5R, 10%	0603	Std	Std
C5	Open	Capacitor, ceramic	0603	Std	Std
C6	2200 pF	Capacitor, ceramic, 50 V, X7R, 10%	0603	Std	Std
C7	0.01 µF	Capacitor, ceramic, 25 V, X7R, 10%	0603	Std	Std
C14	220 pF	Capacitor, ceramic, 50 V, C0G, 5%	0603	Std	Std
C15	150 pF	Capacitor, ceramic, 50 V, C0G, 5%	0603	Std	Std

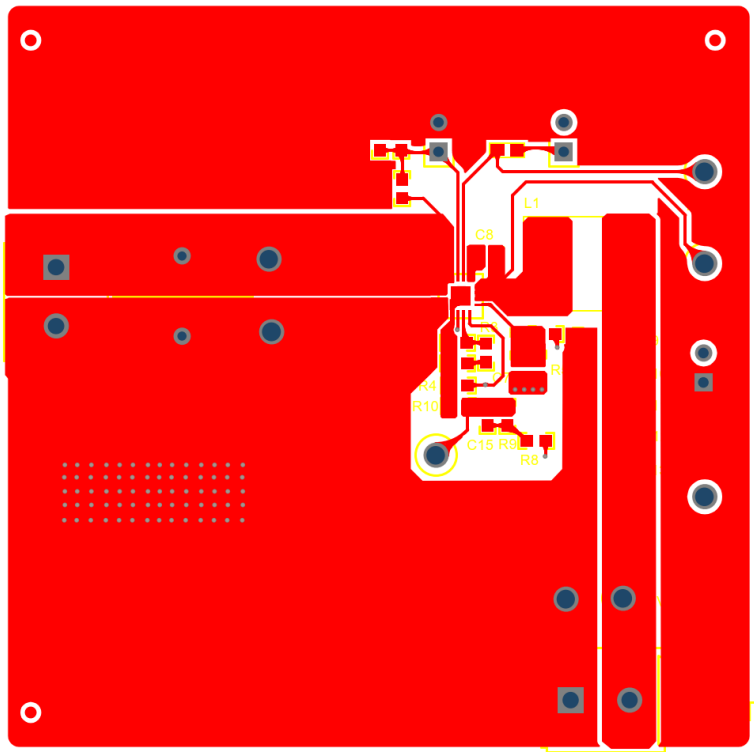
C1-3,C9-13	47 µF	Capacitor, ceramic, 10 V, X5R, ±20%	1206	Std	Std
C16	220 µF	Capacitor, Electrolytic, 25 VDC	8*8mm	860020474012	Wurth
L1	1.2 µH	Inductor, SMD Shielded Power, 11.8 A, 7.4 mΩ	5.3 × 5.5 mm	XAL5030-122ME	Coilcraft
R1	14.7 kΩ	Resistor, chip, 1/10W, 1%	0603	Std	Std
R2	12.7 kΩ	Resistor, chip, 1/10W, 1%	0603	Std	Std
R3	26.7 kΩ	Resistor, chip, 1/10W, 1%	0603	Std	Std
R4	82.5 kΩ	Resistor, chip, 1/10W, 1%	0603	Std	Std
R5-6	Open	Resistor, chip, 1/10W, 1%	0603	Std	Std
R7	100 kΩ	Resistor, chip, 1/10W, 1%	0603	Std	Std
R8	51.1 Ω	Resistor, chip, 1/10W, 1%	0603	Std	Std
R9, R10	20.0 kΩ	Resistor, chip, 1/10W, 1%	0603	Std	Std
U1	TPP05608	IC, 3-V to 6-V Input, 6-A Output, 2 MHz, Sync. Step-Down Switcher With Integrated FET	QFN	TPP05608	3peak

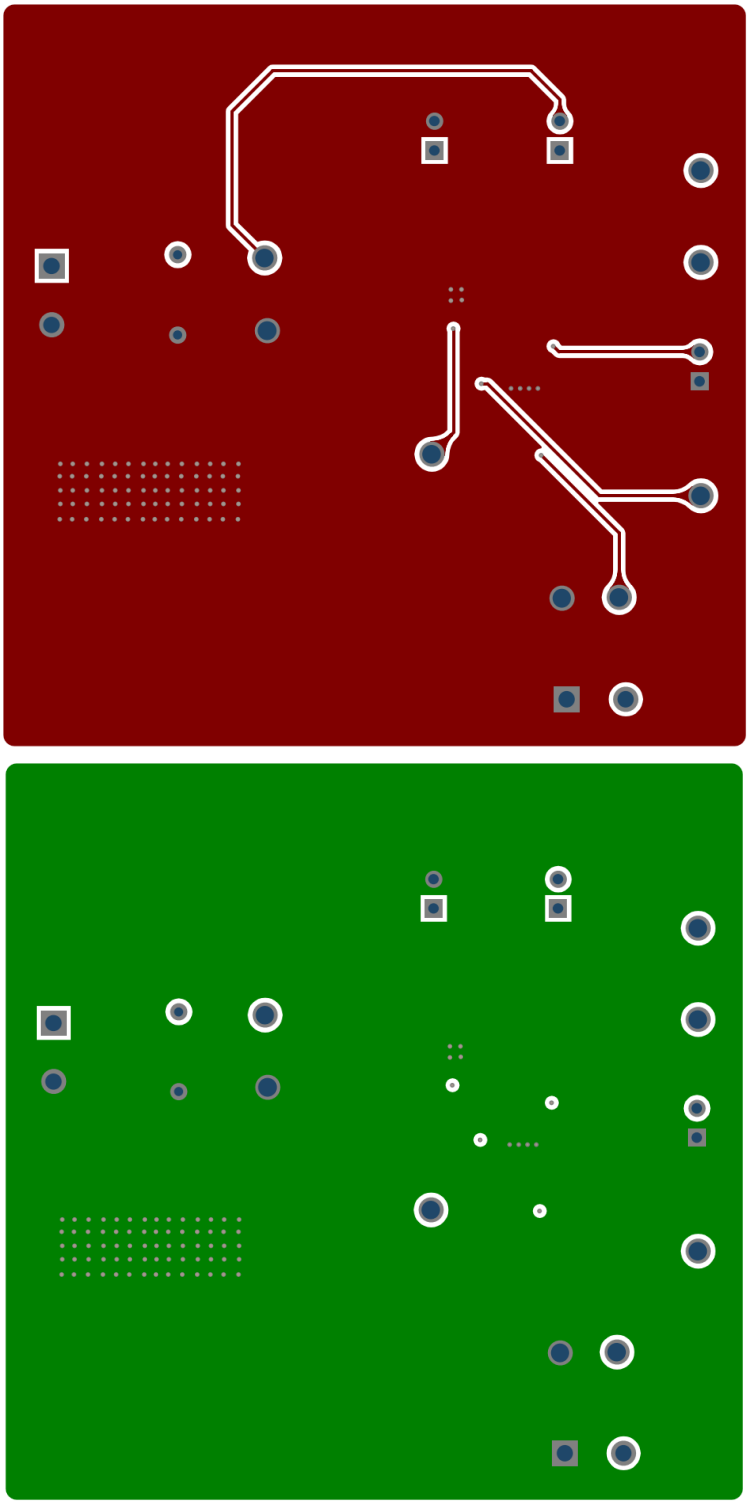
Layout

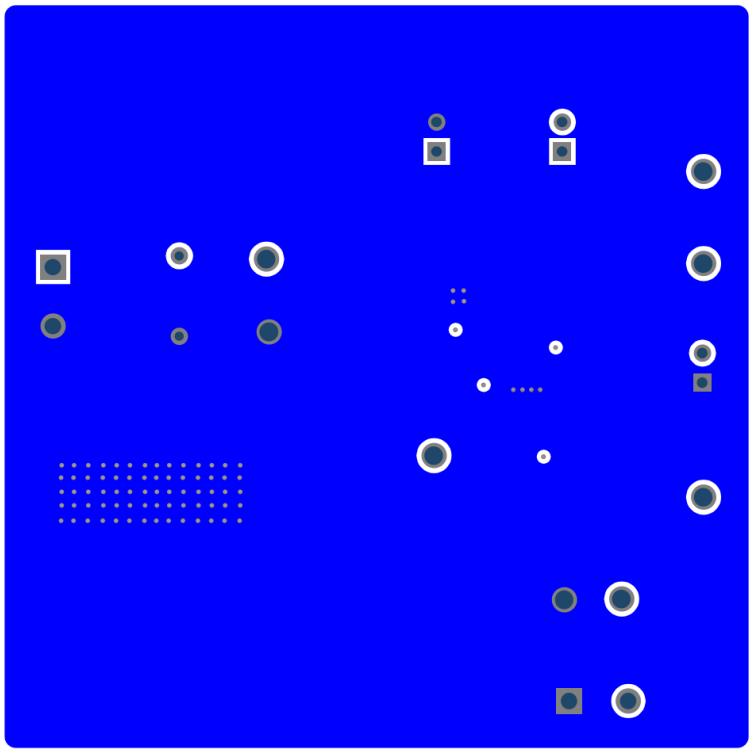
Layout Guideline

- Exposed pad must be connected to the PCB ground plane directly, the copper area must be as large as possible.
-

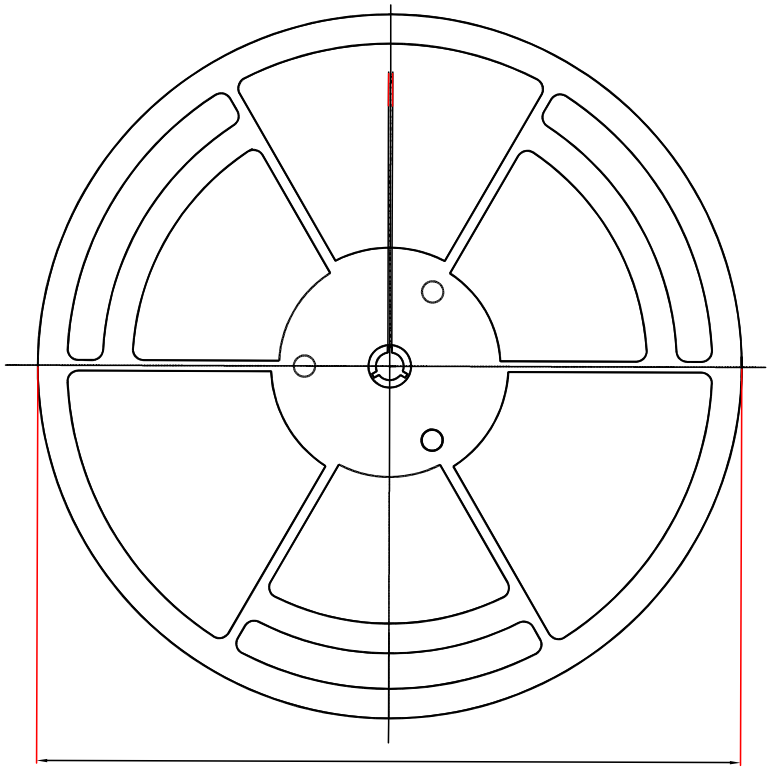
Layout Example

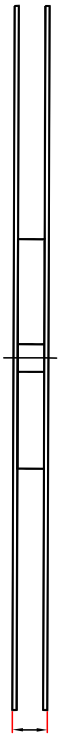


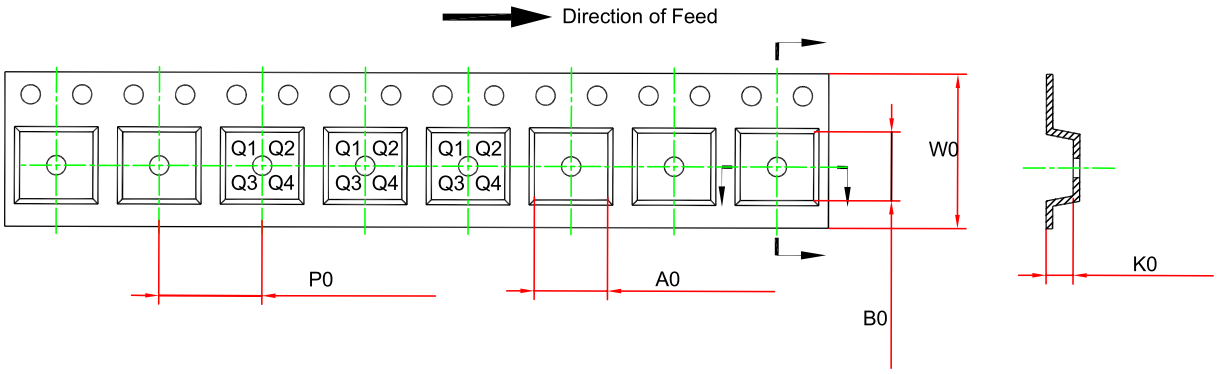




Tape and Reel Information





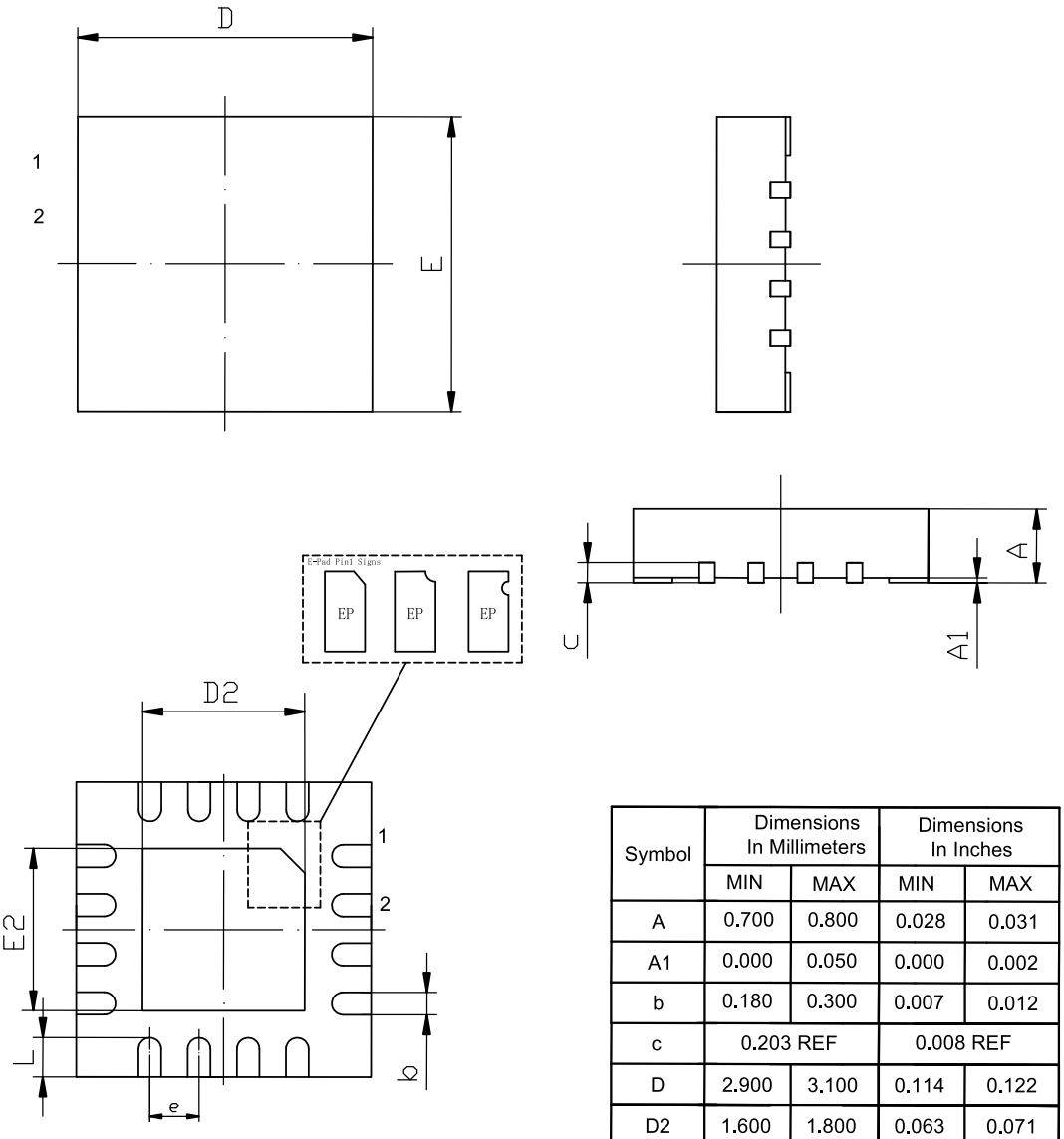


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPP056080-QFMR	QFN3X3-16	330	17.6	3.3	3.3	1	8	12	Q2

Package Outline Dimensions

QFN3X3-16-B

Package Outline Dimensions QFN(QFN3X3-16-B)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.180	0.300	0.007	0.012
c	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D2	1.600	1.800	0.063	0.071
E	2.900	3.100	0.114	0.122
E2	1.600	1.800	0.063	0.071
e	0.500 BSC		0.020 BSC	
L	0.250	0.500	0.010	0.020

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPP056080-QFMR	−40 to 125°C	QFN3X3-16	5680	3	Tape and Reel, 4000	Green

(1) For future products, contact the 3PEAK factory for more information and sample.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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