2.5-V to 5.5-V Input, 3-A Synchronous Step-Down Regulator in the SOT563 Package

Features

- Wide Input Voltage Range: 2.5 V to 5.5 V
- Output Adjustable from 0.6 V to the Input Voltage
- Low 100-nA (Typical) Shutdown Current and 25-μA (Typical) Quiescent Current
- 0.6 V ±1% Reference Voltage Accuracy
- Power-Save Mode or Forced-PWM Mode Version Available
- 2.2 MHz Switching Frequency
- Integrated 65-mΩ High-Side and 30-mΩ Low-Side Power MOSFETs
- Internal Soft Start-up with Pre-bias Output
- Enable Compatible with 1.2-V I/O Input
- 100% Duty Cycle Mode Operation
- Cycle-by-Cycle Current Limit and Hiccup When Overload or Short Circuit
- Available in the SOT563 (1.6 mm*1.6 mm) Package

Applications

- Router, Switch, and Access Point
- IP Camera, Drone
- TV, DVR, STB
- General Purpose Power Supply

Description

The TPP05301 is an easy-to-use, high-efficiency, synchronous, step-down regulator with integrated high-side and low-side MOSFETs. It provides up to 3-A output current and operates over a wide input voltage range.

The TPP05301 operates over a wide input voltage range from 2.5 V to 5.5 V with 25-μA ultra-low quiescent current. It is ideal for battery power systems due to its low quiescent current. The TPP05301 employs an adaptive- off time with a peak current control for fast loop response, simple loop design, and external components. The TPP05301 series supports power-saved mode to improve efficiency in light load operation and forced-PWM mode to maintain a fixed switching frequency and release low output ripple during all load conditions.

The TPP05301 has built-in robust protections such as thermal shutdown, UVLO, and enable (EN) control. Additionally, during the overload or short circuit condition, the cycle-by-cycle current limit and hiccup protection are provided. Thermal shutdown provides reliable and fault-tolerant operation. A power good signal indicates that the output voltage is in correct regulation.

The TPP05301 is available in the SOT563 (1.6 mm*1.6 mm) package.

Typical Application Circuit

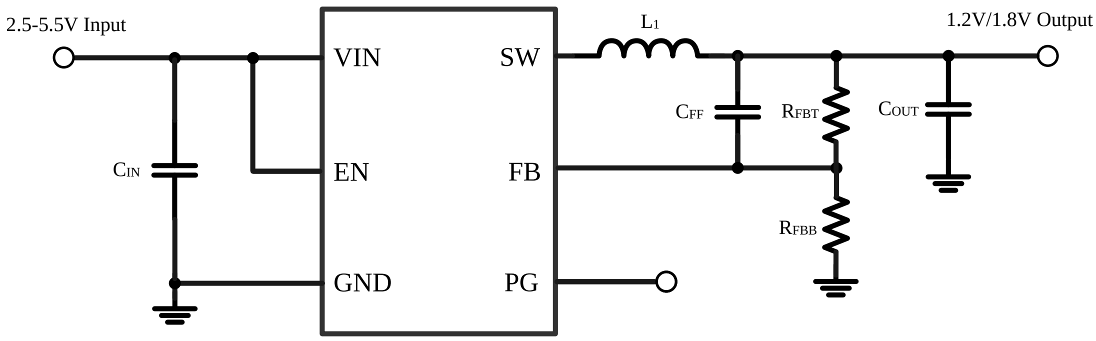


Table of Contents

Features 1
Applications 1
Description 1
Typical Application Circuit 1
Product Family Table 3
Revision History 3
Pin Configuration and Functions 4
Specifications 5
Absolute Maximum Ratings (1) 5
ESD, Electrostatic Discharge Protection 5
Recommended Operating Conditions 5
Thermal Information 5
Electrical Characteristics 6
Typical Performance Characteristics 8
Detailed Description 9
Overview 9
Functional Block Diagram 9
Feature Description 10
Application and Implementation 12
Application Information 12
Application Waveforms 15
Layout 20
Layout Guideline 20
Layout Recommendations 20
Tape and Reel Information 21
Package Outline Dimensions 22
SOT563-6 22
Order Information 23
IMPORTANT NOTICE AND DISCLAIMER 24

Product Family Table

Order Number	Light Load Mode
TPP053010-S56R	Power-Save Mode
TPP053011-S56R	Forced-PWM Mode

Revision History

Date	Revision	Notes
2025-04-15	Rev A.0	Initial released.

Pin Configuration and Functions

TPP05301
SOT563
Top View

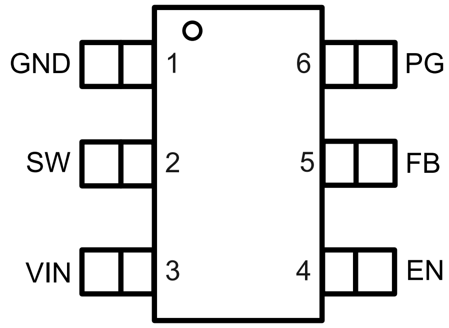


Table 1. Pin Functions: TPP05301

Pin	Name	I/O	Description
1	GND	G	Ground pin. Power and controller circuit ground. Use star connection to the GND pin with good contact.
2	SW	O	Switching output pin. Connect this pin to the external inductor.
3	VIN	I	Input voltage supply pin. Input capacitors should be placed as close to this pin and the PGND pin as possible.
4	EN	I	Enable input pin. The input signal to turn the regulator on or off, High = on, Low = off.
5	FB	I	Voltage feedback pin. Connect to the middle point of a feedback resistor divider to set the output value.
6	PG	O	Power-good indicator pin with open-drain output. Connect a pull-up resistor to the system voltage rail.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
VIN	Supply Voltage	−0.3	6	V
SW	Switching Node Voltage	−0.3	VIN + 0.3	V
SW	Switching Node Voltage (10 ns Transient)	−3	10	V
PG	Power Good Voltage	−0.3	6	V
FB	Feedback Voltage	−0.3	6	V
EN	Enable Input	−0.3	6	V
T_A	Operating Temperature Range	−40	150	°C
T_{STG}	Storage Temperature Range	−55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
V_{IN}	Supply Voltage	2.5	5.5	V
V_{EN}	Enable Input Voltage	0	V_{IN}	V
V_{OUT}	Output Voltage	0.6	V_{IN}	V
T_A	Ambient Temperature	−40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
SOT563	143.8	16.7	88.2	°C/W

Electrical Characteristics

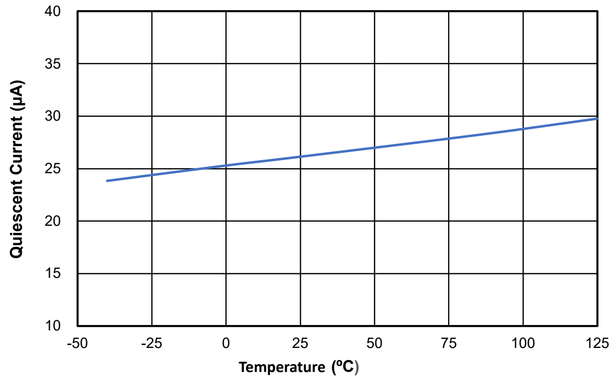
Unless otherwise noted, the min and max limits apply over the recommended operating ambient temperature range (T_A) of −40°C to 125°C. Typical values are measured under V_{IN} = 5 V and T_A = 25°C and represents the most likely parameters normally for reference.

Parameter		Condition	Min	Typ	Max	Unit
Power Supply						
V_{IN}	Supply Voltage Range		2.5		5.5	V
V_{IN_UV}	Under Voltage Lockout Thresholds	Rising Threshold	2.3	2.4	2.5	V
		Falling Threshold		2.3		V
I_{SD}	Shutdown Supply Current	V_{EN} = 0 V		0.1		μA
I_Q	Non-Switching Quiescent Current	V_{EN} = High, Non-Switching		25		μA
Enable						
V_{EN_H}	Enable High Threshold	Rising Threshold			0.88	V
V_{EN_L}	Enable Low Threshold	Hysteresis	0.33			V
I_{EN_LKG}	Enable Input Leakage Current	V_{EN} = High		10		nA
Soft Start						
Tss	Internal Soft-Start Time				1.3	ms
Voltage Reference						
V_{FB}	Feedback Voltage	2.5 V ≤ V_{IN} ≤ 5.5 V	594	600	606	mV
V_{FB}	Feedback Voltage	T_A = -40°C to +125°C	588	600	612	mV
I_{FB_LKG}	Feedback Input Leakage Current	V_{FB} = 0.6 V		10		nA
MOSFETs						
R_{DSON_H}	High Side MOSFET ON Resistance	V_{IN} = 5 V		65		mΩ
R_{DSON_L}	Low Side MOSFET ON Resistance	V_{IN} = 5 V		30		mΩ
Current Limits						
I_{LIMIT_H}	High Side Current Limit	Inductor Peak Current, V_{IN} = 3.3 V	3.8	4.6	5.6	A
I_{LIMIT_L}	Low Side Current Limit	Inductor Valley Current, V_{IN} = 3.3 V		4.3		A
I_{LIMIT_N}	Negative Current Limit			-2		A
Power Good						
V_{PG_HR}	Power Good High Threshold	Rising Threshold, % of V_{FB}		110		%
V_{PG_LF}	Power Good Low Threshold	Falling Threshold, % of V_{FB}		94.5		%
V_{PG_HYST}	Power Good Threshold Hysteresis	% of V_{FB}		1.5		%
t_{PG_F}	Power Good Delay Falling			20		μs
t_{PG_R}	Power Good Delay Rising			20		μs
I_{PG_LKG}	Power Good Leakage Current, Open Drain Output is High	V_{PG} = 5 V			100	nA
V_{PG_LOW}	Power Good Output Low-level Voltage	V_{IN} = 5 V, I_{PG} = 1 mA			400	mV

Parameter		Condition	Min	Typ	Max	Unit
Output Discharge						
I_{DISCHG}	Output Discharge Current on SW	V_{IN} = 3 V, V_{OUT} = 2 V		90		mA
Switching Frequency Timing						
f_{SW}	Switching Frequency, FPWM Mode	V_{IN} = 5 V, V_{OUT} = 1.8 V		2200		kHz
Thermal Shutdown						
T_{SD}	Thermal Shutdown			160		°C
T_{SD_HYS}	Thermal Shutdown Hysteresis			20		°C

Typical Performance Characteristics

All test conditions: V_{IN} = 5 V, V_{OUT} = 1.8 V, PFM mode, T_A = 25 °C, unless otherwise noted.



V_{FB} = 0.65 V

Figure 1. Non-Switching Quiescent Current

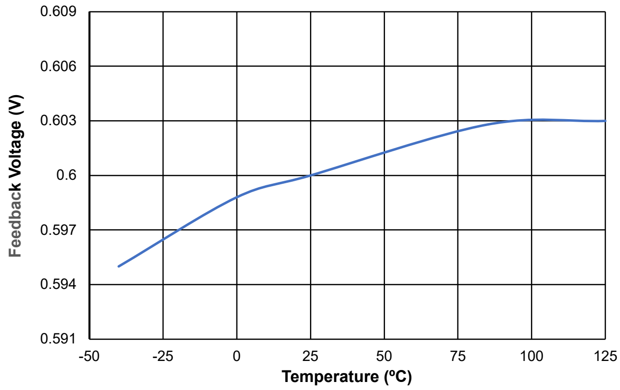


Figure 2. Feedback Voltage

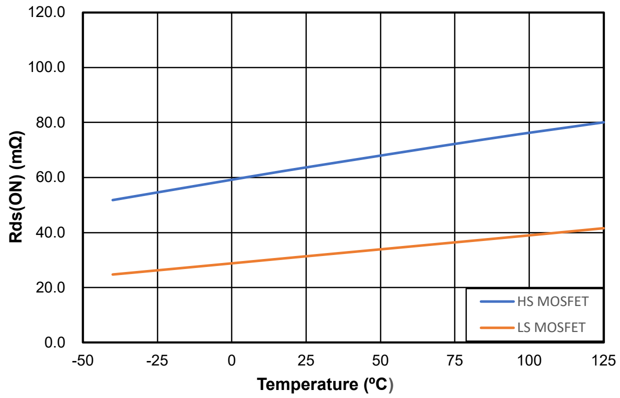


Figure 3. High-Side and Low-Side MOSFET

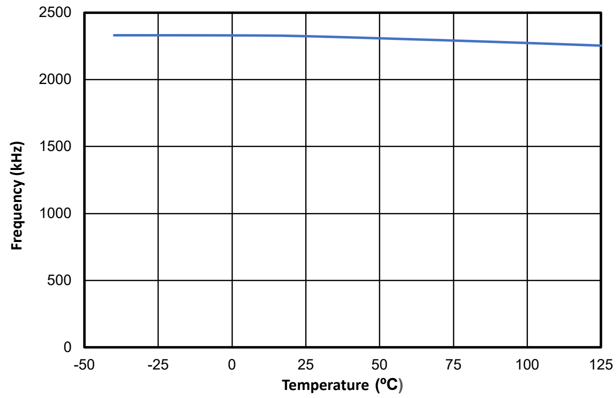


Figure 4. Switching Frequency

Detailed Description

Overview

The TPP05301 is an easy-to-use, high-efficiency, synchronous, step-down regulator with integrated high-side and low-side MOSFETs. It provides up to 3-A output current and operates over a wide input voltage range.

The TPP05301 operates over a wide input voltage range from 2.5 V to 5.5 V with 25-μA ultra-low quiescent current. It is ideal for battery power systems due to its low quiescent current. The TPP05301 employs an adaptive- off time with a peak current control for fast loop response, simple loop design, and external components. The TPP05301 series supports power-saved mode to improve efficiency in light load operation and forced-PWM mode to maintain a fixed switching frequency and release low output ripple during all load conditions.

The TPP05301 has built-in robust protections such as thermal shutdown, UVLO, and enable (EN) control. Additionally, during the overload or short circuit condition, the cycle-by-cycle current limit and hiccup protection are provided. Thermal shutdown provides reliable and fault-tolerant operation. A power good signal indicates that the output voltage is in correct regulation.

Functional Block Diagram

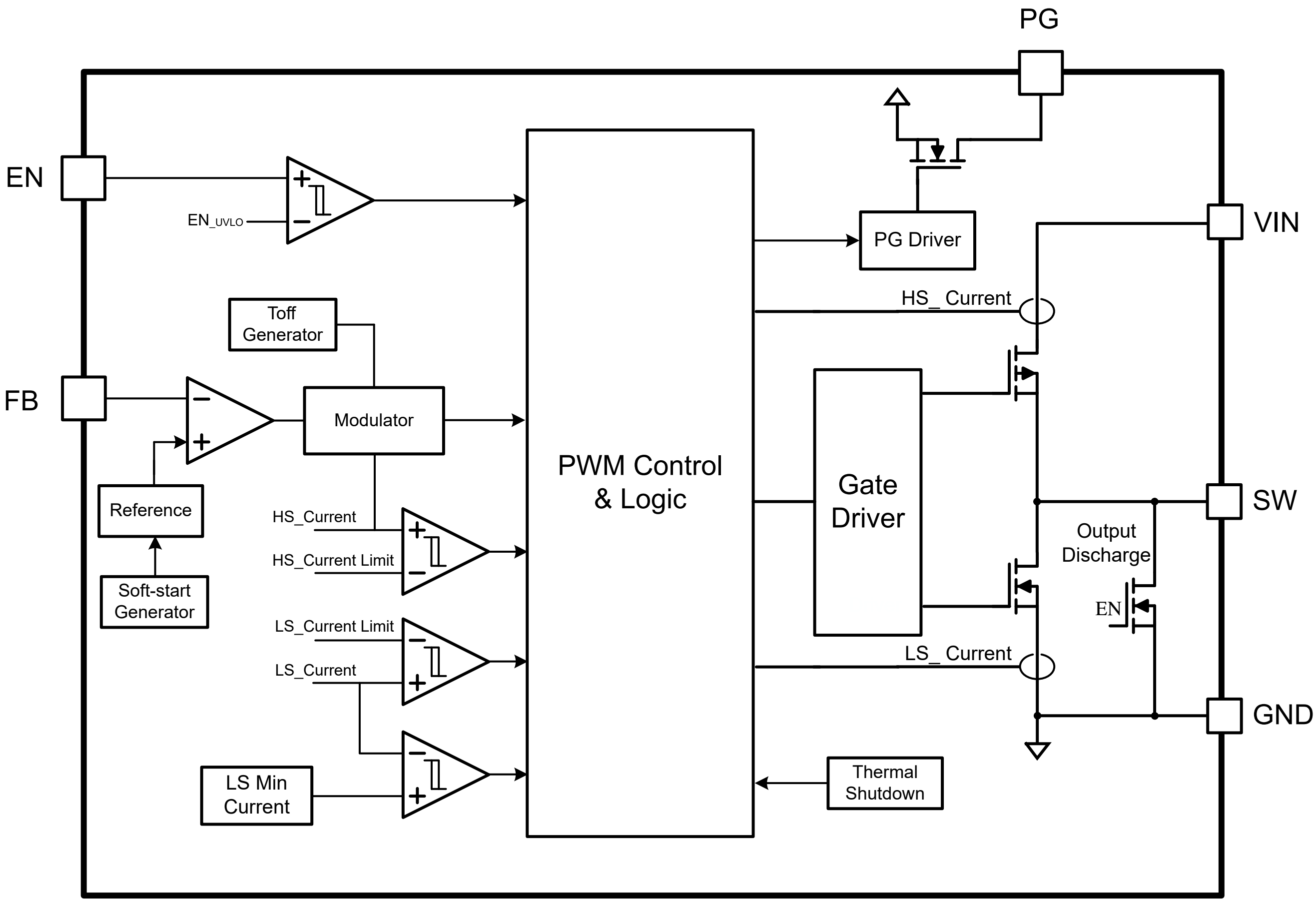


Figure 5. Functional Block Diagram

Feature Description

Adaptive-off Time with Peak Current Control

The TPP05301 adopts adaptive-off time with peak current control. The feedback voltage is sensed from the resistor divider through the FB pin to compare with the internal voltage reference. The required off time for the low-side MOSFET is calculated based on the input and output voltage, making the switching frequency relatively constant regardless of different duty cycles and load current.

Light Load Operation

The TPP05301 integrates two behaviors in light-load operation. One behavior is power-saved mode (PSM) control to improve efficiency in light load working condition. When the loading current decreases, the device approaches discontinuous conduction mode and the low-side MOSFET is turned off when the zero current detection is triggered to improve system efficiency. In this operation, the device reduces the switching frequency and minimizes the current consumption. In power-saved mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor or adding a feedforward capacitor.

The other behavior is forced-PWM mode (FPWM) to optimize the output ripple. In FPWM mode, the device operates in continuous conduction mode during light load operation, and the switching frequency is almost constant over the entire load range. To maintain the switching frequency, a limited negative current is allowed to flow through the inductor and low-side power switch.

100% Duty Cycle Operation

The TPP05301 offers a low input-to-output voltage difference by entering 100% duty cycle operation. In this operation, the high-side MOSFET is constantly turned on, and the low-side MOSFET is switched off.

Soft-Start with Pre-Biased Capability

The TPP05301 implements a soft-start circuit to prevent the inrush current during start-up. The soft-start time is fixed internally. When the start-up period begins, the internal reference voltage slowly ramps up.

The TPP05301 also supports a monotonic start-up with pre-biased loads. If the output voltage is pre-biased to a certain value during start-up, the device disables switching for both high-side and low-side power switches until the soft-start reference voltage exceeds the feedback voltage.

Power Good

The device employs an open-drain output PG signal to check whether the output voltage is operating within the normal range. The external pull-up voltage resource is recommended to be less than 5.5 V with a 1-kΩ resistor. Once the feedback voltage is lower than 94.5% or greater than 109% of the internal reference voltage, the PG is pulled low.

Undervoltage Lockout (UVLO) Protection

Once the input voltage falls below the UVLO threshold, the device is shut off. Once the device recovers above the UVLO threshold, the device returns to normal operation.

Current Limits

The TPP05301 employs both cycle-by-cycle peak and valley current limits to protect the high-side and low-side MOSFET overloaded. Once the inductor current reaches the high-side peak current limit, the high-side switch is turned off immediately to avoid the inductor current from further increasing. When the low-side valley current limit is triggered, the next duty cycle is held until the inductor current recovers within the valley current limit. Both peak and valley current limits determine the device's maximum output current, and the valley current limit can prevent inductor current from running away during unexpected overload or short circuit conditions. Also, the device integrates one zero-current detector to turn off the low-side MOSFET at light loads of the PFM version.

Thermal Shutdown

Once the junction temperature rises above the internal over-temperature shutdown threshold, the device shuts off and recovers when the temperature falls below the threshold with hysteresis.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPP05301 is typically used to convert a wide range of input voltage to the desired output voltage, which can be set by the feedback resistor dividers. Some typical parameters and external component values are recommended to help speed up the developing process. In most power systems, a lower voltage rail, such as 1.2 V/1.8 V, is typically used for microcontrollers, I/Os, and other low-voltage components.

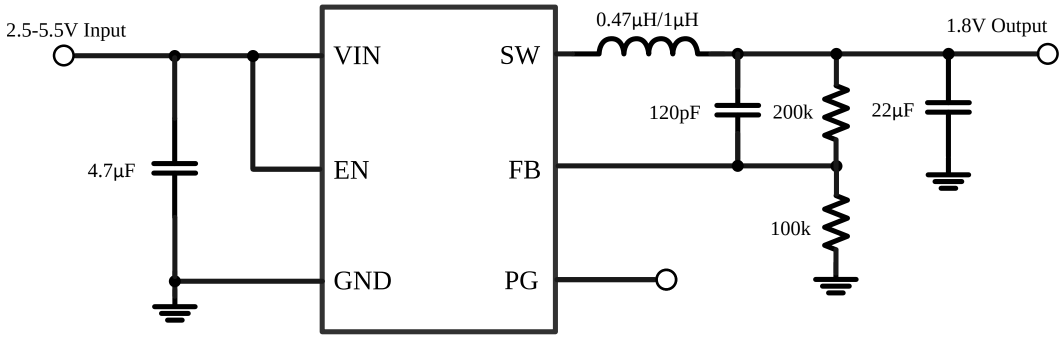


Figure 6. Typical Application Circuit

Setting Output Voltage

The external resistor divider network connected to the FB pin sets the output voltage. The resistance of the divider is a compromise between noise suppression and output current consumption. The smaller value resistor will reduce noise sensitivity but will also increase the system's quiescent current and reduce light load efficiency. Once the top feedback resistor is selected, the feedback resistors value can be calculated with the following equation.

$$R_{FBB} = \frac{V_{FB} * R_{FBT}}{V_{OUT} - V_{FB}} \quad (1)$$

where V_{FB} is the internal reference voltage which is typical 0.6 V for TPP05301.

Inductor Selection

The selection of the inductor affects steady-state operation as well as transient behavior and loop stability. These factors make it the most important component in power regulator design. There are three important inductor specifications: inductor value, dc resistance, and saturation current. The inductor value is designed based on the desired peak-to-peak ripple current and is typically chosen to be in the range of 20% to 40% of the maximum output current. Once the desired inductor ripple current is selected, the inductor value can be calculated with the following equation.

$$L = \frac{V_{OUT}}{f_{SW} * \Delta I_L} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (2)$$

where f_{SW} is the switching frequency and ΔI_L is the inductor ripple current.

When the inductor current approaches its saturation level, the effective inductance can fall to a fraction of the zero current value. Although one high-side valley current limit is integrated to avoid the current run-away, the inductor current can rise to a high value very rapidly if the inductor is saturated. The inductor saturation current must leave a safe margin from the high-side peak current limit in the worst-case conditions. The inductor's RMS current and peak current can be calculated with the equation below.

$$I_{L\_PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (3)$$

$$I_{L\_RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}} \quad (4)$$

Input Capacitor Selection

The input capacitor of the step-down converter is used to supply the AC input current and maintain a stable DC input voltage. At least a 10-μF capacitance of ceramic input capacitor is recommended. Additional input capacitance may be required to meet ripple and/or transient requirements. High-quality ceramic, X5R or X7R, is recommended because of its low ESR characteristic and small capacitance variations over the temperature range. In addition, one small value and small case size, ceramic capacitor (such as 100nF, 0603 package) is recommended to be used at the input and be placed as close as possible to the VIN and GND pins. This can provide a high -frequency bypass for the internal control circuits. The input capacitor can be calculated with the equation below when the input voltage ripple is determined.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} * C_{IN}} * \frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

where C_{IN} is the input capacitance value.

The input capacitor ripple current rating should be greater than the maximum input current ripple. The RMS current of the input capacitor can be calculated with the following equation.

$$I_{CIN\_RMS} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (6)$$

The worst case for the input voltage ripple and RMS current occurs when the duty cycle is 50%.

Output Capacitor Selection

The output capacitance is mainly selected to meet the requirement of the output ripple and voltage change during a load transient. Then the control loop is compensated for the output capacitor selected. The output voltage ripple is related to the capacitance and equivalent series resistance (ESR) of the output capacitor. Assuming the capacitor with a small ESR, the minimum output capacitance needed for a given output ripple voltage can be calculated with the equation below.

$$C_{OUT} > \frac{\Delta I_L}{8 * f_{SW} * \Delta V_{OUT}} \quad (7)$$

where ΔI_L is the inductor ripple current, and ΔV_{VOUT} is the output voltage ripple.

If high ESR capacitors are used, it will contribute additional output ripple. ESR ripple can be neglected for ceramic capacitors but must be considered if electrolytic capacitors are used. The maximum ESR for a given ripple can be calculated with the below equation.

$$R_{ESR} < \frac{\Delta V_{OUT}}{\Delta I_L} - \frac{1}{8 * f_{SW} * C_{OUT}} \quad (8)$$

The effective value of the ceramic capacitor decreasing should be considered when the output DC bias voltage is added across the capacitors. The RMS current of the output capacitor can be calculated with the following equation.

$$I_{COUT\_RMS} = \frac{V_{OUT} * (V_{IN\_MAX} - V_{OUT})}{\sqrt{12} * V_{IN\_MAX} * L * f_{SW}} \quad (9)$$

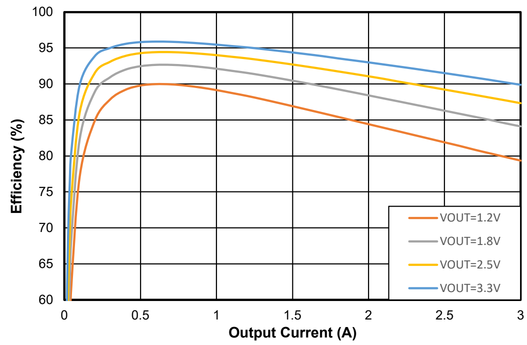
where V_{IN_MAX} is the maximum input voltage, L is the selected inductor value.

Feed Forward Capacitor Selection

A feed-forward capacitor reduces the output ripple in PFM mode and improves the load transient response. A 120-pF feed-forward capacitor is recommended for the 1.8-V output in the typical application.

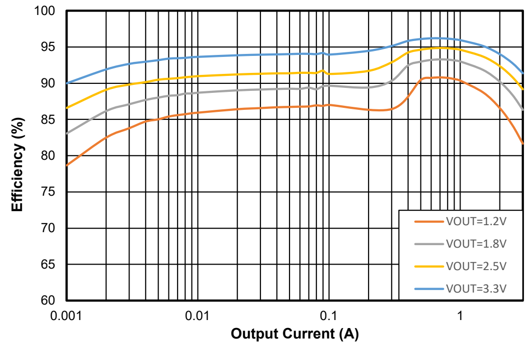
Application Waveforms

All test conditions: V_{IN} = 5 V, V_{OUT} = 1.8 V, PFM mode, T_A = 25 °C, unless otherwise noted.



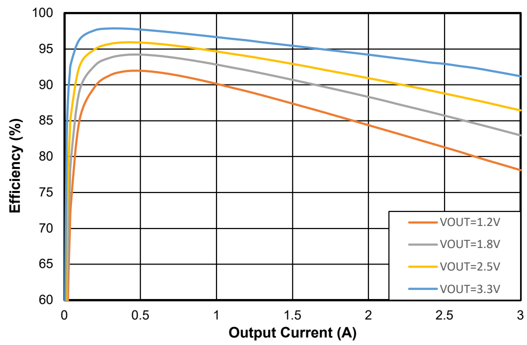
FPWM Mode

Figure 7. Efficiency



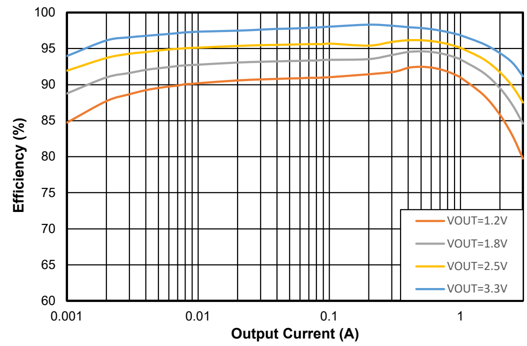
PFM Mode

Figure 8. Efficiency



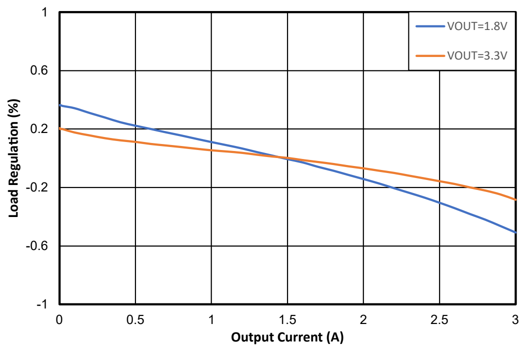
V_{IN} = 3.6 V, FPWM Mode

Figure 9. Efficiency



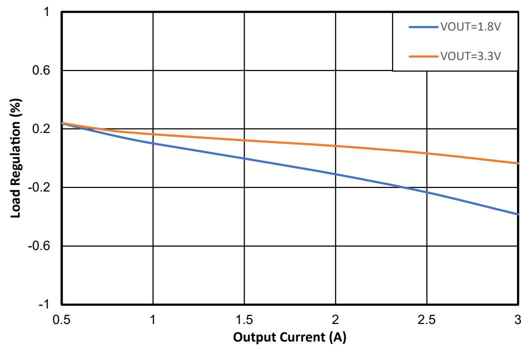
V_{IN} = 3.6 V, PFM Mode

Figure 10. Efficiency



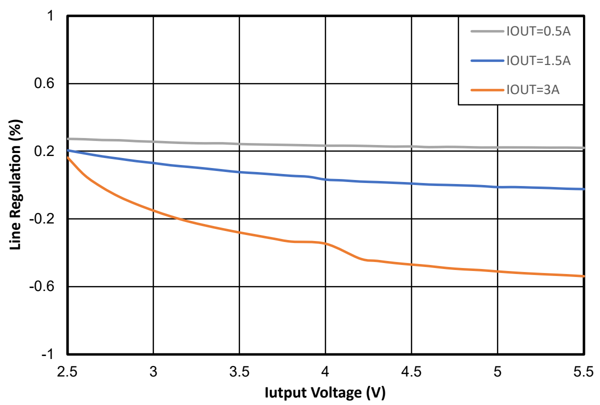
FPWM Mode

Figure 11. Load Regulation



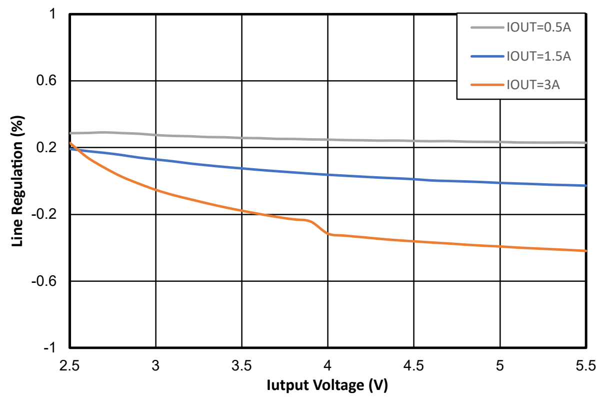
PFM Mode

Figure 12. Load Regulation



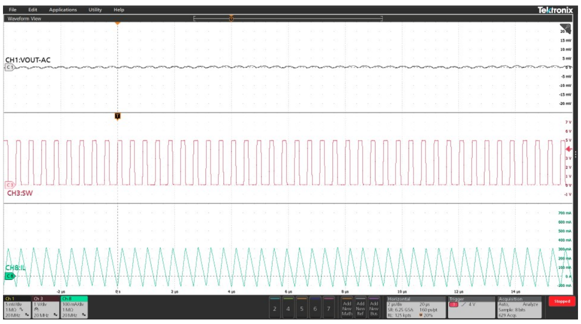
FPWM Mode

Figure 13. Line Regulation



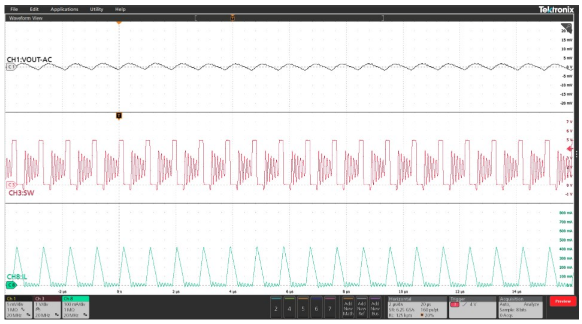
PFM Mode

Figure 14. Line Regulation



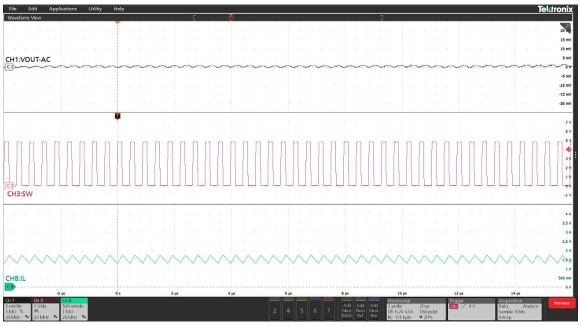
I_{OUT} = 0.1 A, FPWM Mode

Figure 15. Switching Waveform and Output Ripple



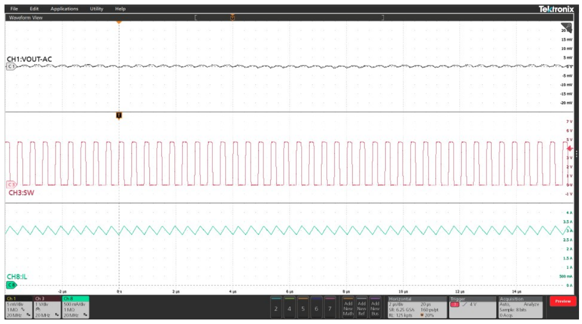
I_{OUT} = 0.1 A, PFM Mode

Figure 16. Switching Waveform and Output Ripple



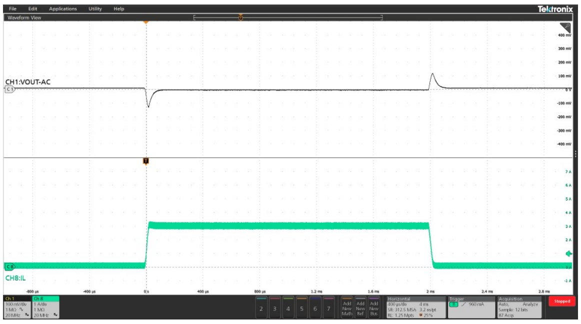
I_{OUT} = 1.5 A

Figure 17. Switching Waveform and Output Ripple



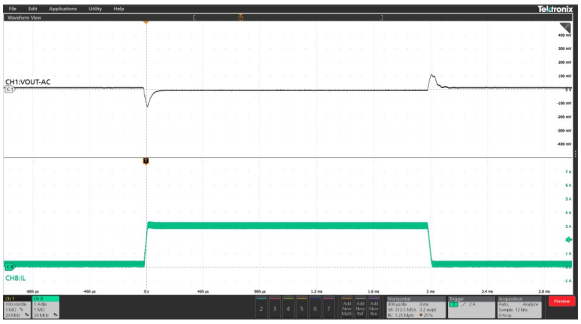
I_{OUT} = 3 A

Figure 18. Switching Waveform and Output Ripple



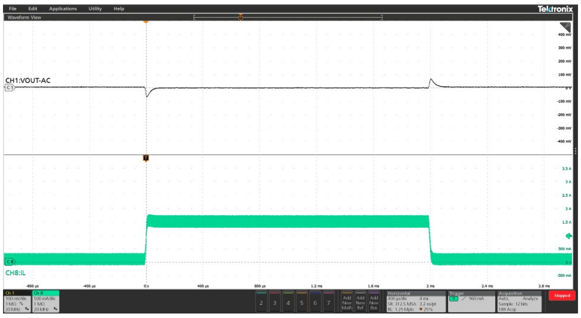
I_{OUT} = 0.1 A to 3 A to 0.1 A, FPWM Mode

Figure 19. Load Transient



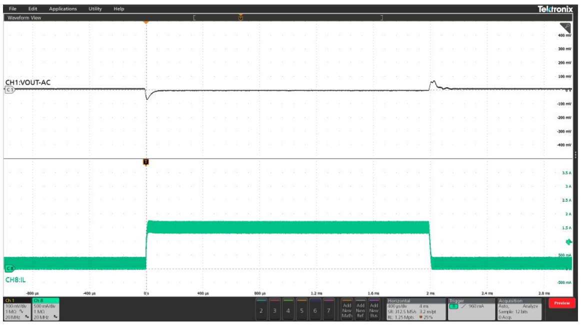
I_{OUT} = 0.1 A to 3 A to 0.1 A, PFM Mode

Figure 20. Load Transient



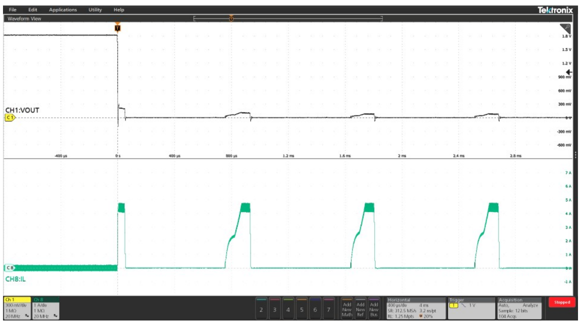
I_{OUT} = 0.1 A to 1.5 A to 0.1 A, FPWM Mode

Figure 21. Load Transient



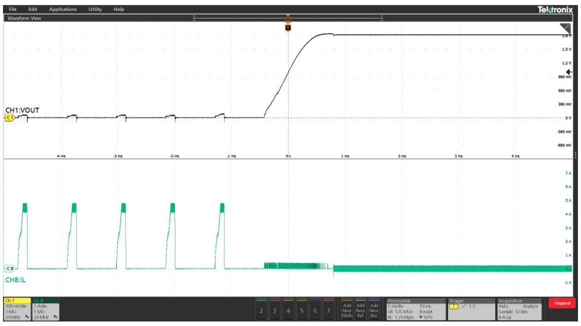
I_{OUT} = 0.1 A to 1.5 A to 0.1 A, PFM Mode

Figure 22. Load Transient



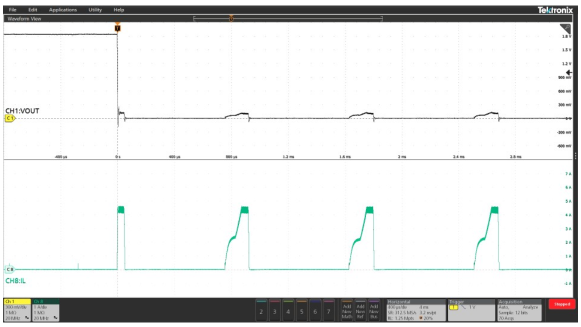
I_{OUT} = 0 A, FPWM Mode, Entry

Figure 23. Short Circuit Protection



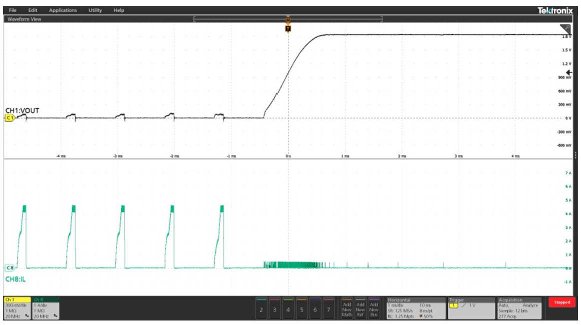
I_{OUT} = 0 A, FPWM Mode, Recovery

Figure 24. Short Circuit Protection



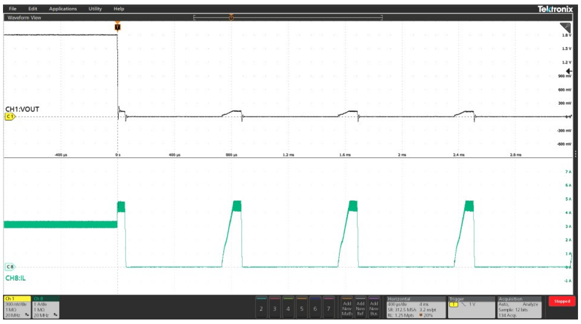
I_{OUT} = 0 A, PFM Mode, Entry

Figure 25. Short Circuit Protection



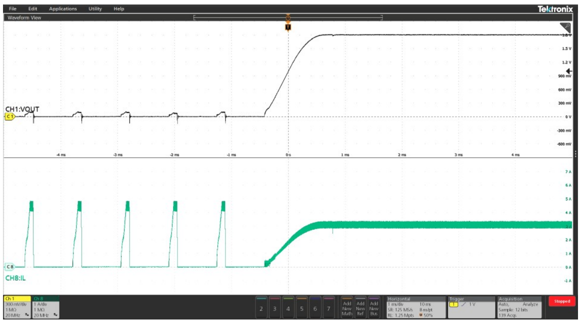
I_{OUT} = 0 A, PFM Mode, Recovery

Figure 26. Short Circuit Protection



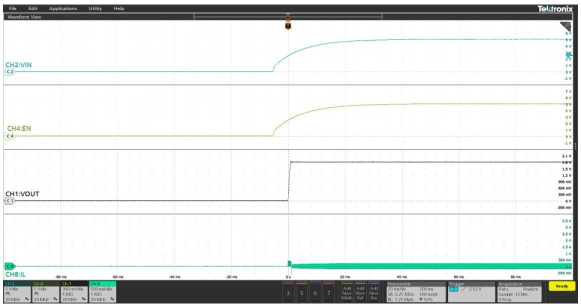
I_{OUT} = 3 A, Entry

Figure 27. Short Circuit Protection



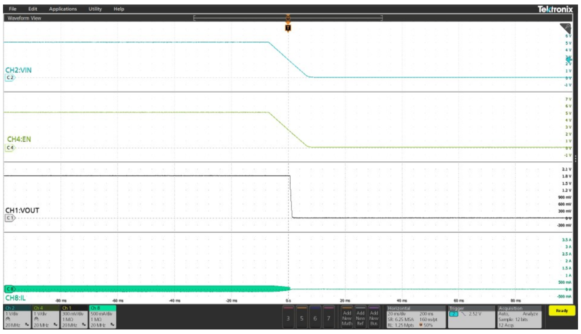
I_{OUT} = 3 A, Recovery

Figure 28. Short Circuit Protection



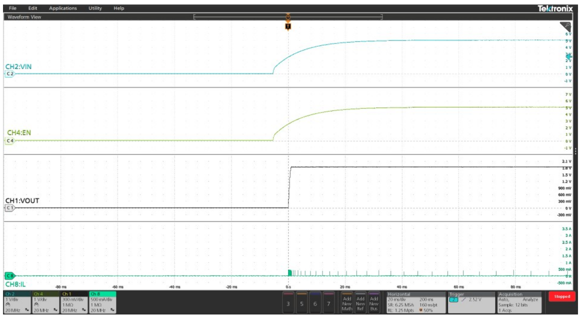
I_{OUT} = 0 A, FPWM Mode

Figure 29. Power up by Inputs



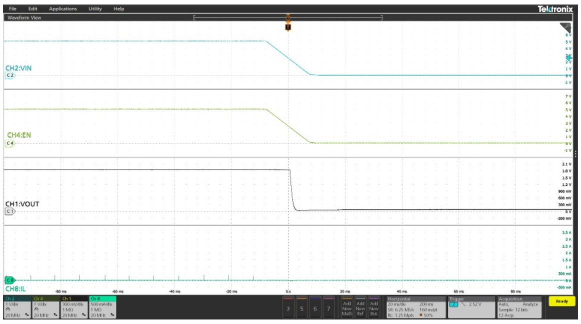
I_{OUT} = 0 A, FPWM Mode

Figure 30. Power down by Inputs



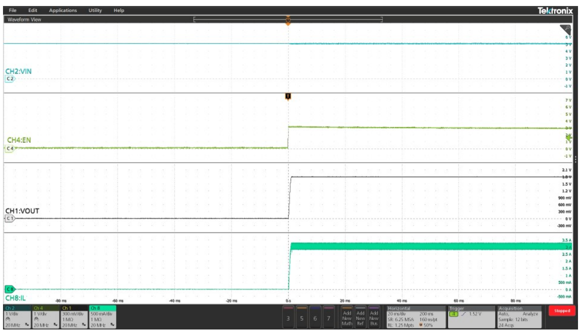
I_{OUT} = 0 A, PFM Mode

Figure 31. Power up by Inputs



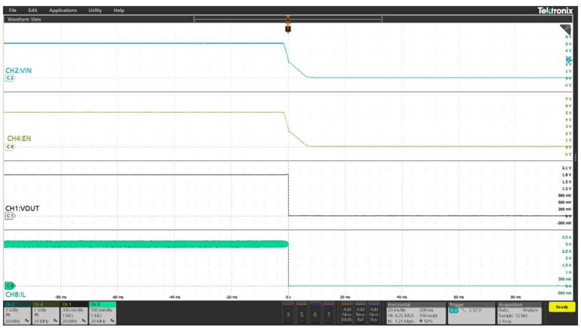
I_{OUT} = 0 A, PFM Mode

Figure 32. Power down by Inputs



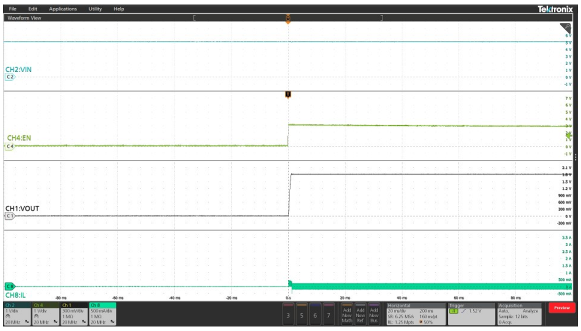
I_{OUT} = 3 A, FPWM Mode

Figure 33. Power up by Inputs



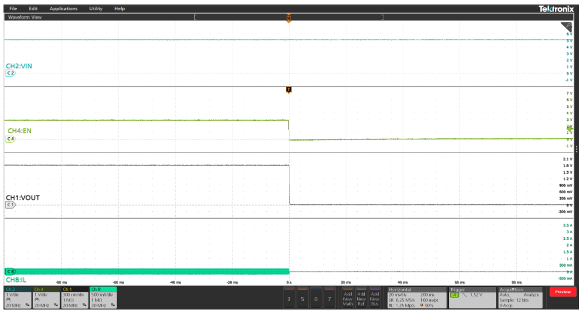
I_{OUT} = 3 A, FPWM Mode

Figure 34. Power down by Inputs



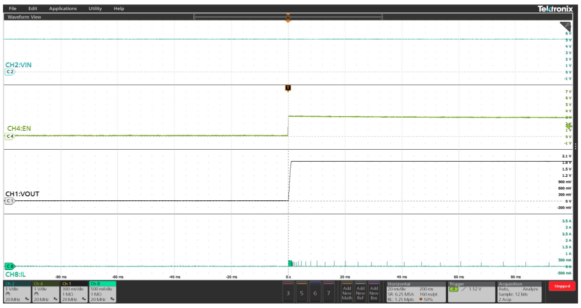
I_{OUT} = 0 A, FPWM Mode

Figure 35. Power up by Enable



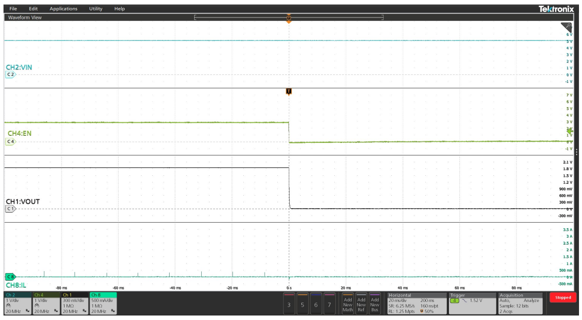
I_{OUT} = 0 A, FPWM Mode

Figure 36. Power down by Enable



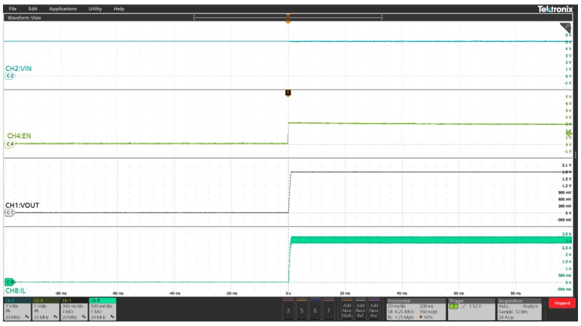
I_{OUT} = 0 A, PFM Mode

Figure 37. Power up by Enable



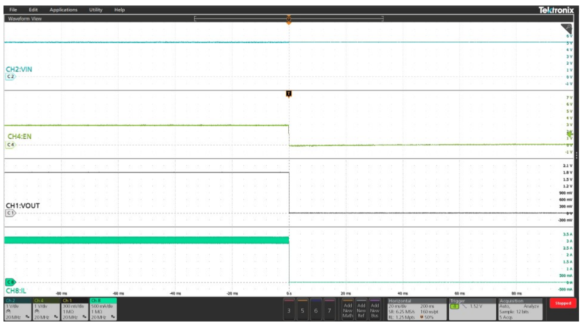
I_{OUT} = 0 A, PFM Mode

Figure 38. Power down by Enable



I_{OUT} = 3 A, FPWM Mode

Figure 39. Power up by Enable



I_{OUT} = 3 A, FPWM Mode

Figure 40. Power down by Enable

Layout

Layout Guideline

The performance of switching converters heavily depends on the quality of the PCB layout. especially for thermal design and EMI design. Even if the schematic design is good, a bad PCB layout can disrupt the converter's operation.

1. Place a low ESR ceramic capacitor as close to the VIN pin and the ground as possible.
2. Make sure the top switching loop with power has the lowest impendence of grounding.
3. The output inductor should be placed close to the SW pin to minimize the SW area.
4. The FB terminal is sensitive to noise so the feedback resistor should be located as close as possible to the IC.
5. Keep the connection of the input capacitor and VIN as short and wide as possible.

Layout Recommendations

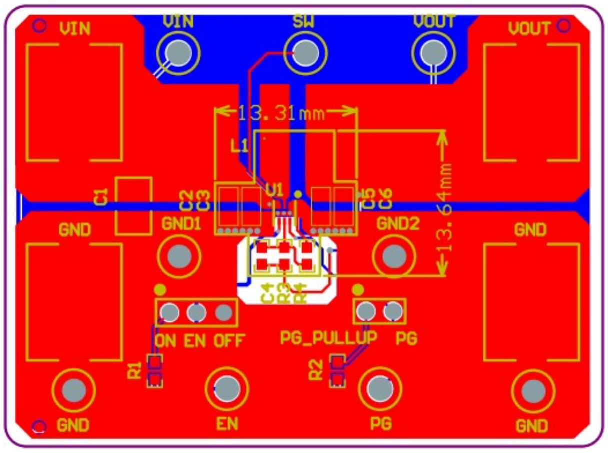
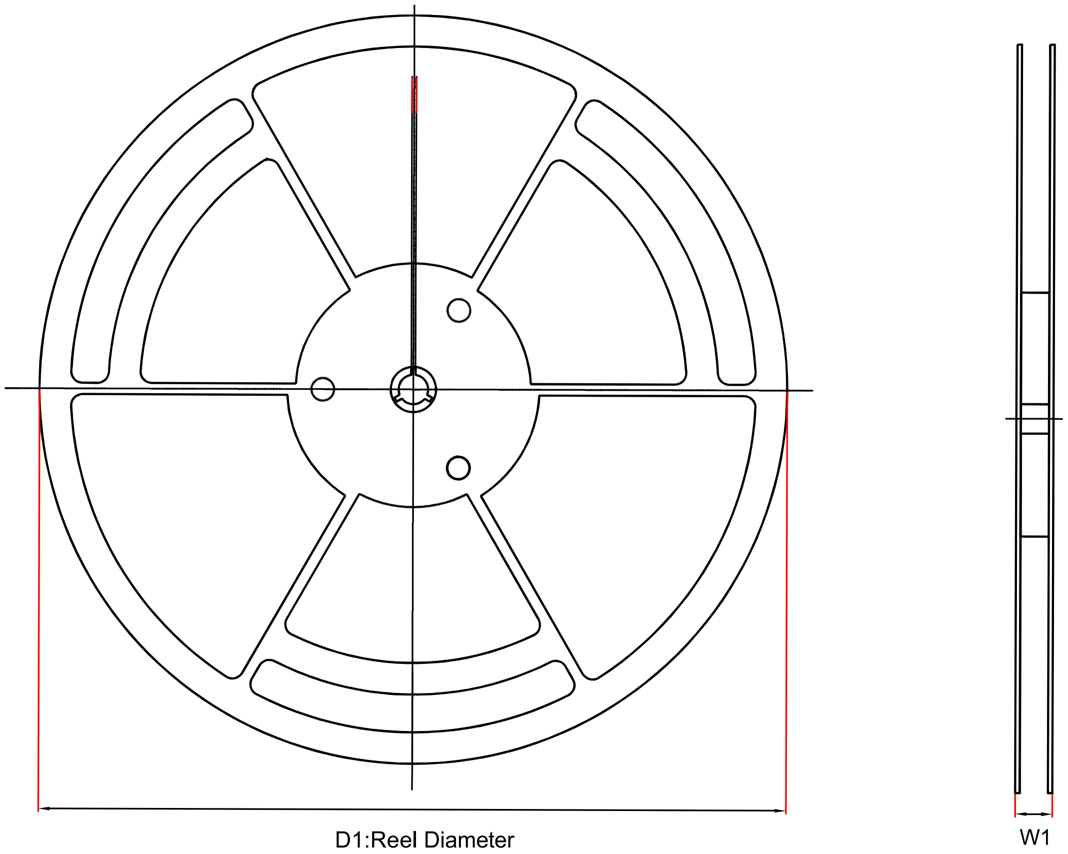
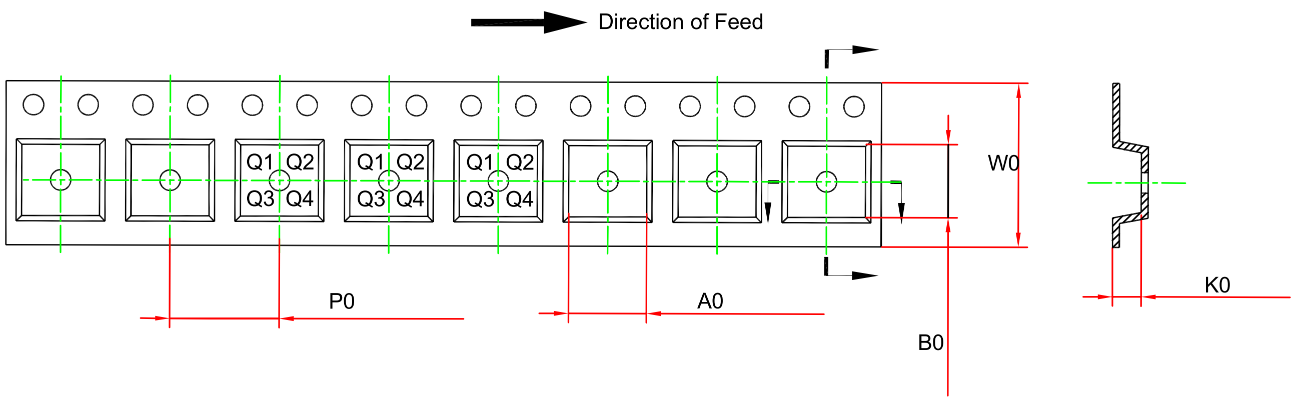


Figure 41. Layout Example

Tape and Reel Information



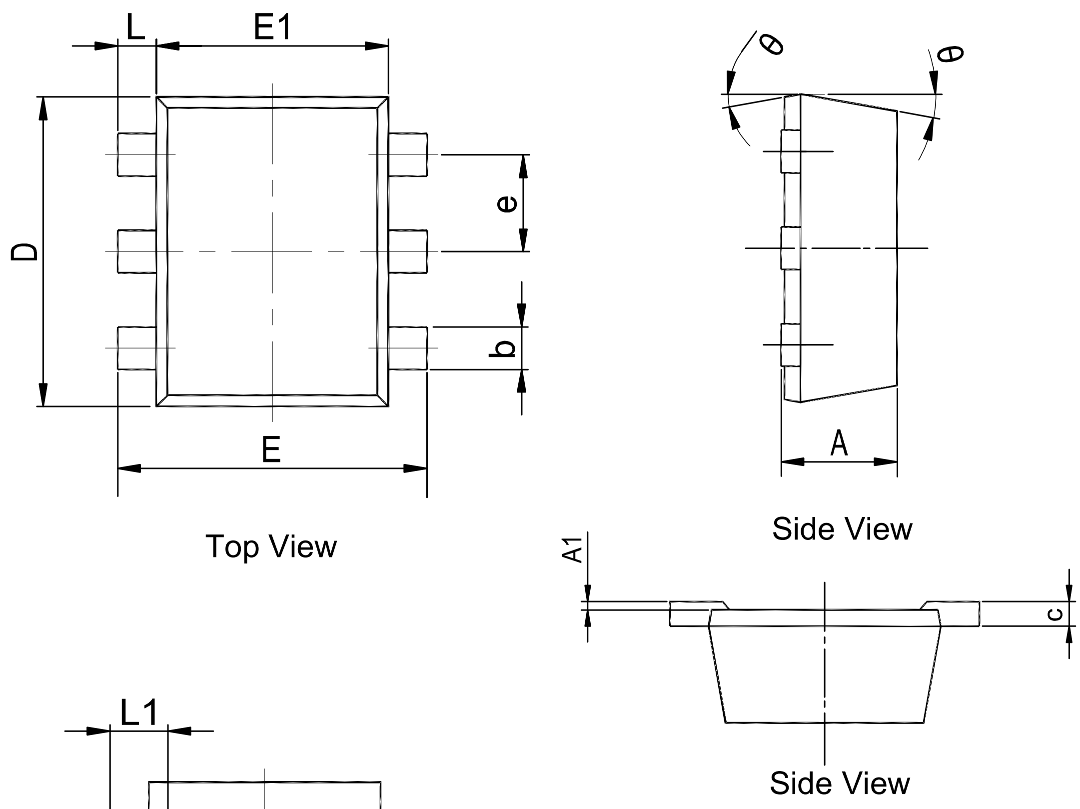


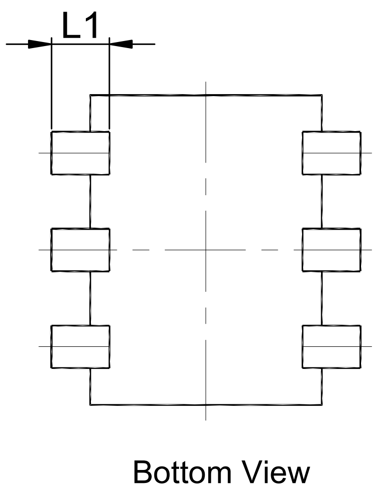
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPP053010-S56R	SOT563	180	13.1	1.78	1.78	0.69	4.0	8.0	Q3
TPP053011-S56R	SOT563	180	13.1	1.78	1.78	0.69	4.0	8.0	Q3

Package Outline Dimensions

SOT563-6

Package Outline Dimensions S56(SOT563-6-A)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.525	0.600	0.021	0.024
A1	0.000	0.050	0.000	0.002
b	0.170	0.270	0.007	0.011
c	0.090	0.180	0.004	0.007
D	1.500	1.700	0.059	0.067
E	1.500	1.700	0.059	0.067
E1	1.100	1.300	0.043	0.051
e	0.450	0.550	0.018	0.022
L	0.260	0.460	0.010	0.018
L1	0.200	0.400	0.008	0.016
θ	9° REF		9° REF	

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPP053010-S56R	−40 to 125°C	SOT563	530	MSL3	Tape and Reel, 5000	Green
TPP053011-S56R	−40 to 125°C	SOT563	531	MSL3	Tape and Reel, 5000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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