16-CH, 80-V, 1-A Half-bridge Driver for VCSEL

Features

- Automotive Qualified for AEC-Q100 Grade 1
- 16-CH 80-V 1-A Half-bridge Driver Array
- Constant Charge and Discharge Current for Capacitive Loads
- High-speed Direct Control Inputs with 4-16 Decoder and Chip Enable
- Output Tri-state and Push-Pull Mode Control
- Diagnostics for Functional Safety Considerations
  - Capacitor Charge Voltage Indicator with Programmable Reference Input
  - Capacitor Residual Voltage Indicator with Programmable Reference Input
  - Open-drain Fault Feedback
  - Over Temperature Protection
- Small Outline Package QFN5X5-32
- −40°C to 125°C Operation Ambient Temperature Range

Applications

- Capacitor Array Driver for VCSEL
- LiDAR
- Capacitive Loads

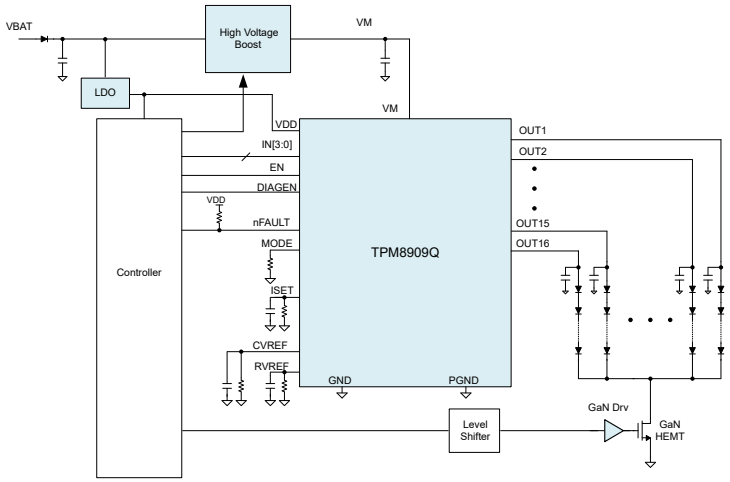
Description

The TPM8909Q is a 16-channel, high-speed half-bridge driver IC, capable of handling 80V and providing up to 1A per channel. Engineered for the control of capacitor arrays in VCSEL driver circuits, it is pivotal in the operation of solid-state LiDAR systems.

In the field of LiDAR, the generation of short, high-power pulses is critical. The VCSEL array, known for its robustness and cost efficiency, excels in applications requiring blind-spot detection in LiDAR technology. The TPM8909Q utilizes capacitor arrays to efficiently store and manage the energy required for these pulses. By charging capacitors of specific channels, it enables precise and controllable VCSEL output, ensuring the system's accuracy and responsiveness in high-resolution LiDAR applications.

The TPM8909Q features a high-speed 4-to-16 multiplexer for directing energy to specific channels, with the ability to tri-state or pull down non-selected channels based on operational mode. It uses an external resistor to precisely control the maximum current to each channel, up to a capacity of 1A. For channels in the discharge phase, internal current limiting is in place to mitigate the risk of excessive current during switching. The device is equipped with voltage indicators to monitor charge and residual voltage levels for safety and system performance. Additionally, it includes an open-drain fault output and a diagnostics enable input for fault detection and management.

Typical Application Circuit



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Revision History

Date	Revision	Notes
2025-05-21	Rev A.0	Initial release

Pin Configuration and Functions

TPM8909Q
QFN5X5-32 Package
Top View

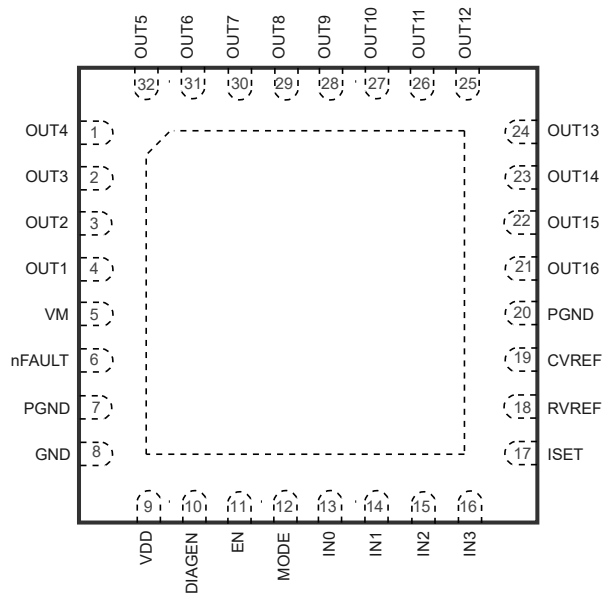


Table 1. Pin Functions

Pin	Name	I/O	Description
1	OUT4	Output	Half-bridge output, pull-up current is determined by the ISET, pull-down current is with the internal current limit
2	OUT3	Output	Half-bridge output, pull-up current is determined by the ISET, pull-down current is with the internal current limit
3	OUT2	Output	Half-bridge output, pull-up current is determined by the ISET, pull-down current is with the internal current limit
4	OUT1	Output	Half-bridge output, pull-up current is determined by the ISET, pull-down current is with the internal current limit
5	VM	Power	Power supply, 8 V - 80 V
6	nFAULT	Output	Open-drain fault output, connect a 10 kΩ pull-up resistor to the external MCU supply
7	PGND	Ground	Power Ground, suggest connecting to GND via a Kelvin connection
8	GND	Ground	Ground
9	VDD	Power	Logic Supply Input, 2.9 V to 5.5 V, connect 1 μF + 0.1 μF capacitors close to the device
10	DIAGEN	Input	nFAULT output enable, DIAGEN = L to reset fault register, 100 kΩ pull down to GND
11	EN	Input	Device enable input, active high, internal pull down with 100 kΩ. Refer to the truth table

Pin	Name	I/O	Description
12	MODE	Input	Device output HiZ mode selection. internal pull down with 100 kΩ. Refer to the truth table.
13	IN0	Input	4-16 MUX Channel Selection, BIT0, internal pull down with 100 kΩ
14	IN1	Input	4-16 MUX Channel Selection, BIT1, internal pull down with 100 kΩ
15	IN2	Input	4-16 MUX Channel Selection, BIT2, internal pull down with 100 kΩ
16	IN3	Input	4-16 MUX Channel Selection, BIT3, internal pull down with 100 kΩ
17	ISET	Input	Output current setting with external resistor and capacitor (1 nF − 10 nF), R = 5 kΩ − 50 kΩ, Output current = 100 mA − 1 A
18	RVREF	Input	Diagnostics reference, use an external resistor to set diagnostics voltage threshold from 1 V to 10 V, R =2.5 kΩ − 25 kΩ, 1-nF decoupling capacitor is also recommended
19	CVREF	Input	Diagnostics reference, use an external resistor to set diagnostics voltage threshold from 1 V to 10 V, R = 2.5 kΩ − 25 kΩ, 1-nF decoupling capacitor is also recommended
20	PGND	Ground	Power Ground, suggest connecting to GND via a Kelvin connection
21	OUT16	Output	Half-bridge output, pull-up current is determined by the ISET, pull-down current is with the internal current limit
22	OUT15	Output	Half-bridge output, pull-up current is determined by the ISET, pull-down current is with the internal current limit
23	OUT14	Output	Half-bridge output, pull-up current is determined by the ISET, pull-down current is with the internal current limit
24	OUT13	Output	Half-bridge output, pull-up current is determined by the ISET, pull-down current is with the internal current limit
25	OUT12	Output	Half-bridge output, pull-up current is determined by the ISET, pull-down current is with the internal current limit
26	OUT11	Output	Half-bridge output, pull-up current is determined by the ISET, pull-down current is with the internal current limit
27	OUT10	Output	Half-bridge output, pull-up current is determined by the ISET, pull-down current is with the internal current limit
28	OUT9	Output	Half-bridge output, pull up current is determined by the ISET, pull-down current is with the internal current limit
29	OUT8	Output	Half-bridge output, pull up current is determined by the ISET, pull-down current is with the internal current limit
30	OUT7	Output	Half-bridge output, pull-up current is determined by the ISET, pull-down current is with the internal current limit
31	OUT6	Output	Half-bridge output, pull-up current is determined by the ISET, pull-down current is with the internal current limit
32	OUT5	Output	Half-bridge output, pull-up current is determined by the ISET, pull-down current is with the internal current limit
EPAD	EPAD	Ground	Connect to GND

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{DD}	Logic Supply Voltage	−0.5	6.5	V
V_M	Output Supply Voltage	−0.5	80	V
I_{OUT}	Output Current	Internally limited		A
V_{OUT}	Output Voltage	−0.5	V_M + 0.5	V
	Output Voltage (20-ns pulse)	−2	V_M + 0.5	V
Logic Inputs	Input Voltage	−0.5	6.5	V
nFAULT	Open-drain fault output	−0.5	40	V
GND − PGND	Ground	−0.5	0.5	V
T_J	Maximum Junction Temperature	−40	150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 300 mV beyond the power supply, the input current should be limited to less than 10 mA.
(3) A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	AEC-Q100-002 (1)	±4	kV
CDM	Charged Device Model ESD	AEC-Q100-011 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
VIN	Supply Input Voltage Range	9		70	V
VDD	Logic Power Supply Voltage	2.9		5.5	V
C_{OUT}	Load Capacitance			1000	nF
I_{OUT}	Output Current	−1		1	A
PGND − GND	Power Ground	−0.3		0.3	V
T_A	Ambient Junction Temperature	–40		125	°C
P_D	Device Power Dissipation			2	W

Thermal Information

Package Type	θ_{JA}	θ_{Jb}	θ_{JC}	Unit
QFN5X5-32	29.3	5.4	16.3	°C/W

Electrical Characteristics

All test conditions: V_M = 60 V, V_{DD}= 5 V, T_A = −40°C to +125°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Power Supply						
I_{VDD}	VDD Supply Current, Standby	VM = 60 V, EN = 5 V		4.5	20	μA
I_{Q_VDD}	VDD Quiescent Current	VM = 60 V, EN = 0 V		4.4	10	μA
I_{VM}	VM Supply Current, Standby	VM = 60 V, EN = 5 V, MODE = 0 V	0.7	1.08	1.4	mA
		VM = 60 V, EN = 5 V, MODE = 5 V	1	1.43	1.9	mA
I_{Q_VM}	VM Quiescent Current	VM = 60 V, EN = 0 V, MODE = 0 V	0.5	0.77	1.1	mA
		VM = 60 V, EN = 0 V, MODE = 5 V	0.7	1.13	1.5	mA
$t_{D\_powerup}$	VM UVLO to Driver Ready	Rise till 10% of I_{OUT} current. R_{ISET} = 5 kΩ, VM rises from 0 to 60 V	4	11	50	μs
LOGIC LEVEL INPUTS (IN0−IN3, EN, MODE)						
V_{IL}	Input Low Voltage	VDD = 2.9 V to 5.5 V			0.3×V DD	V
V_{IH}	Input High Voltage	VDD = 2.9 V to 5.5 V	0.7×V DD			V
V_{HYS}	Input Threshold Hysteresis			0.1×V DD		V
I_{IL}	Input Logic Low Current, VIN = 0 V		−1		1	μA
I_{IH}	Input Logic High Current, VIN = VDD			34	80	μA
C_{ID}	Input Capacitance (1)				15	pF
Open drain fault output						
V_{OL}	Output Logic Low Voltage	I_{FAULT} = 5 mA		0.16	0.4	V
I_{OH}	Output Logic High Current	V_{FAULT} = 5 V	−1	0	1	μA
Driver Outputs (OUTx)						
$R_{DS(ON)H}$	High-side MOSFET On-resistance	VM = 60 V, I_{OUT} = 0.4 A, T_A = 25 °C		6		Ω
$R_{DS(ON)H}$	High-side MOSFET On-resistance	VM = 60 V, I_{OUT} = 0.4 A, T_A = −40°C to 125°C		6	10	Ω
$R_{DS(ON)L}$	High-side MOSFET On-resistance	VM = 60 V, I_{OUT} = 0.4 A, T_A = 25°C		2.6		Ω
$R_{DS(ON)L}$	High-side MOSFET On-resistance	VM = 60 V, I_{OUT} = 0.4 A, T_A = −40°C to 125°C		2.6	5	Ω
C_{OUT}	Maximum Load Capacitance (1)				1	μF

Parameter		Conditions	Min	Typ	Max	Unit
T_R	Output Rise Time (1)	VM = 60 V ， 10% to 90%, R_{ISET} = 5 kΩ, C_{Load} = 5 nF	240	250	300	ns
T_F	Output Fall Time (1)	VM = 60 V, 30 V to 3 V, C_{Load} = 5 nF	130	200	350	ns
T_{PD_IN}	Propagation Delay (1)	Input change, (INx) rises to 10% of I_{OUT}, R_{ISET} = 5 KΩ, C_{Load} = 5 nF	37	50	100	ns
T_{PD_EN}	Propagation Delay (1)	Input change, (ENx) rises to 10% of I_{OUT}, R_{ISET} = 5 KΩ, C_{Load} = 5 nF	37	50	100	ns
I_{LEAKH}	V_{OUTx} to VM Leakage Current			0.27	100	nA
I_{LEAKL}	V_{OUTx} to GND Leakage Current		1	6.3	10	μA
V_{ISET}	ISET Reference Voltage			502		mV
I_{SET_50k}	Output Current	R_{ISET} = 50 kΩ, V_{OUT} = 0 to VM − 10 V, C_{LOAD} = 5 nF	110	133	160	mA
I_{SET_25k}	Output Current	R_{ISET} = 25 kΩ, V_{OUT} = 0 V to VM − 10 V, C_{LOAD} = 5 nF	210	246	280	mA
I_{SET_10k}	Output Current	R_{ISET} = 10 kΩ, V_{OUT} = 0 V to VM − 10 V, C_{LOAD} = 5 nF	490	560	630	mA
I_{SET_5k}	Output Current	R_{ISET} = 5 kΩ, V_{OUT} = 0 V to VM − 10 V, C_{LOAD} = 5 nF	900	970	1150	mA
t_{limit}	Current Limit Settling Time	R_{ISET} = 10 kΩ, I_{OUT} rises from 10% to 90%		22	50	ns
I_{LIMIT_HS}	High-side Current Limit	R_{ISET} = 0 Ω, V_{OUT} = 0 V to VM −10 V, C_{LOAD} = 5 nF	0.95	1.3	1.65	A
I_{LIMIT_LS}	Low-side Current Limit	V_{OUT} = 30 V to 3 V, C_{LOAD} = 5 nF	0.5	1.06	1.4	A
t_{min_on}	Minimal Pulse Width (1)	VM = 60 V, C_{LOAD} = 5 nF			500	ns
f_{PWM}	Switching Frequency (1)				2	MHz
Diagnostics & Protection						
V_{UVLOR_VM}	Rising VM			7.6	8	V
V_{UVLOF_VM}	Falling VM		6.5	7.1		V
$V_{UVLOHYS\_VM}$	Hysteresis			0.5		V
V_{UVLOR_VDD}	Rising VDD			2.7	2.9	V
V_{UVLOF_VDD}	Falling VDD		2.3	2.5		V
$V_{UVLOHYS\_VDD}$	Hysteresis			0.2		V
t_{UVLO}	UVLO Deglitch Timer			10		μs
V_{THCV}	Charge Voltage Monitor Threshold, VM − V_{OUTx}	R_{CVREF} = 5 kΩ		2		V
V_{THRV}	Residual Voltage Monitor Threshold on V_{OUTx}	R_{RVREF} = 20 kΩ		8		V
$t_{blanking\_RV}$	Residual Voltage Monitor Blanking Timer			22		μs

Parameter		Conditions	Min	Typ	Max	Unit
$t_{deglitch\_RV}$	Residual Voltage Monitor Deglitch Timer			2		μs
$I_{FAULTREF}$	Fault Reference Current Output on RVREF and CVREF	R = 20 kΩ		100		μA
Thermal Shutdown						
T_{SD}	Thermal Shut Down Temperature		150	165		°C
T_{SD_hys}	Thermal Hysteresis			15		°C
t_{OTP_deg}	Over Temperature Protection Deglitch Timer			10		μs

(1) Guaranteed by design

Typical Performance Characteristics

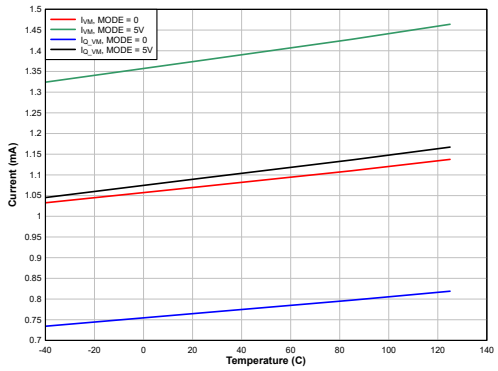


Figure 1. VM Current vs. Temperature

VM = 60 V

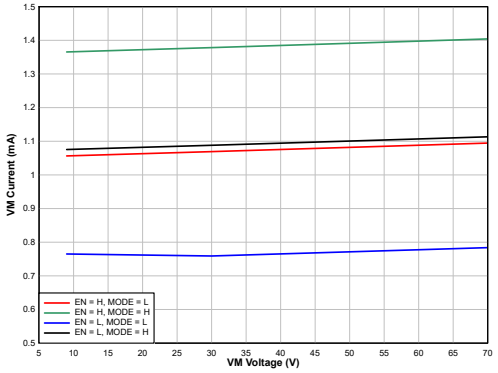


Figure 2. VM Current vs. VM Voltage

Temperature = 25°C

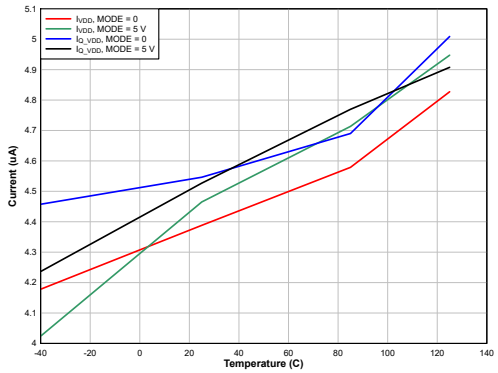


Figure 3. VDD Current vs. Temperature

VDD = 3.3 V

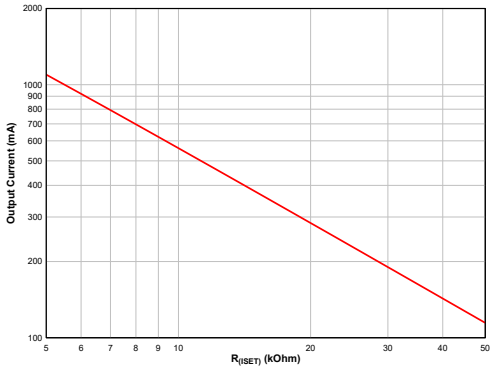


Figure 4. Output Current Setting

VM = 60 V

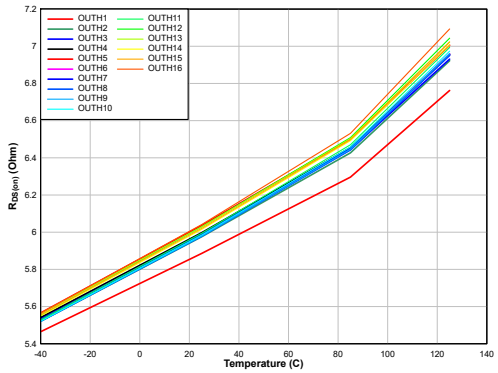


Figure 5. High-side On-Resistance

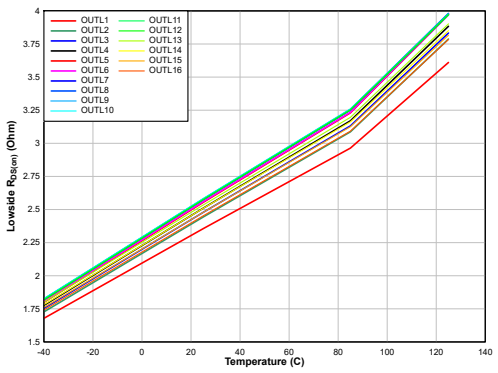


Figure 6. Low-side On-Resistance

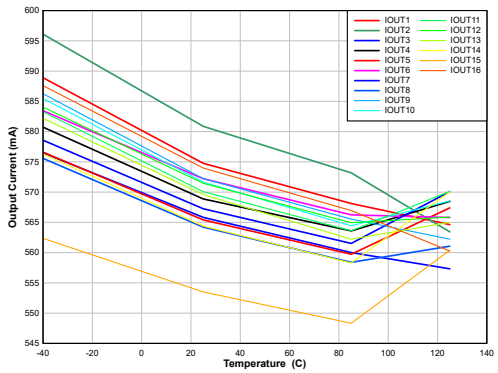


Figure 7. Output Current vs. Temperature

VM = 60 V, V_{OUT} = 55 V, R_{ISET} =10 kΩ

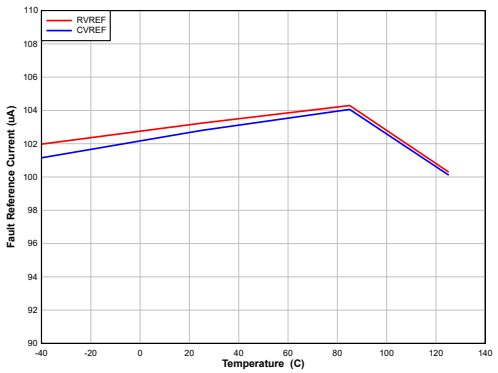


Figure 8. Fault Reference Current vs. Temperature

VM = 60 V

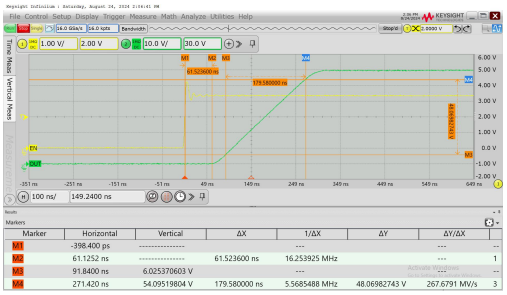


Figure 9. Rise-time vs. Temperature

VM = 60 V, C_{Load} = 5nF, 10% to 90%

Figure 10. Fall-time vs. Temperature

VM = 60 V, C_{Load} = 5 nF, 30 V to 3 V

Figure 11. 500-mA Constant Current Driver Pulse

VM = 60 V, V_{OUT} = 0 V, R_{ISET} = 10 kΩ

Figure 12. 1-A Constant Current Driver Pulse

VM = 60 V, V_{OUT} = 0 V, R_{ISET} = 5 kΩ

Detailed Description

Overview

The TPM8909Q is a 16-channel, high-speed half-bridge driver IC, capable of handling 80 V and providing constant current charging up to 1 A per channel. Engineered for the control of capacitor arrays in VCSEL driver circuits, it is pivotal in the operation of solid-state LiDAR systems.

In the field of LiDAR, the generation of short, high-power pulses is critical. The VCSEL array, known for its robustness and cost efficiency, excels in applications requiring blind-spot detection in LiDAR technology. The TPM8909Q utilizes capacitor arrays to efficiently store and manage the energy required for these pulses. By using programmable constant current charging capacitors of specific channels, it enables precise and controllable VCSEL output, ensuring the system's accuracy and responsiveness in high-resolution LiDAR applications.

The TPM8909Q features a high-speed 4-to-16 multiplexer for directing energy to specific channels, with the ability to tri-state or pull down non-selected channels based on operational mode. It uses an external resistor to precisely control the maximum constant current to each channel, up to 1A. For channels in the discharge phase, internal current limiting is in place to mitigate the risk of excessive current during switching. The device is equipped with voltage indicators to monitor charge and residual voltage levels for safety and system performance. Additionally, it includes an open-drain fault output and a diagnostics enable input for fault detection and management.

Functional Block Diagram

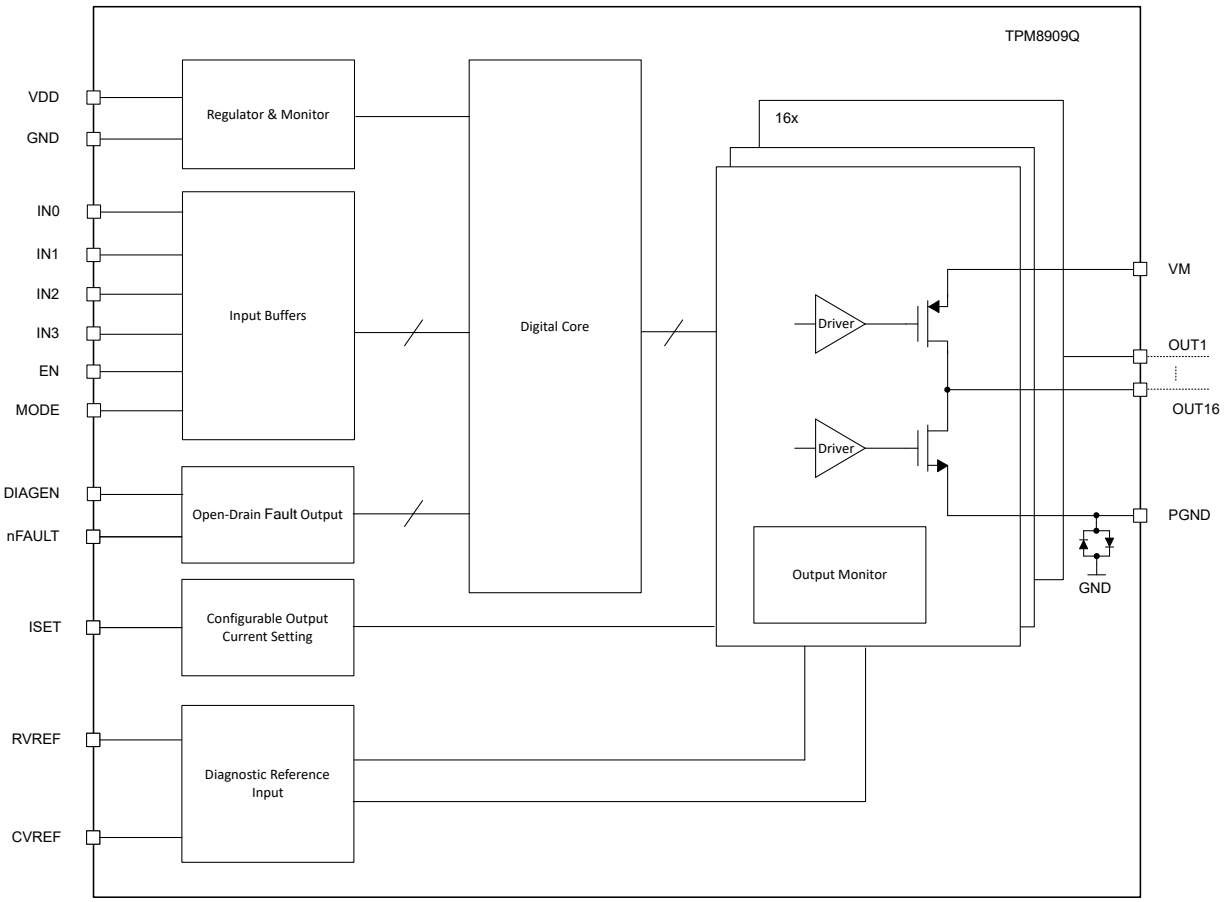


Figure 13. Functional Block Diagram

Feature Description

Power Supply

The TPM8909Q is designed with two power rails the VM rail for the half-bridge output drivers and the VDD rail for the internal logic and control circuits. Both rails are equipped with under-voltage lock-out (UVLO) protection to prevent operation below a safe voltage threshold. If the input voltage to either rail falls below this threshold, the device's outputs are disabled, going into a tri-state condition. Once the voltage is restored above the threshold, the device automatically resumes normal operation.

3PEAK recommends a bulk capacitor to sustain high current output pulse together with a small decoupling capacitance for high frequency response. The capacitance should be enough to sustain the pulsed output current with an acceptable voltage drop on the supply. The capacitors should be placed close to the device and low-output impedance capacitors are recommended such as 3-terminal capacitors.

High-speed Logic Inputs

The TPM8909Q includes four high-speed logic inputs that allow for the individual selection and activation of a specific output channel, with the system design ensuring that only one channel is active at any given time. By employing a 4-to-16 multiplexer, the device achieves low latency and rapid switching. Activating a channel's high side, the device simultaneously pulls down or tri-states the other channels, depending on the selected MODE. For scenarios demanding the concurrent activation of multiple channels, 3PEAK recommends the use of multiple TPM8909Q devices in parallel. INx are internally pulled down with 100-kΩ resistance to GND.

The device has EN input for output enable. When an EN is high, the outputs are enabled. When EN is low, outputs are pulled down if MODE is HIGH or tri-stated if MODE is LOW. The EN pin has an internal 100-kΩ resistance pulled down to GND.

Output Driver

The TPM8909Q incorporates 16 half-bridge channels, each channel has a pair of complementary NMOS drivers for the high side and low side. Upon channel selection, the high-side NMOS driver is turned on, with the current regulated with the limit set by an external ISET resistor. In scenarios where the low-side mode is enabled by MODE selection, the low-side NMOS drivers of the non-selected channels are activated, with an internal current limit to prevent high current. This design limits charge current on capacitors and protects Lidar systems from overcurrent conditions.

When driving capacitive loads, a significant amount of energy is dissipated on TPM8909Q. 3PEAK recommends evaluating driver efficiency and power dissipation requirements for system robustness. 3PEAK recommends a maximum 2-W average power dissipation for automotive applications.

The high-side current can be set via the ISET resistor, the value is calculated via the equation below. When output voltage rises close to supply voltage, the device pull-up current is lower than the current limit because of insufficient headroom of the high-side driver; similarly, when output voltage falls close to ground, the device pull-down current is also lower than the current limit cause of insufficient headroom of the low-side driver.

$$I_{OUT} = \frac{11.3 \times 10^3 \cdot V_{ISET}}{R_{ISET} + 250\Omega} \quad (1)$$

When the output capacitor is very low with high limit current, 3PEAK recommends carefully inspecting loop parasitic resistance, inductance and capacitance (RLC). The parasitic RLC may cause ringing on each of the outputs and may result in negative voltage on OUTx and impact system-level robustness.

Diagnostics and Fault

The TPM8909Q includes four high-speed logic inputs that allow for the individual selection and activation of a specific output channel, with the system design ensuring that only one channel is active at any given time. By employing a 4-to-16 multiplexer, the device achieves low latency and rapid switching. Activating a channel's high side, the device simultaneously pulls down or tri-states the other channels, depending on the selected MODE. For scenarios demanding the concurrent activation of multiple channels, 3PEAK recommends the use of multiple TPM8909Q devices in parallel.

Residual Voltage Diagnostics (RVD)

Residual Voltage Diagnostics is designed for LiDAR system-level functional safety. When there is residual voltage on output capacitors, the VCSEL is not reverse-biased. During a transient event when the cathode of VCSEL is fast pulled low, the residual voltage on the capacitors may unintendedly illuminate VCSEL. The value of output capacitors should be selected so that after a normal illumination cycle, the output voltage is low enough and does not trigger RVD. Thus, once RVD is detected, it may reflect potential discharge path failure, such as VCSEL open-circuit of GaN open-circuit. Care must be taken when MODE = L without an internal pull-down path.

When a channel is selected, the RVD is not enabled. Once the channel is turned off and DiagEN = H, with either MODE = H or L, the RVD of unselected channels starts to monitor capacitor voltages after a period of blanking time tblanking_RV. If the monitor voltage is above the RVD threshold, VTH_RV, with duration longer than deligtch timer tdeglitch_RV, the device

latches fault and report by pulling open-drain output nFAULT low. To clear the fault, the controller needs to pull down DiagEN to L longer than 1 μs.

RVD does not impact the output channel, in the case diagnostics is not needed, nFAULT can be left open or connected to GND.RV threshold is set by RVREF pin. RVREF sources a constant current 100μA through RVSET resistor to GND with maximum voltage up to VDD. The voltage on the RVSET pin is multiplied by 4 as RVREF threshold with the equation below.

$$V_{THRV} = 4 \cdot I_{FAULTREF} \cdot R_{RV} \quad (2)$$

Charge Voltage Diagnostics (CVD)

Charge Voltage Diagnostics is designed for LiDAR system functional safety considerations. The device monitors output capacitor voltage, through the whole high-side ON-time.

When the voltage of the selected channel has not surpassed CV threshold VTHCV at least once in the whole high-side ON-time, the device latches fault and report by pulling open-drain output nFAULT low. To clear the fault, the controller needs to pull down DiagEN to L longer than 1μs. CVD fault does not impact the output channel. In the case diagnostic is not needed, nFAULT can be left open to connected GND. The CV threshold is set by the CVREF pin. CVREF sources a constant current 100 μA through CVSET resistor to GND with a maximum voltage up to VDD. The voltage on the CVSET pin is multiplied by 4 as the CVREF threshold with the equation below.

$$V_{THCV} = V_M - 4 \cdot I_{FAULTREF} \cdot R_{CV} \quad (3)$$

MODE and EN

The MODE pin, equipped with a 100kΩ internal pull-down resistor to GND, can be connected to either VDD or GND. It plays a pivotal role in controlling the behavior of the unselected output channels, as outlined in the accompanying truth table. When the MODE pin is set HIGH, the unselected channels are internally pulled down by a low-side FET, ensuring they remain inactive. Conversely, setting the MODE pin LOW tri-states the unselected channels, rendering them in a high-impedance state.

The low-side mode (MODE=HIGH) is designed to discharge residual charge from the VCSEL channels, preventing unintended illumination due to parasitic coupling. This is essential for avoiding crosstalk that could activate unselected VCSEL channels. However, if a VCSEL channel has a short-circuit fault, the low-side mode may create a leakage path, leading to persistent illumination and potential eye safety issues. In such cases, 3PEAK advises the use of the high-impedance mode (MODE = LOW) for safety. Additionally, the diagnostic capabilities of the system vary with the MODE pin setting, and users should refer to the truth table for detailed information on the impact of mode selection on diagnostics.

For the EN (Enable) pin, it offers the flexibility to interface with either VDD or GND voltage sources. It features an integrated pull-down resistor with a resistance value of 100 kΩ to the GND, ensuring stable voltage configuration upon connection. This internal resistor aids in maintaining a consistent and reliable voltage level when the EN pin is not actively driven, facilitating a clear and defined logic state for the pin's operation.

Over-Temperature Protection

The over-temperature protection feature protects the device from excessive junction temperatures. Once triggered, the device disables the outputs when the device junction temperature exceeds 165°C (typical). Hysteresis maintains the shutdown state until the junction temperature drops below approximately 150°C. When the junction temperature falls below 150°C (typical), the TPM8909Q recovers to normal operation. 3PEAK recommends evaluating thermal constraints and avoiding frequently triggering over-temperature protection.

MODE Truth Table

MODE	EN	IN3	IN2	IN1	IN0		OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	OUT7	OUT8	OUT9	OUT10	OUT11	OUT12	OUT13	OUT14	OUT15	OUT16	Charge Voltage Indicator	Residual Voltage Indicator
H	L	X	X	X	X		L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	n/a	all
H	H	0	0	0	0		High	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	OUT1	all except OUT1
H	H	0	0	0	1		L	High	L	L	L	L	L	L	L	L	L	L	L	L	L	L	OUT2	all except OUT2
H	H	0	0	1	0		L	L	High	L	L	L	L	L	L	L	L	L	L	L	L	L	OUT3	all except OUT3
H	H	0	0	1	1		L	L	L	High	L	L	L	L	L	L	L	L	L	L	L	L	OUT4	all except OUT4
H	H	0	1	0	0		L	L	L	L	High	L	L	L	L	L	L	L	L	L	L	L	OUT5	all except OUT5
H	H	0	1	0	1		L	L	L	L	L	High	L	L	L	L	L	L	L	L	L	L	OUT6	all except OUT6
H	H	0	1	1	0		L	L	L	L	L	L	High	L	L	L	L	L	L	L	L	L	OUT7	all except OUT7
H	H	0	1	1	1		L	L	L	L	L	L	L	High	L	L	L	L	L	L	L	L	OUT8	all except OUT8
H	H	1	0	0	0		L	L	L	L	L	L	L	L	High	L	L	L	L	L	L	L	OUT9	all except OUT9
H	H	1	0	0	1		L	L	L	L	L	L	L	L	L	High	L	L	L	L	L	L	OUT10	all except OUT10
H	H	1	0	1	0		L	L	L	L	L	L	L	L	L	L	High	L	L	L	L	L	OUT11	all except OUT11
H	H	1	0	1	1		L	L	L	L	L	L	L	L	L	L	L	High	L	L	L	L	OUT12	all except OUT12
H	H	1	1	0	0		L	L	L	L	L	L	L	L	L	L	L	L	High	L	L	L	OUT13	all except OUT13
H	H	1	1	0	1		L	L	L	L	L	L	L	L	L	L	L	L	L	High	L	L	OUT14	all except OUT14
H	H	1	1	1	0		L	L	L	L	L	L	L	L	L	L	L	L	L	L	High	L	OUT15	all except OUT15
H	H	1	1	1	1		L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	High	OUT16	all except OUT16
L	L	X	X	X	X		Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	n/a	all
L	H	0	0	0	0		High	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	OUT1	all except OUT1
L	H	0	0	0	1		Z	High	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	OUT2	all except OUT2
L	H	0	0	1	0		Z	Z	High	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	OUT3	all except OUT3
L	H	0	0	1	1		Z	Z	Z	High	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	OUT4	all except OUT4
L	H	0	1	0	0		Z	Z	Z	Z	High	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	OUT5	all except OUT5
L	H	0	1	0	1		Z	Z	Z	Z	Z	High	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	OUT6	all except OUT6
L	H	0	1	1	0		Z	Z	Z	Z	Z	Z	High	Z	Z	Z	Z	Z	Z	Z	Z	Z	OUT7	all except OUT7
L	H	0	1	1	1		Z	Z	Z	Z	Z	Z	Z	High	Z	Z	Z	Z	Z	Z	Z	Z	OUT8	all except OUT8
L	H	1	0	0	0		Z	Z	Z	Z	Z	Z	Z	Z	High	Z	Z	Z	Z	Z	Z	Z	OUT9	all except OUT9
L	H	1	0	0	1		Z	Z	Z	Z	Z	Z	Z	Z	Z	High	Z	Z	Z	Z	Z	Z	OUT10	all except OUT10
L	H	1	0	1	0		Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	High	Z	Z	Z	Z	Z	OUT11	all except OUT11
L	H	1	0	1	1		Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	High	Z	Z	Z	Z	OUT12	all except OUT12
L	H	1	1	0	0		Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	High	Z	Z	Z	OUT13	all except OUT13
L	H	1	1	0	1		Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	High	Z	Z	OUT14	all except OUT14
L	H	1	1	1	0		Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	High	Z	OUT15	all except OUT15
L	H	1	1	1	1		Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	High	OUT16	all except OUT16

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPM8909Q supports direct charging and resonant charging topologies.

Typical Application

Direct Charging

The TPM8909Q achieves precise driving of VCSEL through controlled charging and discharging of external capacitors. The detailed operation process is as follows:

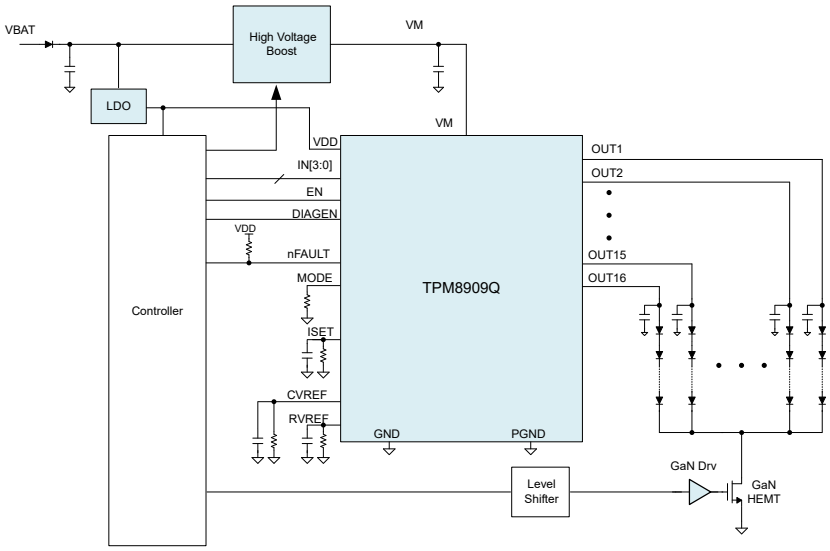


Figure 14. TPM8909Q Application Diagram

Capacitor Charging: When a specific channel is selected, the high-side MOS in the TPM8909Q turns on, enabling the supply voltage (VM) to charge the external capacitor (C_{OUT}) with a constant current. The charging current is determined by an external resistor connected to the ISET pin. If the ISET resistor is set to 10kΩ, the charging current is:

$$I_{OUT} = \frac{11.3 \times 10^3 \cdot V_{ISET}}{R_{ISET} + 250\Omega} = \frac{11.3 \times 10^3 \cdot 502mV}{10k\Omega + 250\Omega} = 553mA \quad (4)$$

A higher charging current reduces the charging time, allowing the system to operate at higher pulse frequencies. The device has a fast response time and regulates output current to charge load capacitors. Thermal constraints need to be taken care of, especially when repetitive frequency is high or load capacitance is high. The average device power dissipation can be estimated using the equation below, assuming all power is dissipated on TPM8909Q.

$$P_D = VM \cdot I_{Q\_VM} + VDD \cdot I_{VDD} + VM^2 \cdot C_{LOAD} \cdot f \cdot D \quad (5)$$

In this equation, VM and V_{DD} are voltage supplies. I_{VM} and I_{VDD} are input quiescent currents, respectively.

The C_{LOAD} is the output load capacitance of a single channel. *f* is the repetitive driving frequency. D is the average operation duty cycle.

It is recommended for a 2-oz, 4-layer FR4 PCB board, the maximum average power dissipation is 2 W. For a 64-channel VCSEL driver system, the average operation duty cycle D is 25%. For 40-V VM and 5-nF each channel's load capacitance. The maximum repetitive frequency should be approximately 1 MHz.

Caution must be taken under abnormal conditions, such as VCSEL short-circuit scenarios. If a short-circuit occurs on a channel's VCSEL and the system is operating in MODE = H, the output of TPM8909Q may form a direct path from VM to GND. This can result in a large current flow through the chip, potentially causing overheating or permanent damage. To mitigate this risk, it is recommended to promptly disable EN or stop charging the affected channel when an abnormal condition is detected by Residual Voltage Diagnostics or Charge Voltage Diagnostics.

Energy Storage: Once the capacitor C_{OUT} is fully charged, the energy remains stored in the capacitor, awaiting the discharge trigger.

VCSEL Illumination: For the VCSEL driver, the charged capacitor Cout, VCSEL, and GaN form a closed loop, allowing the stored energy to discharge through the VCSEL and GaN. This current pulse illuminates the VCSEL, emitting a short-duration, high-intensity laser pulse.

Diagnostics Settings: The TPM8909Q supports both Charge Voltage Diagnostics (CVD) and Residual Voltage Diagnostics (RVD). By configuring reference thresholds via the CVREF and RVREF pins, the device can detect abnormal conditions such as insufficient charging or incomplete capacitor discharge, and signal faults through the nFAULT open-drain output to enhance system safety and reliability. Note that when operating in MODE = L, a channel switch may trigger an RVD fault if C_{OUT} lacks a discharge path.

For a RVD threshold of 8V and CVD threshold of VM−2 V, R_{RVREF} = 20 kΩ and R_{CVREF} = 5 kΩ is recommended. The detection thresholds for RVD and CVD can be calculated as follows:

$$V_{THRV} = 4 \cdot I_{FAULTREF} \cdot R_{RV} = 4 \cdot 100\mu A \cdot 20k\Omega = 8V \quad (6)$$

$$V_{THCV} = V_M - 4 \cdot I_{FAULTREF} \cdot R_{CV} = V_M - 4 \cdot 100\mu A \cdot 5k\Omega = V_M - 2V \quad (7)$$

When the high-side MOS is turned off, if the OUTx voltage exceeds 8 V, an RVD fault is reported. Throughout the entire charging cycle, if the OUTx voltage is not charged to VM - 2V or higher, a CVD fault is reported.

The GaN low-side driver can be turned on either during the high-side charging cycle or after charging is completed.

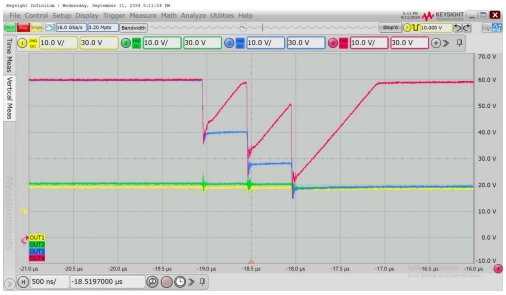


Figure 15. Discharge During Charging

CH4: OUT4 Channel highside is ON, the GaN lowside driver turned on 3 times.
CH3: OUT3 Channel capacitor fully charged, the GaN lowside driver turned on 3 times. MODE = L.

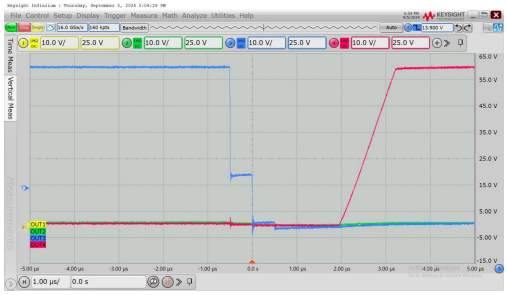
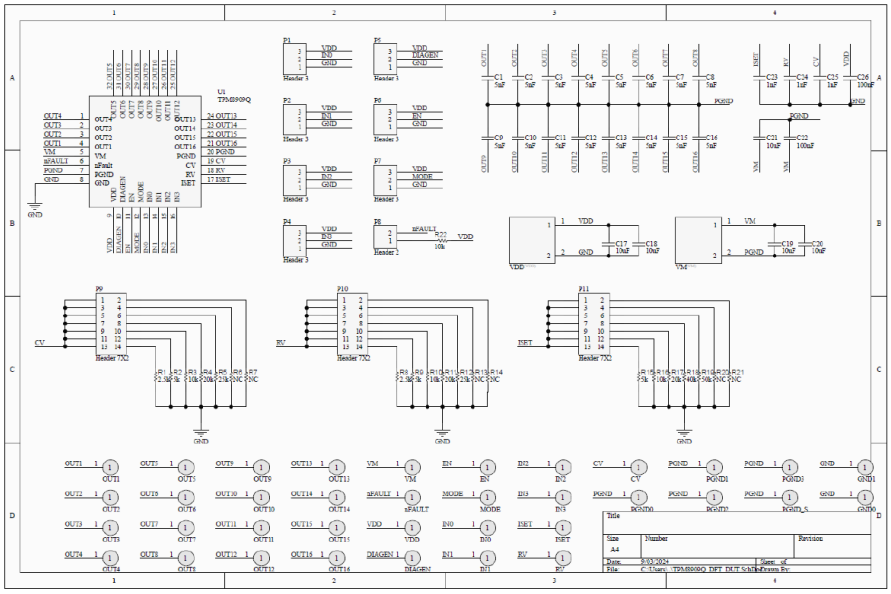


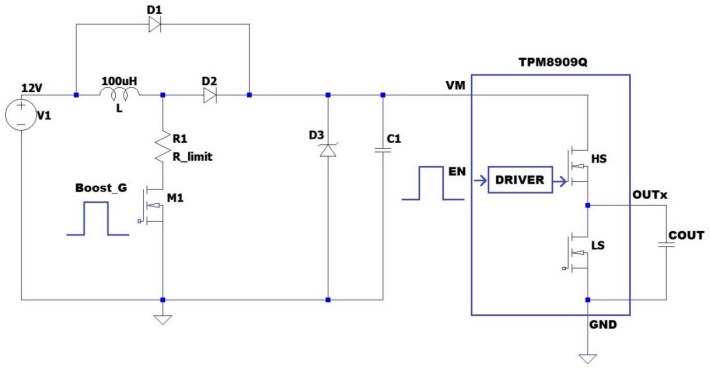
Figure 16. Discharge After Charging

CH4: OUT4 Channel highside is charged after CH3 capacitor voltage is depleted.
CH3: OUT3 Channel capacitor fully charged, the GaN lowside driver turned on 3 times. MODE = L.



Resonant Charging

To improve efficiency and minimize thermal dissipation, a soft switching approach can be used to turn on the driver before VM reaches high voltage. VM must keep above the UVLO threshold to avoid under voltage lockout protection.



In this approach, VM remains at a lower standby voltage. Prior to VCSEL activation, switch M1 is turned on to build current in the inductor. The peak inductor current is calculated as: (ideal case @R1 = 0).

$$I_L = \frac{V_1 \cdot T_{+(BOOST\_G)}}{L}$$

Once the desired current is reached, EN is asserted high to enable the selected TPM8909Q channel, followed by turning off M1. The stored energy in the inductor then charges Cout. The resulting capacitor voltage ideally reaches: (ideal case).

$$U_{out} = \sqrt{\frac{LI_L^2}{C_1 + C_{out}}} + V_1$$

Due to the switch voltage drop and system losses, the output voltage is slightly lower than the theoretical value. After charging completes, deassert EN to initiate the VCSEL discharge cycle. The next charging cycle begins automatically once discharge finishes. Performance was verified through theoretical calculation, simulation, and measurement using the parameters listed below.

V1	L	R1	C1	Cout	$T+_{Boost\_G}$	Tdelay

12V	100μH	0Ω	100pF	5nF	2.5μs	250ns

By substituting the above parameters into the formulas, the calculated inductor current and capacitor charging voltage are as follows:

$$I_L = \frac{V_1 \cdot T_{+(BOOST\_G)}}{L} = \frac{12\ V \cdot 2.5\ \mu s}{100\ \mu H} = 0.3\ A$$

$$U_{out} = \sqrt{\frac{LI_L^2}{C_1 + C_{out}}} + V_1 = \sqrt{\frac{100\ \mu H \cdot (0.3\ A)^2}{100\ pF + 5\ nF}} + 12\ V = 54\ V$$

Simulated Results: Peak inductor current = 0.3 A, C_{OUT} voltage = 53 V (matches theoretical expectations).

Measured Results: Inductor current = 0.3 A. Final C_{OUT} voltage = 48.6 V (slightly lower due to real-world losses and component tolerances).

Efficiency Gain: System efficiency improves from <50% to ~80% with this method.

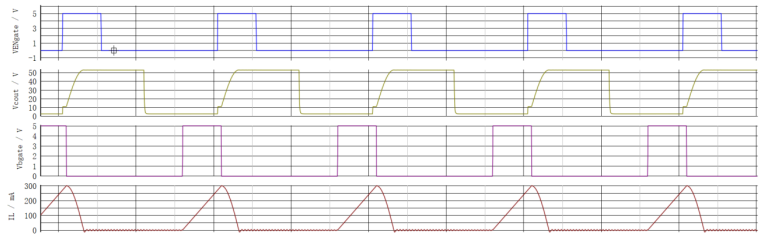


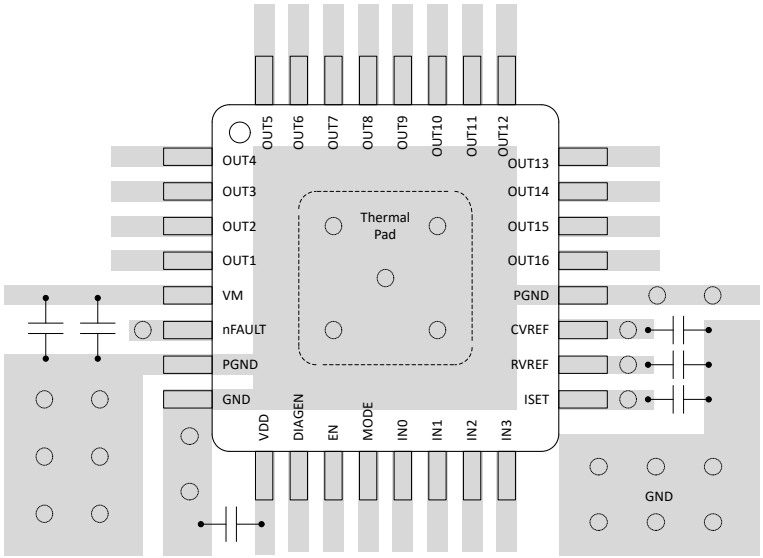
Figure 17. Resonant Charging Simulation

Figure 18. Resonant Charging Measurement

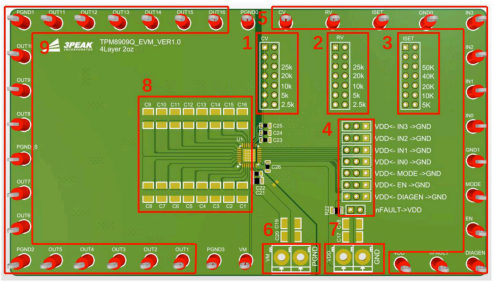
Layout

Layout Guideline

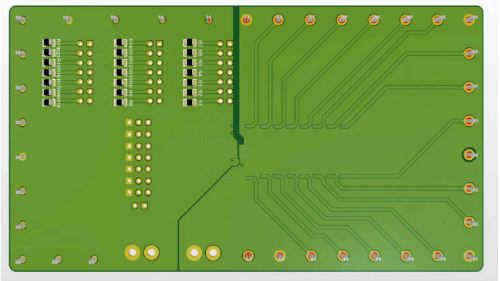
- It is recommended to bypass the VM pin to ground with a 10 μF + 0.1 μF capacitor, and to place a 1-μF bypass capacitor on the VDD pin.
- 1-nF decoupling capacitor is also recommended on the R_{VREF}, C_{VREF}, and I_{SET} pins to reduce noise and ensure stable reference levels.
- Route GND and PGND as separate copper areas and connect them at a single point near the chip. Avoid routing analog signals across PGND and keep high-current paths away from GND regions.
- It is recommended to use wide and thick copper to minimize I×R drop and heat dissipation.
- The exposed thermal pad must be connected to the PCB ground plane directly, and the copper area must be as large as possible.



Layout Recommendations

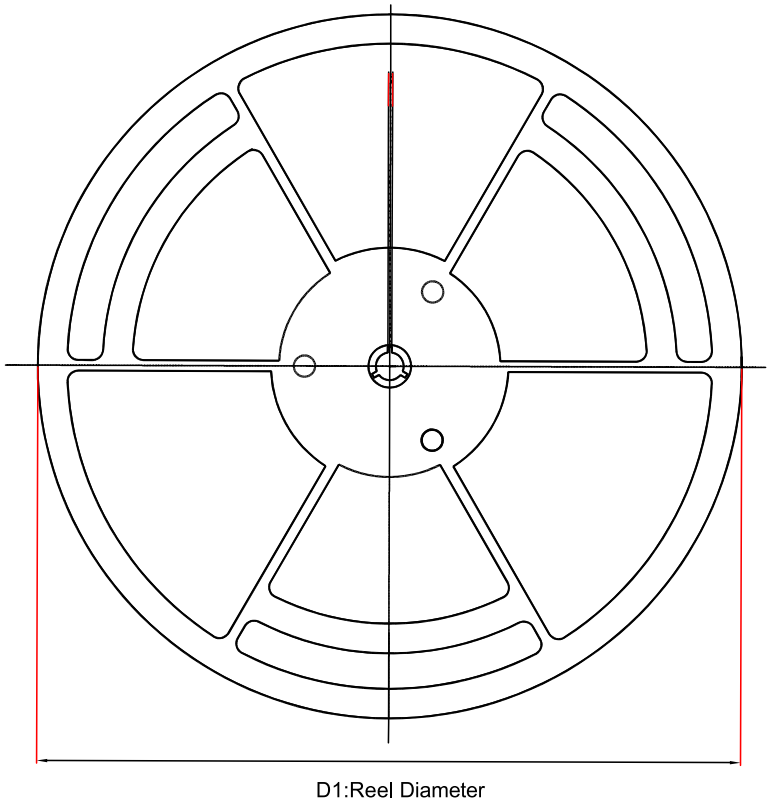


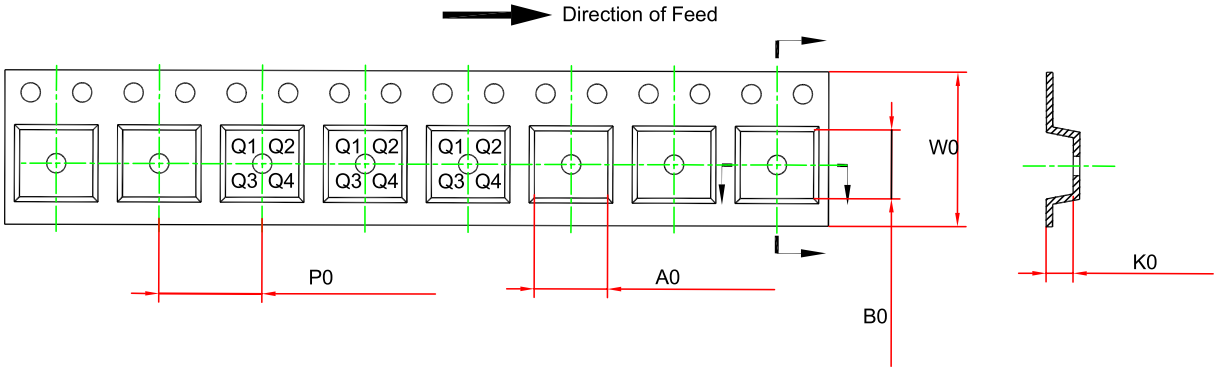
Top Layer



Bottom Layer

Tape and Reel Information



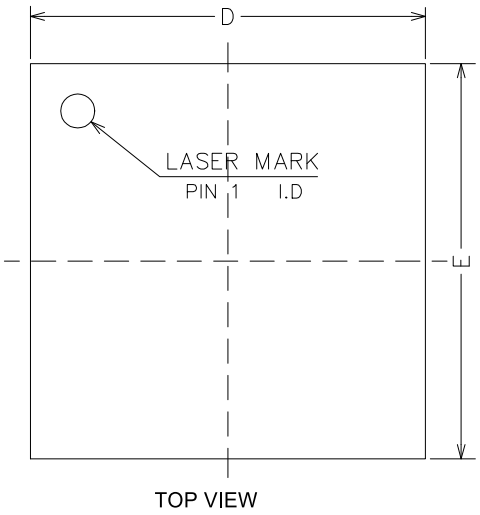


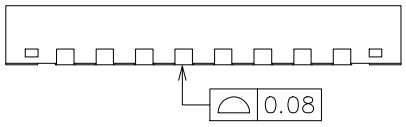
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM8909Q-QFZR-S	QFN5X5-32	330	17.6	5.3	5.3	1.1	8.0	12	Q1

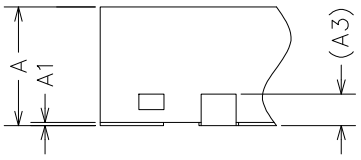
Package Outline Dimensions

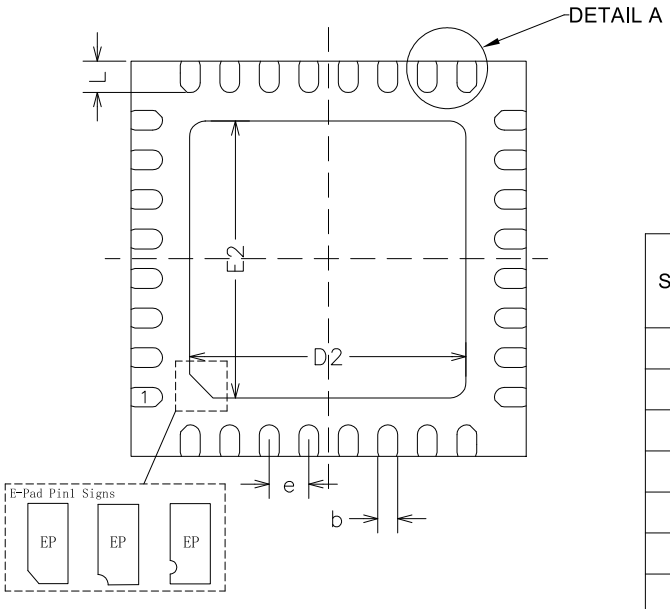
QFN5X5-32

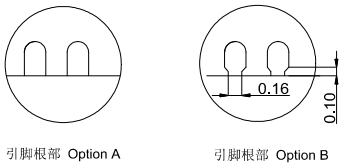
Package Outline Dimensions QFZ(QFN5X5-32-I)











Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.180	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	4.900	5.100	0.193	0.201
E	4.900	5.100	0.193	0.201
e	0.400	0.600	0.157	0.236
D2	3.400	3.600	0.134	0.142
E2	3.400	3.600	0.134	0.142
L	0.300	0.450	0.012	0.018

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPM8909Q-QFZR-S	−40 to 125°C	QFN5X5-32	M8909	MSL3	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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