4.2-A Source, 7.8-A Sink, 5-kV$_{RMS}$ Dual-Channel Isolated Gate Drivers with Miller Clamp Options

Features

- Dual-Channel Isolated Gate Drivers with TTL/CMOS-Compatible Inputs
- 4.2-A Source/7.8-A Sink Peak Output Current with Rail-to-Rail Output
- 30-V Output Driver Supply Voltage
- 3-V to 18-V V_{CCI} Input Supply Range
- 8-V and 12-V V_{DD} UVLO Options
- Programmable Overlap and Dead Time
- Ultra-Fast Output Driving
  - 30-ns Propagation Delay
  - 10-ns Minimum Pulse Width
  - 5-ns Delay Matching
  - 6-ns Pulse Width Distortion
- 5-kV$_{RMS}$ Reinforced Isolation Rating
- ±125-kV/µs Common-Mode Transient Immunity (CMTI)
- Industrial Standard Wide-Body WSOP20 Package
- Operating Ambient Temperature T_A −40°C to +125°C
- Safety-Related Certifications: (In progress)
  - VDE Reinforced Insulation according to DIN VDE V 0884-11: 2017-01
  - 5-kV$_{RMS}$ Isolation Rating per UL 1577 (in progress)
  - CSA Certification per IEC 60950-1, IEC 62368-1, and IEC 60601-1 End Equipment Standards (in progress)
  - TÜV Certification according to EN 60950-1 and EN 61010-1 (in progress)
  - CQC Certification per GB4943.1-2011 (in progress)

Applications

- Automotive OBC and DC-DC Converters
- Automotive Compressor and Thermal Management
- Isolated DC-DC and AC-DC Power Supplies
- Server, Telecom, and Industrial Infrastructure
- Motor Drives and DC-to-AC Solar Inverters
- Battery and Energy Storage Systems

Description

The TPM81530 series consists of isolated dual-channel gate drivers that feature 4.2-A source and 7.8-A sink peak current. These drivers are specifically designed to power MOSFETs, IGBTs, and SiC MOSFETs, with ultra-low propagation delay and minimal pulse-width distortion.

The input side of the TPM81530 series is isolated from its two output drivers by a reinforced isolation barrier rated at 5 kV$_{RMS}$, providing a typical of 125 kV/µs common-mode transient immunity (CMTI). Additionally, the two secondary-side drivers feature internal functional isolation, enabling a working voltage of up to 1500 V$_{DC}$.

Each driver within the series offers flexible configuration options, functioning as either two low-side drivers, two high-side drivers, or as a half-bridge driver with a programmable dead time. For safety measures, a dedicated disable pin is included, which when set to high, simultaneously shuts down both outputs. The DISABLE pin is internally pulled up, so it must be tied to ground for normal operation. Furthermore, the system incorporates a fail-safe mechanism that forces both outputs to go low in the event of a primary-side logic failure.

The device has integrated Miller Clamp to prevent false turn-on by Miller current.

Typical Application Circuit

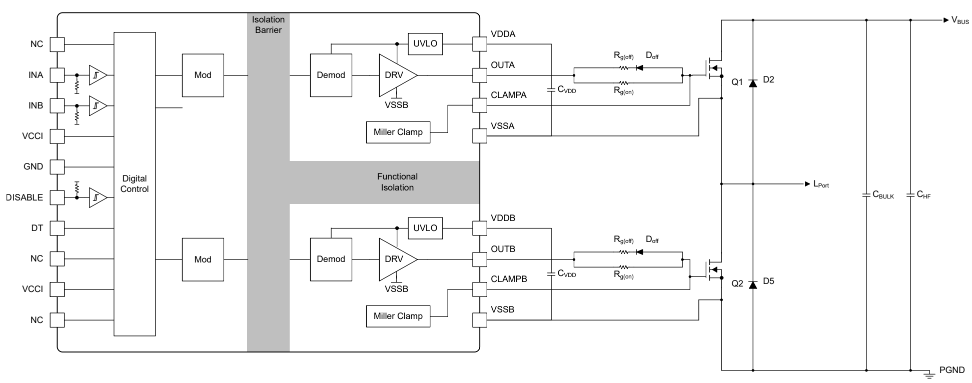


Table of Contents

Product Family Table

Order Number	UVLO Threshold (V)	Package	Feature	Quality Grade
TPM81530M-SOIR	12.5	WSOP20	Internal Miller Clamp	Industrial
TPM815301M-SOIR (1)	8.5	WSOP20	Internal Miller Clamp	Industrial
TPM81530S-SOIR (1)	12.5	WSOP20	Split Output	Industrial
TPM815301S-SOIR (1)	8.5	WSOP20	Split Output	Industrial
TPM81530E-SOIR (1)	12.5	WSOP20	External Miller Clamp	Industrial
TPM815301E-SOIR (1)	8.5	WSOP20	External Miller Clamp	Industrial

(1) Contact sales representatives for more details.

Revision History

Date	Revision	Notes
2026-05-27	Rev A.0	Initial release

Pin Configuration and Functions

TPM81530M
WSOP20
Top View

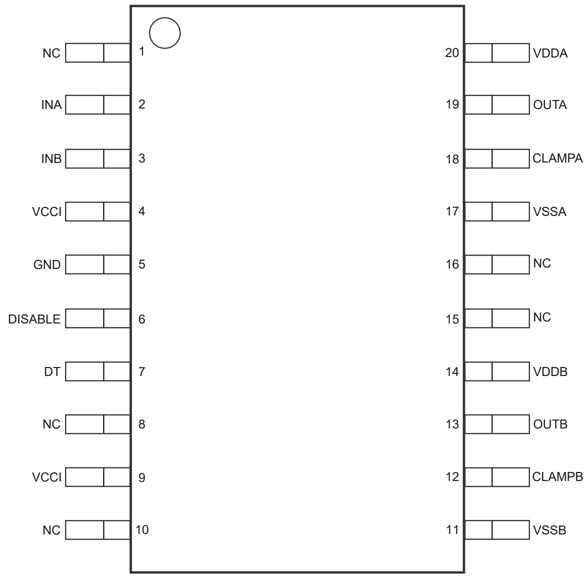


Table 1. Pin Functions: TPM81530x

Pin		I/O	Description
No.	Name		
1	NC	−	Not connected
2	INA	I	Input for A Channel, TTL/CMOS input threshold, pulled down internally. If unused, connect this pin to ground for better noise resistance.
3	INB	I	Input for B Channel, TTL/CMOS input threshold, pulled down internally. If unused, connect this pin to ground for better noise resistance.
4	VCCI	P	Primary side supply voltage. Internally connected to PIN 9. Use a low ESR/ESL capacitor close to the device to decouple the ground for stable operation.
5	GND	P	Primary side GND. All signals on the primary side are referenced to this ground connection.
6	DISABLE	I	Device disable. Internally pulled up. Drive this pin low for normal operation; drive high or leave floating to disable both outputs. If connecting to a distant microcontroller, use a 1-nF capacitor near the DISABLE pin for bypassing.
7	DT	I	Deadtime control input. Programmable deadtime between output signals. Connect DT to VCCI for no delay, or use a resistor (500 Ω to 500 kΩ) between DT and GND to adjust the delay. Add a 2.2-nF or larger ceramic capacitor next to the resistor and avoid leaving the DT pin unconnected.
8	NC	−	Not connected

Pin		I/O	Description
No.	Name		
9	VCCI	P	Primary side supply voltage. Internally connected to PIN 4. Use a low ESR/ESL capacitor close to the device to decouple the ground for stable operation.
10	NC	−	Not connected
11	VSSB	P	Channel B secondary ground. Ground reference for secondary side B channel.
12	CLAMPB	O	Channel B active Miller-clamp input to prevent false turn-on of the power switches.
13	OUTB	O	Channel B secondary output. Connect this pin to the gate terminal of the MOSFET, IGBT, GaN HEMT, or SiC FET in the B channel.
14	VDDB	P	Channel B secondary power. Use a low ESR/ESL capacitor close to the device to decouple the ground for stable operation.
15	NC	−	Not connected
16	NC	−	Not connected
17	VSSA	P	Channel A secondary ground. Ground reference for secondary side A channel.
18	CLAMPA	O	Channel A active Miller-clamp input to prevent false turn-on of the power switches.
19	OUTA	O	Channel A secondary output. Connect this pin to the gate terminal of the MOSFET, IGBT, GaN HEMT, or SiC FET in the A channel.
20	VDDA	P	Channel A secondary power. Use a low ESR/ESL capacitor close to the device to decouple the ground for stable operation.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Input Voltage	Input Bias Pin Supply Voltage, VCCI Refer to GND	−0.3	25	V
	Input Signal Voltage, INA, INB, DISABLE, Refer to GND	−5	VCCI + 0.3	V
	Input Signal Voltage, DT Refer to GND	−0.3	VCCI + 0.3	V
Output Voltage	Output Supply Voltage, $V_{DDA} – V_{SSA} V_{DDB} – V_{SSB}$	−0.3	30	V
	OUTA to VSSA, OUTB to VSSB	− 0.3	V_{DDx} + 0.3	V
	CLAMPA to VSSA, CLAMPB to VSSB	− 0.3	V_{DDx} + 0.3	V
	OUTA to VSSA, OUTB to VSSB, Transient for 200ns	− 2	V_{DDx} + 0.3	V
	CLAMPA to VSSA, CLAMPB to VSSB, Transient for 200ns	− 2	V_{DDx} + 0.3	V
	Channel-to-Channel Voltage, VSSA-VSSB, VSSB-VSSA	−1500	1500	V
T_J	Maximum Junction Temperature	−40	150	°C
T_A	Operating Ambient Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.
(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
V_{CCI} – GND	Primary Side Supply Voltage	3	20	V
V_{DDA} – V_{EEA} V_{DDB} – V_{EEB} –	Output Supply Voltage (12-V UVLO)	13.5	28	V
	Output Supply Voltage (10-V UVLO)	11.5	28	V
	Output Supply Voltage (8-V UVLO)	9.2	28	V
	Output Supply Voltage (5-V UVLO)	6.5	28	V
T_J	Junction Temperature	−40	150	°C

Parameter		Min	Max	Unit
T_A	Operating Ambient Temperature	−40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JB}	$\theta_{JC(top)}$	Unit
WSOP20	54.27	48.87	18.1	°C/W

Safety Limiting Values

Parameter		Test Conditions	Min	Typ	Max	Unit
P_D	Safety Input, Output, or Total Power	V_{CCI} = 18 V, $V_{DDA/B}$ = 12 V, INA/B = 3.3 V, 3 MHz 50% duty cycle square wave 1-nF load			1.05	W
P_{DA} P_{DB}	Power Dissipation by Each Output Driver				0.5	W
P_I	Power Dissipation by the Primary Side				0.05	W
I_S	Safety Output Supply Current	$R_{\theta JA}$ = 70°C/W, VDDA/B = 12 V, T_A = 25°C, T_J = 150°C			70	mA
		$R_{\theta JA}$ = 70°C/W, VDDA/B = 25 V, T_A = 25°C, T_J = 150°C			35	mA
P_S	Safety Supply Power, INPUT	$R_{\theta JA}$ = 70°C/W, T_A = 25°C, T_J = 150°C			50	mW
	Safety Supply Power, DRIVER A				900	mW
	Safety Supply Power, DRIVER B				900	mW
	Safety Supply Power, Total				1850	mW
T_S	Maximum Safety Temperature				150	°C

Insulation Specifications

Parameter		Conditions	Value	Unit
CLR	External Clearance	Shortest terminal-to-terminal distance through air	> 8	mm
CPG	External Creepage	Shortest terminal-to-terminal distance across the package surface	> 8	mm
DTI	Distance Through the Insulation	Minimum internal gap (internal clearance)	> 21	μm
CTI	Comparative Tracking Index		> 600	V
	Material Group		I	
	Installation Classification per IEC 60664-1	For Rated Mains Voltage ≤ 600 V_{RMS}	I-IV	
		For Rated Mains Voltage ≤ 1000 V_{RMS}	I-III	
	Pollution Degree		2	
	Climate Category		40/125/21	
C_{IO}	Isolation Capacitance	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	1.2	pF
R_{IO}	Isolation Resistance	V_{IO} = 500 V, T_A = 25 °C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125 °C	> 10^{11}	
		V_{IO} = 500 V, T_A = 150 °C	> 10^9	
V_{IORM}	Maximum Repetitive Isolation Voltage	AC voltage (bipolar)	1700	V_{PK}
	Maximum Working Isolation Voltage	AC voltage (sine wave); time dependent dielectric breakdown (TDDB)	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IOWM}	Maximum Working Isolation Voltage	AC voltage; TDDB Test	1060	V_{RMS}
		DC voltage	1500	V_{DC}
V_{IOTM}	Maximum Transient Isolation Voltage	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production)	8000	V_{PK}
V_{IOSM}	Maximum Surge Isolation Voltage	Test method per IEC 62368-1, 1.2/50 μs waveform, V_{TEST} = 1.3 × V_{IOSM}(qualification) = 10000 V	7692	V_{PK}
V_{ISO}	UL 1577 Withstand Isolation Voltage	V_{TEST} = V_{ISO} = 5000 V_{RMS}, t = 60 s (in qualification); V_{TEST} = 1.2 × V_{ISO} = 6000 V_{RMS}, t = 1 s (100% in production)	5000	V_{RMS}
q_{pd}	Apparent Charge	Method a, After Input/Output safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10 s	≤ 5	pC
		Method a, After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10 s	≤ 5	

Parameter		Conditions	Value	Unit
		Method b1; At routine test (100% production) and preconditioning (type test), V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1 s	≤ 5	

(1) All pins on each side of the barrier tied together create a two-terminal device.

Electrical Characteristics

All test conditions: V_{DDA} = V_{DDB} = 15 V, V_{SSA} and V_{SSB} referred as GND, T_A = −40°C to 125°C, unless otherwise noted. Typical value tested at V_{DDA} = V_{DDB} = 15 V

Parameter		Conditions	Min	Typ	Max	Unit
Supply						
I_{VCCI}	VCCI Quiescent Current	VINA = 0 V, VINB = 0 V		1.5	2	mA
I_{VDDA},I_{VDDB}	VDDA and VDDB Quiescent Current	VINA = 0 V, VINB = 0 V, VDD = 15 V		1.25	2.5	mA
I_{VCCI}	VCCI Operating Current	*f* = 500 kHz, current per channel, C_{OUT} = 100 pF		2.0		mA
I_{VDDA},I_{VDDB}	VDDA and VDDB Operating Current	*f* = 500 kHz, current per channel, C_{OUT} = 100 pF, VDD = 15 V		2.5		mA
V_{VCCI_ON}	Rising Threshold		2.55	2.7	2.85	V
V_{VCCI_OFF}	Falling Threshold VCCI_OFF		2.35	2.5	2.68	V
V_{VCCI_HYS}	Threshold Hysteresis			0.2		V
Input						
VINAH, VINBH,	Input High Voltage VDISH		1.6	1.7	1.9	V
VINAL, VINBL, VDISL	Input Low Voltage		1.15	1.3	1.45	V
VINA_HYS, VINB_HYS, VDIS_HYS	Input Hysteresis			0.4		V
VINA, VINB	Negative Transient, Ref to GND, 50 ns Pulse		−5			V
Output UVLO - 8-V						
V_{VDDA_ON}, V_{VDDB_ON}	Rising Threshold VDDA_ON, VDDB_ON		8.3	8.7	9.2	V
V_{VDDA_OFF}, V_{VDDB_OFF}	Falling Threshold VDDA_OFF, VDDB_OFF		7.8	8.2	8.7	V
V_{VDDA_HYS}, V_{VDDB_HYS}	Threshold Hysteresis			0.5		V
Output UVLO - 12-V						
V_{VDDA_ON}, V_{VDDB_ON}	Rising Threshold VDDA_ON, VDDB_ON		13.3	13.6	14	V

Parameter		Conditions	Min	Typ	Max	Unit
V_{VDDA_OFF}, V_{VDDB_OFF}	Falling Threshold VDDA_OFF, VDDB_OFF		12.2	12.8	13.2	V
V_{VDDA_HYS}, V_{VDDB_HYS}	Threshold Hysteresis			0.8		V
Output						
V_{OUTPD}	Output Active Pull Down on OUTx	I_{OUT} = 0.1*$I_{OUT(L)}$,V_{DDx}=OPEN		2.4		V
I_{OA+}, I_{OB+}	Peak Output Source Current	C_{VDD} = 10 μF, C_{LOAD} = 0.18 μF, f = 1 kHz		4.2		A
I_{OA-}, I_{OB-}	Peak Output Sink Current	C_{VDD} = 10 μF, C_{LOAD} = 0.18 μF, f = 1 kHz		7.8		A
R_{OHA}, R_{OHB}	Output Resistance at High State	I_{OUT} = −10 mA, TA = 25°C, R_{OHA}, R_{OHB}		5		Ω
R_{OLA}, R_{OLB}	Output Resistance at Low State	I_{OUT} = 10 mA, T_A = 25°C		0.55		Ω
V_{OHA}, V_{OHB}	Output Voltage at High State	V_{VDDA}, V_{VDDB} = 15 V, I_{OUT} = −10 mA, TA = 25°C		14.95		V
V_{OLA}, V_{OLB}	Output Voltage at Low State	V_{VDDA}, V_{VDDB} = 15 V, I_{OUT} = 10 mA, TA = 25°C		5.5		mV
Internal Miller Clamp						
V_{CLMPTH}	Miller Clamp Threshold Voltage	Refer to VSSx	1.5	2	2.5	V
V_{CLMPI}	Output Low Clamp Voltage	Refer to VSSx, ICLMPI = 1A		0.5		V
I_{CLAMP}	Output Low Clamp Current	VCLMPI = 0 V, VEE = −2.5 V		3		A
t_{CLAMPI}	Miller Clamp ON Delay Time	CL = 1.8 nF		30	50	ns
Timing						
t_{DEAD}	Dead Time	Pull DT pin to VCCI	Determined by INA and INB			
		DT pin floating	0.8		15	ns
		R_{DT}= 20 kΩ	160	200	240	ns
t_{RISE}	Output Rise Time, 20% to 80% Measured Points	COUT = 1.8 nF		6	16	ns
t_{FALL}	Output Fall Time, 90% to 10% Measured Points	COUT = 1.8 nF		7	12	ns
t_{PWmin}	Minimum Pulse Width	Output off for less than minimum, COUT = 0 pF			20	ns
t_{PDHL}	Propagation Delay from INx to OUTx Falling Edges			30		ns
t_{PDLH}	Propagation Delay from INx to OUTx Rising Edges			30		ns
t_{PWD} (1)	Pulse Width Distortion |tPDLH − tPDHL|				6	ns

Parameter		Conditions	Min	Typ	Max	Unit
t_{DM} (1)	Propagation Delays Matching Between VOUTA, VOUTB	f = 100 kHz			5	ns
t_{VDD+} to OUT VDDA, VDDB	Power-Up Delay Time: UVLO Rise to OUTA, OUTB. See	INA or INB tied to VCCI	8	10	12	μs

(1) Guaranteed by design

Parameter Measurement

The switching parameters in the Electrical Characteristics table are measured with the test circuits shown in Figure 1 (propagation delay, rise time, fall time, pulse width distortion, dead time) and Figure 2 (Common Mode Transient Immunity, CMTI). All measurements use the recommended bypass capacitor configuration on V_{CCI}, V_{DDA}, and V_{DDB}.

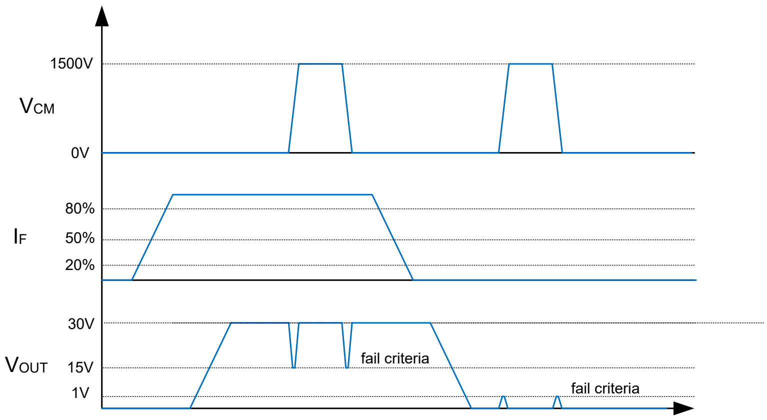


Figure 1. Switching Parameter Test Circuit

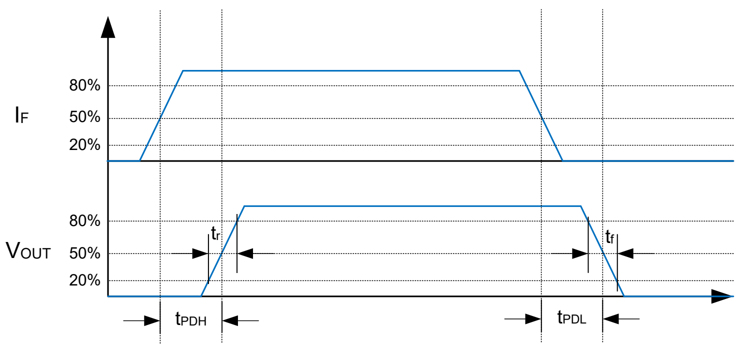
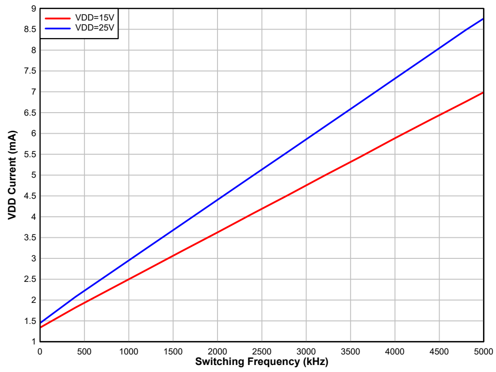


Figure 2. CMTI Test Circuit

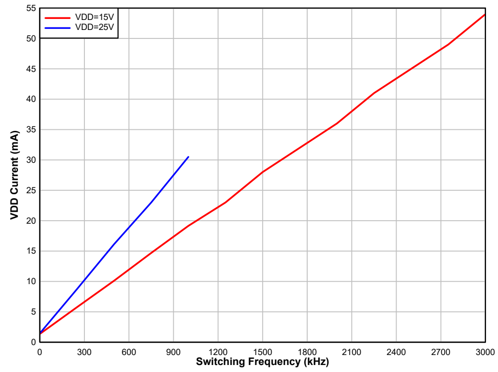
4.2-A Source, 7.8-A Sink, 5-kV$_{RMS}$ Dual-Channel Isolated Gate Drivers with Miller Clamp Options

Typical Performance Characteristics



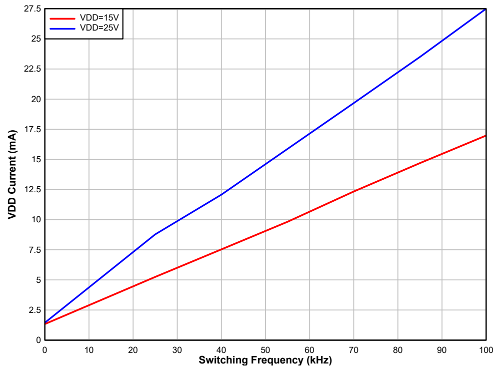
No Load, VDD = 15 V or 25 V

Figure 3. VDDx Current Consumption vs. Frequency



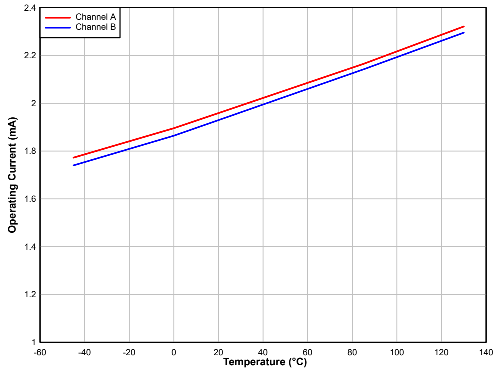
1-nF Load, VDD = 15 V or 25 V

Figure 4. VDDx Current Consumption vs. Frequency



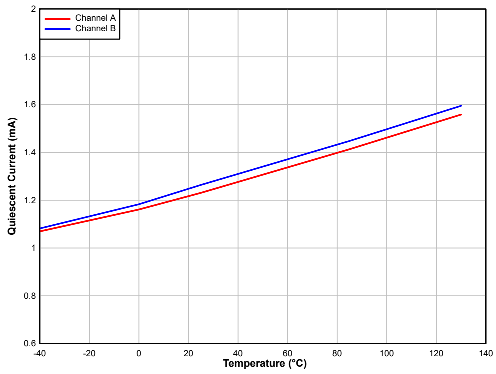
10-nF Load, VDD = 15 V or 25 V

Figure 5. VDDx Current Consumption vs. Frequency



No Load, VDD = 15 V, *f* = 500 kHz

Figure 6. VDDx Current Consumption vs. Temperature



No Load, IN Low, No Switching, VDD = 15 V

Figure 7. VDDx Quiescent Current Consumption vs. Temperature

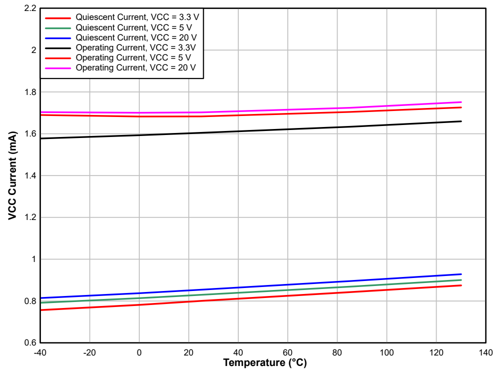
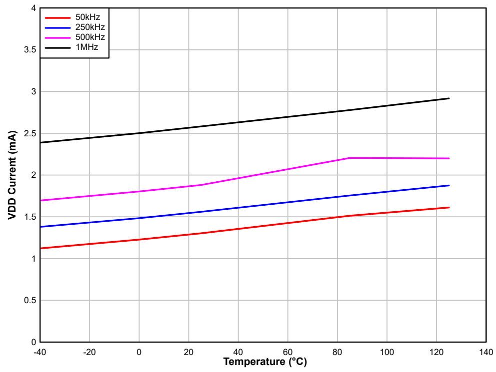


Figure 8. VCCI Current Consumption vs. Temperature



No Load, IN Low, VDD = 15 V

Figure 9. VDDx Switching Current Consumption vs. Temperature

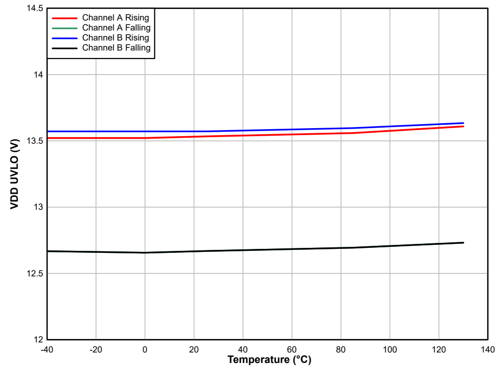


Figure 10. VDD 12-V UVLO Threshold vs. Temperature

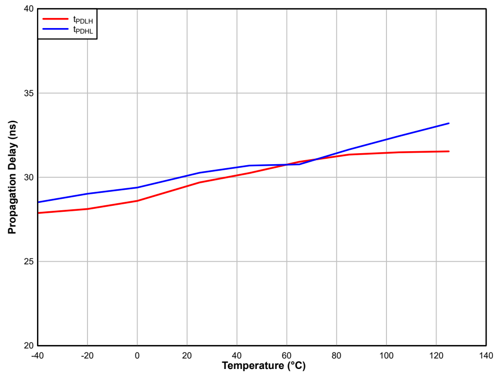


Figure 11. Propagation Delay vs. Temperature

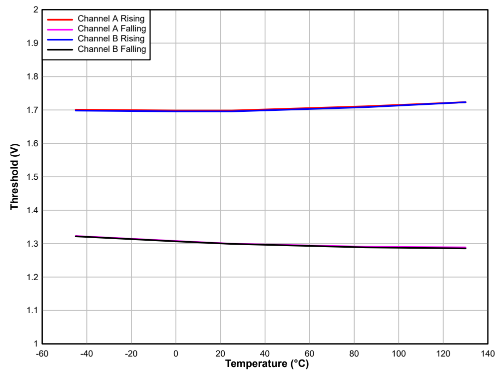


Figure 12. INx/DISABLE Threshold vs. Temperature

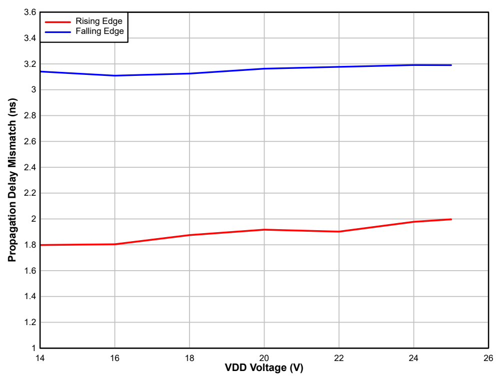


Figure 13. Propagation Delay Matching (t_{DM}) vs. VDD

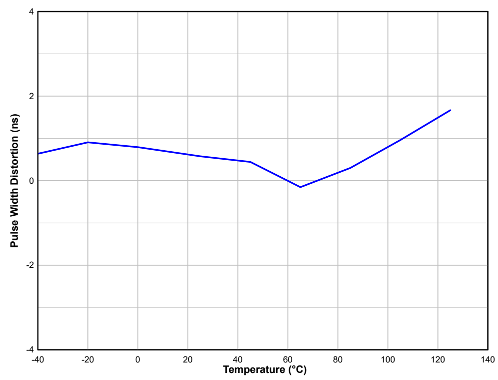
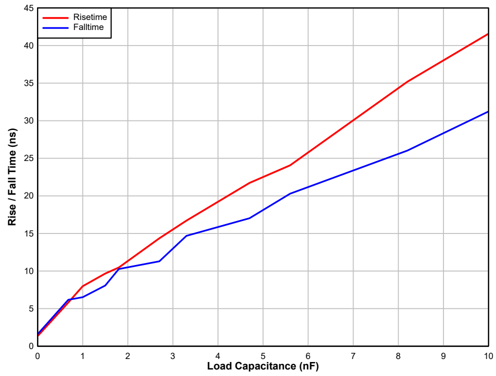
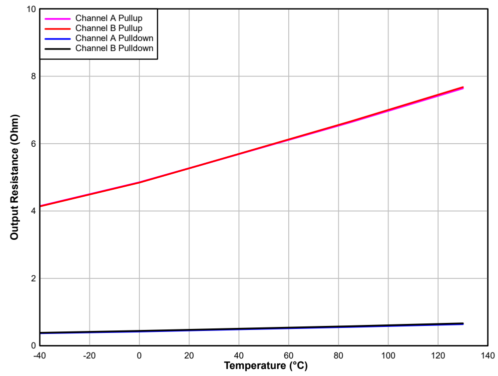


Figure 14. Pulse Width Distortion vs. Temperature



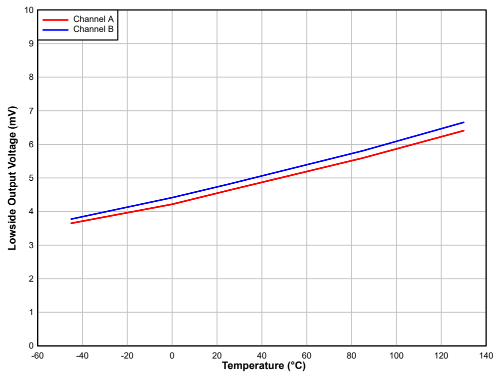
VDD = 12 V

Figure 15. Rise and Fall Time vs. Load Capacitance



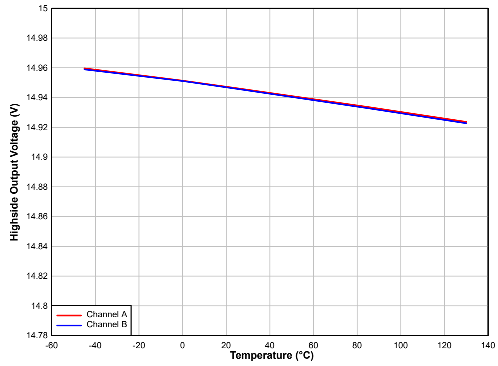
VDD = 12 V

Figure 16. Output Resistance vs. Temperature



VDD = 15 V, I_{OUT} = 10 mA

Figure 17. VOL vs. Temperature



VDD = 15 V, I_{OUT} = −10 mA

Figure 18. VOH vs. Temperature

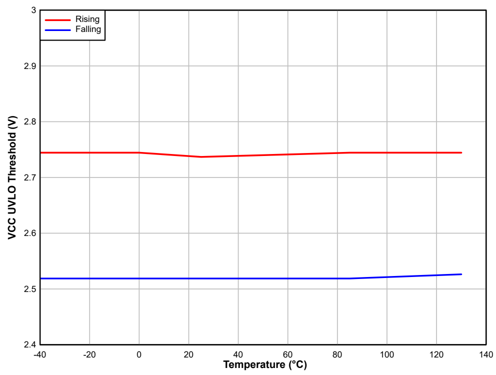


Figure 19. VCC UVLO Threshold vs. Temperature

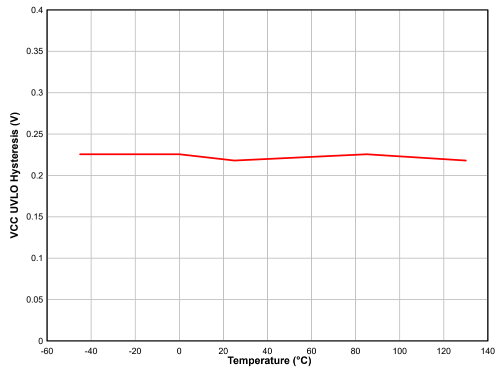


Figure 20. VCC UVLO Hysteresis vs. Temperature

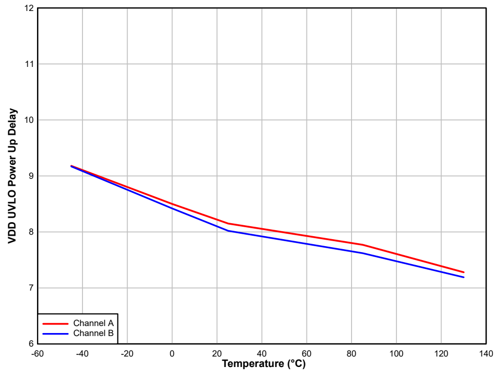


Figure 21. VDD UVLO Delay vs. Temperature

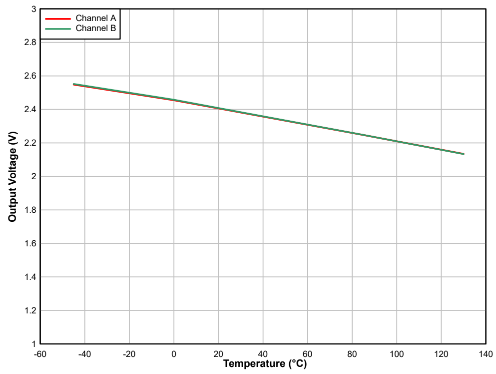


Figure 22. Active Pulldown Voltage vs. Temperature

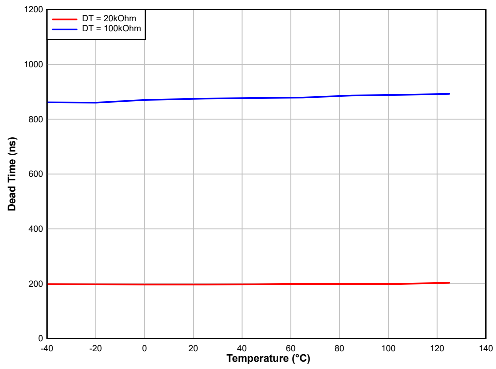


Figure 23. Dead Time vs. Temperature

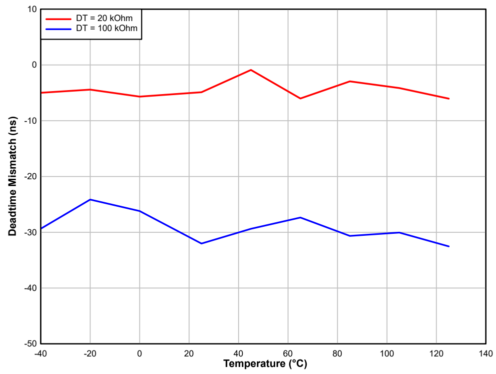
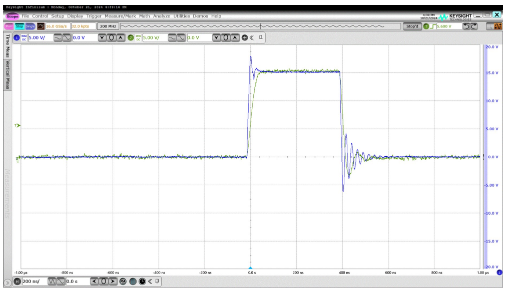


Figure 24. Dead Time Mismatch vs. Temperature



CH: 1-nF Load; CH2 10-nF Load

Figure 25. Typical Output Waveform

Detailed Description

Overview

The TPM81530 family of dual gate drivers is designed for high-performance power transistor switching. These drivers act as an isolated bridge between controllers and transistor gates, ensuring efficient and reliable operation. With their ability to adapt to various power supply and motor systems, as well as support for different transistors including GaN HEMT, IGBT and SiC MOSFETs, the TPM81530 family offers versatility and flexibility. Advanced features such as programmable dead time control and voltage protection enhance system safety and stability. Whether used with digital or analog controllers, the TPM81530 family provides a robust solution for power transistor driving needs. The TPM81530 family provides Miller Clamp features enhanced for SiC MOSFETs.

Functional Block Diagram

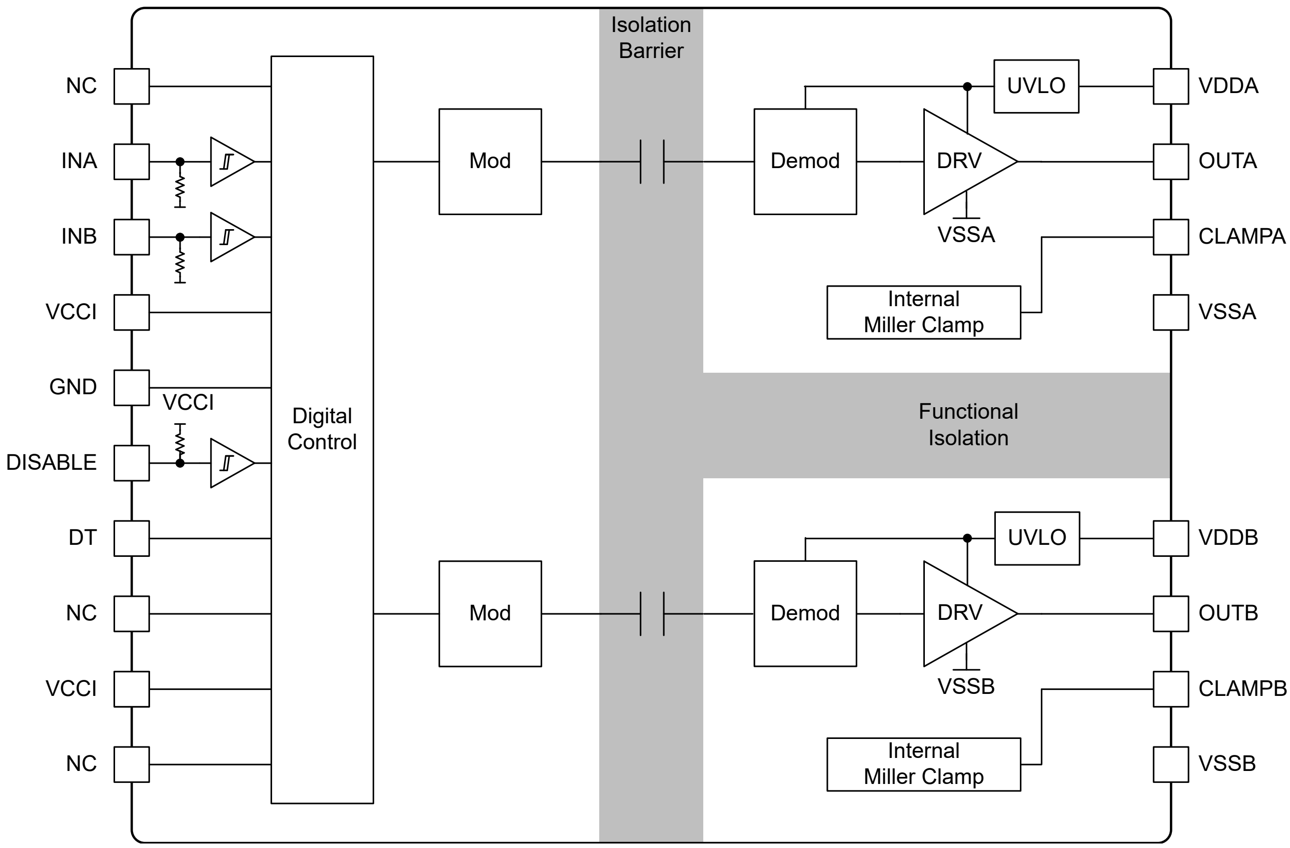


Figure 26. Functional Block Diagram

Feature Description

Supply and UVLO

The TPM81530 family of gate drivers features internal undervoltage lock-out (UVLO) protection on both the supply circuit and the input side. This UVLO function ensures reliable operation by monitoring the VDD and VCCI voltages.

For the VDD supply circuit, if the bias voltage falls below a certain threshold (V_{VDD_ON} at rising edge or V_{VDD_OFF} at falling edge), the UVLO protection activates, holding the affected output low regardless of the input pin status. This prevents potential damage or malfunction due to insufficient bias voltage.

Additionally, the TPM81530 family incorporates an active clamp circuit that keeps the driver outputs low when the output stages are in an unbiased or UVLO condition. This clamp circuit limits the voltage rise on the driver outputs, effectively clamping them to the threshold voltage of the lower NMOS device, typically around 2 V, when no bias power is available.

To enhance stability and prevent chatter caused by ground noise from the power supply, the VDD UVLO protection in the TPM81530 family includes a hysteresis feature (V_{VDD_HYS}). This hysteresis also allows the device to tolerate small drops in bias voltage that may occur during switching operations or sudden increases in operating current consumption.

The input side of the TPM81530 family has a UVLO protection feature that monitors the VCCI voltage. The device remains inactive until the VCCI voltage exceeds a certain threshold (V_{VCCI_ON}) during start-up. Once operational, if the VCCI voltage drops below another threshold (V_{VCCI_OFF}), the output will not follow inputs and hold low regardless of the input pin status. This input UVLO also includes hysteresis (V_{VCCI_HYS}) for stable operation.

Input Stage

The TPM81530 family of gate drivers incorporates TTL and CMOS compatible input pins, specifically INA, INB, and DIS, which maintain complete isolation from the VDD supply voltage. These pins are characterized by a high threshold voltage (V_{INAH}) of 1.7 V and a low threshold voltage of 1.3 V, facilitating seamless integration with logic-level control signals originating from devices such as 3.3-V microcontrollers. Additionally, the input pins exhibit a hysteresis of 0.4 V, significantly enhancing noise immunity and ensuring robust operational stability.

To guarantee reliable device performance, the TPM81530 family incorporates internal pull-down resistors, typically rated at 200 kΩ, which serve to automatically drive any unused input pins to a low voltage state. Nonetheless, it is still recommended to manually ground any unused input pins for optimal device operation.

The isolation between the input circuitry and the output drivers within the TPM81530 family provides flexibility for different applications. The amplitude of the input signal can exceed or fall below the VDD voltage, provided it remains within the manufacturer's recommended operating limits. Crucially, the voltage amplitude of signals applied to the INA or INB pins must never surpass the VCCI voltage. This inherent flexibility facilitates seamless integration with a wide range of control signal sources, empowering users to select the most appropriate VDD voltage for their specific gate driver requirements.

Output Stage

The TPM81530 family, features an enhanced output stage designed to optimize power switch turn-on transitions, particularly during the critical Miller plateau region.

Both outputs of the TPM81530 family are capable of delivering robust 4.2-A peak source and 7.8-A peak sink current pulses. The output voltage operates rail-to-rail between VDD and VSS, with minimal dropout. This design enhances the overall performance and reliability of the gate drivers in demanding applications.

Active Miller Clamp

The TPM81530M family incorporates an active Miller-clamp function to mitigate false turn-on of the power switches that may be caused by Miller current in applications utilizing a unipolar power supply. This function is designed to address the specific challenges associated with the use of a unipolar power supply.

The active Miller-clamp function is achieved by introducing a low impedance path between the gate terminal of the power switch and ground (VSSx) to effectively sink the Miller current. By providing this clamp, the gate voltage of the power switch is limited to less than 2 V during the off state, preventing unintended turn-on.

By implementing the active Miller-clamp function, the TPM81530 family ensures reliable operation by suppressing the effects of Miller current and preventing false turn-on of the power switches. This feature is particularly beneficial in applications utilizing a unipolar power supply, enhancing the overall performance and robustness of the system.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPM81530 provides reinforced isolation between PWM control logic and high-voltage SiC gate driving. This section describes the design considerations for typical isolated half-bridge applications.

Input Signal Interface

INA and INB accept TTL- and CMOS-compatible PWM signals. The input thresholds are specified in the Electrical Characteristics table. The DISABLE pin overrides INA and INB and forces both outputs low. An internal pull-up on DISABLE keeps both outputs disabled when the pin is left open; tie DISABLE to ground for normal operation.

Dead-Time Programming

The DT pin sets the dead time inserted between OUTA and OUTB transitions. An external resistor at DT programs the delay. The dead time scales linearly with the DT resistance over the programmable range. Typical values for SiC half-bridges are 100 ns to 500 ns depending on switching speed and gate-drive impedance.

UVLO Selection

The TPM81530 family offers 8-V and 12-V V_{DD} UVLO options. Choose the 8-V variant for low-loss SiC drive at V_{DD} = 12 V. Choose the 12-V variant for IGBT applications at V_{DD} = 15 V or higher. The UVLO threshold protects against insufficient gate drive during start-up and brown-out events.

Negative Gate Bias

Asymmetric V_{CC2} and V_{EE2} supplies provide a negative turn-off voltage at each gate. The negative bias prevents Miller-induced false turn-on at high dV/dt. Typical SiC bias values are +15 V / −3 V or +18 V / −4 V referenced to the local source.

Miller Clamp

The CLAMPA and CLAMPB pins activate during the off-state and short Miller current to the local source. Each CLAMP pin connects directly to the corresponding gate without intervening impedance. The clamp activates when V_{GS} falls below the clamp threshold specified in the Electrical Characteristics.

Isolation Barrier

The TPM81530 provides 5-kV$_{RMS}$ reinforced isolation per DIN VDE V 0884-11. The package creepage and clearance distances meet the requirements for 1500-V$_{DC}$ working voltage. Maintain PCB clearance equal to or greater than the package specification under the body of the device.

Bypass and Layout

Place bypass capacitors directly at the VCCI, VDDA, VDDB, VSSA, and VSSB pins. Use 0.1-μF ceramic capacitors on each bias pin. Add a 1-μF bulk capacitor in parallel with each isolated bias rail. Keep the gate-loop trace short to minimize parasitic inductance and switching ringing.

Typical Application

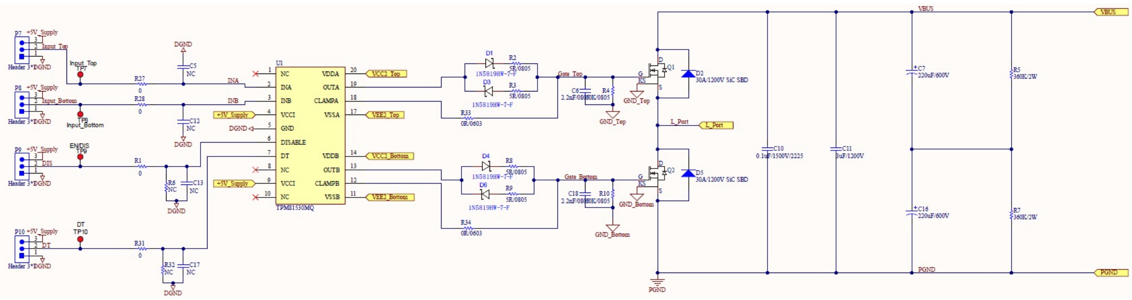


Figure 27. TPM81530 Typical Application Schematic

The TPM81530 drives a half-bridge that switches two 1200-V SiC MOSFETs Q1 and Q2.

The primary side runs from a 5-V logic supply on the VCCI pins. INA and INB receive the high-side and low-side PWM signals through R27 and R28. The DISABLE pin shuts down both outputs simultaneously when driven high. The DT pin sets the dead time through R31 and the R32-C17 network.

The secondary side uses two isolated bias rails for asymmetric SiC gate drive. VCC2_Top and VEE2_Top supply the top driver. VCC2_Bottom and VEE2_Bottom supply the bottom driver. Each rail delivers a positive turn-on voltage and a negative turn-off voltage referenced to the local source.

OUTA and OUTB drive each SiC gate through a split gate-resistor network. D1 and R2 set the turn-on path; D3 and R3 set the turn-off path. The split allows independent tuning of dV/dt during each transition. C6 and R4 at the gate node prevent V_{GS} floating and suppress Miller-induced bouncing.

The CLAMPA and CLAMPB pins connect directly to the SiC gates. Each pin pulls the gate to the negative rail when V_{GS} falls below the clamp threshold. The clamp absorbs Miller current during the off-state and prevents shoot-through.

The DC bus places two 220-μF, 600-V electrolytics (C7, C16) in series across the 1200-V VBUS rail. C10 (0.1 μF, 1500 V) and C11 (3 μF, 1200 V) provide high-frequency bypass at the half-bridge node. R5 and R7 (360 kΩ, 2 W) balance and bleed the bulk capacitors. Q1 and Q2 each include an external 30-A, 1200-V SiC SBD (D2, D5) for free-wheeling current.

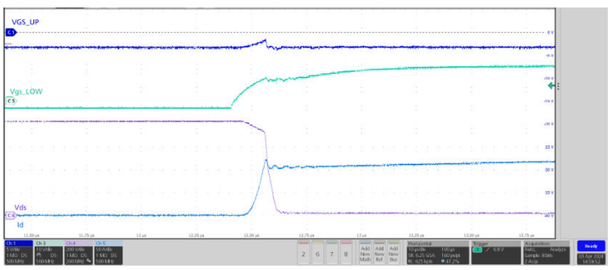


Figure 28. Switching Waveform — Rising Edge

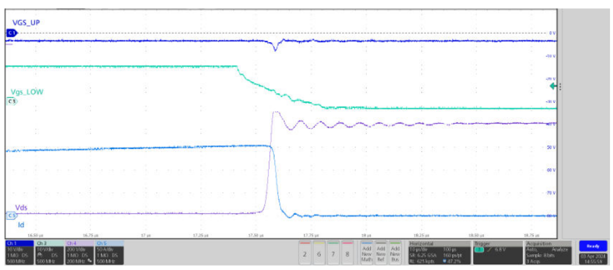


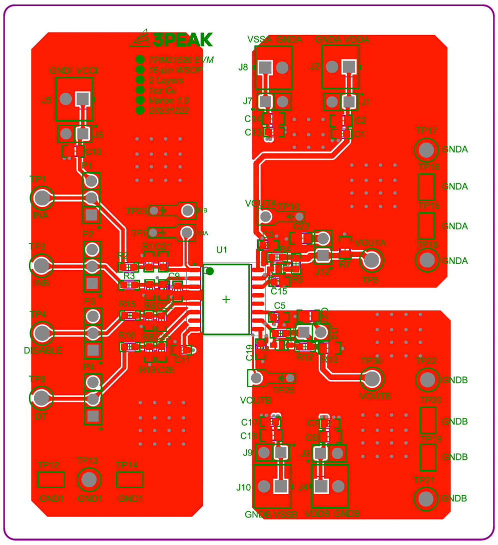
Figure 29. Switching Waveform — Falling Edge

Layout

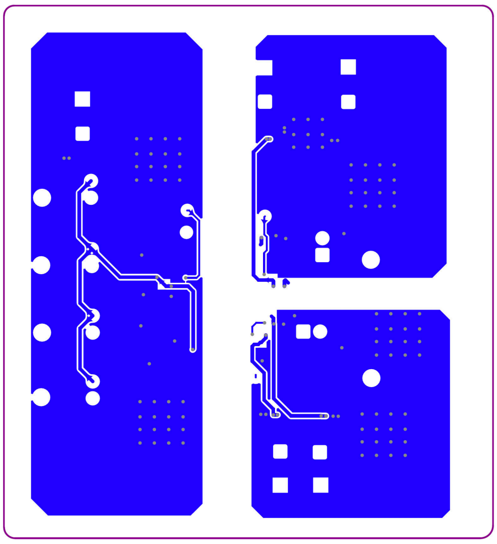
Layout Guideline

- For voltage mode input drivers, a low ESR and ESL capacitor should be placed close to the VCC and VEE pins, and the loop from VCC to VEE should be made small.
- For current mode input drivers, a low ESR and ESL capacitor should be placed close to the Cathode and Anode pins.
- To minimize the inductance of the drive circuit loop, the driver should be placed close to the transistor.
- The Miller clamp trace should be directly connected to the transistor's gate, and the trace should be kept short.
- To ensure isolation between the primary and secondary sides, avoid placing any PCB traces or copper directly below the driver device. A PCB cutout or groove is recommended to increase the creepage distance.
- To enhance thermal performance, it is recommended to enlarge the PCB copper connected to VCC and VEE.

Layout Example

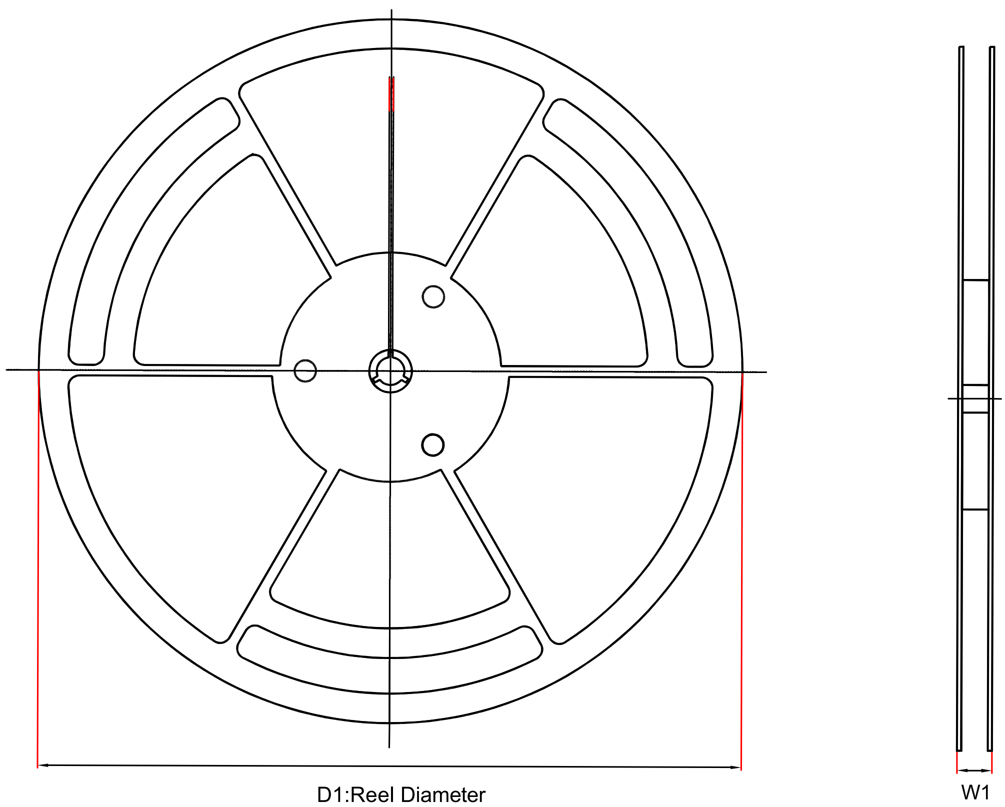


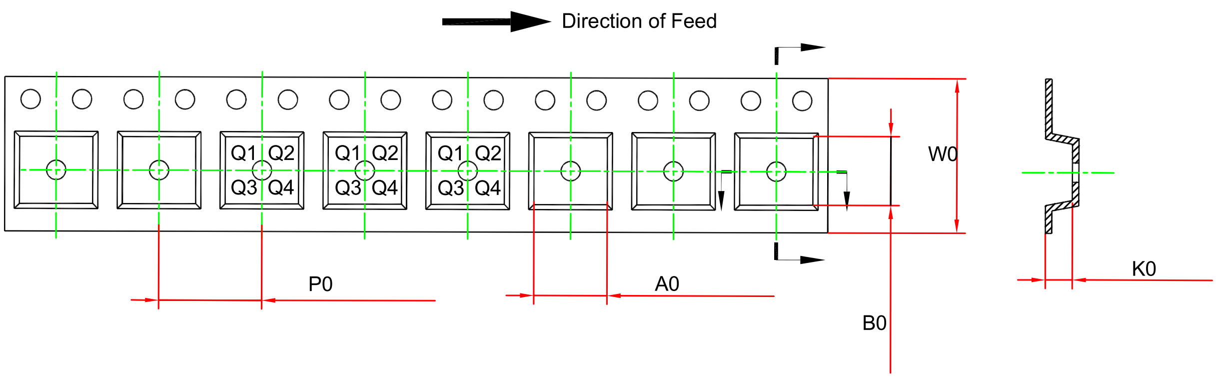
Top Layer



Bottom Layer

Tape and Reel Information





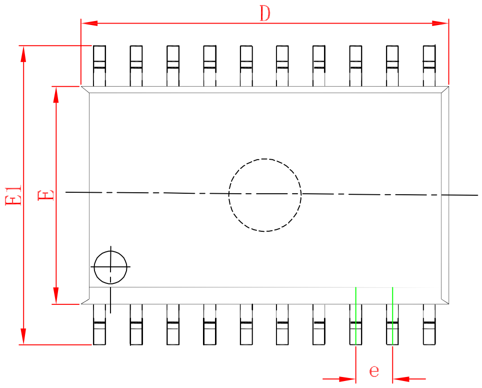
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM81530M-SOIR	WSOP20	330	31.6	10.8	13.3	3.2	16	24	Q1
TPM815301M-SOIR	WSOP20	330	31.6	10.8	13.3	3.2	16	24	Q1
TPM81530S-SOIR	WSOP20	330	31.6	10.8	13.3	3.2	16	24	Q1
TPM815301S-SOIR	WSOP20	330	31.6	10.8	13.3	3.2	16	24	Q1
TPM81530E-SOIR	WSOP20	330	31.6	10.8	13.3	3.2	16	24	Q1

Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM815301E-SOIR	WSOP20	330	31.6	10.8	13.3	3.2	16	24	Q1

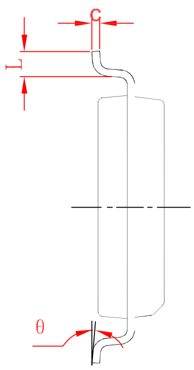
Package Outline Dimensions

WSOP20

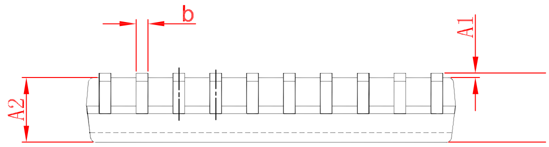
Package Outline Dimensions SOI (WSOP-20-A)



TOP VIEW



SIDE VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	2.350	2.650	0.093	0.104
A1	0.100	0.300	0.004	0.012
A2	2.100	2.500	0.083	0.098
b	0.330	0.510	0.013	0.020
c	0.204	0.330	0.008	0.013
D	12.520	13.000	0.493	0.512
E	7.400	7.600	0.291	0.299
E1	10.210	10.610	0.402	0.418
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Ambient Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPM81530M-SOIR	−40 to 125°C	WSOP20	M853M	3	1000	Green
TPM815301M-SOIR (1)	−40 to 125°C	WSOP20	M856M	3	1000	Green
TPM81530S-SOIR (1)	−40 to 125°C	WSOP20	M853S	3	1000	Green
TPM815301S-SOIR (1)	−40 to 125°C	WSOP20	M856S	3	1000	Green
TPM81530E-SOIR (1)	−40 to 125°C	WSOP20	M853E	3	1000	Green
TPM815301E-SOIR (1)	−40 to 125°C	WSOP20	M856E	3	1000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

(1) Contact 3PEAK representatives for more information.

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