4-A/7-A, 1-Ch Isolated Gate Driver with Miller Clamp, Split Gate

Features

- Single-Channel Isolated Gate Driver with CMOS/TTL-Compatible Input
- 4-A Source/7-A Sink Peak Output Current with Rail-to-Rail Output
- Feature Options
  - Split Outputs (TPM5355S)
  - Miller Clamp (TPM5355M)
- Up to 35-V Output Driver Supply Voltage
- 6-V, 8-V, 12-V, 18-V V_{CC2} UVLO Options
- 3-V to 5.5-V Input Supply Voltage
- Ultra-Fast Output Driving
  - 60-ns Propagation Delay
  - 25-ns Delay Matching
  - 5-ns Pulse Width Distortion
- 5.7-kV_{RMS} Reinforced Isolation Rating for WSOP8
- ±150-kV/μs Common-Mode Transient Immunity (CMTI)
- Industrial Standard Wide-Body WSOP8 & SOP8 Packages
- TPM5355xQ : AEC-Q100 Qualified for Automotive Applications
  - Grade 1 : −40°C to +125°C
- Safety-Related Certifications: (In progress)
  - VDE Reinforced Insulation according to DIN VDE V 0884-11: 2017-01 (In Progress)
  - 5-kV_{RMS} Isolation Rating per UL 1577
  - CQC Certification per GB4943.1-2011

Applications

- Industrial Motor-Control Drives
- Industrial Power Supplies, UPS
- Solar Inverters
- Automotive On-board Charger, High-Voltage DC/DC Converter
- Silicon Carbide (SiC) Driver

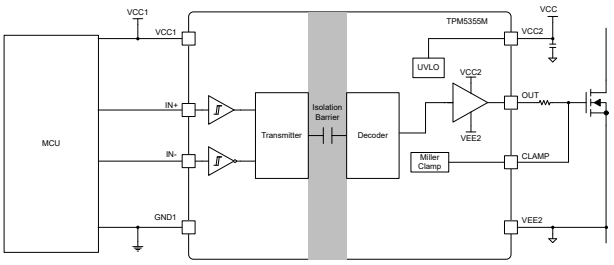
Description

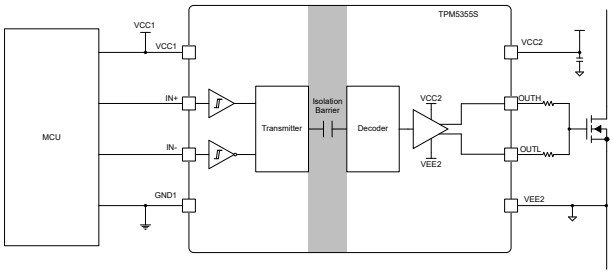
The TPM5355x family is a series of reinforced-isolation single-channel gate drivers for IGBTs, silicon MOSFETs, and SiC MOSFETs. Each device couples a logic-side input stage to an isolated high-current output stage through a double-capacitive silicon-dioxide (SiO_2) barrier, galvanically separating the controller from the power switch while faithfully reproducing the input signal at the gate.

The family covers three branches. The TPM5355 is the industrial-grade baseline. The TPM5355Q is the automotive-grade, AEC-Q100 qualified, pin- and electrically-compatible counterpart. The TPM53551 is a pin-compatible industrial variant that uses TTL-compatible input thresholds in place of the CMOS-compatible thresholds used on the TPM5355 and the TPM5355Q. Miller-Clamp (M) variants add an active gate clamp for unipolar supplies; Split-Output (S) variants expose separate source and sink paths for independent slew-rate tuning.

The TPM5355x family is intended for industrial motor drives, power conversion, UPS, solar inverters, automotive on-board chargers, and high-voltage DC/DC converters — any application that needs robust, low-latency, noise-immune gate drives across an isolation barrier. Reinforced isolation and high common-mode transient immunity make the family suitable for fast-switching SiC and GaN power stages.

Typical Application Circuit





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Product Family Table

Order Number	UVLO Rising Threshold (V)	Input Threshold Type	Feature	Package	Marking	Quality Grade
TPM5355AM-SO1R (1)	6	CMOS (% V_{CCI})	Miller Clamp	SOP8	M5355A	Industrial
TPM5355AM-SOAR (1)	6	CMOS (% V_{CCI})	Miller Clamp	WSOP8	M5355A	Industrial
TPM5355AS-SO1R (1)	6	CMOS (% V_{CCI})	Split Output	SOP8	S5355A	Industrial
TPM5355AS-SOAR (1)	6	CMOS (% V_{CCI})	Split Output	WSOP8	S5355A	Industrial
TPM5355BM-SO1R	8.5	CMOS (% V_{CCI})	Miller Clamp	SOP8	M5355B	Industrial
TPM5355BM-SOAR	8.5	CMOS (% V_{CCI})	Miller Clamp	WSOP8	M5355B	Industrial
TPM5355BS-SO1R	8.5	CMOS (% V_{CCI})	Split Output	SOP8	S5355B	Industrial
TPM5355BS-SOAR	8.5	CMOS (% V_{CCI})	Split Output	WSOP8	S5355B	Industrial
TPM5355CM-SO1R	12.5	CMOS (% V_{CCI})	Miller Clamp	SOP8	M5355C	Industrial
TPM5355CM-SOAR	12.5	CMOS (% V_{CCI})	Miller Clamp	WSOP8	M5355C	Industrial
TPM5355CS-SO1R	12.5	CMOS (% V_{CCI})	Split Output	SOP8	S5355C	Industrial
TPM5355CS-SOAR	12.5	CMOS (% V_{CCI})	Split Output	WSOP8	S5355C	Industrial
TPM5355DM-SO1R (1)	17.6	CMOS (% V_{CCI})	Miller Clamp	SOP8	M5355D	Industrial
TPM5355DM-SOAR(1)	17.6	CMOS (% V_{CCI})	Miller Clamp	WSOP8	M5355D	Industrial
TPM5355DS-SO1R (1)	17.6	CMOS (% V_{CCI})	Split Output	SOP8	S5355D	Industrial
TPM5355DS-SOAR (1)	17.6	CMOS (% V_{CCI})	Split Output	WSOP8	S5355D	Industrial
TPM5355AMQ-SO1R-S (1)	6	CMOS (% V_{CCI})	Miller Clamp	SOP8	M5355A	Automotive
TPM5355AMQ-SOAR-S (1)	6	CMOS (% V_{CCI})	Miller Clamp	WSOP8	M5355A	Automotive
TPM5355ASQ-SO1R-S (1)	6	CMOS (% V_{CCI})	Split Output	SOP8	S5355A	Automotive
TPM5355ASQ-SOAR-S (1)	6	CMOS (% V_{CCI})	Split Output	WSOP8	S5355A	Automotive
TPM5355BMQ-SO1R-S (1)	8.5	CMOS (% V_{CCI})	Miller Clamp	SOP8	M5355B	Automotive
TPM5355BMQ-SOAR-S	8.5	CMOS (% V_{CCI})	Miller Clamp	WSOP8	M5355B	Automotive
TPM5355BSQ-SO1R-S	8.5	CMOS (% V_{CCI})	Split Output	SOP8	S5355B	Automotive

Order Number	UVLO Rising Threshold (V)	Input Threshold Type	Feature	Package	Marking	Quality Grade
TPM5355BSQ-SOAR-S (1)	8.5	CMOS (% V_{CCI})	Split Output	WSOP8	S5355B	Automotive
TPM5355CMQ-SO1R-S (1)	12.5	CMOS (% V_{CCI})	Miller Clamp	SOP8	M5355C	Automotive
TPM5355CMQ-SOAR-S (1)	12.5	CMOS (% V_{CCI})	Miller Clamp	WSOP8	M5355C	Automotive
TPM5355CSQ-SO1R-S (1)	12.5	CMOS (% V_{CCI})	Split Output	SOP8	S5355C	Automotive
TPM5355CSQ-SOAR-S (1)	12.5	CMOS (% V_{CCI})	Split Output	WSOP8	S5355C	Automotive
TPM5355DMQ-SO1R-S (1)	17.6	CMOS (% V_{CCI})	Miller Clamp	SOP8	M5355D	Automotive
TPM5355DMQ-SOAR-S (1)	17.6	CMOS (% V_{CCI})	Miller Clamp	WSOP8	M5355D	Automotive
TPM5355DSQ-SO1R-S (1)	17.6	CMOS (% V_{CCI})	Split Output	SOP8	S5355D	Automotive
TPM5355DSQ-SOAR-S (1)	17.6	CMOS (% V_{CCI})	Split Output	WSOP8	S5355D	Automotive
TPM53551AM-SO1R (1)	6	TTL (Absolute V)	Miller Clamp	SOP8	M5351A	Industrial
TPM53551AM-SOAR (1)	6	TTL (Absolute V)	Miller Clamp	WSOP8	M5351A	Industrial
TPM53551AS-SO1R (1)	6	TTL (Absolute V)	Split Output	SOP8	S5351A	Industrial
TPM53551AS-SOAR (1)	6	TTL (Absolute V)	Split Output	WSOP8	S5351A	Industrial
TPM53551BM-SO1R (1)	8.5	TTL (Absolute V)	Miller Clamp	SOP8	M5351B	Industrial
TPM53551BM-SOAR (1)	8.5	TTL (Absolute V)	Miller Clamp	WSOP8	M5351B	Industrial
TPM53551BS-SO1R (1)	8.5	TTL (Absolute V)	Split Output	SOP8	S5351B	Industrial
TPM53551BS-SOAR	8.5	TTL (Absolute V)	Split Output	WSOP8	S5351B	Industrial
TPM53551CM-SO1R (1)	12.5	TTL (Absolute V)	Miller Clamp	SOP8	M5351C	Industrial
TPM53551CM-SOAR (1)	12.5	TTL (Absolute V)	Miller Clamp	WSOP8	M5351C	Industrial
TPM53551CS-SO1R (1)	12.5	TTL (Absolute V)	Split Output	SOP8	S5351C	Industrial

Order Number	UVLO Rising Threshold (V)	Input Threshold Type	Feature	Package	Marking	Quality Grade
TPM53551CS-SOAR (1)	12.5	TTL (Absolute V)	Split Output	WSOP8	S5351C	Industrial
TPM53551DM-SO1R (1)	17.6	TTL (Absolute V)	Miller Clamp	SOP8	M5351D	Industrial
TPM53551DM-SOAR (1)	17.6	TTL (Absolute V)	Miller Clamp	WSOP8	M5351D	Industrial
TPM53551DS-SO1R (1)	17.6	TTL (Absolute V)	Split Output	SOP8	S5351D	Industrial
TPM53551DS-SOAR (1)	17.6	TTL (Absolute V)	Split Output	WSOP8	S5351D	Industrial

(1) Contact 3PEAK sales representatives for more details.

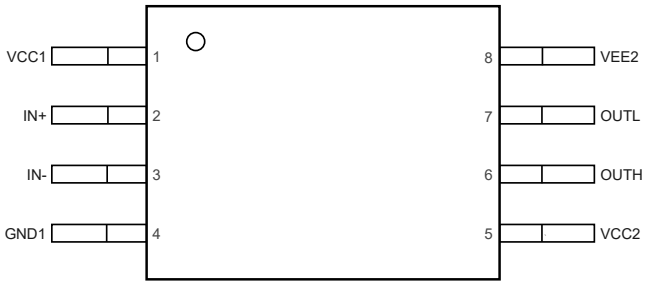
Revision History

Date	Revision	Notes
2026-07-25	Rev.A.0	Initial release

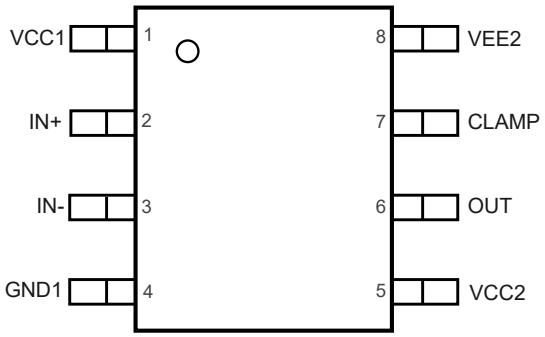
Pin Configuration and Functions

TPM5355M
WSOP8
Top View

TPM5355S
WSOP8
Top View



TPM5355M
SOP8
Top View



TPM5355S
SOP8
Top View

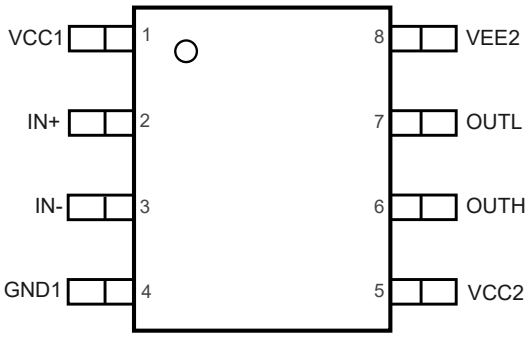


Table 1. Pin Functions: TPM5355M

Pin		I/O	Description
No.	Name		
1	VCC1	P	Input-side power supply. Connect a 0.1-μF capacitor to GND and place it close to the device.
2	IN+	I	Non-inverting input. Internally pulled low if left open.
3	IN–	I	Inverting input. Internally pulled high if left open.
4	GND1	G	Input side power ground
5	VCC2	P	Output side power rail. Connect a capacitor close to the device to support transient output current.
6	OUT	O	Gate driver output.
7	CLAMP	O	Gate driver Miller clamp output.
8	VEE2	G	Output side ground.

Table 2. Pin Functions: TPM5355S

Pin		I/O	Description
No.	Name		
1	VCC1	P	Input-side power supply. Connect a 0.1-μF capacitor to GND and place it close to the device.
2	IN+	I	Non-inverting input. Internally pulled low if left open.
3	IN–	I	Inverting input. Internally pulled high if left open.
4	GND1	G	Input side power ground
5	VCC2	P	Output side power rail. Connect a capacitor close to the device to support transient output current.
6	OUTH	O	Gate driver pull-up output.
7	OUTL	O	Gate driver pull-down output.
8	VEE2	G	Output side ground.

Specifications

Absolute Maximum Ratings (1)

Symbol	Parameter	Min	Max	Unit
VCC1 to GND1	Input Supply Voltage	–0.3	6	V
VCC2 to VEE2	Output Supply Voltage	–0.3	35	V
OUT to VEE2	Output Signal DC Voltage	–0.3	VCC2 + 0.3	V
IN+, IN- to GND	Input Signal DC Voltage	–0.3	VCC1 + 0.3	V
T_J	Junction Temperature	–40	150	℃
T_A	Operating Ambient Temperature Range	-40	125	℃
T_{STG}	Storage Temperature	–65	150	℃

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.
(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Table 3. TPM5355xQ

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	AEC Q100-002 (1)	±2	kV
CDM	Charged Device Model ESD	AEC Q100-011	±1.5	kV

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

Table 4. TPM5355x

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
VCC1	Input Supply Voltage, reference to GND1	3	5.5	V
VCC2	Output Supply Voltage, reference to VEE2, 18-V UVLO option TPM5355Dx	18.8	33	V
	Output Supply Voltage, reference to VEE2, 12-V UVLO option, TPM5355Cx	13.5	33	V
	Output Supply Voltage, reference to VEE2, 8-V UVLO option TPM5355Bx	9.2	33	V
	Output Supply Voltage, reference to VEE2, 6-V UVLO option TPM5355Ax	6.5	33	V

Parameter		Min	Max	Unit
T_J	Junction Temperature	−40	150	°C
T_A	Operating Ambient Temperature	−40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOP8	79.2	28.75	°C/W
WSOP8	117.78	49.88	°C/W

Safety Limiting Values

Parameter		Test Conditions	Min	Typ	Max	Unit
P_D	Maximum power dissipation on input and output	V_{CC1} = 5 V, V_{CC2} = 15 V, f = 2.1 MHz, 50% duty cycle, square wave, 2.2-nF load			1.2	W
P_{D1}	Maximum input power dissipation	V_{CC1} = 5 V, V_{CC2} = 15 V, f = 2.1 MHz, 50% duty cycle, square wave, 2.2-nF load			50	mW
P_{D2}	Maximum output power dissipation	V_{CC1} = 5 V, V_{CC2} = 15 V, f = 2.1 MHz, 50% duty cycle, square wave, 2.2-nF load			1.05	W

Insulation Specifications

WSOP8

Parameter		Conditions	Value	Unit
CLR	External Clearance	Shortest terminal-to-terminal distance through air	> 8.5	mm
CPG	External Creepage	Shortest terminal-to-terminal distance across the package surface	> 8.5	mm
DTI	Distance through the Insulation	Minimum internal gap (internal clearance)	> 22	μm
CTI	Comparative Tracking Index		> 600	V
	Material Group		I	
	Overvoltage Category per IEC 60664-1	For Rated Mains Voltage ≤ 600 V_{RMS}	I-III	
		For Rated Mains Voltage ≤ 1000 V_{RMS}	I-II	
	Pollution Degree		2	
	Climate Category		40/125/21	
C_{IO}	Isolation Capacitance	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	0.5	pF
R_{IO}	Isolation Resistance	V_{IO} = 500 V, T_A = 25 °C	> 10^{11}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125 °C	> 10^{10}	
		V_{IO} = 500 V, T_A = 150 °C	> 10^9	
V_{IORM}	Maximum Repetitive Isolation Voltage	AC voltage (bipolar)	1500	V_{PK}
V_{IOWM}	Maximum Working Isolation Voltage	AC voltage; TDDB Test	1060	V_{RMS}
		DC voltage	1500	V_{DC}
V_{IOTM}	Maximum Transient Isolation Voltage	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 × V_{IOTM}, t = 1 s (100% production)	8000	V_{PK}
V_{IOSM}	Maximum Surge Isolation Voltage	Test method per IEC 62368-1, 1.2/50 μs waveform, V_{TEST} = 1.3 × V_{IOSM}(qualification) = 11700	9000	V_{PK}
V_{ISO}	UL 1577 Withstand Isolation Voltage	V_{TEST} = V_{ISO} = 5700 V_{RMS}, t = 60 s (in qualification), V_{TEST} = 1.2 × V_{ISO} − 6840 V_{RMS}, t = 1 s (100% in production)	5700	V_{RMS}
q_{pd}	Apparent Charge	Method a, After Input/Output safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10 s	≤ 5	pC
		Method a, After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10 s	≤ 5	
		Method b1; At routine test (100% production) and preconditioning (type	≤ 5	

Parameter		Conditions	Value	Unit
		test), V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1 s		

SOP8

Parameter		Conditions	Value	Unit
CLR	External Clearance	Shortest terminal-to-terminal distance through air	> 4	mm
CPG	External Creepage	Shortest terminal-to-terminal distance across the package surface	> 4	mm
DTI	Distance through the Insulation	Minimum internal gap (internal clearance)	> 21	μm
CTI	Comparative Tracking Index		> 600	V
	Material Group		I	
	Overvoltage Category per IEC 60664-1	For Rated Mains Voltage ≤ 150 V_{RMS}	I-IV	
		For Rated Mains Voltage ≤ 300 V_{RMS}	I-III	
	Pollution Degree		2	
	Climate Category		40/125/21	
C_{IO}	Isolation Capacitance	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	1.2	pF
R_{IO}	Isolation Resistance	V_{IO} = 500 V, T_A = 25 °C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125 °C	> 10^{11}	
		V_{IO} = 500 V, T_A = 150 °C	> 10^9	
V_{IORM}	Maximum Repetitive Isolation Voltage	AC voltage (bipolar)	990	V_{PK}
V_{IOWM}	Maximum Working Isolation Voltage	AC voltage;	700	V_{RMS}
		DC voltage	990	V_{DC}
V_{IOTM}	Maximum Transient Isolation Voltage	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 × V_{IOTM}, t = 1 s (100% production)	4242	V_{PK}
V_{IOSM}	Maximum Surge Isolation Voltage	Test method per IEC 62368-1, 1.2/50 μs waveform, V_{TEST} = 1.3 × V_{IOSM} (qualification) = 5515V	4242	V_{PK}
V_{ISO}	UL 1577 Withstand Isolation Voltage	V_{TEST} = V_{ISO} = 3000 V_{RMS}, t = 60 s (in qualification), V_{TEST} = 1.2 × V_{ISO} − 3600 V_{RMS}, t = 1 s (100% in production)	3000	V_{RMS}
q_{pd}	Apparent Charge	Method a, After Input/Output safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10 s	≤ 5	pC
		Method a, After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10 s	≤ 5	
		Method b1; At routine test (100% production) and preconditioning (type	≤ 5	

Parameter		Conditions	Value	Unit
		test), V_{ini} = 1.2 × V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1 s		

Electrical Characteristics

All test conditions: VCC1 − GND1 = 3.3 V or 5 V, VCC2 − VEE2 = 15 V, V_{EE2} referred as GND, T_A = −40°C to 125°C, Output capacitance C_L = 100 pF, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Supply						
I_{VCC1}	Input Supply Quiescent Current			1.67	2.4	mA
I_{VCC2}	Output Supply Quiescent Current	VCC2 − VEE2 = 15 V		1.1	1.8	mA
V_{UVLOR1}	Undervoltage Lock out, VCC1, Rising edge			2.6	2.8	V
V_{UVLOF1}	Undervoltage Lock out, VCC1, Falling edge		2.4	2.5		V
$V_{UVLOHYS1}$	Undervoltage Lock out, VCC1, Hysteresis			0.1		V
C_{IN}	Input Parasitic Capacitance	*f* = 0.5 MHz		15		pF
Under Voltage Lockout, TPM5355A (6-V UVLO Version)						
V_{UVLO_R}	Under Voltage Lock-out Threshold, Rising Edge		5.7	6	6.3	V
V_{UVLO_F}	Under Voltage Lock-out Threshold, Falling Edge		5.4	5.7	6	V
V_{UVLO_HYS}	UVLO Hysteresis			0.3		V
Under Voltage Lockout, TPM5355B (8-V UVLO Version)						
V_{UVLO_R}	Under Voltage Lock-out Threshold, Rising Edge		7.7	8.5	8.9	V
V_{UVLO_F}	Under Voltage Lock-out Threshold, Falling Edge		7.2	7.9	8.4	V
V_{UVLO_HYS}	UVLO Hysteresis			0.6		V
Under Voltage Lockout, TPM5355C (12-V UVLO Version)						
V_{UVLO_R}	Under Voltage Lock-out Threshold, Rising Edge		11.7	12.5	13.3	V
V_{UVLO_F}	Under Voltage Lock-out Threshold, Falling Edge		10.7	11.5	12.3	V
V_{UVLO_HYS}	UVLO Hysteresis			1		V
Under Voltage Lockout, TPM5355D (18-V UVLO Version)						

Parameter		Conditions	Min	Typ	Max	Unit
V_{UVLO_R}	Under Voltage Lock-out Threshold, Rising Edge		16.4	17.6	18.8	V
V_{UVLO_F}	Under Voltage Lock-out Threshold, Falling Edge		15.4	16.6	17.8	V
V_{UVLO_HYS}	UVLO Hysteresis			1		V
LOGIC I/O						
$V_{IT+(IN)}$	Input Threshold, rising edge, IN+, IN−, TPM5355x (CMOS)		0.4 × VCC1	0.55 × VCC1	0.7 × VCC1	V
$V_{IT-(IN)}$	Input Threshold, falling edge, IN+, IN−, TPM5355x (CMOS)		0.3 × VCC1	0.45 × VCC1	0.6 × VCC1	V
$V_{HYS(IN)}$	Input Threshold Hysteresis, IN+, IN−, TPM5355x (CMOS)			0.1*VCC1		V
$V_{IT+(IN)}$	Input Threshold, rising edge, IN+, IN−, TPM53551 (TTL)		1.5	1.7	1.9	V
$V_{IT-(IN)}$	Input Threshold, falling edge, IN+, IN−, TPM53551 (TTL)		1.1	1.3	1.5	V
$V_{HYS(IN)}$	Input Threshold Hysteresis, IN+, IN−, TPM53551 (TTL)			0.4		V
I_{IH}	Input Leakage Current	IN+ = VCC1		40	240	μA
I_{IL}	Input Leakage Current	IN− = GND1	−240	−40		μA
Gate Driver Stage						
V_{OH}	High-Level Output Voltage (VCC2 − OUT) and (VCC2 − OUTH)	I_{OUT} = –20 mA	40	80	150	mV
V_{OL}	Low-Level Output Voltage (OUT and OUTL)	IN+ = low, IN– = high; I_O= 20 mA		10	20	mV
I_{OH}	Peak Source Current	IN+ = high, IN– = low, C_{LOAD} = 220 nF, VCC2 = 12 V		4		A
I_{OL}	Peak Sink Current	IN+ = low, IN– = high		7		A
I_{CLAMP}	Clamp Low-level Current	V_{CLAMP}= V_{EE2} + 15 V		6		A
I_{CLAMP}	Clamp Low-level Current for Low-output Voltage	V_{CLAMP}= V_{EE2} + 2 V		2.5		A
$V_{CLAMPTH}$	Clamp Threshold Voltage			2.1	2.3	V
V_{CLP_OUT}	Clamping Voltage VOUTH − VCC2 to VOUT − VCC2	IN+ = HIGH, IN− = LOW, t_{CLAMP} = 10 μs, I_{OUTH}/I_{OUT} = 500 mA		80		mV
V_{CLP_OUT}	Clamping Voltage VEE2 − VOUTL or VEE2 − VCLAMP or VEE2 − VOUT	IN+ = LOW, IN− = HIGH, t_{CLAMP} = 10 μs, I_{OUTH}/I_{OUT} = −500 mA		30		mV
		IN+ = LOW, IN– = HIGH, I_{CLAMP} or I_{OUTL} = −20 mA		12		mV
Active Pulldown						

Parameter		Conditions	Min	Typ	Max	Unit
V_{OUTSD}	Active Pulldown Voltage on OUTL, CLAMP, and OUT	I_{OUT} = 200 mA, VCCx floating and unpowered.		1.85	2.2	V
		I_{OUT} = 200 mA, C_{Vcc}= 100 nF and unpowered.		1.85	2.2	V

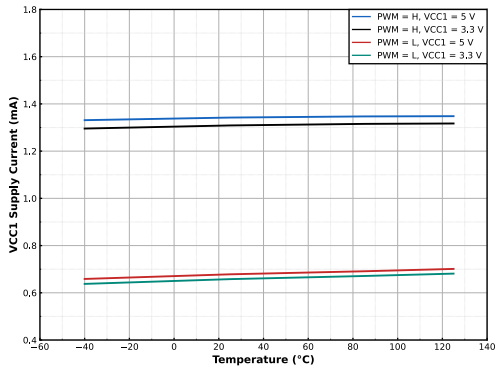
(1) Guaranteed by design

Timing Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
t_r	Output Rise Time (1)	F_{SW} = 20 kHz, (50% Duty Cycle) V_{CC} = 12 V, C_{LOAD} = 1.8 nF. Measured from 10% VCC2 to 90% VCC2 or 90% VCC2 to 10% VCC2		12		ns
t_f	Output Fall Time (1)			12		ns
t_{PLH}	Propagation Delay, Low to High, VIH to 10% of VCC2	F_{SW} = 20 kHz, (50% Duty Cycle) V_{CC} = 15 V, C_{LOAD} = 1.8 nF		58	90	ns
t_{PHL}	Propagation Delay, High to Low, VIL to 90% of VCC2			58	90	ns
t_{PWD}	Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$			2	5	ns
t_{sk_pp}	Part-to-Part Skew in Propagation Delay between any Two Parts (2)	F_{SW} = 20 kHz, (50% Duty Cycle) V_{CC} = 15 V			25	ns
$V_{CC1UVLO\_rec}$	UVLO Recovery Delay, VCC1		15	24.5	40	μs
$t_{VCC2UVLO\_rec}$	UVLO Recovery Delay, VCC2		6.5	9.2	15	μs
CMTI	Common-Mode Transient Immunity (1)	IN+ and IN- are tied to GND or V_{CC1}, V_{CM} = 1200 V	150			kV/μs

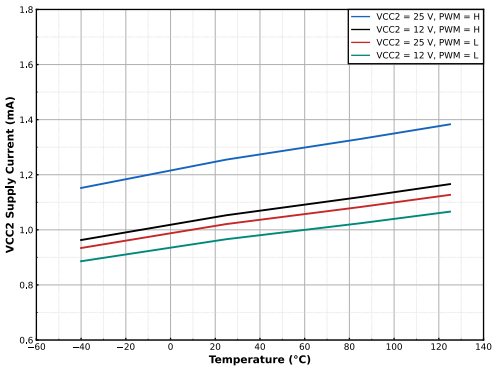
(1) Guaranteed by design.
(2) $t_{sk(pp)}$is the magnitude of the difference in propagation delay times between the output of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals, and loads guaranteed by characterization.

Typical Performance Characteristics



No load

Figure 1. VCC1 Supply Current vs. Temperature



No load, V_{CC1} = 3.3 V

Figure 2. VCC2 Supply Current vs. Temperature

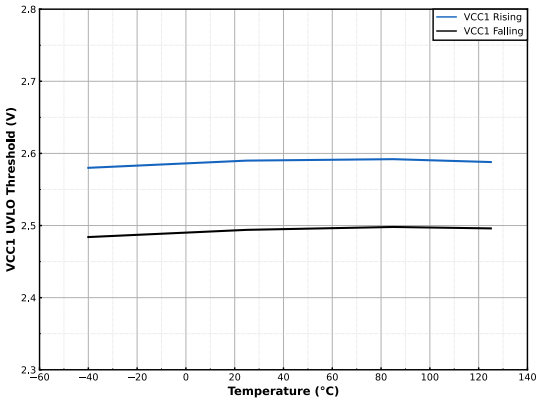
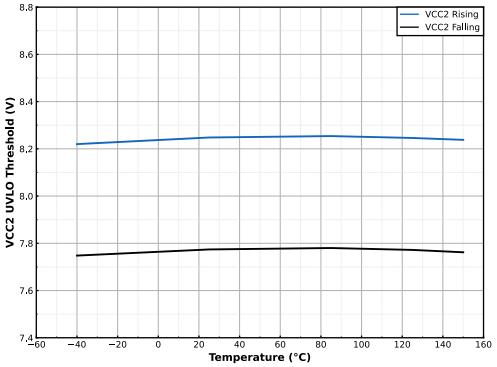
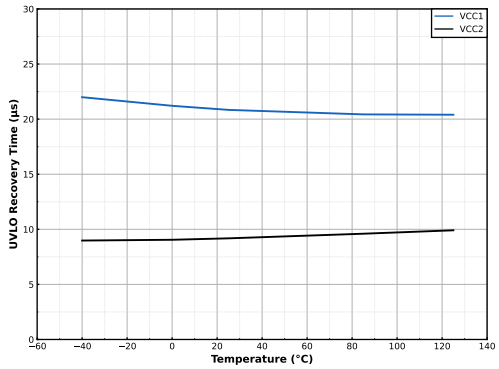


Figure 3. VCC1 UVLO Threshold vs. Temperature



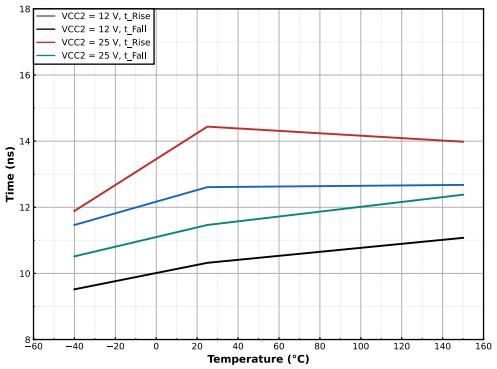
8-V UVLO (TPM5355xB)

Figure 4. VCC2 UVLO Threshold vs. Temperature



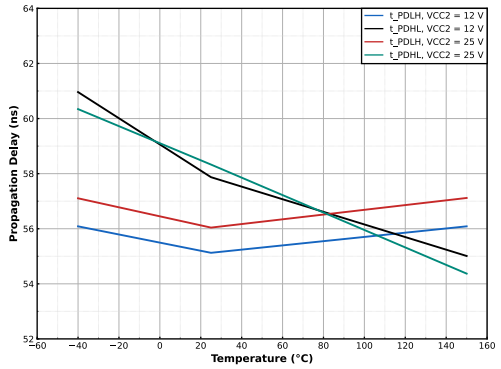
V_{CC2} = 12 V

Figure 5. UVLO Recovery Time vs. Temperature



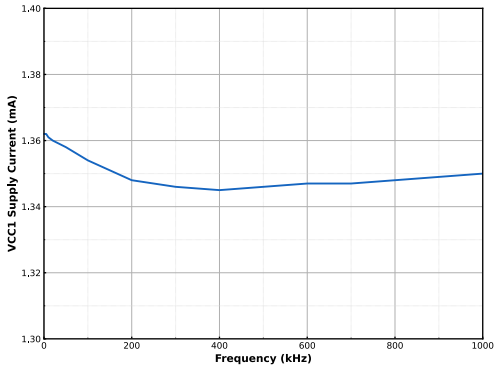
C_{LOAD} = 1.8 nF

Figure 6. Output Rise and Fall Time vs. Temperature



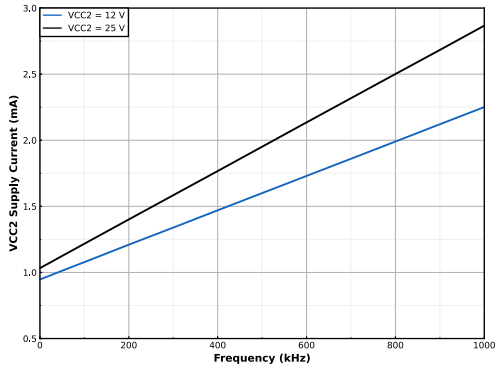
C_{LOAD} = 1.8 nF

Figure 7. Output Propagation Delay vs. Temperature



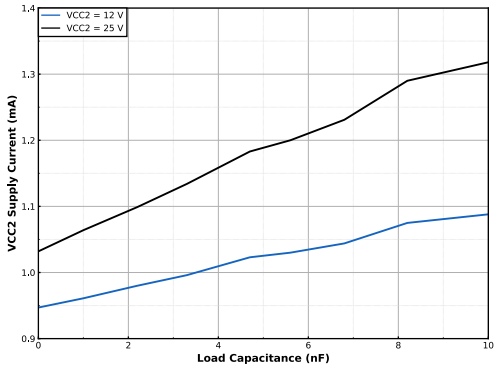
No switching load, V_{CC1} = 5 V, T_A = 25 °C

Figure 8. VCC1 Supply Current vs. Frequency



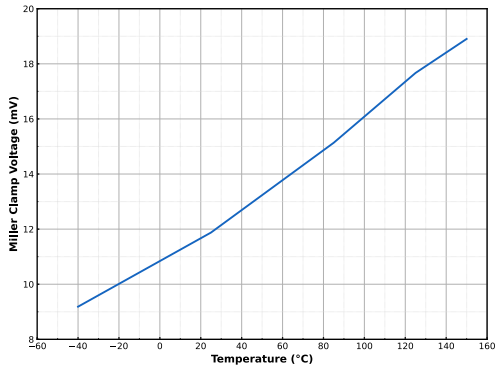
No load, T_A = 25 °C

Figure 9. VCC2 Supply Current vs. Frequency



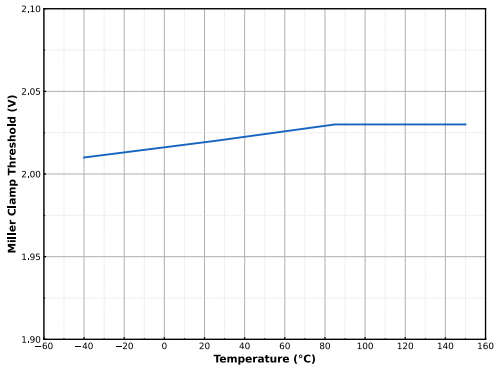
f = 1 kHz, T_A = 25 °C

Figure 10. VCC2 Supply Current vs. Load Capacitance



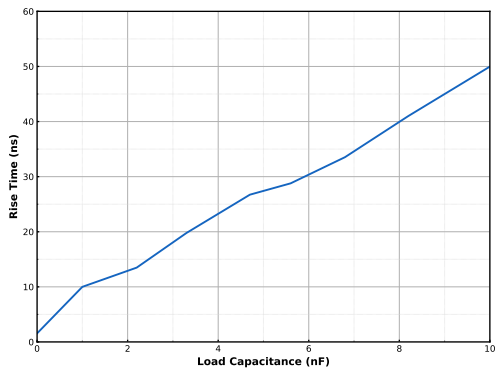
M variants, I_O = 20 mA

Figure 11. Miller Clamp Voltage vs. Temperature



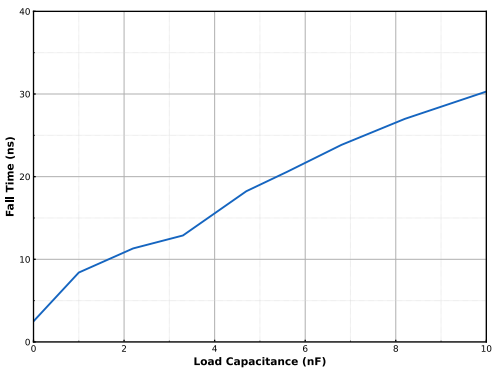
M variants

Figure 12. Miller Clamp Threshold Voltage vs. Temperature



V_{CC2} = 15 V, T_A = 25 °C

Figure 13. Rise Time vs. Load Capacitance



V_{CC2} = 15 V, T_A = 25 °C

Figure 14. Fall Time vs. Load Capacitance

Detailed Description

Overview

The TPM5355x family is a single-channel isolated gate driver for MOSFETs, IGBTs, and SiC FETs with TTL/CMOS input stage. It has a 35-V maximum operating driver voltage, which is especially suitable for high-power fast-transient IGBT / SiC applications.

The TPM5355x family is designed to replace the optocoupler gate driver with an industry-standard wide-body 8-pin package of WSOP8, with more than 8.5-mm creepage and clearance to withstand over 1060-V_{RMS} working voltage, reinforced isolation, and 5.7 kV_{RMS} for 60 s, and a surge rating of 9-kV_{PK}. 3PEAK proprietary isolation technology supports common-mode transient immunity of greater than 150 kV/μs.

The TPM5355x offers two variations: split output and Miller clamp (refer to the Device Comparison Table). Isolation in the TPM5355 is achieved using high-voltage SiO_2-based capacitors with 3PEAK proprietary On-Off keying (OOK) modulation scheme. The TPM5355 incorporates advanced circuit techniques to optimize CMTI performance and minimize radiated emissions resulting from high-frequency carrier and IO buffer switching.

Functional Block Diagram

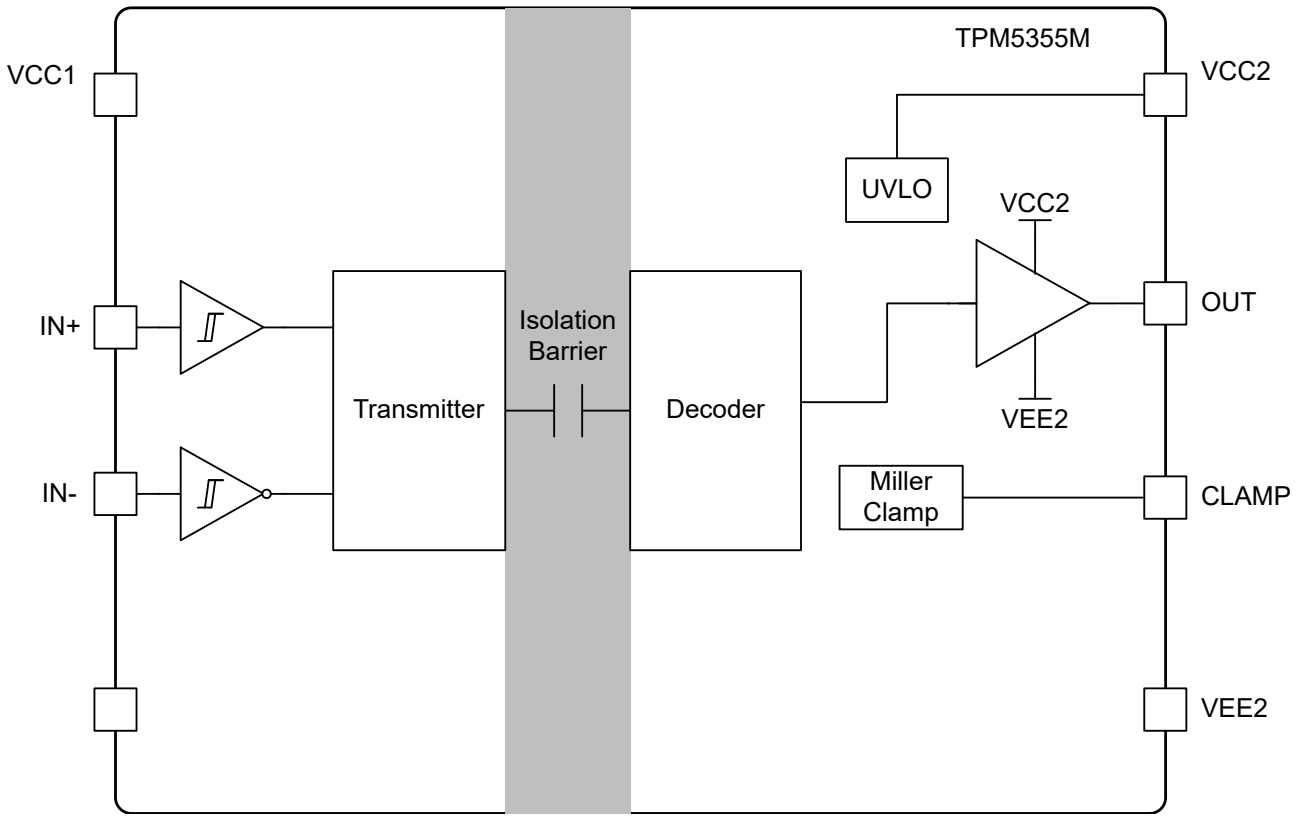


Figure 15. TPM5355M Functional Block Diagram

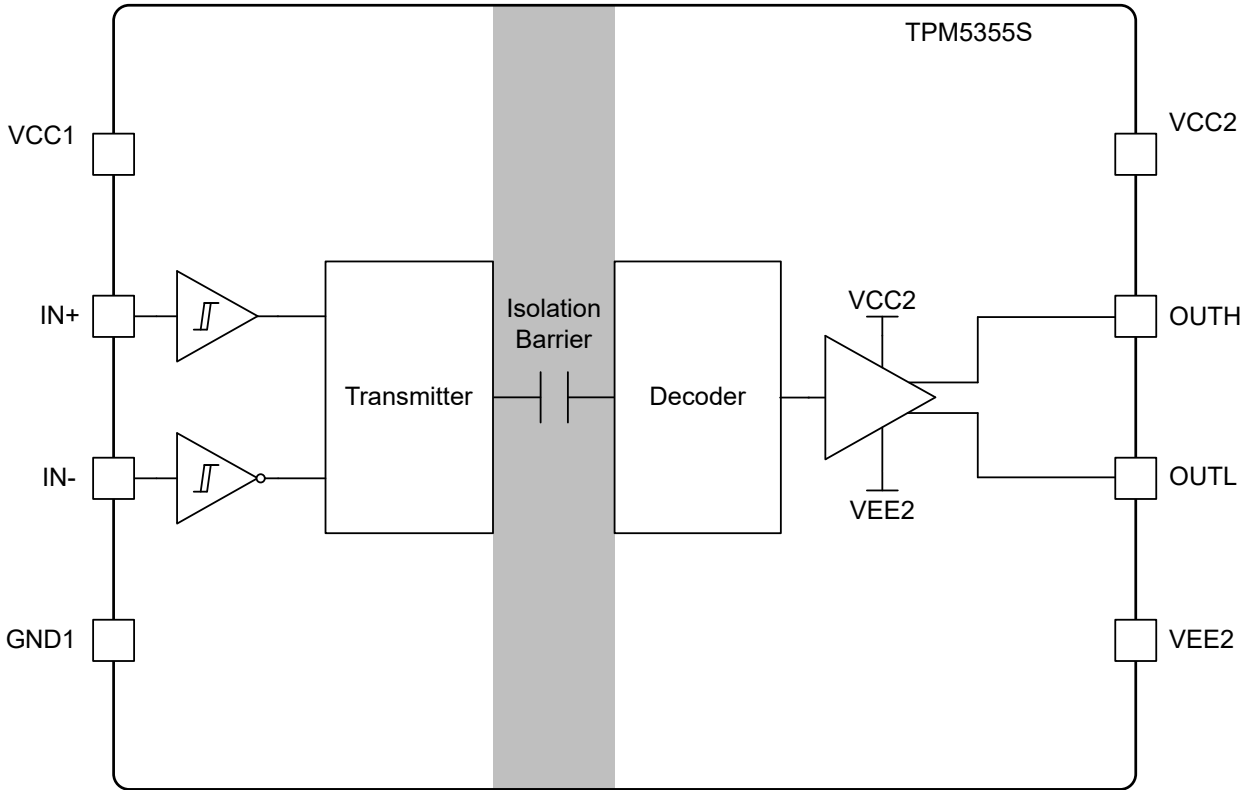


Figure 16. TPM5355S Functional Block Diagram

Feature Description

Power Supply

The VCC1 input power supply of the TPM5355 supports a wide voltage range from 3 V to 5.5 V, while the VCC2 output supply accommodates a voltage range up to 33 V.

When operating with bipolar supplies, the power device is turned off by applying a negative voltage to the gate relative to the emitter or source. This configuration prevents unintentional activation of the power device due to current induced by the Miller effect. In the case of modern SiC MOSFETs, the typical values are 15 V and −3 V. When operating with a unipolar supply, the VCC2 supply is connected to 15 V for SiC MOSFETs. The VEE2 supply is connected to 0 V.

In both scenarios, the TPM5355M device with Miller clamping function can be utilized. The Miller clamping function is implemented by establishing a low-impedance path between the gate of the power device and the VEE2 supply. This allows the Miller current to sink through the clamp pin, thereby ensuring that the gate voltage remains below the turn-on threshold value.

Input Stage

TPM5355 and TPM5355Q use CMOS-compatible input thresholds on IN+ and IN−. The high threshold ($V_{IT+(IN)}$) sits at 0.55 × VCC1 and the low threshold at 0.45 × VCC1, with a wide hysteresis ($V_{hys(IN)}$) of 0.1 × VCC1 — scaling automatically with the logic-side supply for consistent noise margin across the 3 V to 5.5 V VCC1 range.

TPM53551 uses TTL-compatible input thresholds on IN+ and IN−. $V_{IT+(IN)}$ sits at 1.6 V typical and the low threshold at 1.2 V typical — both fixed, independent of VCC1 — with a typical hysteresis of 0.4 V, giving direct compatibility with legacy 5-V TTL / 3.3-V logic signal levels regardless of the logic-side supply rail.

In the event that any of the inputs are left unconnected, an internal pulldown resistance of 128 kΩ ensures that the IN+ pin is pulled low, while an internal resistance of 128 kΩ pulls the IN− pin high. 3PEAK recommends, for enhanced noise immunity, to ground any unused input or connect it to the VCC1 voltage.

A notable advantage of the TPM5355 family is the isolation between the input and output drivers. As a result, the input signal amplitude can be either larger or smaller than VCC2, as long as it remains within the recommended limits. This feature provides flexibility when integrating the gate driver with various control signal sources and allows the user to choose the most suitable VCC2 voltage for a specific gate. However, it is crucial to ensure that the amplitude of any signal applied to IN+ or IN− never exceeds the voltage of VCC1.

Decoder & Output Stage

The high-frequency signal is converted by the decoder via a double-capacitive insulation barrier as the output stage's input. The rail-to-rail output stage provides a high-peak current during the output slewing. The output V_{CC2} supports a maximum of 35-V input.

The output stages of the TPM5355 family are designed with a pull-up structure that optimizes the delivery of peak-source current when it is most needed, specifically during the Miller plateau region of the power-switch turn-on transition. This occurs when the power-switch drain or collector voltage experiences a dV/dt change. The pull-up structure consists of a P-channel MOSFET and an additional N-channel MOSFET connected in parallel.

The N-channel MOSFET plays a crucial role in enhancing the peak-sourcing current for fast turn-on. During the narrow instant when the output is transitioning from a low to a high state, the N-channel MOSFET is briefly turned on, providing a boost to the current. This enables a faster turn-on operation. To provide further insight, the table below provides typical internal resistance values for both the pullup and pulldown structures of the TPM5355, illustrating their characteristics and performance.

Device	Grade	R_{NMOS}	R_{OH}	R_{OL}	R_{CLAMP}	Unit
TPM5355xM	Industrial	1.54	12	0.35	1	Ω
TPM5355xS	Industrial	1.54	12	0.35	n/a	Ω

In the TPM5355S version, the pulldown structure consists solely of an N-channel MOSFET. However, in the M version, an additional FET is connected in parallel with the pulldown structure when the CLAMP and OUT pins are linked to the gate of the IGBT or MOSFET. This configuration allows for rail-to-rail operation, providing an output voltage swing between VCC2 and VEE2.

Protection

Under-Voltage Lock Out (UVLO)

The TPM5355 family incorporates UVLO (Undervoltage Lockout) functions for both the VCC1 and VCC2 supplies to safeguard IGBTs and MOSFETs from underdriven conditions. These functions monitor the voltages between the VCC1 and GND1, as well as VCC2 and VEE2 pins.

During device start-up or if the VCC voltage falls below the $V_{IT+\ (UVLO)}$ threshold or drops below the $V_{IT-\ (UVLO)}$ threshold after start-up, the UVLO feature activates, holding the affected output low, regardless of the input pins (IN+ and IN−). This ensures that the power devices are not operated under insufficient voltage conditions.

The VCC UVLO protection incorporates a hysteresis feature ($V_{hys(UVLO)}$). This hysteresis prevents rapid toggling or instability caused by ground noise in the power supply. It allows the device to tolerate small drops in bias voltage that may occur when the device starts switching and experiences a sudden increase in operating current consumption.

By implementing UVLO functions with hysteresis, the TPM5355 family ensures reliable operation and effectively safeguards IGBTs and MOSFETs against underdriven conditions, thereby enhancing the overall performance and protection of the system.

VCC1 UVLO Logic

Conditions	Inputs		Outputs	
	IN+	IN−	OUTH	OUT, OUTL
VCC1 UVLO	H	L	HiZ	L
	L	H	HiZ	L
	H	H	HiZ	L
	L	L	HiZ	L

VCC2 UVLO Logic

Conditions	Inputs		Outputs	
	IN+	IN−	OUTH	OUT, OUTL
VCC2 UVLO	H	L	HiZ	L
	L	H	HiZ	L
	H	H	HiZ	L
	L	L	HiZ	L

Active Pulldown

The TPM5355 family incorporates an active pulldown function to ensure that the IGBT or MOSFET gate remains in a low state when no power is connected to the VCC2 supply. This feature is designed to prevent false turn-on of the IGBT or MOSFET on the OUT, OUTL, and CLAMP pins by clamping the output voltage to 1.85V.

By utilizing the active pulldown and clamp circuitry, the TPM5355 ensures that the driver outputs are held low and prevents unintended turn-on of the IGBT or MOSFET under unbiased or UVLO conditions. This feature adds an extra layer of protection and ensures the reliable operation of the overall system.

Short Circuit Clamping

The TPM5355 family incorporates a short-circuit clamping function to protect the IGBT or MOSFET gate from overvoltage breakdown or degradation during short-circuit conditions. This function works by clamping the voltages at the driver output and slightly raising the voltage of the active Miller clamp pins above the VCC2 voltage.

To implement the short-circuit clamping function, a diode connection is added between the dedicated pins and the VCC2 pin within the driver. These internal diodes are capable of conducting up to 500 mA of current for a duration of 10 μs, and they can handle a continuous current of 20 mA. If higher current conduction capability is required, external Schottky diodes can be used to enhance the performance.

By employing the short-circuit clamping function, the TPM5355 provides an additional layer of protection by limiting voltage spikes and current surges during short-circuit events. This helps safeguard the IGBT or MOSFET gate, ensuring its long-term reliability and preventing potential damage from overvoltage conditions.

Active Miller Clamp

The TPM5355M family incorporates an active Miller-clamp function to mitigate false turn-on of the power switches that may be caused by Miller current in applications utilizing a unipolar power supply. This function is designed to address the specific challenges associated with the use of a unipolar power supply.

The active Miller-clamp function is achieved by introducing a low-impedance path between the gate terminal of the power switch and ground (VEE2) to effectively sink the Miller current. By providing this clamp, the gate voltage of the power switch is limited to less than 2 V during the off state, preventing unintended turn-on.

By implementing the active Miller-clamp function, the TPM5355M family ensures reliable operation by suppressing the effects of Miller current and preventing false turn-on of the power switches. This feature is particularly beneficial in applications utilizing a unipolar power supply, enhancing the overall performance and robustness of the system.

Function Table

Function Tables for TPM5355S

Inputs		Outputs	
IN+	**IN−**	**OUTH**	**OUT, OUTL**
H	L	H	HiZ
L	H	HiZ	L
H	H	HiZ	L
L	L	HiZ	L

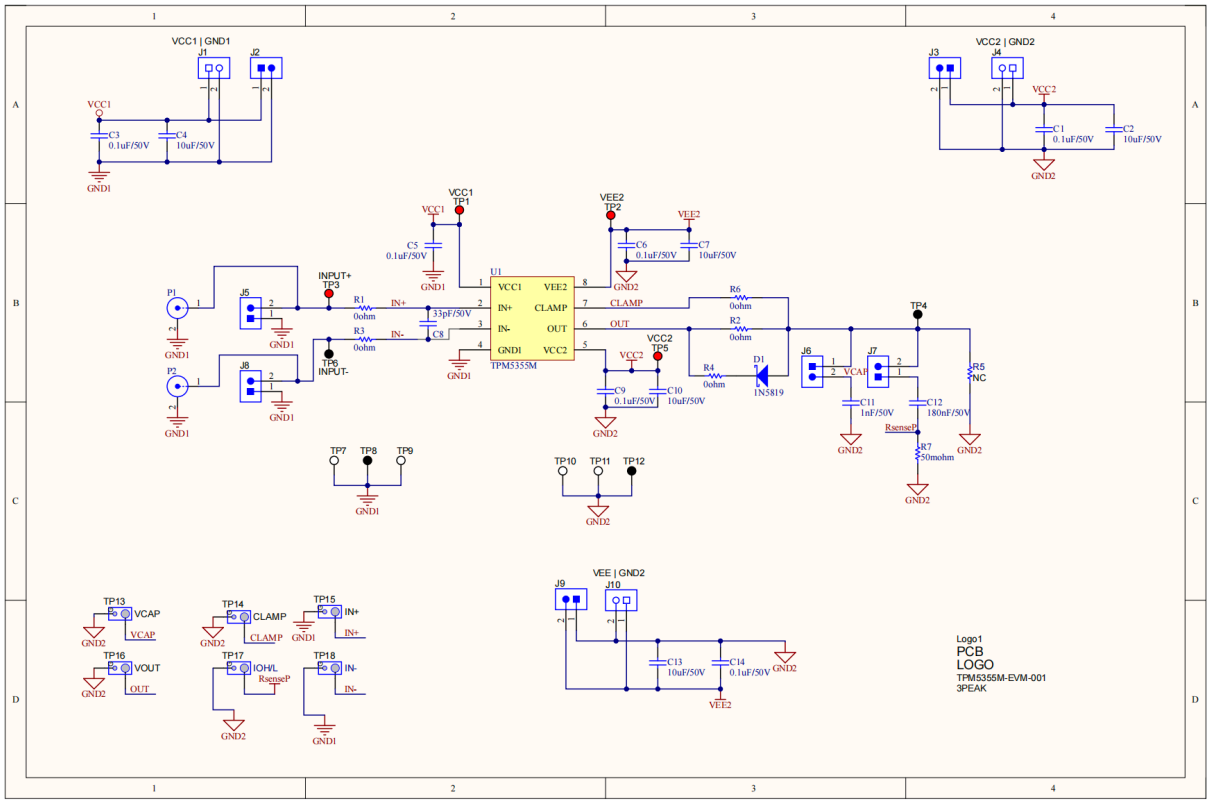
Function Tables for TPM5355M

Inputs		Outputs	
IN+	**IN−**	**OUT**	**CLAMP**
H	L	H	Inactive
L	H	Low	Active
H	H	Low	Active
L	L	Low	Active

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Typical Application

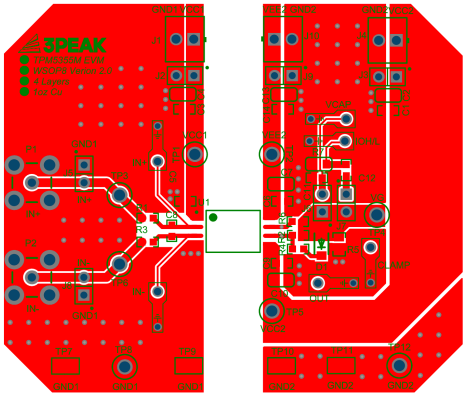


Layout

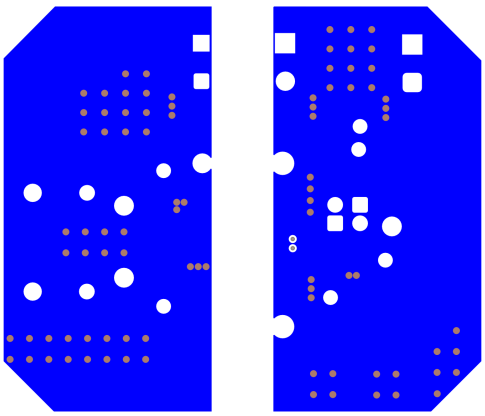
Layout Guideline

- For voltage mode input drivers, a low ESR and ESL capacitor should be placed close to the VCC and VEE pins, and the loop from VCC to VEE should be made small.
- To minimize the inductance of the drive circuit loop, the driver should be placed close to the transistor.
- The Miller clamp trace should be directly connected to the transistor's gate, and the trace should be kept short.
- To ensure isolation between the primary and secondary sides, avoid placing any PCB traces or copper directly below the driver device. A PCB cutout or groove is recommended to increase the creepage distance.
- To enhance thermal performance, it is recommended to enlarge the PCB copper connected to VCC and VEE.

Layout Recommendations

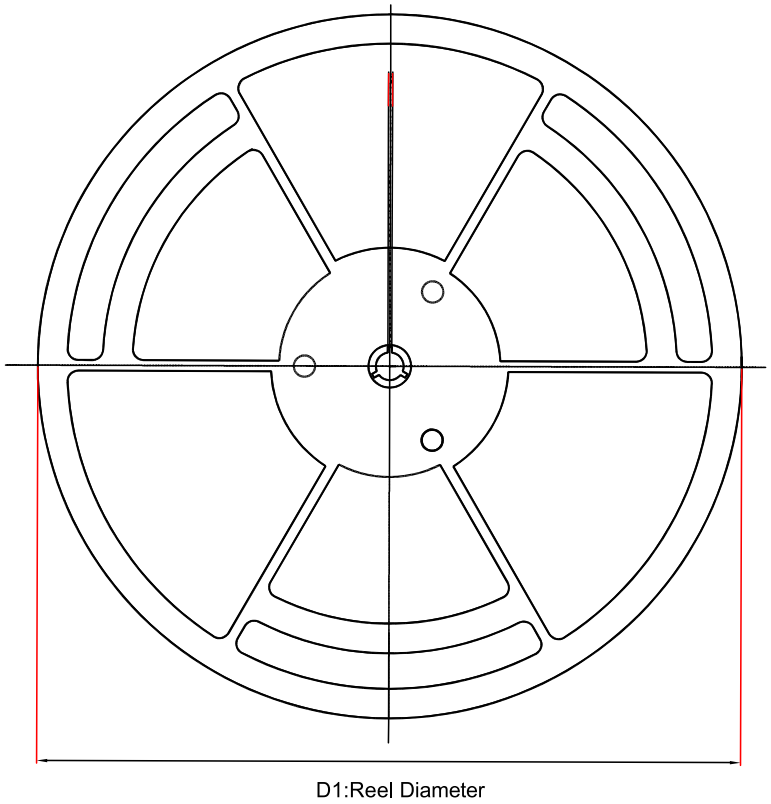


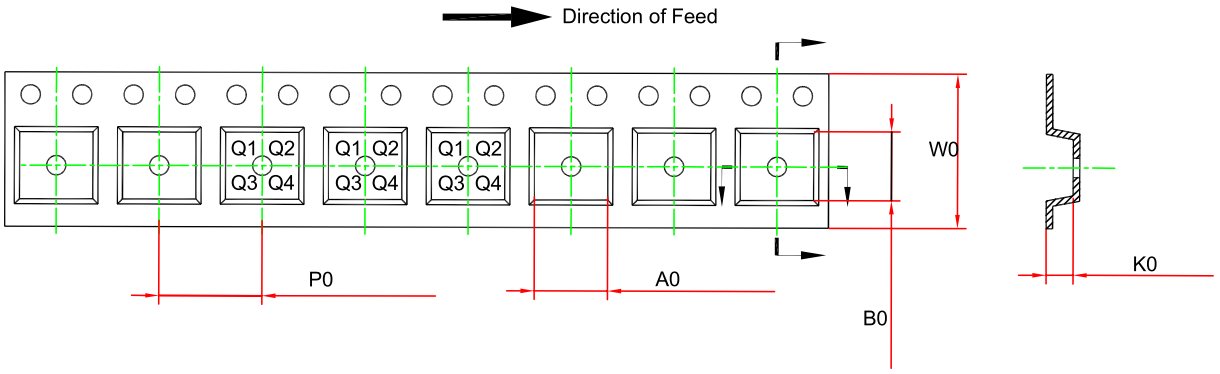
Top Layer



Bottom Layer

Tape and Reel Information





Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM5355AM-SO1R	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TPM5355AM-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM5355AS-SO1R	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TPM5355AS-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM5355BM-SO1R	SOP8	330	17.6	6.5	5.4	2	8	12	Q1

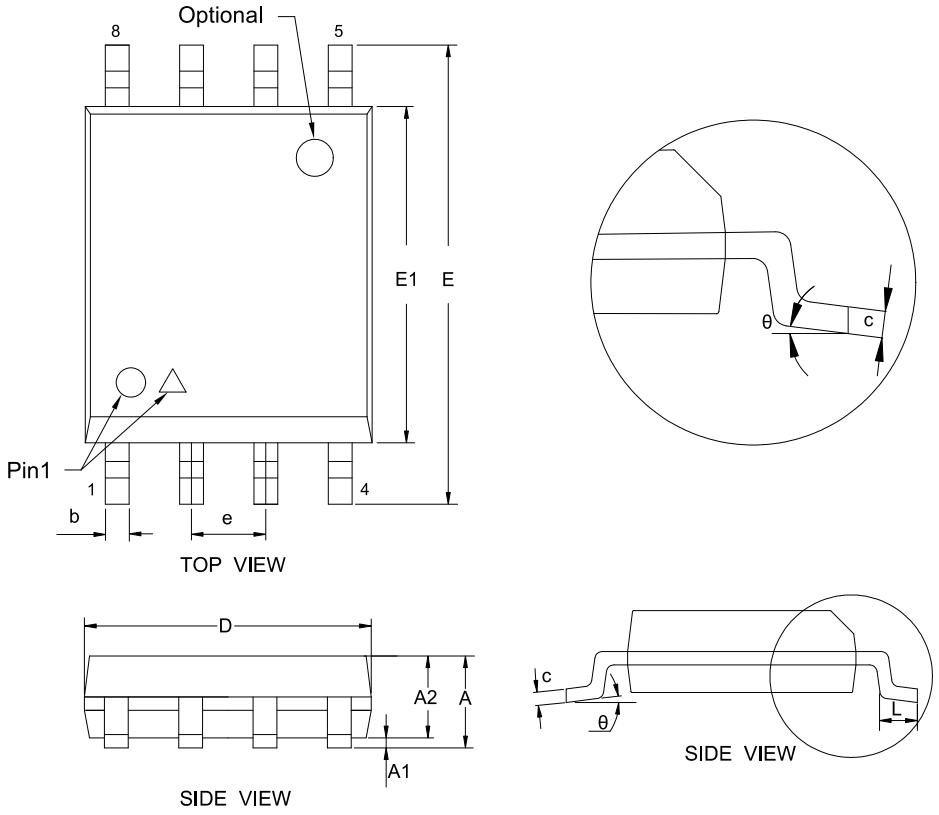
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM5355BM-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM5355BS-SO1R	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TPM5355BS-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM5355CM-SO1R	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TPM5355CM-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM5355CS-SO1R	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TPM5355CS-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM5355DM-SO1R	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TPM5355DM-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM5355DS-SO1R	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TPM5355DS-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM5355AMQ-SO1R-S	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TPM5355AMQ-SOAR-S	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM5355ASQ-SO1R-S	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TPM5355ASQ-SOAR-S	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM5355BMQ-SO1R-S	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TPM5355BMQ-SOAR-S	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM5355BSQ-SO1R-S	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TPM5355BSQ-SOAR-S	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM5355CMQ-SO1R-S	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TPM5355CMQ-SOAR-S	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM5355CSQ-SO1R-S	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TPM5355CSQ-SOAR-S	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM5355DMQ-SO1R-S	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TPM5355DMQ-SOAR-S	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM5355DSQ-SO1R-S	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TPM5355DSQ-SOAR-S	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM53551AM-SO1R	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TPM53551AM-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM53551AS-SO1R	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TPM53551AS-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM53551BM-SO1R	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TPM53551BM-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM53551BS-SO1R	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TPM53551BS-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM53551CM-SO1R	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TPM53551CM-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1

Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM53551CS-SO1R	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TPM53551CS-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM53551DM-SO1R	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TPM53551DM-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM53551DS-SO1R	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TPM53551DS-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1

Package Outline Dimensions

WSOP8

Package Outline Dimensions SOA(WSOP-8-C)

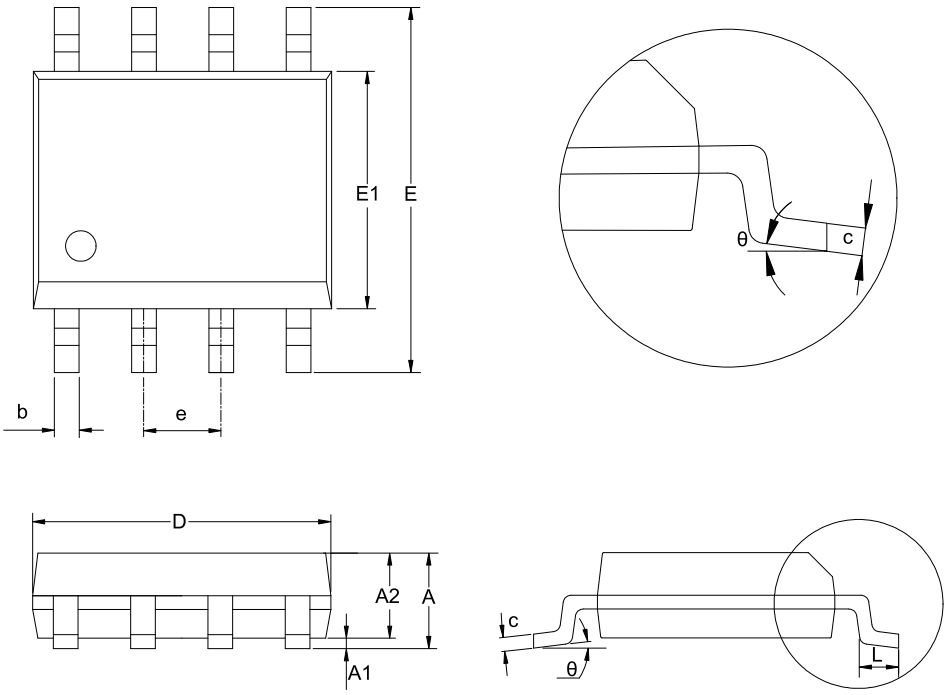


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	2.350	2.750	0.093	0.108
A1	0.130	0.450	0.005	0.018
A2	2.190	2.390	0.086	0.094
b	0.310	0.510	0.012	0.020
c	0.150	0.300	0.006	0.012
D	5.750	5.950	0.226	0.234
E	11.250	11.750	0.443	0.463
E1	7.400	7.600	0.291	0.299
e	1.270BSC		0.050BSC	
L	0.500	1.000	0.020	0.039
θ	0°	8°	0°	8°

NOTES:
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

SOP8

Package Outline Dimensions SO1(SOP-8-B)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	1.550	0.049	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.000	0.016	0.039
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Ambient Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPM5355AM-SO1R (1)	−40 to 125°C	SOP8	M5355A	3	4000	Green
TPM5355AM-SOAR (1)	−40 to 125°C	WSOP8	M5355A	3	1000	Green
TPM5355AS-SO1R (1)	−40 to 125°C	SOP8	S5355A	3	4000	Green
TPM5355AS-SOAR (1)	−40 to 125°C	WSOP8	S5355A	3	1000	Green
TPM5355BM-SO1R	−40 to 125°C	SOP8	M5355B	3	4000	Green
TPM5355BM-SOAR	−40 to 125°C	WSOP8	M5355B	3	1000	Green
TPM5355BS-SO1R	−40 to 125°C	SOP8	S5355B	3	4000	Green
TPM5355BS-SOAR	−40 to 125°C	WSOP8	S5355B	3	1000	Green
TPM5355CM-SO1R	−40 to 125°C	SOP8	M5355C	3	4000	Green
TPM5355CM-SOAR	−40 to 125°C	WSOP8	M5355C	3	1000	Green
TPM5355CS-SO1R	−40 to 125°C	SOP8	S5355C	3	4000	Green
TPM5355CS-SOAR	−40 to 125°C	WSOP8	S5355C	3	1000	Green
TPM5355DM-SO1R (1)	−40 to 125°C	SOP8	M5355D	3	4000	Green
TPM5355DM-SOAR (1)	−40 to 125°C	WSOP8	M5355D	3	1000	Green
TPM5355DS-SO1R (1)	−40 to 125°C	SOP8	S5355D	3	4000	Green
TPM5355DS-SOAR (1)	−40 to 125°C	WSOP8	S5355D	3	1000	Green
TPM5355AMQ-SO1R-S (1)	−40 to 125°C	SOP8	M5355A	3	4000	Green
TPM5355AMQ-SOAR-S (1)	−40 to 125°C	WSOP8	M5355A	3	1000	Green
TPM5355ASQ-SO1R-S (1)	−40 to 125°C	SOP8	S5355A	3	4000	Green
TPM5355ASQ-SOAR-S (1)	−40 to 125°C	WSOP8	S5355A	3	1000	Green

Order Number	Operating Ambient Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPM5355BMQ-SO1R-S (1)	−40 to 125°C	SOP8	M5355B	3	4000	Green
TPM5355BMQ-SOAR-S	−40 to 125°C	WSOP8	M5355B	3	1000	Green
TPM5355BSQ-SO1R-S	−40 to 125°C	SOP8	S5355B	3	4000	Green
TPM5355BSQ-SOAR-S (1)	−40 to 125°C	WSOP8	S5355B	3	1000	Green
TPM5355CMQ-SO1R-S (1)	−40 to 125°C	SOP8	M5355C	3	4000	Green
TPM5355CMQ-SOAR-S (1)	−40 to 125°C	WSOP8	M5355C	3	1000	Green
TPM5355CSQ-SO1R-S (1)	−40 to 125°C	SOP8	S5355C	3	4000	Green
TPM5355CSQ-SOAR-S (1)	−40 to 125°C	WSOP8	S5355C	3	1000	Green
TPM5355DMQ-SO1R-S (1)	−40 to 125°C	SOP8	M5355D	3	4000	Green
TPM5355DMQ-SOAR-S (1)	−40 to 125°C	WSOP8	M5355D	3	1000	Green
TPM5355DSQ-SO1R-S (1)	−40 to 125°C	SOP8	S5355D	3	4000	Green
TPM5355DSQ-SOAR-S (1)	−40 to 125°C	WSOP8	S5355D	3	1000	Green
TPM53551AM-SO1R (1)	−40 to 125°C	SOP8	M5351A	3	4000	Green
TPM53551AM-SOAR (1)	−40 to 125°C	WSOP8	M5351A	3	1000	Green
TPM53551AS-SO1R (1)	−40 to 125°C	SOP8	S5351A	3	4000	Green
TPM53551AS-SOAR (1)	−40 to 125°C	WSOP8	S5351A	3	1000	Green
TPM53551BM-SO1R (1)	−40 to 125°C	SOP8	M5351B	3	4000	Green
TPM53551BM-SOAR (1)	−40 to 125°C	WSOP8	M5351B	3	1000	Green
TPM53551BS-SO1R (1)	−40 to 125°C	SOP8	S5351B	3	4000	Green
TPM53551BS-SOAR	−40 to 125°C	WSOP8	S5351B	3	1000	Green
TPM53551CM-SO1R (1)	−40 to 125°C	SOP8	M5351C	3	4000	Green
TPM53551CM-SOAR (1)	−40 to 125°C	WSOP8	M5351C	3	1000	Green

Order Number	Operating Ambient Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPM53551CS-SO1R (1)	−40 to 125°C	SOP8	S5351C	3	4000	Green
TPM53551CS-SOAR (1)	−40 to 125°C	WSOP8	S5351C	3	1000	Green
TPM53551DM-SO1R (1)	−40 to 125°C	SOP8	M5351D	3	4000	Green
TPM53551DM-SOAR (1)	−40 to 125°C	WSOP8	M5351D	3	1000	Green
TPM53551DS-SO1R (1)	−40 to 125°C	SOP8	S5351D	3	4000	Green
TPM53551DS-SOAR (1)	−40 to 125°C	WSOP8	S5351D	3	1000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

(1) Contact 3PEAK representatives for more information.

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