5-A / 5-A, Single-Channel Isolated Gate Driver with Miller Clamp, Split Gate

Features

- Single-Channel Isolated Gate Driver with CMOS/TTL-Compatible Input
- Automotive AEC-Q100 Grade 1 (TPM5350xQ)
- 5-A Source/5-A Sink Peak Output Current with Rail-to-Rail Output
- Feature Options
  - Split Outputs (TPM5350S, TPM5350SQ)
  - Miller Clamp (TPM5350M, TPM5350MQ)
- Up to 40-V Output Driver Supply Voltage
- 8-V and 12-V V_{CC} UVLO Options
- 3-V to 15-V Input Supply Voltage
- Negative 5-V Reverse Polarity Voltage Handling Capability on Input Stage
- Ultra-Fast Output Driving
  - 60-ns Propagation Delay
  - 25-ns Delay Matching
  - 35-ns Pulse Width Distortion
- 5-kV_{RMS} Reinforced Isolation Rating
- ±100-kV/μs Common-Mode Transient Immunity (CMTI)
- Industrial Standard Wide-Body WSOP8 & SOP8 Packages
- Operating Ambient Temperature T_A: −40°C to +125°C
- Safety-Related Certifications: (In progress)
  - VDE Reinforced Insulation according to DIN VDE V 0884-11: 2017-01 (Planned)
  - 5.7-kV_{RMS} Isolation Rating per UL 1577 (Planned)
  - CSA Certification per IEC 60950-1, IEC 62368-1, and IEC 60601-1 End Equipment Standards (Planned)
  - TÜV Certification according to EN 60950-1 and EN 61010-1 (Planned)
  - CQC Certification per GB4943.1-2011 (Planned)

Applications

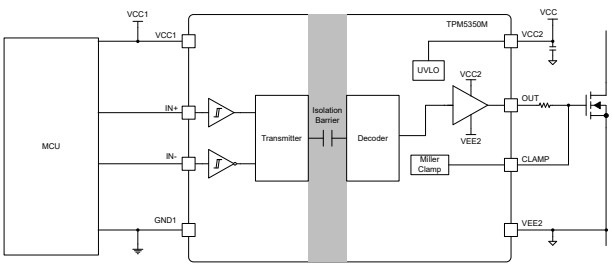
- Industrial Motor-Control Drives
- Industrial Power Supplies, UPS
- Solar Inverters
- Automotive On-board-charger, High Voltage DC/DC Converter
- Silicon Carbide (SiC) Driver

Description

The TPM5350xQ driver is an automotive-grade single-channel isolated gate driver for IGBTs, MOSFETs, and SiC MOSFETs. Its input is CMOS/TTL compatible with the industrial standard wide-body WSOP8 and standard SOP8 packages. Its driving capability can support a 5-A source and 5-A sink current. The output stage can withstand high voltages up to 40 V and support the latest generation of IGBT and SiC-based applications.

The TPM5350xQ device provides high electromagnetic immunity and low emissions at low power consumption. Its isolation channel is separated by a double-capacitive silicon dioxide (SiO2) insulation barrier. 3PEAK proprietary galvanic isolation technology supports 150-kV/μs common-mode transient immunity (CMTI), which is critical especially for SiC applications. The TPM5350M device has integrated Miller Clamp to prevent false turn on by miller current. The TPM5350S has split outputs to adjust rising and falling slew rates without the needs of external diodes. Its enhanced reliability can support high-power industrial applications.

Typical Application Circuit



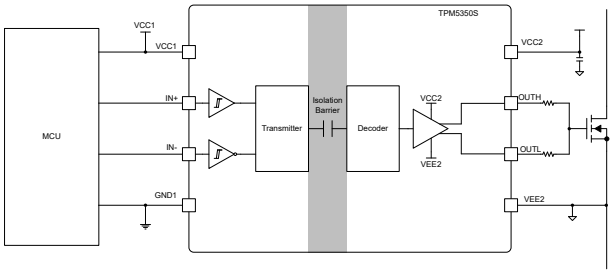


Table of Contents

Product Family Table

Order Number	UVLO Threshold (V)	Feature	Package	Quality Grade
TPM5350MQ-SOAR-S	12.5	Miller Clamp	WSOP8	Automotive
TPM5350BMQ-SOAR-S (1)	8.5	Miller Clamp	WSOP8	Automotive
TPM5350MQ-SO1R-S (1)	12.5	Miller Clamp	SOP8	Automotive
TPM5350SQ-SOAR-S (1)	12.5	Split Outputs	WSOP8	Automotive
TPM5350BSQ-SOAR-S (1)	8.5	Split Outputs	WSOP8	Automotive
TPM5350SQ-SO1R-S (1)	12.5	Split Outputs	SOP8	Automotive
TPM5350M-SOAR	12.5	Miller Clamp	WSOP8	Industrial
TPM5350S-SOAR (1)	12.5	Split Outputs	WSOP8	Industrial
TPM5350BS-SOAR (1)	8.5	Split Outputs	WSOP8	Industrial

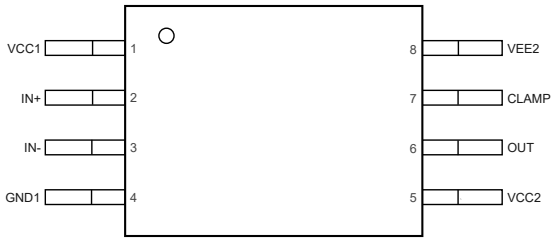
(1) Contact sales representatives for more details.

Revision History

Date	Revision	Notes
2024-05-15	Rev A.0	Initial release

Pin Configuration and Functions

TPM5350M
WSOP8
Top View



TPM5350S
WSOP8
Top View

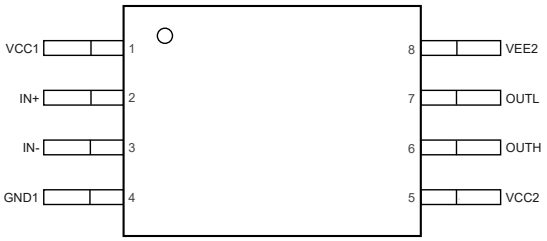


Table 1. Pin Functions: TPM5350M

Pin		I/O	Description
No.	Name		
1	VCC1	P	Input side power supply. Connect a 0.1-uF capacitor to GND and place it close to the device.
2	IN+	I	Non-inverting input. Internally pulled low if left open.
3	IN–	I	Inverting input. Internally pulled high if left open.
4	GND1	G	Input side power ground
5	VCC2	P	Output side power rail. Connect a capacitor close to the device to the support transient output current.
6	OUTH	O	Gate driver pull-up output.
7	OUTL	O	Gate driver pull-down output.
8	VEE2	G	Output side ground.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Input Voltage	Input Supply Voltage, VCC1 - GND1	−0.3	18	V
	Input Signal Voltage, V_{IN+} - GND1, V_{IN-} - GND1	−5	VCC1 + 0.3	V
Output Voltage	Output Supply Voltage, VCC2 - VEE2	−0.3	40	V
	Output Side Voltage with reference to VEE2, VOUTH, VOUTL, VOUT, VCLAMP	VEE2−0.3	VCC2 + 0.3	V
T_J	Maximum Junction Temperature	−40	150	°C
T_A	Operating Ambient Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.
(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Table 2. TPM5350M

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

Table 3. TPM5350S

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
VCC1	Input Supply Voltage, reference to GND1	3	18	V
VCC2	Output Supply Voltage, reference to VEE2, 12V UVLO option, TPM5350x	13	36	V
VCC2	Output Supply Voltage, reference to VEE2, 8V UVLO option TPM5350Bx	9.5	36	V
T_J	Junction Temperature	−40	150	°C
T_A	Operating Ambient Temperature	−40	125	°C

(1) Contact 3PEAK representatives for more information.

Safety Limiting Values

Parameter		Test Conditions	Min	Typ	Max	Unit
P_D	Maximum power dissipation on input and output	V_{CC1} = 15 V, V_{CC2} = 15 V, f = 2.1-MHz, 50% duty cycle, square wave, 2.2-nF load			1.2	W
P_{D1}	Maximum input power dissipation	V_{CC1} = 15 V, V_{CC2} = 15 V, f = 2.1-MHz, 50% duty cycle, square wave, 2.2-nF load			50	mW
P_{D2}	Maximum output power dissipation	V_{CC1} = 15 V, V_{CC2} = 15 V, f = 2.1-MHz, 50% duty cycle, square wave, 2.2-nF load			1.05	W

Insulation Specifications

Parameter		Conditions	Value	Unit
CLR	External Clearance	Shortest terminal-to-terminal distance through air	> 8.5	mm
CPG	External Creepage	Shortest terminal-to-terminal distance across the package surface	> 8.5	mm
DTI	Distance through the Insulation	Minimum internal gap (internal clearance)	> 21	μm
CTI	Comparative Tracking Index		> 600	V
	Material Group		I	
	Overvoltage Category per IEC 60664-1	For Rated Mains Voltage ≤ 600 V_{RMS}	I-III	
		For Rated Mains Voltage ≤ 1000 V_{RMS}	I-II	
	Pollution Degree		2	
	Climate Category		40/125/21	
C_{IO}	Isolation Capacitance	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	1.2	pF
R_{IO}	Isolation Resistance	V_{IO} = 500 V, T_A = 25 °C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125 °C	> 10^{11}	
		V_{IO} = 500 V, T_A = 150 °C	> 10^9	
V_{IORM}	Maximum Repetitive Isolation Voltage	AC voltage (bipolar)	1500	V_{PK}
V_{IOWM}	Maximum Working Isolation Voltage	AC voltage; TDDB Test	1060	V_{RMS}
		DC voltage	1500	V_{DC}
V_{IOTM}	Maximum Transient Isolation Voltage	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production)	8000	V_{PK}
V_{IOSM}	Maximum Surge Isolation Voltage	Test method per IEC 62368-1, 1.2/50 μs waveform, V_{TEST} = 1.3 × V_{IOSM}(qualification) = 11700v	9000	V_{PK}
V_{ISO}	UL 1577 Withstand Isolation Voltage	V_{TEST} = V_{ISO} = 5700 V_{RMS}, t = 60 s (in qualification), V_{TEST} = 1.2 × V_{ISO}- 6840 V_{RMS} ， t = 1 s (100% in production)	5700	V_{RMS}
q_{pd}	Apparent Charge	Method a, After Input/Output safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10 s	≤ 5	pC
		Method a, After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10 s	≤ 5	
		Method b1; At routine test (100% production) and preconditioning (type test), V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1 s	≤ 5	

(1) All pins on each side of the barrier tied together create a two-terminal device.

Electrical Characteristics

All test conditions: VCC1 − GND1 = 3.3 V or 5 V, VCC2 - VEE2 = 15 V, V_{EE2} referred as GND, T_A = −40°C to 125°C, Output capacitance C_L = 100 pF, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Supply						
I_{VCC1}	Input Supply Quiescent Current	*f* = 500 kHz, Duty = 50%	1.6	2.1	2.5	mA
I_{VCC2}	Output Supply Quiescent Current	VCC2 − GND2 = 15V	0.9	1.56	2.3	mA
		VCC2 − GND2 = 36V		1.73		
V_{UVLOR1}	Undervoltage Lock out, VCC1, Rising edge			2.72	2.85	V
V_{UVLOF1}	Undervoltage Lock out, VCC1, Falling edge		2.4	2.58		V
$V_{UVLOHYS1}$	Undervoltage Lock out, VCC1, Hysteresis			0.14		V
C_{IN}	Input Parasitic Capacitance	*f* = 0.5 MHz		15		pF
Under Voltage Lockout, TPM5350 (12-V UVLO Version)						
V_{UVLO_R}	Under Voltage Lock-out Threshold, Rising Edge		10.8	12.5	13.5	V
V_{UVLO_F}	Under Voltage Lock-out Threshold, Falling Edge		10	11.5	12.6	V
V_{UVLO_HYS}	UVLO Hysteresis		0.7	1	1.2	V
Under Voltage Lockout, TPM5350B (8-V UVLO Version)						
V_{UVLO_F}	Under Voltage Lock-out Threshold, Falling Edge			8.7		V
V_{UVLO_F}	Under Voltage Lock-out Threshold, Falling Edge			8		V
V_{UVLO_HYS}	UVLO Hysteresis			0.7		V
LOGIC I/O						
$V_{IT+(IN)}$	Input Threshold, rising edge, IN+, IN-		1.6	1.7	1.9	V
$V_{IT-(IN)}$	Input Threshold, falling edge, IN+, IN-		1.1	1.24	1.4	V
$V_{HYS(IN)}$	Input Threshold Hysteresis, IN+, IN-		0.3	0.46	0.65	V
I_{IH}	Input Leakage Current	IN+ = VCC1		10	100	µA
I_{IL}	Input Leakage Current	IN− = GND1	−240	−40		µA
		IN− = GND1 − 5V	−310	−80		µA
Gate Driver Stage						

Parameter		Conditions	Min	Typ	Max	Unit
V_{OH}	High-Level Output Voltage(VCC2 - OUT) and(VCC2 - OUTH)	I_{OUT} = –20 mA	70	180	360	mV
V_{OL}	Low-Level Output Voltage (OUT and OUTL)	IN+ = low, IN– = high; I_O= 20 mA		12	25	mV
I_{OH}(1)	Peak Source Current	IN+ = high, IN– = low		5		A
I_{OL}(1)	Peak Sink Current	IN+ = high, IN– = low		5		A
V_{CLAMP}	Clamp Low-level Current	I_{CLAMP} = 20 mA		26	50	mV
I_{CLAMP}(1)	Clamp Low-level Current for Low-output Voltage	V_{CLAMP}= V_{EE2} + 2 V		1.2		A
$V_{CLAMPTH}$	Clamp Threshold Voltage			2.1	2.3	V
V_{CLP_OUT} (1)	Clamping Voltage VOUTH − VCC2 to VOUT − VCC2	IN+ = HIGH, IN− = LOW, t_{CLAMP} = 10µs, I_{OUTH}/I_{OUT} = 500 mA		1		V
V_{CLP_OUT}(1)	Clamping Voltage VEE2 − VOUTL or VEE2 − VCLAMP or VEE2 − VOUT	IN+ = HIGH, IN− = LOW, t_{CLAMP} = 10 µs, I_{OUTH}/I_{OUT} = −500 mA		1.5		V
		IN+ = LOW, IN– = HIGH, I_{CLAMP} or I_{OUTL} = −20 mA		0.9		V
Active Pulldown						
V_{OUTSD}	Active Pulldown Voltage on OUTL, CLAMP, and OUT	I_{OUTL} or I_{OUT} = 750 mA, VCC2 = OPEN	2		2.5	V

(1) Guranteed by design

Timing Characteristics

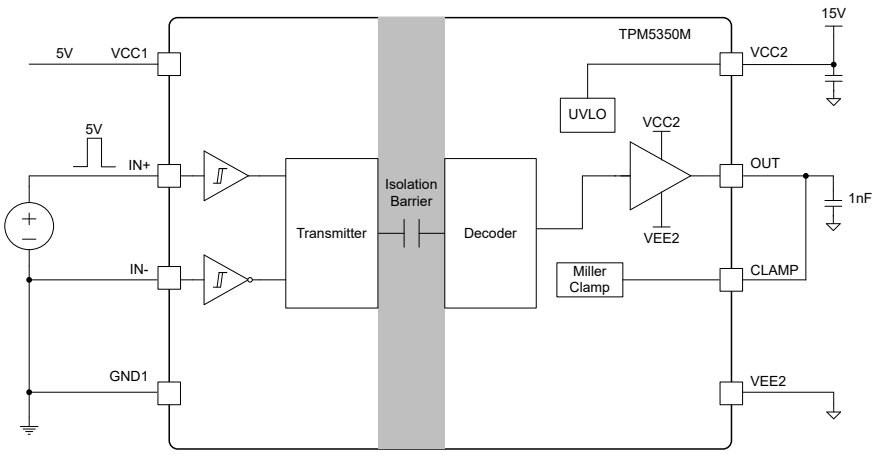
Parameter		Test Conditions	Min	Typ	Max	Unit
t_r	Output Rise Time (1)	F_{SW} = 20 kHz, (50% Duty Cycle) V_{CC} = 15 V , C_{LOAD} = 100 pF		16		ns
t_f	Output Fall Time (1)			9.2		ns
t_{PLH}	Propagation Delay, Low to High			39	65	ns
t_{PHL}	Propagation Delay, High to Low			39	65	ns
t_{PWD}	Pulse Width Distortion $\|t_{PHL} - t_{PLH}\|$		0	1.4	20	ns
$t_{sk(pp)}$	Part-to-Part Skew in Propagation Delay between any Two Parts (2)	F_{SW} = 20 kHz, (50% Duty Cycle) V_{CC} = 15 V, I_F = 10 mA			25	ns
$V_{CC1UVLO\_rec}$	UVLO Recovery Delay, VCC1		15	24.5	40	μs
$t_{VCC2UVLO\_rec}$	UVLO Recovery Delay, VCC2		15	27.5	45	μs
CMTI	Common-Mode Transient Immunity (1)	PWM is tied to GND or V_{CC1}, V_{CM} = 1200 V	100	150		kV/μs

(1) Guaranteed by design.

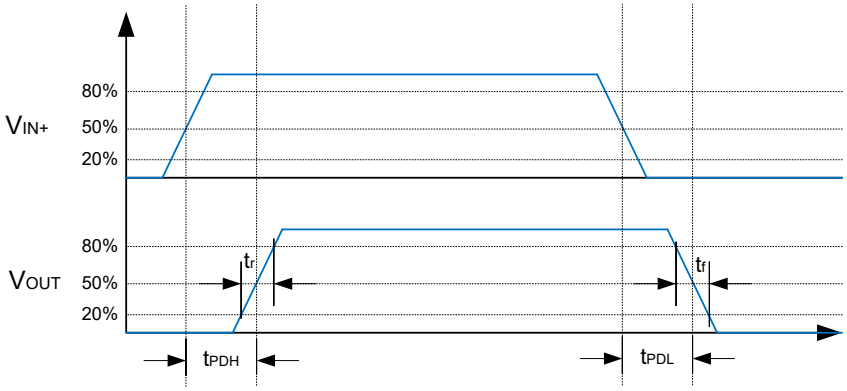
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between the output of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals, and loads guaranteed by characterization

Parameter Measurement

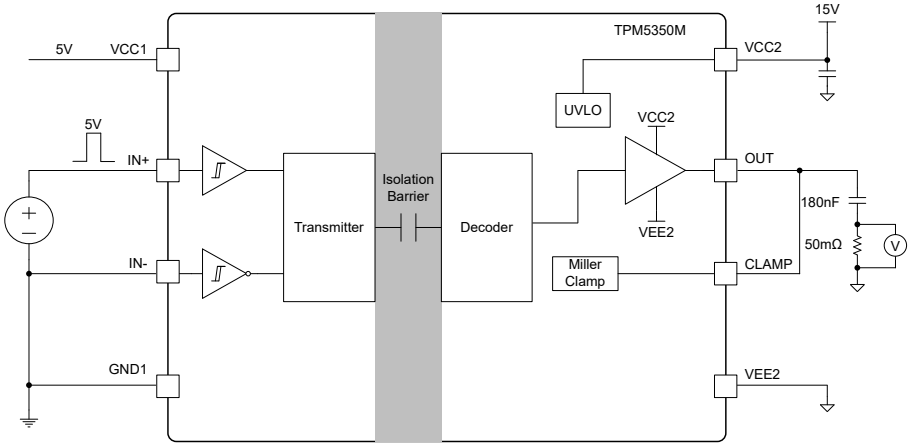
Driver Parameter



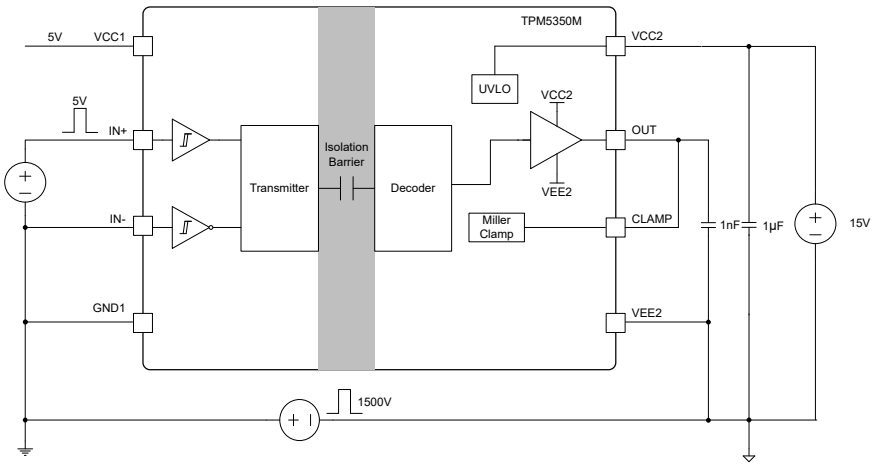
Driver Timing Diagram



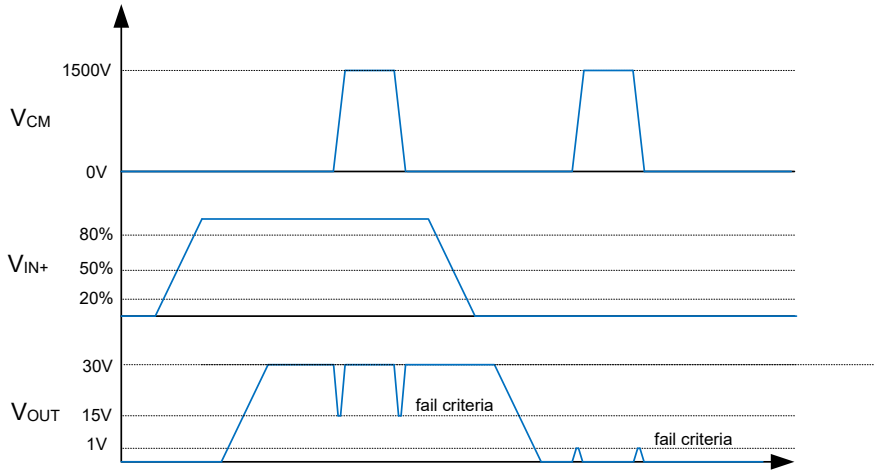
Output Current Measurement



CMTI Test Circuit



CMTI Test Criteria


1500V
VCM
0V
80%
VIN+
50%
20%
30V
VOUT
15V
1V
fail criteria
fail criteria

Typical Performance Characteristics

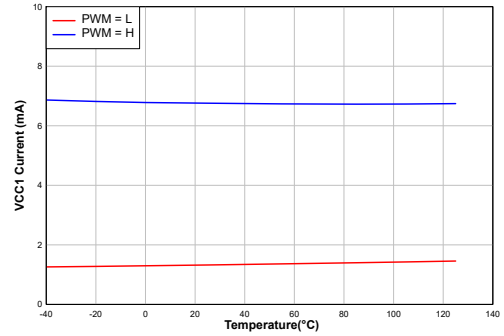


Figure 1. VCC1 Current vs. Temperature

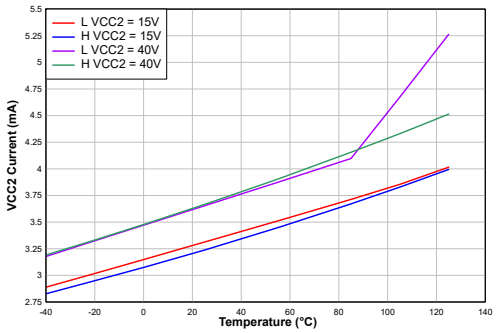


Figure 2. VCC2 Current vs. Temperature

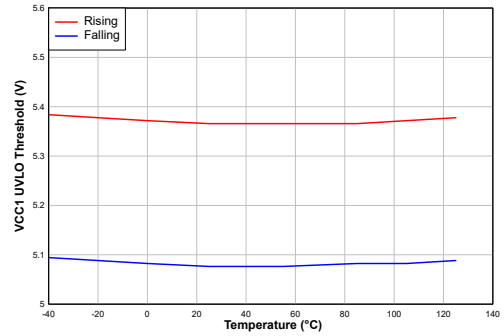


Figure 3. VCC1 UVLO Threshold vs. Temperature

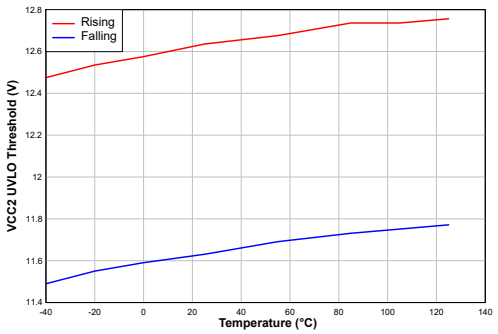


Figure 4. VCC2 UVLO Threshold vs. Temperature

I_{OUT} = 20 mA

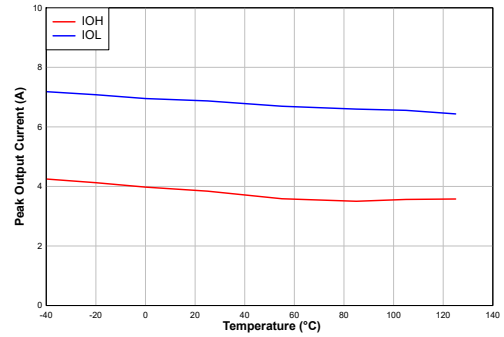


Figure 5. Peak Output Current vs. Temperature

I_{OUT} = −20 mA

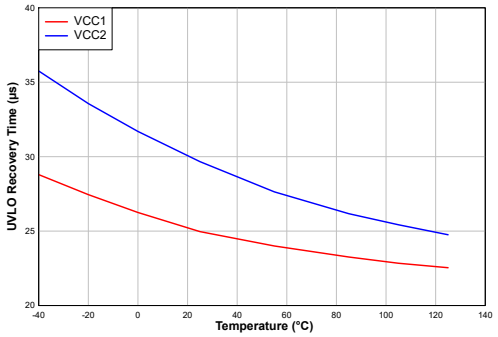


Figure 6. UVLO Recovery Time vs. Temperature

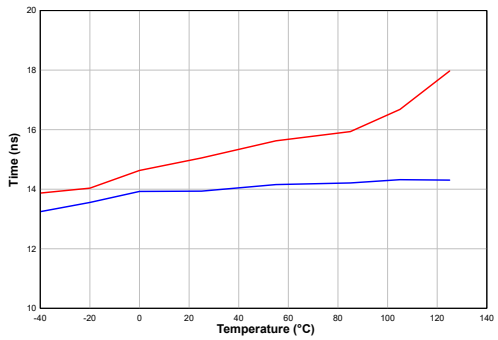


Figure 7. Output Rise and Fall Time vs. Temperature

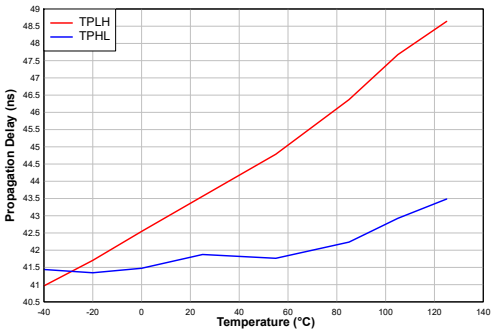


Figure 8. Output Propagation Delay vs. Temperature

Detailed Description

Overview

The TPM5350xQ is a single-channel isolated gate driver for MOSFETs, IGBTs, and SiC FETs with TTL/CMOS input stage. It has a 40-V maximum operating driver voltage, which is especially suitable for high-power fast-transient IGBT / SiC applications.

The TPM5350xQ is designed to replace the optocoupler gate driver with an industry-standard wide-body 8-pin package of WSOP8, with more than 8.5-mm creepage and clearance to withstand over 1060-V_{RMS} working voltage, reinforced isolation, and 5.7 kV_{RMS} for the 60 s and a surge rating of 8-k V_{PK}. 3PEAK proprietary isolation technology supports common-mode transient immunity of greater than 150 kV/μs.

The TPM5350x offers two variations: split output and Miller clamp (refer to the Device Comparison Table). Isolation in the TPM5350 is achieved using high-voltage SiO2-based capacitors with 3PEAK proprietary on-off keying (OOK) modulation scheme. The TPM5350 incorporates advanced circuit techniques to optimize CMTI performance and minimize radiated emissions resulting from high-frequency carrier and IO buffer switching.

Functional Block Diagram

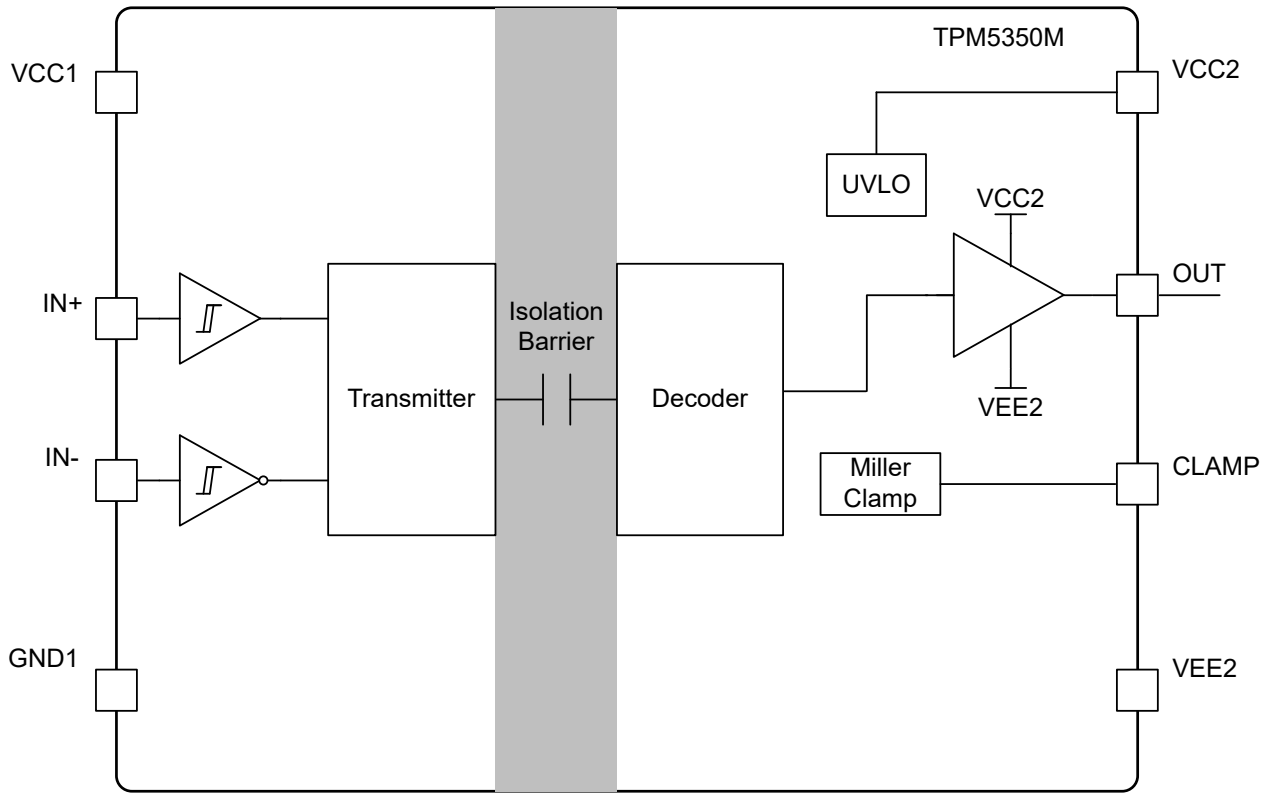


Figure 9. TPM5350M Functional Block Diagram

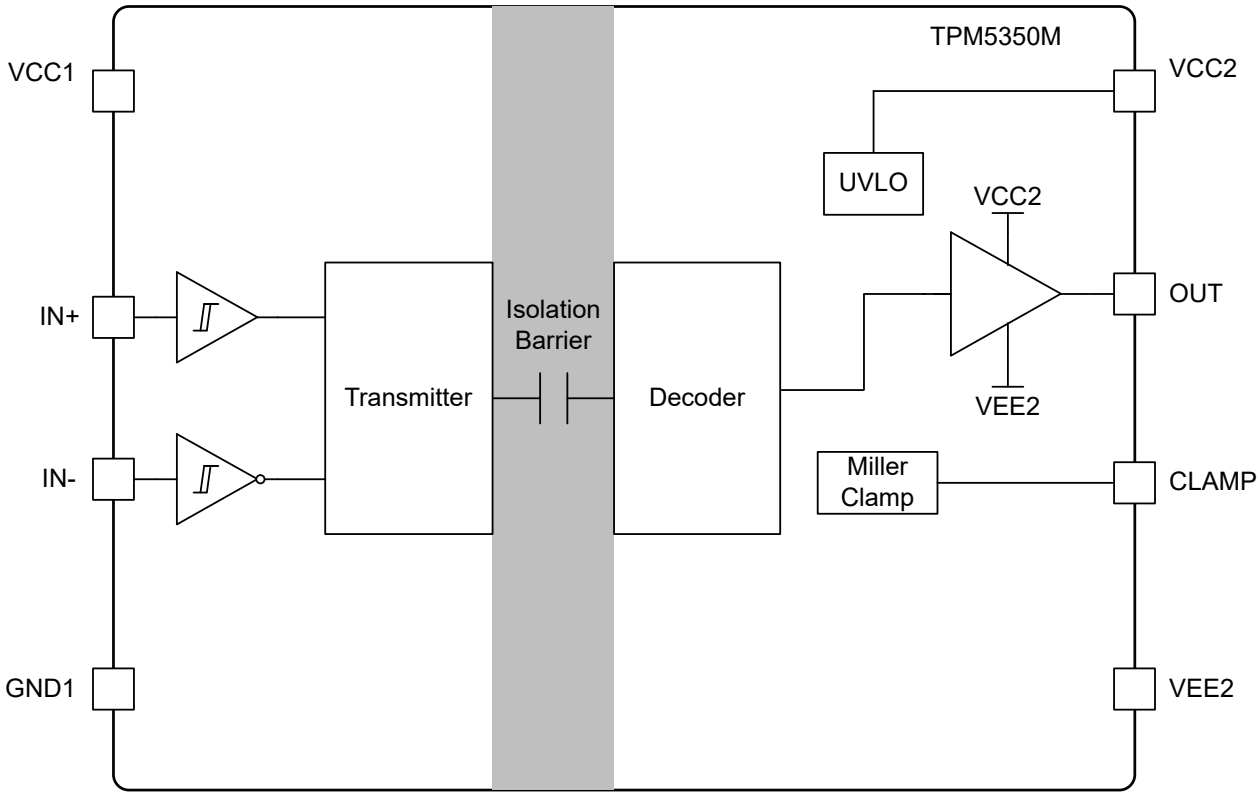


Figure 10. TPM5350S Functional Block Diagram

Feature Description

Power Supply

The VCC1 input power supply of the TPM5350 supports a wide voltage range from 3 V to 15 V, while the VCC2 output supply accommodates a voltage range from 9.5 V to 33 V.

When operating with bipolar supplies, the power device is turned off by applying a negative voltage on the gate relative to the emitter or source. This configuration prevents unintentional activation of the power device due to current induced by the Miller effect. In the case of modern SiC MOSFETs, the typical values are 15 V and −3 V. When operating with a unipolar supply, the VCC2 supply is connected to 15 V for SiC MOSFETs. The VEE2 supply is connected to 0 V.

In both scenarios, the TPM5350M device with Miller clamping function can be utilized. The Miller clamping function is implemented by establishing a low-impedance path between the gate of the power device and the VEE2 supply. This allows the Miller current to sink through the clamp pin, thereby ensuring that the gate voltage remains below the turn-on threshold value.

Input Stage

The input pins (IN+ and IN-) of the TPM5350 family employ CMOS-compatible input-threshold logic, ensuring complete isolation from the VCC2 supply voltage. These pins are designed to be easily driven by logic-level control signals, such as those from 3.3-V microcontrollers. The TPM5350 family typically operates with a high threshold (VIT+(IN)) of 0.55 × VCC1 and a low threshold of 0.45 × VCC1, offering reliable signal compatibility. With a wide hysteresis (Vhys(IN)) of 0.1 × VCC1, the devices exhibit excellent noise immunity and stable performance.

In the event that any of the inputs are left unconnected, an internal pulldown resistance of 128 kΩ ensures that the IN+ pin is pulled low, while internal resistance of 128 kΩ pulls the IN- pin high. 3PEAK recommends, for enhanced noise immunity, to ground any unused input or connecting it to the VCC1 voltage.

A notable advantage of the TPM5350 family is the isolation between the input and output drivers. As a result, the input signal amplitude can be either larger or smaller than VCC2, as long as it remains within the recommended limits. This feature provides flexibility when integrating the gate driver with various control signal sources and allows the user to choose the most suitable VCC2 voltage for a specific gate. However, it is crucial to ensure that the amplitude of any signal applied to IN+ or IN- never exceeds the voltage of VCC1.

Decoder & Output Stage

The high-frequency signal is converted by the decoder via double-capacitive insulation barrier as the output stage's input. The rail-to-rail output stage provides a high-peak current during the output slewing. The output V_{CC} supports a maximum of 40-V input.

The output stages of the TPM5350 family are designed with a pull-up structure that optimizes the delivery of peak-source current when it is most needed, specifically during the Miller plateau region of the power-switch turn-on transition. This occurs when the power-switch drain or collector voltage experiences a dV/dt change. The pull-up structure consists of a P-channel MOSFET and an additional N-channel MOSFET connected in parallel.

The N-channel MOSFET plays a crucial role in enhancing the peak-sourcing current for fast turn-on. During the narrow instant when the output is transitioning from a low to a high state, the N-channel MOSFET is briefly turned on, providing a boost to the current. This enables a faster turn-on operation. To provide further insight, the table below provides typical internal resistance values for both the pullup and pulldown structures of the TPM5350, illustrating their characteristics and performance.

Device	Grade	R_{NMOS}	R_{OH}	R_{OL}	R_{CLAMP}	Unit
TPM5350M	Industrial	1.54	12	0.35	1	Ω
TPM5350MQ	Automotive	1.54	12	0.35	1	Ω
TPM5350S	Industrial	1.54	12	0.35	n/a	Ω
TPM5350SQ	Automotive	1.54	12	0.35	n/a	Ω

In the TPM5350S version, the pulldown structure consists solely of an N-channel MOSFET. However, in the M version, an additional FET is connected in parallel with the pulldown structure when the CLAMP and OUT pins are linked to the gate of the IGBT or MOSFET. This configuration allows for rail-to-rail operation, providing an output voltage swing between VCC2 and VEE2.

Protection

Under-Voltage Lock Out (UVLO)

The TPM5350 family incorporates UVLO (Undervoltage Lockout) functions for both the VCC1 and VCC2 supplies to safeguard IGBTs and MOSFETs from underdriven conditions. These functions monitor the voltages between the VCC1 and GND1, as well as VCC2 and VEE2 pins.

During device start-up or if the VCC voltage falls below the VIT+ (UVLO) threshold or drops below the VIT- (UVLO) threshold after start-up, the UVLO feature activates, holding the affected output low, regardless of the input pins (IN+ and IN-). This ensures that the power devices are not operated under insufficient voltage conditions.

The VCC UVLO protection incorporates a hysteresis feature (Vhys(UVLO)). This hysteresis prevents rapid toggling or instability caused by ground noise in the power supply. It allows the device to tolerate small drops in bias voltage that may occur when the device starts switching and experiences a sudden increase in operating current consumption.

By implementing UVLO functions with hysteresis, the TPM5350 family ensures reliable operation and effectively safeguards IGBTs and MOSFETs against underdriven conditions, thereby enhancing the overall performance and protection of the system.

Table 4. VCC1 UVLO Logic

CONDITIONS	INPUTS		OUTPUTS	
	IN+	IN−	OUTH	OUT, OUTL
VCC1 UVLO	H	L	HiZ	L
	L	H	HiZ	L
	H	H	HiZ	L
	L	L	HiZ	L

Table 5. VCC2 UVLO Logic

CONDITIONS	INPUTS		OUTPUTS	
	IN+	IN−	OUTH	OUT, OUTL
VCC2 UVLO	H	L	HiZ	L
	L	H	HiZ	L
	H	H	HiZ	L
	L	L	HiZ	L

Active Pulldown

The TPM5350 family incorporates an active pulldown function to ensure that the IGBT or MOSFET gate remains in a low state when no power is connected to the VCC2 supply. This feature is designed to prevent false turn-on of the IGBT or MOSFET on the OUT, OUTL, and CLAMP pins by clamping the output voltage to approximately 2 V.

When the output stages of the driver are unbiased or in a UVLO (Undervoltage Lockout) condition, an active clamp circuit is engaged to limit the voltage rise on the driver outputs. In this state, the upper PMOS (P-channel MOSFET) is held off by a pull-up resistor, while the gate of the lower NMOS (N-channel MOSFET) is connected to the driver output through a 500-kΩ resistor. This configuration effectively clamps the output voltage to the threshold voltage of the lower NMOS device, which is approximately 1.5 V when no bias power is available.

By utilizing the active pulldown and clamp circuitry, the TPM5350 ensures that the driver outputs are held low and prevents unintended turn-on of the IGBT or MOSFET under unbiased or UVLO conditions. This feature adds an extra layer of protection and ensures the reliable operation of the overall system.

Short Circuit Clamping

The TPM5350 family incorporates a short-circuit clamping function to protect the IGBT or MOSFET gate from overvoltage breakdown or degradation during short-circuit conditions. This function works by clamping the voltages at the driver output and slightly raising the voltage of the active Miller clamp pins above the VCC2 voltage.

To implement the short-circuit clamping function, a diode connection is added between the dedicated pins and the VCC2 pin within the driver. These internal diodes are capable of conducting up to 500 mA of current for a duration of 10 µs, and they can handle a continuous current of 20 mA. If higher current conduction capability is required, external Schottky diodes can be used to enhance the performance.

By employing the short-circuit clamping function, the TPM5350 provides an additional layer of protection by limiting voltage spikes and current surges during short-circuit events. This helps safeguard the IGBT or MOSFET gate, ensuring its long-term reliability and preventing potential damage from overvoltage conditions.

Active Miller Clamp

The TPM5350 family incorporates an active Miller-clamp function to mitigate false turn-on of the power switches that may be caused by Miller current in applications utilizing a unipolar power supply. This function is designed to address the specific challenges associated with the use of a unipolar power supply.

The active Miller-clamp function is achieved by introducing a low impedance path between the gate terminal of the power switch and ground (VEE2) to effectively sink the Miller current. By providing this clamp, the gate voltage of the power switch is limited to less than 2 V during the off state, preventing unintended turn-on.

By implementing the active Miller-clamp function, the TPM5350 family ensures reliable operation by suppressing the effects of Miller current and preventing false turn-on of the power switches. This feature is particularly beneficial in applications utilizing a unipolar power supply, enhancing the overall performance and robustness of the system.

Function Table

Table 6. Function Tables for TPM5350S

INPUTS		OUTPUTS	
IN+	**IN−**	**OUTH**	**OUT, OUTL**
H	L	H	HiZ
L	H	HiZ	L
H	H	HiZ	L
L	L	HiZ	L

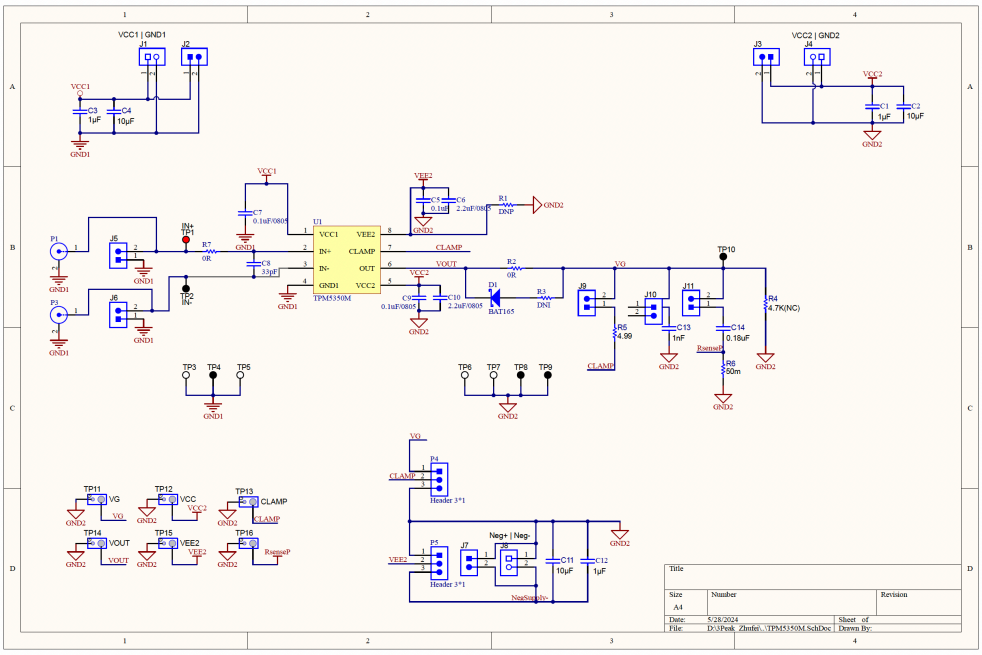
Table 7. Function Tables for TPM5350M

INPUTS		OUTPUTS	
IN+	**IN−**	**OUT**	**CLAMP**
H	L	H	Inactive
L	H	Low	Active
H	H	Low	Active
L	L	Low	Active

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Typical Application

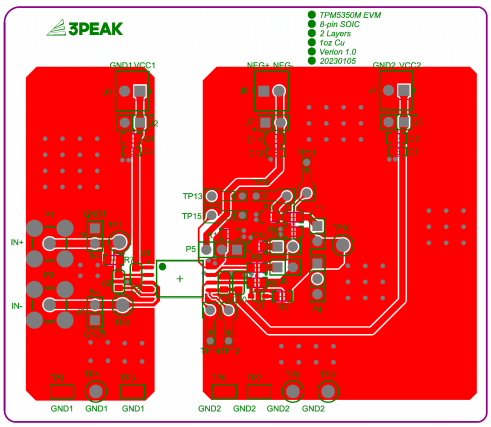


Layout

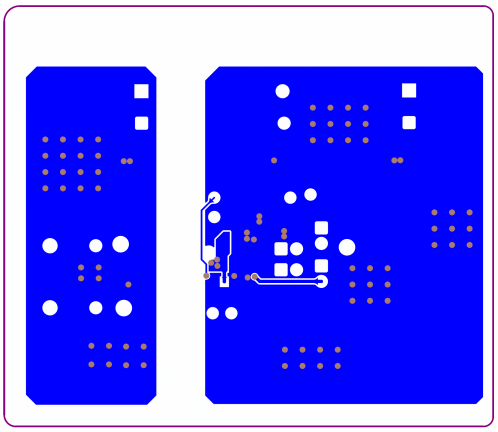
Layout Guideline

- For voltage mode input drivers, a low ESR and ESL capacitor should be placed close to the VCC and VEE pins, and the loop from VCC to VEE should be made small.
- To minimize the inductance of the drive circuit loop, the driver should be placed closely to the transistor.
- The Miller clamp trace should be directly connected to the transistor's gate, and the trace should be kept short.
- To ensure isolation between the primary and secondary sides, avoid placing any PCB traces or copper directly below the driver device. A PCB cutout or groove is recommended to increase the creepage distance.
- To enhance thermal performance, it is recommended to enlarge the PCB copper connected to VCC and VEE.

Layout Recommendations

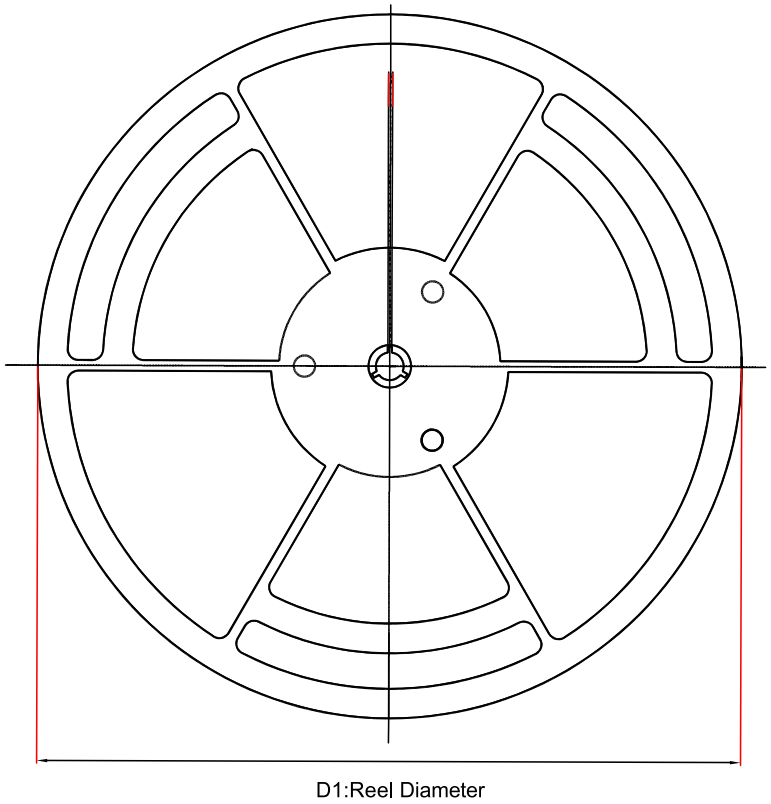


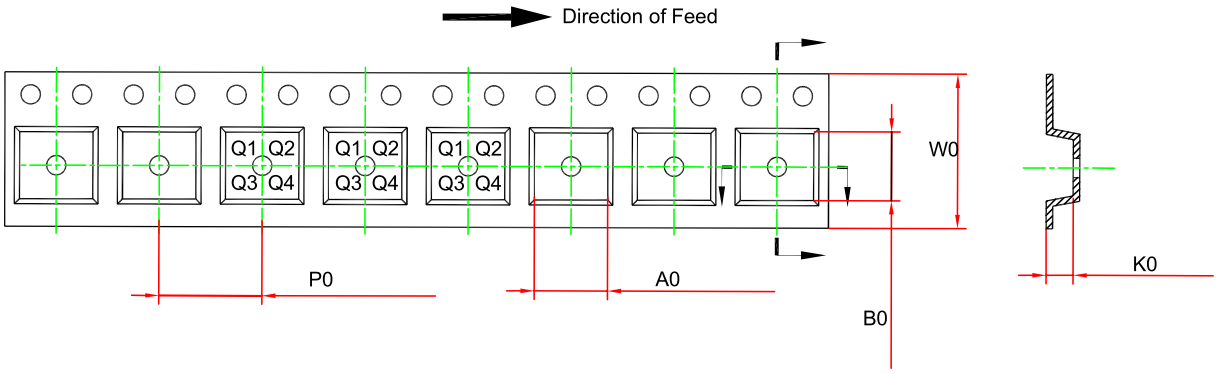
Top Layer



Bottom Layer

Tape and Reel Information





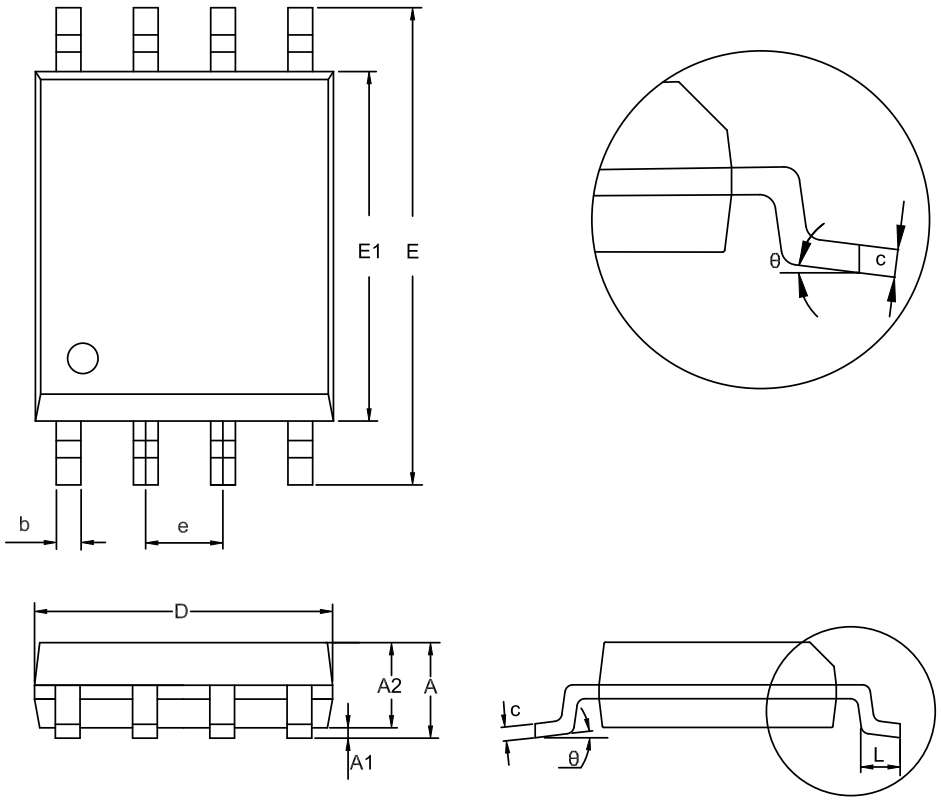
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM5350MQ-SOAR-S	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM5350BMQ-SOAR-S	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM5350M-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1

Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM5350SQ-SOAR-S	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM5350S-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM5350BSQ-SOAR-S	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1
TPM5350BS-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16	16	Q1

Package Outline Dimensions

WSOP8-A

Package Outline Dimensions SOA(WSOP-8-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	2.550	2.800	0.100	0.110
A1	0.360	0.460	0.014	0.018
A2	2.190	2.390	0.086	0.094
b	0.310	0.510	0.012	0.020
c	0.150	0.300	0.006	0.012
D	5.750	5.950	0.226	0.234
E	11.250	11.750	0.443	0.463
E1	7.400	7.600	0.291	0.299
e	1.270 BSC		0.050 BSC	
L	0.500	1.000	0.020	0.039
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Ambient Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPM5350MQ-SOAR-S	−40 to 125°C	WSOP8	535MQ	3	1000	Green
TPM5350BMQ-SOAR-S (1)	−40 to 125°C	WSOP8	53BMQ	3	1000	Green
TPM5350MQ-SO1R-S (1)	−40 to 125°C	WSOP8	535MQ	3	1000	Green
TPM5350SQ-SOAR-S (1)	−40 to 125°C	WSOP8	535SQ	3	1000	Green
TPM5350BSQ-SOAR-S (1)	−40 to 125°C	WSOP8	Q535BS	3	1000	Green
TPM5350SQ-SO1R-S (1)	−40 to 125°C	WSOP8	535SQ	3	1000	Green
TPM5350M-SOAR	−40 to 125°C	WSOP8	M535M	3	1000	Green
TPM5350S-SOAR (1)	−40 to 125°C	WSOP8	M535S	3	1000	Green
TPM5350BS-SOAR (1)	−40 to 125°C	WSOP8	M535BS	3	1000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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