Single-Channel 5-A High-Speed, Low-Side Gate Driver

Features

- Industry-Standard Pin-Out
- 4.5-V to 23-V Single-Supply Range
- Single Channel 5-A Peak Source and Sink-Drive Current
- TTL and CMOS Compatible Threshold
- Outputs Held Low during VCC-UVLO or Input Floating
- Low Propagation Delay (13-ns Typical)
- Fast Rise-and-Fall Times (7-ns and 6-ns Typical)
- ESD Protection Exceeds JESD 22 – 6-kV HBM, 1.5-kV CDM
- Available in SOT23-5 Package

Applications

- Switched-Mode Power Supplies
- DC-DC Converters
- Motor Control, Solar Inverters, UPS
- Gate & IGBT Drive

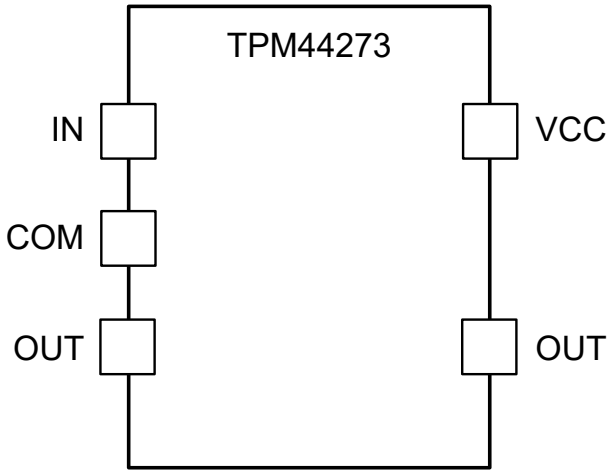
Description

The TPM44273 is a single-channel low-side gate driver for MOSFET, IGBT, and GaN power switches.

High sourcing and sinking current capability of 5 A allows for improving switching efficiencies by minimizing slew time and switching loss. The device supports maximum 25-V supply voltage and –5 V, improving system robustness especially in noisy industrial applications. Ultra-low propagation delay allows applications with tight timing requirements.

A small SOT23-5 package assists design for high-density power supply.

Typical Application Circuit



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Revision History

Date	Revision	Notes
2022-08-12	Rev.A.0	Initial Release
2023-04-09	Rev.A.1	Misc. updates
2024-02-02	Rev.A.2	Updated with new document format

Pin Configuration and Functions

TPM44273
SOT23-5
Top View

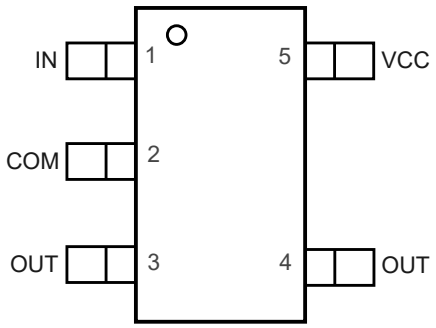


Table 1. Pin Functions: TPM44273

Pin No.	Name	I/O	Description
2	COM	Ground	Device Ground
1	IN	Input	Logic Non-inverting Input.
3,4	OUT	Output	Channel Output
5	VCC	Power	Power Supply Input

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{CC}	Power Supply Voltage	−0.3	25	V
	Output Voltage Range OUT	−0.3	V_{CC} + 0.3	V
		−2	V_{CC} + 0.3 (200-ns pulse)	V
	Input Voltage Range IN	−5	20	V
	Continuous Output Channel Current OUT	−300	300	mA
	Pulsed Output Channel Current OUT (500 ns)	−5	5	A
T_J	Operating Junction Temperature Range	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 300 mV beyond the power supply, the input current should be limited to less than 10 mA.
(3) Power dissipation and thermal limits must be observed.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Value	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±6	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
V_{CC}	Power Supply Voltage	4.5	23	V
V_{IN}	Intput Voltage Range	0	20	V
T_A	Operating Ambient Temperature Range	–40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOT23-5	89.1	52.0	°C/W

Electrical Characteristics

All test conditions: V_{CC} = 12 V, T_J = −40 °C – 150 °C, 1-µF capacitor between VCC and GND, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
$I_{DD(off)}$	Start-up Current	VCC = 3.4 V, IN = H		40	100	µA
		VCC = 3.4 V, IN = L		40	100	
V_{ON}	Supply Under Voltage Lock Out Rising Threshold	T_J = 25 °C	3.91	4.2	4.5	V
		T_J = −40 °C – 150 °C	3.7	4.2	4.65	
V_{OFF}	Supply Under Voltage Lock Out Falling Threshold	T_J = −40 °C – 150 °C	3.4	3.9	4.4	V
V_{CC_H}	Supply Under Voltage Lock Out Hysteresis		0.2	0.3	0.5	V
V_{IN_H}	IN Signal High Threshold	IN high threshold		1.95	2.3	V
V_{IN_L}	IN Signal Low Threshold	IN low threshold	1	1.25		V
V_{IN_HYS}	IN Hysteresis			0.7		V
I_{OUT}	Output Peak Current	C_{LOAD} = 0.22 µF, F_{SW} = 1 kHz		±5		A
$V_{CC} – V_{OH}$	Output High Voltage	I_{OUT} = −10 mA			40	mV
V_{OL}	Output Low Voltage	I_{OUT} = 10 mA			10	mV
R_{OH}	Output Pull-up Resistance, PMOS pull-up only	I_{OUT} = −10 mA	1	1.6	3	Ω
R_{OL}	Output Pull-down Resistance	I_{OUT} = 10 mA	0.15	0.5	1	Ω
t_R	Output Rise-time	C_{LOAD} = 1.8 nF		7	18	ns
t_F	Output Fall-time	C_{LOAD} = 1.8 nF		6	10	ns
t_{PW}	Minimal Pulse Width			15	25	ns
t_{D1}	IN to Output Propagation Delay	C_{LOAD} = 1.8 nF, 5-V IN pulse	6	13	23	ns
t_{D2}	IN to Output Propagation Delay	C_{LOAD} = 1.8 nF, 5-V IN pulse	6	13	23	ns

Typical Performance Characteristics

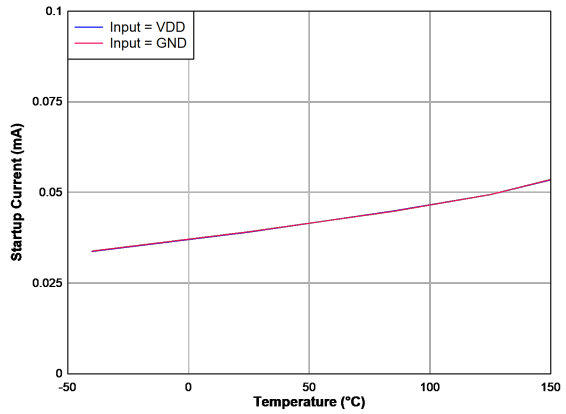


Figure 1. Start-up Current vs. Temperature

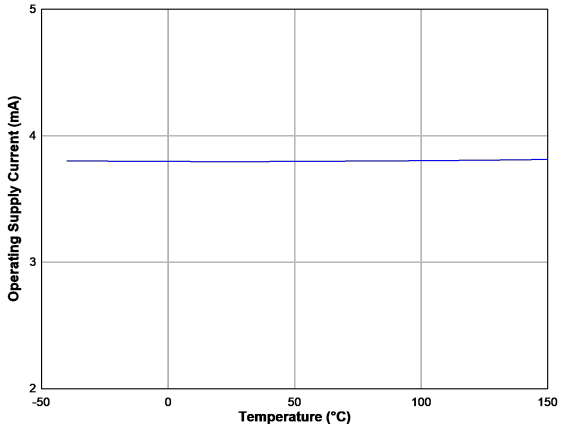


Figure 2. Operating Current vs Ambient Temperature

f = 500 kHz, C_L = 500 pF, VCC = 12 V

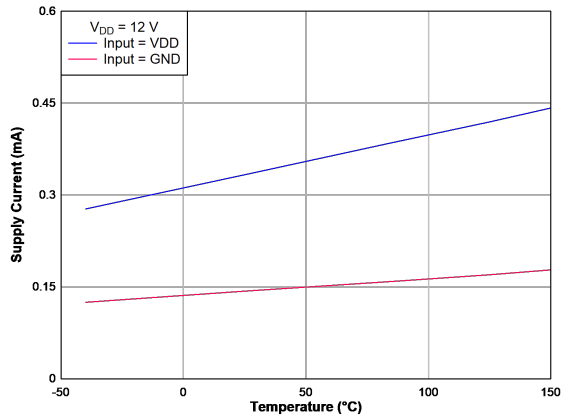


Figure 3. Supply Current vs Temperature (On/Off)

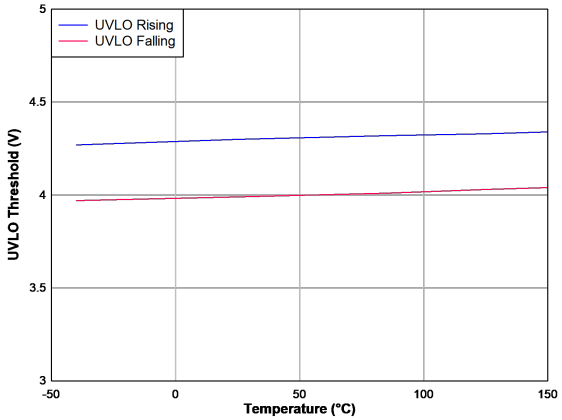


Figure 4. UVLO Threshold vs Temperature

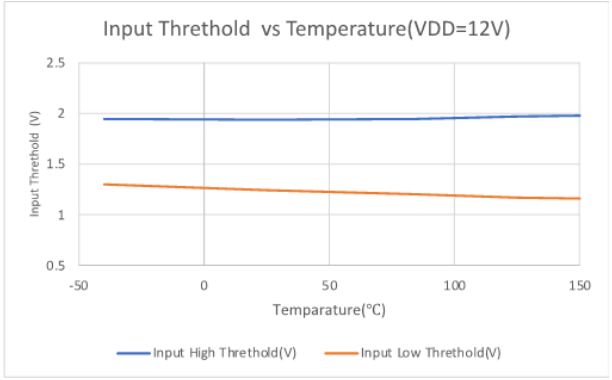


Figure 5. Input Threshold vs Temperature

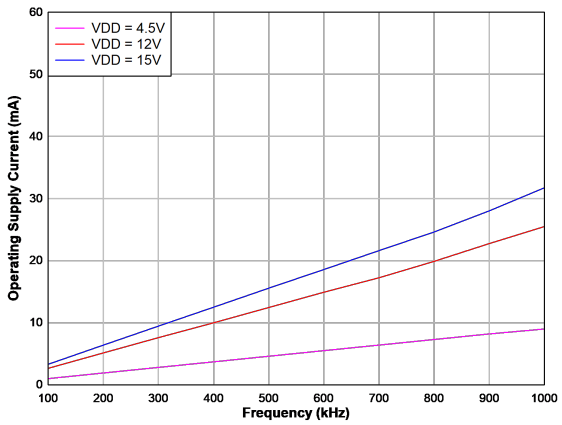


Figure 6. Operating Supply Current vs Frequency

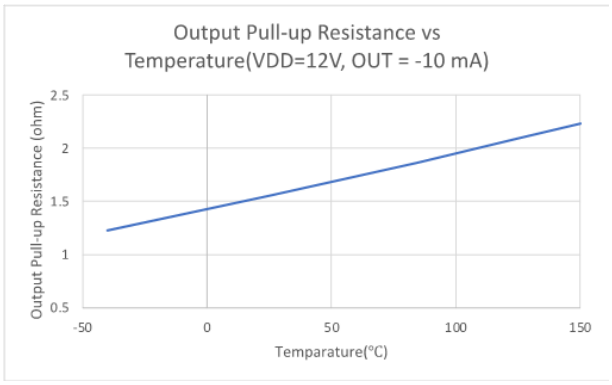


Figure 7. Output Pull-up Resistance vs Temperature

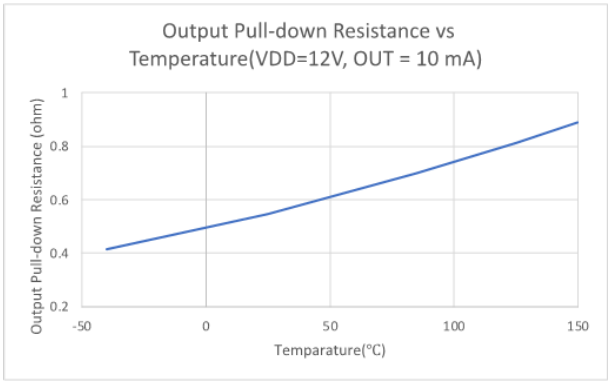


Figure 8. Output Pull-down Resistance vs Temperature

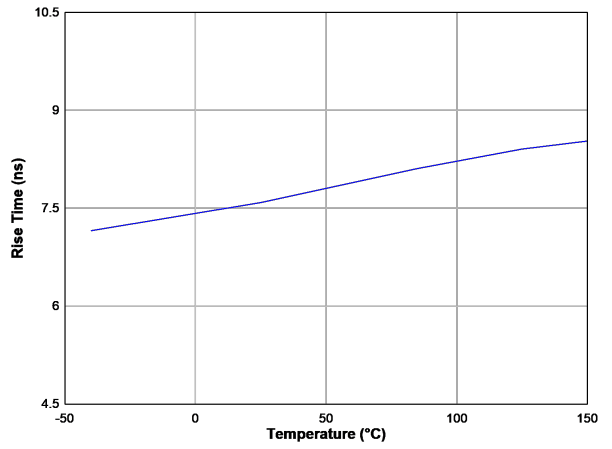


Figure 9. Rise-time vs Temperature

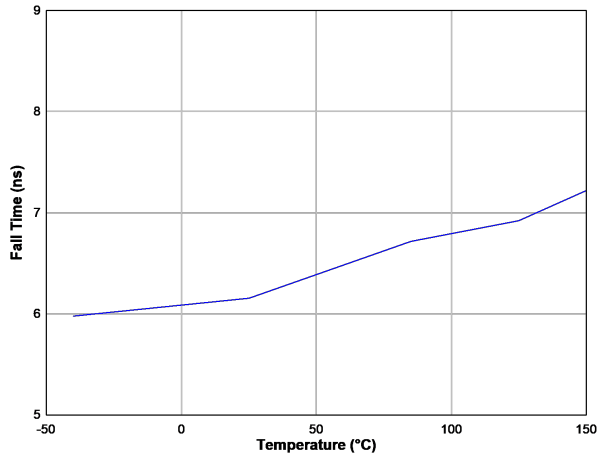


Figure 10. Fall-time vs Temperature

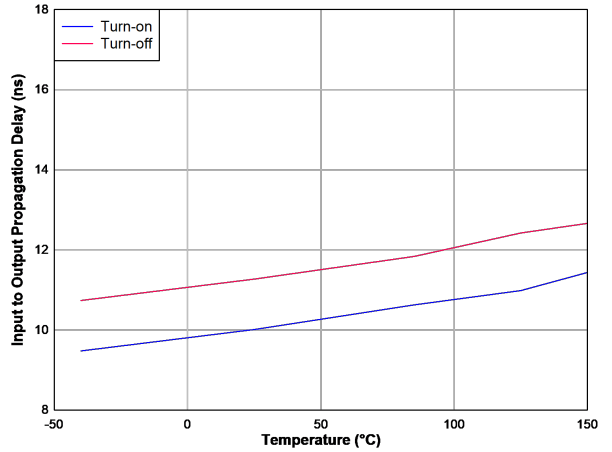


Figure 11. Input to Output Propagation Delay vs Temperature

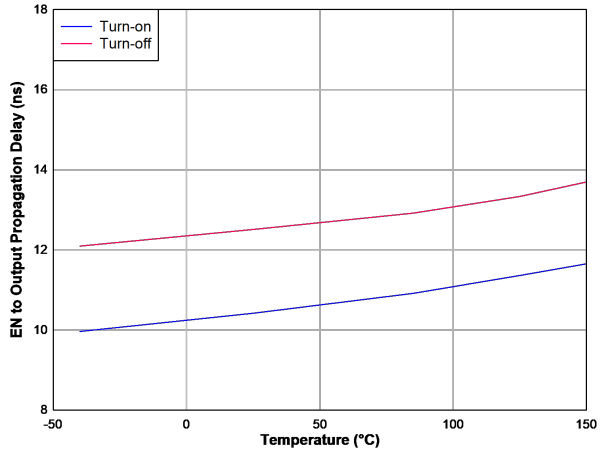


Figure 12. Enable to Output Propagation Delay vs Temperature

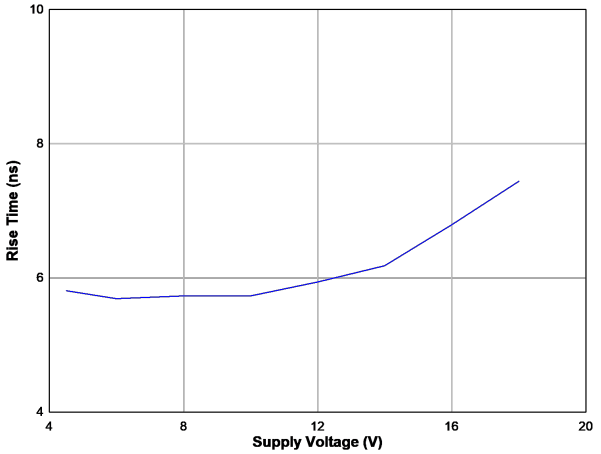


Figure 13. Fall-time vs Supply Voltage

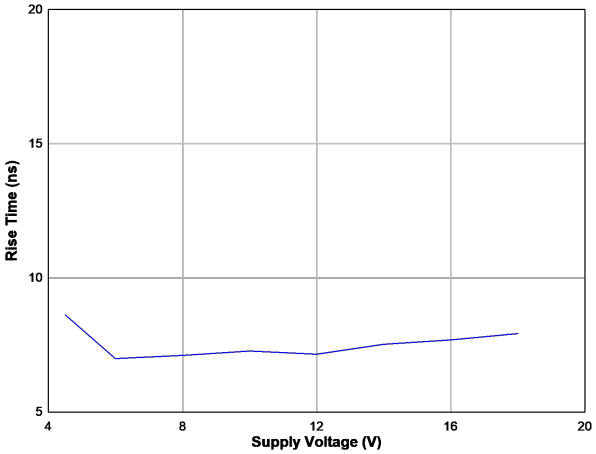


Figure 14. Rise-time vs Supply Voltage

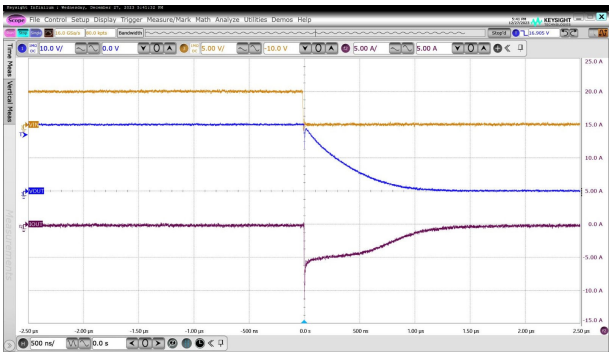


Figure 15. Output Pull-down Current

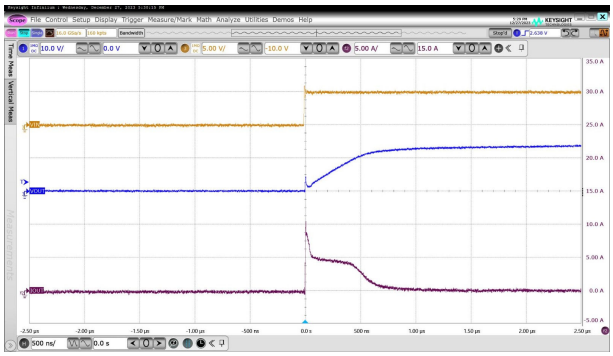


Figure 16. Output Pull-up Current

Detailed Description

Overview

The TPM44273 single-channel low-side gate driver is designed for high-performance power supplies, motor controls, and inverters. Designed with industrial standard pin-out and package, the TPM44273 accelerates the design process. With extended voltage ranges on supply voltage and negative input voltage on inputs, the TPM44273 improves system-level reliability. 5-A Strong driving capability improves gate driver efficiency and lowers heat generation, especially in high-frequency switching applications.

Functional Block Diagram

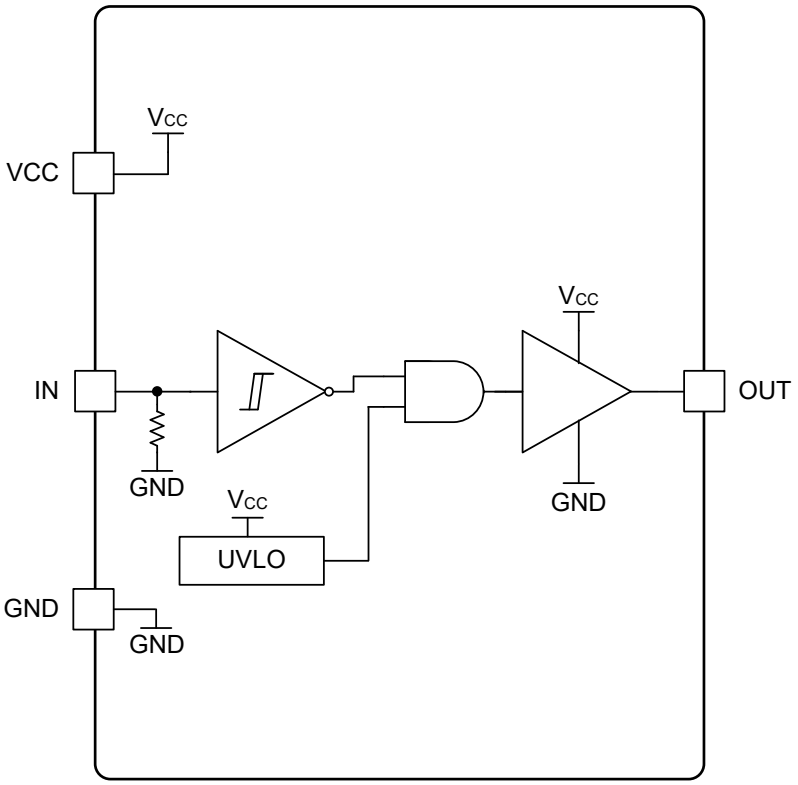


Figure 17. Functional Block Diagram

Feature Description

Low Propagation Delay Driver Output

The low-propagation-delay design allows the device to achieve industrial-leading low propagation delay between device input and output. The low delay enhances driver performance in high-frequency switching regulators.

Supply and UVLO

The device monitors supply voltage with under-voltage lock-out (UVLO). When the supply voltage is below the UVLO threshold, the outputs are held low in UVLO to avoid glitches during power rising and falling.

The quiescent current and operating current of the device are measured as shown in Figure 4. The current is related to internal quiescent current consumption as well as output current. The output current can be calculated using external transistor gate charge times switching frequency f_{sw}.

Channel Input

The input of TPM44273 gate drivers supports TTL and CMOS input with threshold voltage independent of supply voltage. The threshold is also designed as temperature-independent to support a wide range of ambient temperatures. Wide hysteresis enhances system-level noise immunity. The integrated pull-down resistors set the device in a low state when inputs are floating.

Inputs can withstand DC −5V, to improve robustness on ground bouncing.

Output Stage

The TPM44273 output stage can deliver high current sourcing and sink up to 5-A with low propagation delay.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Typical Application

Figure 18 shows the typical application schematic.

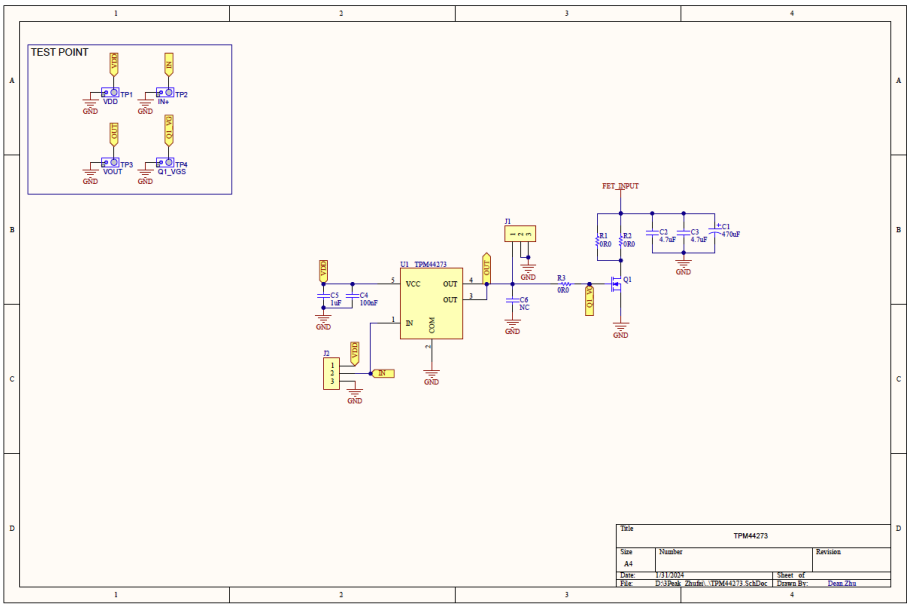


Figure 18. Application Circuit

Layout

Layout Example

Figures below show the location of external components as they appear on the PCB diagram.

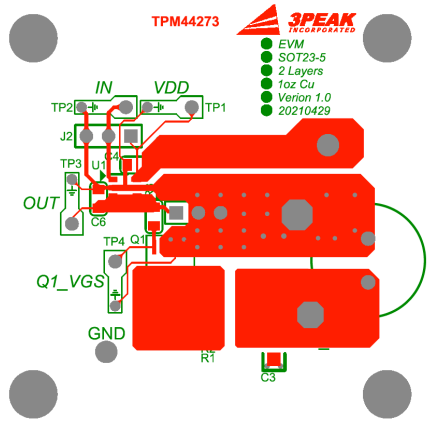


Figure 19. Top Layer

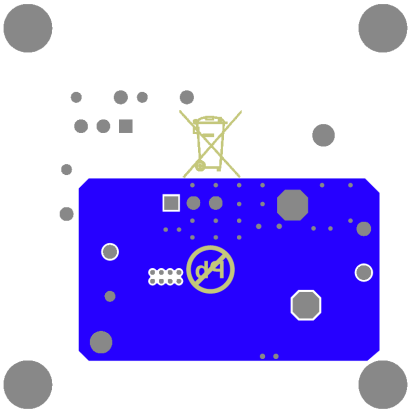
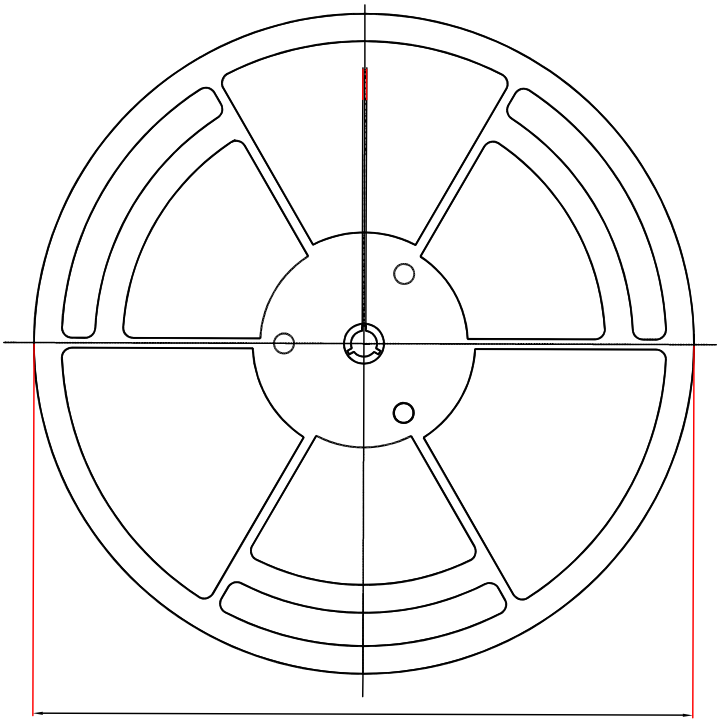
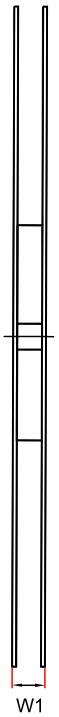
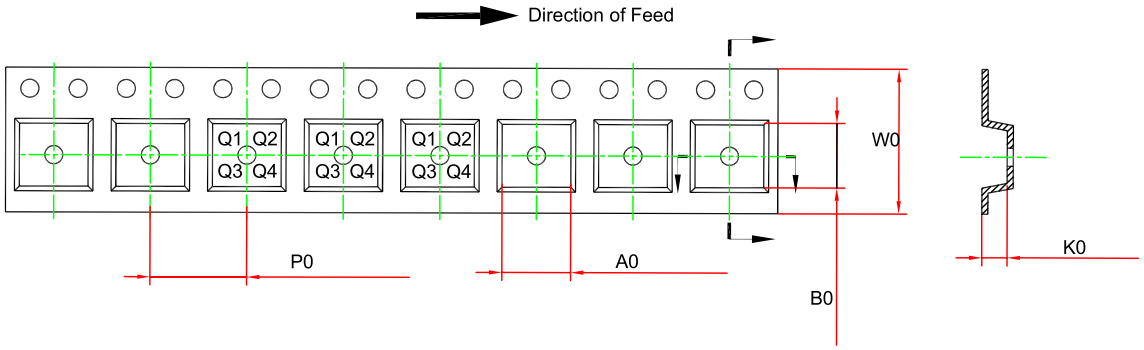


Figure 20. Bottom Layer

Tape and Reel Information





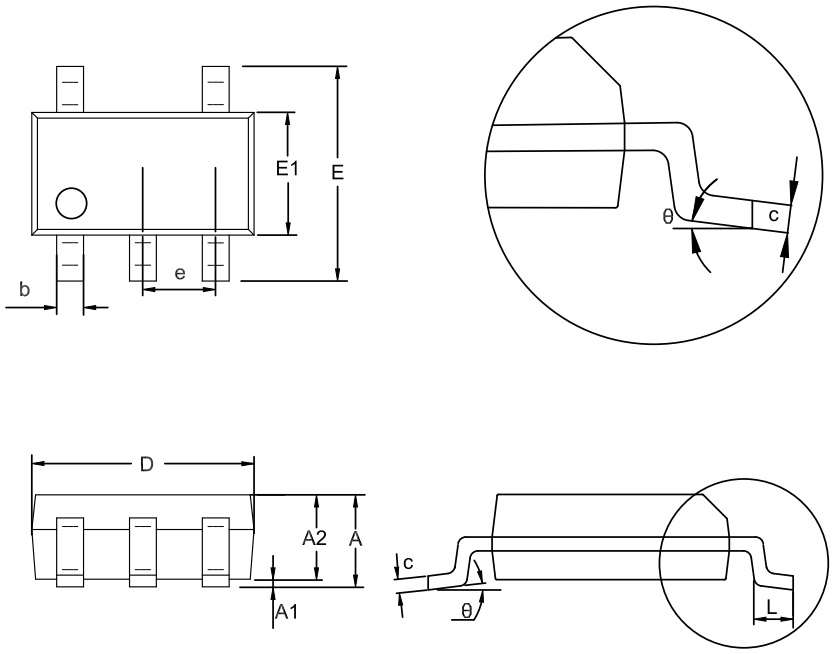


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM44273-S5TR	SOT23-5	179	12	3.3	3.25	1.4	4	8	Q3

Package Outline Dimensions

SOT23-5

Package Outline Dimensions S5T(SOT23-5-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.280	0.500	0.011	0.020
c	0.100	0.230	0.004	0.009
D	2.820	3.020	0.111	0.119
E	2.600	3.000	0.102	0.118
E1	1.500	1.720	0.059	0.068
e	0.950 BSC		0.037 BSC	
L	0.300	0.600	0.012	0.024
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Ambient Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPM44273-S5TR	−40 °C – 125 °C (1)	SOT23-5	M73	MSL3	3000	Green

(1) Ambient temperature indicates device operation condition range. Application thermal behavior needs to be taken care of when operating in high-temperature scenarios

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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