Single-Channel 2.6-A High-Speed, Low-Side Gate Driver with Over Current Protection

Features

- Single-channel Low-side IGBT Gate Driver IC with Over-current Protection
- Over-current Detection with Negative Voltage Input
- Over-current Threshold with Accurate ±5% Tolerance with −246-mV, −125-mV, −60-mV, and −500-mV Options
- Single I/O Pin for Fault Output and Enable
- Programmable Fault Clear Time
- Under Voltage Lockout (UVLO) for IGBTs
- CMOS Schmitt-triggered Inputs with 3.3-V, 5-V, and 15-V Input Compatible Logic
- 25-V VCC Voltage Supply Support
- Output in Phase with Input
- −10 Vdc Negative Input Capability of the OCP Pin
- 4-kV HBM, 1.5-kV CDM
- Available in the SOT23-6 Package

Applications

- Designed for Power Factor Correction Circuitry (PFC)
- Suitable for Home Appliances (Air Conditioners, etc.)
- Applicable in Various Industrial Scenarios
- Ideal for General-purpose Low-side Gate Driver Applications in Single-ended Topologies

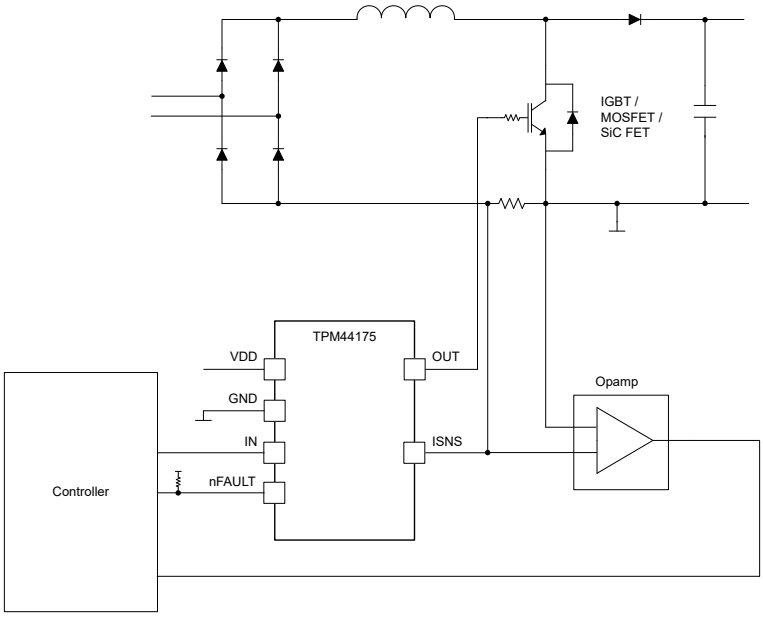
Description

The TPM44175 is a single-channel low-side gate driver for MOSFET, IGBT, and GaN power switches with over current protection.

High sourcing and sinking current capability of 2.6 A allows for improving switching efficiencies by minimizing slew time and switching loss. The device supports maximum 25-V supply voltage and –10 V, improving system robustness, especially in noisy industrial applications. Ultra-low propagation delay allows applications with tight timing requirements. The integrated over current protection feature can help prevent power transistor failure during over current scenarios.

A small SOT23-6 package assists in the design of a high-density power supply.

Typical Application Circuit



Single-Channel 2.6-A High-Speed, Low-Side Gate Driver with Over Current Protection

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Revision History

Date	Revision	Notes
2025-09-04	Rev.A.0	Initial release

Pin Configuration and Functions

TPM44175
SOT23-6
Top View

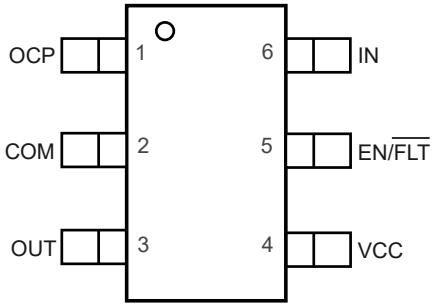


Table 1. Pin Functions: TPM44175

Pin No.	Name	I/O	Description
1	OCP	Input	Current sense input for over-current protection. It can handle a negative voltage input of up to −10 Vdc.
2	COM	Ground	Device Ground
3	OUT	Output	Channel Output, synchronized with the input signal
4	VCC	Power	Power Supply Input
5	EN/$\overline{\text{FLT}}$	I/O	Enable and fault report pin. Enable the device, report fault, and program fault clear time.
6	IN	Power	Input logic, active high.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{CC}	Power Supply Voltage	−0.3	25	V
V_{OUT}	Output Voltage Range OUT	−0.3	V_{CC} + 0.3	V
		−2 (200-ns pulse)	V_{CC} + 2 (200-ns pulse)	V
V_{IN}	Logic Input Voltage Range	−10	V_{CC} + 0.3	V
V_{OCP}	Voltage at Current Sense Pin (OCP)	−10	25	V
$V_{EN/\overline{FLT}}$	Voltage at Enable and Fault Reporting Pin (EN/$\overline{FLT}$)	−0.3	V_{CC} + 0.3	V
I_{OUT}	Continuous Output Channel Current OUT	−300	300	mA
	Pulsed Output Channel Current OUT (500 ns)	−2.6	2.6	A
T_J	Operating Junction Temperature Range	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 300 mV beyond the power supply, the input current should be limited to less than 10 mA.
(3) Power dissipation and thermal limits must be observed.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Value	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
V_{CC}	Power Supply Voltage	12.7	20	V
V_{IN}	Input Voltage Range	−5	VCC	V
V_{OCP}	Sense Pin Voltage	−5	VCC	V
$V_{EN/\overline{FLT}}$	Enable and Fault Reporting Voltage	0	VCC	V
V_{OUT}	Output Voltage Range	0	VCC	V
T_A	Operating Ambient Temperature Range	–40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{Jb}	$\theta_{JC\text{-}top}$	Unit
SOT23-6	143.6	32.6	64.8	°C/W

Electrical Characteristics

All test conditions: V_{CC} = 15 V, T_J = −40 °C – 150 °C, 1-µF capacitor between VCC and GND, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
V_{CCUV+}	VCC Supply Under-voltage Lockout Rising Threshold		11.2	12	12.7	V
V_{CCUV-}	VCC Supply Under-voltage Lockout Falling Threshold		10	11	11.8	V
$V_{CCUVHys}$	VCC Supply Under-voltage Lockout Hysteresis			1		V
V_{INL}	Logic Input Low Voltage (OUT = LO)	T_A = −40℃ to +125℃	0.8	1.0	1.8	V
V_{INH}	Logic Input High Voltage (OUT = HI)	T_A = −40℃ to +125℃	1.9	2.1	3	V
V_{ENL}	EN Input Low Disable Voltage	T_A = −40℃ to +125℃	0.8	1.0	1.2	V
V_{ENH}	EN Input High Enable Voltage	T_A = −40℃ to +125℃	1.8	2.1	2.4	V
V_{OH}	High-level Output Voltage, VCC − VOUT	I_{OUT} = 2 mA		0.02	0.1	V
V_{OL}	Low-level Output Voltage, VOUT	I_{OUT} = 2 mA		0.02	0.1	V
V_{OCTH}	Current Limit Threshold Voltage	V_{OCP} pulse = −0.5 V (−246 mV threshold), TPM44175, T_A = 25°C	−265	−250	−235	mV
		V_{OCP} pulse = −0.25 V (−125 mV threshold), TPM441750, T_A = 25°C		−125		mV
		V_{OCP} pulse = −0.120 V (−60 mV threshold), TPM441751, T_A = 25°C		−60		mV
		V_{OCP} pulse = −1 V (−500 mV threshold), TPM441752, T_A = 25°C	−480	−500	−528	mV
V_{ACTSD}	Active Shut Down Voltage	V_{CC} = open, I_{OUT} = 0.1A, T_A = 25°C		2	2.3	V
I_{IN+}	Input Bias Current, IN = H	V_{IN} = 5 V	35	55	70	µA
I_{IN-}	Input Bias Current, IN = L	V_{IN} = 0 V	−1	−0.5		µA
I_{QCC}	Quiescent VCC Supply Current	V_{IN} = 0 V or 5 V		450	680	µA
I_{O+}	Output Sourcing Short Circuit Pulsed Current	V_{OUT} = 0 V, t_{PW} ≤ 2 µs		4.2		A
I_{O-}	Output Sinking Short Circuit Pulsed Current	V_{OUT} = 15 V, t_{PW} ≤ 2 µs		2.6		A
$I_{\overline{FLT}}$	EN/$\overline{FLT}$ Pull-down Sinking Current	$V_{EN/\overline{FLT}}$ = 0.4 V, T_A = 25°C	30			mA

Parameter		Conditions	Min	Typ	Max	Unit
t_{ON}	Turn-On Propagation Delay	V_{IN} pulse = 5 V		15	30	ns
t_{OFF}	Turn-Off Propagation Delay	V_{IN} pulse = 5 V		15	30	ns
t_R	Turn-On Rise Time	V_{IN} pulse = 5 V		5		ns
t_F	Turn-Off Fall Time	V_{IN} pulse = 5 V		5		ns
t_{DISA}	Disable Propagation Delay	V_{IN} pulse = 5 V		15	30	ns
t_{OCPDEL}	Over-Current Protection Propagation Delay	R_{EN} = 10 kΩ to VCC, V_{OCP} pulse = −0.5 V (−250-mV threshold)		230	350	ns
t_{OCPFLT}	Over-Current Protection to Low-level EN/$\overline{FLT}$ Signal Delay	R_{EN} = 10 kΩ to VCC, V_{OCP} pulse = −0.5 V (−250-mV threshold)		220	320	ns
t_{FLTC}	FAULT Clear Time	VDD = 3.3 V, R_{FLTC} = 1 MΩ to VDD, C_{FLTC} = 240 pF to COM	210	240	265	µs
t_{BLK}	Over-Current Protection Blanking Time	R_{FLT} = 0 Ω, C_{FLT} = NC, V_{OCP} pulse = −0.5 V (−250-mV threshold)		250		ns
t_{VCCUV}	VCC Supply UVLO Filter Time	V_{OCP} pulse = −0.5 V (−250-mV threshold)		4		µs

Typical Performance Characteristics

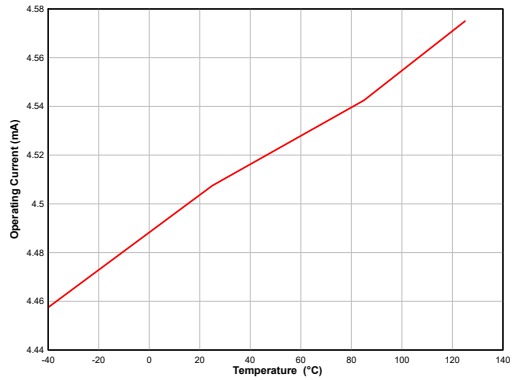
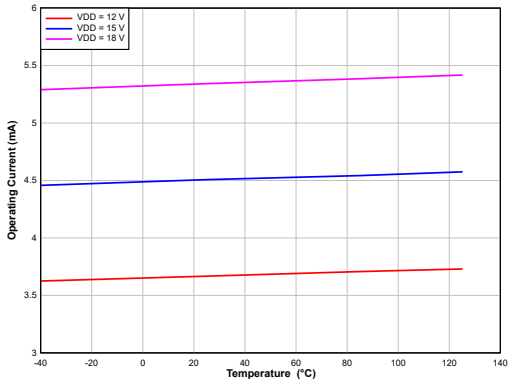
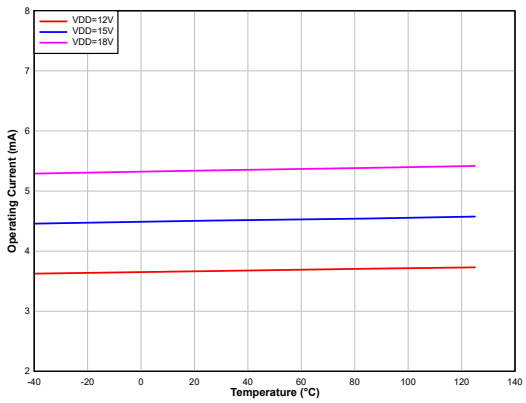


Figure 1. Supply Current vs. Temperature



f = 500 kHz, C_L = 500 pF, VCC = 15 V

Figure 2. Operating Current vs. Ambient Temperature



f = 500 kHz, C_L = 500 pF

Figure 3. Operating Current vs. Temperature

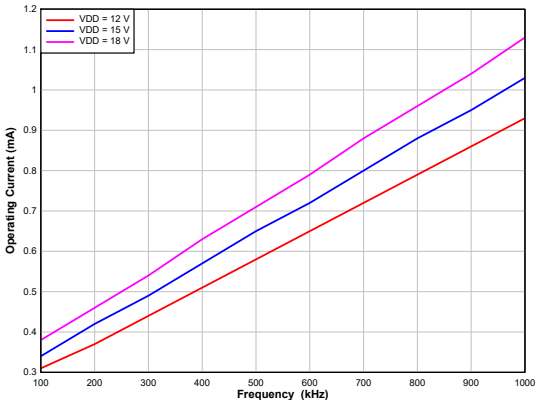


Figure 4. Operating Supply Current vs. Frequency

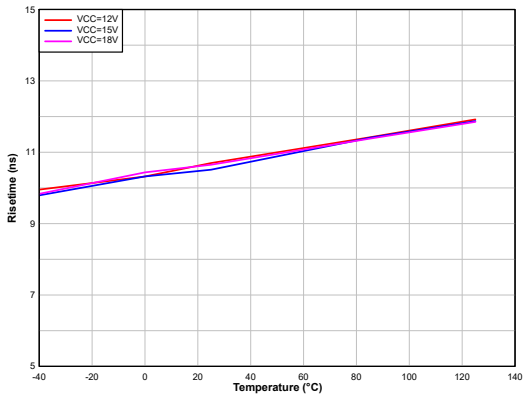


Figure 5. Rise-time vs. Temperature

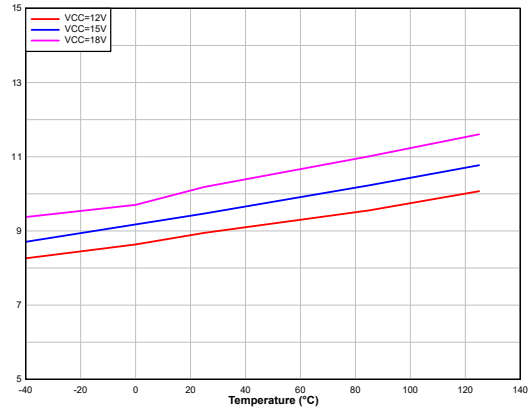
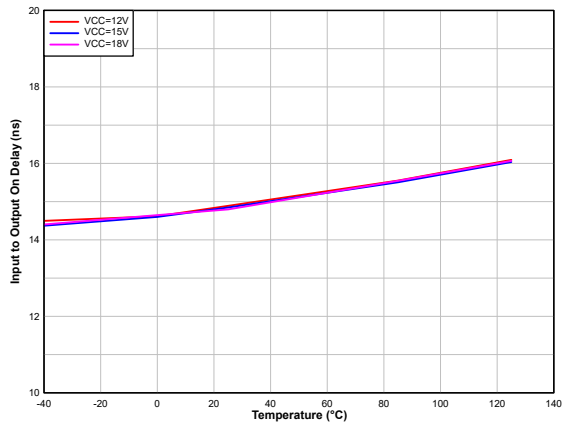
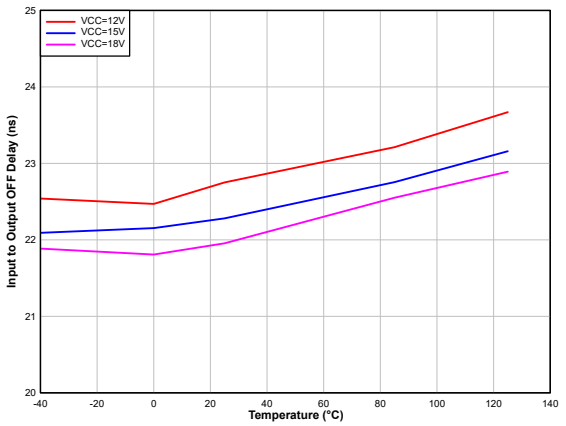


Figure 6. Fall-time vs. Temperature



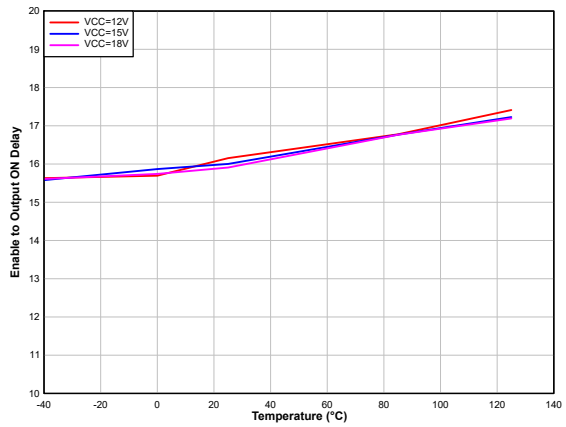
Rising Edge

Figure 7. Input to Output Propagation Delay vs. Temperature



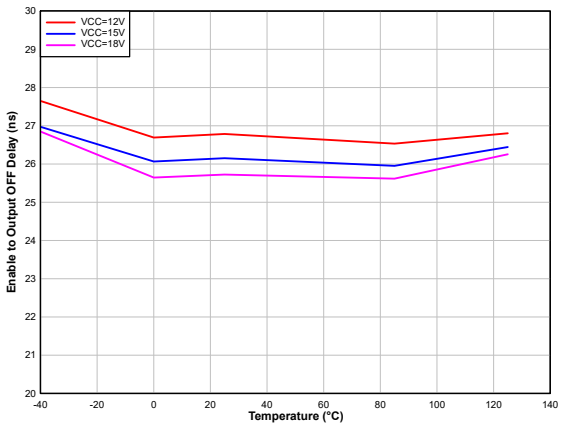
Falling Edge

Figure 8. Input to Output Propagation Delay vs. Temperature



Rising Edge

Figure 9. Enable to Output Propagation Delay vs. Temperature



Falling Edge

Figure 10. Enable to Output Propagation Delay vs. Temperature

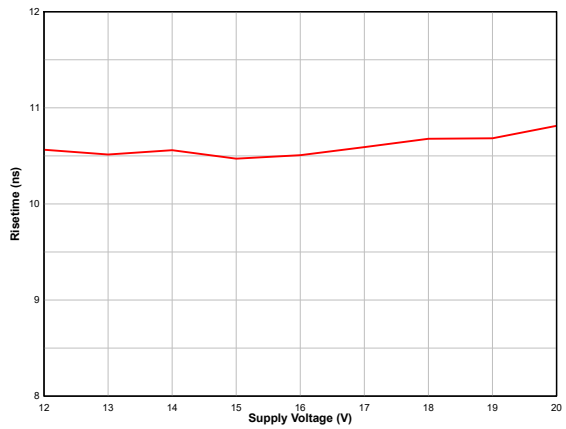


Figure 11. Rise-time vs. Supply Voltage

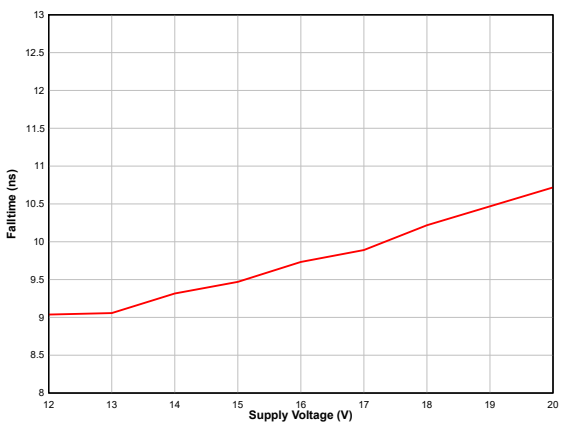


Figure 12. Fall-time vs. Supply Voltage

Detailed Description

Overview

The TPM44175x is a family of single-channel low-side IGBT gate drivers designed for applications requiring over-current protection. The device is compatible with standard CMOS or LSTTL logic inputs and provides a gate driver stage for MOSFET/IGBT/SiC. Key features include over-current detection with a negative voltage input, programmable fault clear time, under voltage lockout protection, and a fault output status pin. It supports a wide range of input logic levels (3.3 V, 5 V, and 15 V) and offers a maximum supply voltage of 25 V. The device family offers multiple options for over-current protection (OCP) threshold levels, including −500 mV, −246 mV, −125 mV, and −60 mV, providing flexibility to suit different application requirements. The device is suitable for use in home appliances, such as air conditioners, and industrial applications where reliable low-side gate driving is required.

Functional Block Diagram

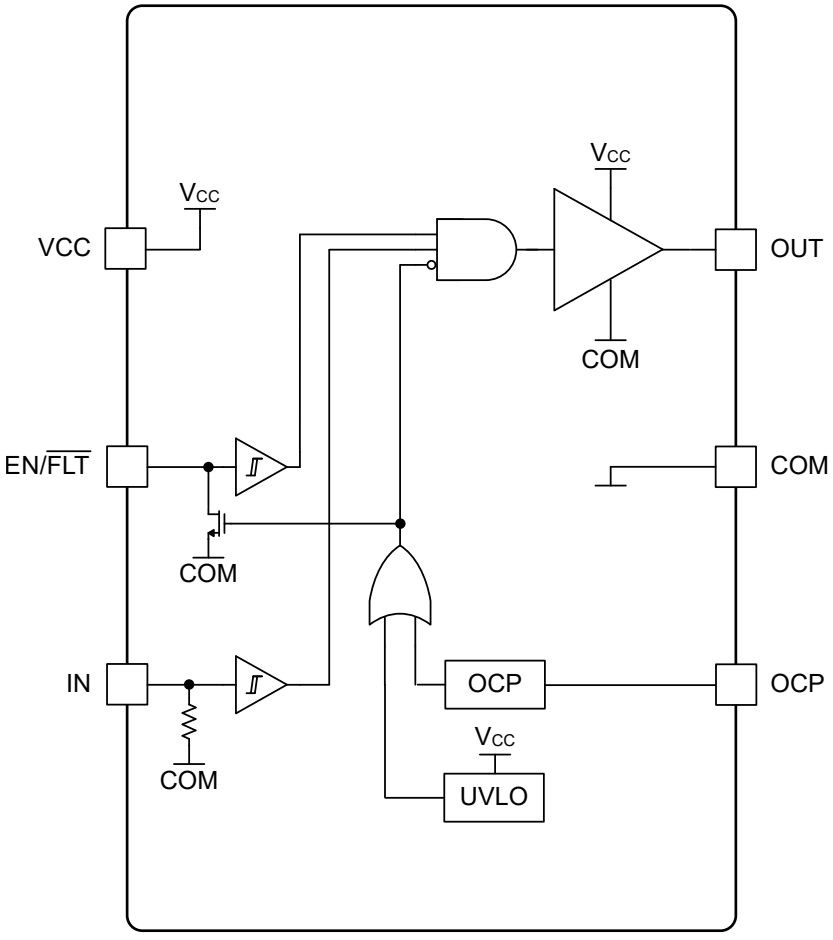


Figure 13. Functional Block Diagram

Feature Description

Low Propagation Delay Driver Output

The output driver of the TPM44175 is designed to provide a robust and reliable gate drive signal for IGBTs. It features a current buffer stage that ensures sufficient drive current for the IGBT gate, enabling efficient switching performance. The output is in phase with the input, ensuring that the gate drive signal accurately follows the input control signal. The output driver also includes over-current protection, which helps prevent damage to the IGBT in case of a short circuit or other over-current events.

Supply and UVLO

The device monitors supply voltage with under-voltage lock-out (UVLO). When the supply voltage falls below the UVLO threshold, the output is held low, and the EN/$\overline{FLT}$ pin is pulled down to indicate a fault condition. This ensures reliable operation and prevents potential damage to the IGBT due to insufficient supply voltage.

The quiescent current and operating current of the device are measured as shown in Figure 4. The current is related to internal quiescent current consumption as well as output current. The output current can be calculated using the external transistor gate charge times switching frequency f_{sw}.

Over Current Protection

The TPM44175 incorporates a robust overcurrent protection (OCP) feature designed to safeguard the power transistor, IGBT for example, from overcurrent conditions. The OCP function is triggered when the voltage at the OCP pin exceeds a predefined threshold, indicating an overcurrent event. Upon detection, the device initiates a fault shutdown sequence, which includes pulling down the EN/$\overline{FLT}$ pin to indicate a fault condition and immediately disabling the gate output to prevent potential damage to the IGBT. The OCP also includes a blanking time to avoid false triggering due to transient currents during IGBT turn-on, ensuring reliable operation in noisy environments. The fault condition remains active until the overcurrent event is resolved and the internal fault clear timer has expired, after which the device can resume normal operation. This comprehensive OCP mechanism ensures reliable and safe operation of the IGBT in various applications.

The device family has multiple options for OCP threshold as the table shown below.

Table 2. OCP Threshold

Part Number	OCP Threshold (mV)
TPM44175	−246
TPM441750	−125
TPM441751	−60
TPM441752	−500

Enable and Fault Reporting

The EN/$\overline{FLT}$ pin of the TPM44175 serves a dual function, providing both enable and fault reporting capabilities. When the EN/$\overline{FLT}$ pin is pulled high, the device is enabled, and the output can operate normally. Pulling the EN/$\overline{FLT}$ pin low disables the output, effectively shutting down the gate driver. Additionally, the EN/$\overline{FLT}$ pin acts as a fault reporting pin. In the event of a fault condition, such as under-voltage lockout (UVLO) or overcurrent protection (OCP) being triggered, the EN/$\overline{FLT}$ pin is internally pulled down to indicate the fault. The pin remains in the low state until the fault condition is resolved and the internal fault clear timer has expired. This dual functionality allows for precise control and monitoring of the device's status, ensuring reliable operation and facilitating system diagnostics.

Channel Input

The TPM44175 features a CMOS Schmitt-triggered input that is compatible with standard CMOS or LSTTL outputs, ensuring seamless integration with a wide range of digital control systems. The input logic is designed to be compatible with 3.3 V, 5 V, and 15 V logic-level signals, providing flexibility for various applications. The input hysteresis enhances noise immunity, making the device suitable for noisy industrial environments. Additionally, the input pin is internally pulled down to GND, ensuring that the output remains in a low state when the input is floating, preventing unintended operation.

The input can withstand negative DC voltage up to −10V, to improve robustness on ground bouncing.

Table 3. Input/Output Logic Truth Table

IN	EN/FLT	UVLO	OCP	OUT	Description
L	H	VCC > UVLO	L	L	Normal operation, output is low
H	H	VCC > UVLO	L	H	Normal operation, output is high
X	L	VCC > UVLO	X	L	EN/FLT pin pulled low, output is disabled
X	Internally pulled down	VCC < UVLO	X	L	Under-voltage lockout (UVLO) active, output is low
X	Internally pulled down	VCC > UVLO	H	L	Overcurrent protection (OCP) active, output is low

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Typical Application

Figure 14 shows the typical application schematic.

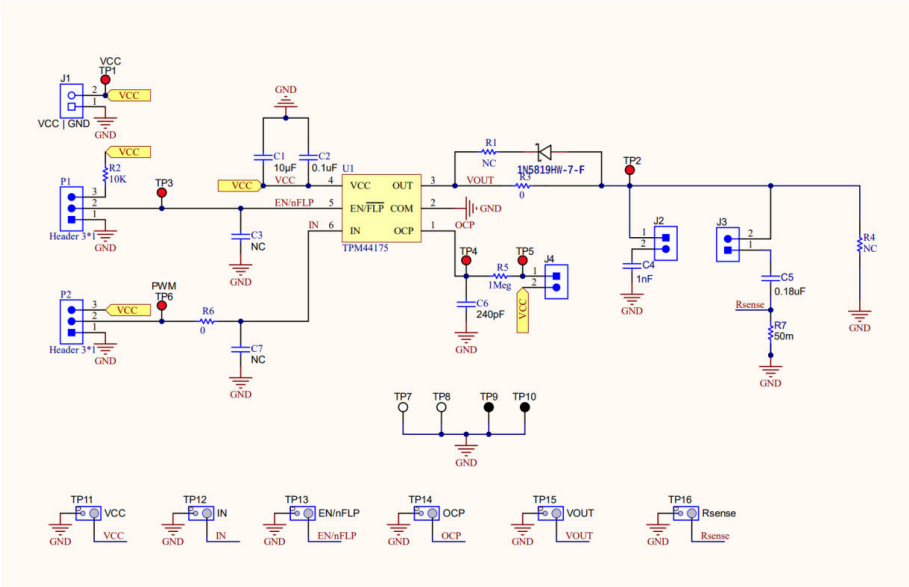


Figure 14. Application Circuit

Table 4. Bill of Material

Comment	Description	Designator	Footprint	LibRef	Quantity
10μF, 50 V,0805	10 μF, 50 V,0805	C1	0805R	C0805C103F1GA CT U	1
0.1uF/50V/0603	0.1 μF/50V/0603	C2	0603RC	Cap	1
NC	NC	C3, C7, R1, R4	0603RC	Cap, Res3	4
NC	NC	C4	0805R	C0805C103F1GA CT U	1
0.18uF/50V/0805	0.18 μF/50V/0805	C5	0805R	C0805C103F1GA CT U	1
240pF	240 pF	C6	0603RC	Cap	1
1N5819HW- 7- F		D1	SOD- 123_L2.8- W1.8- LS3.7- FD	1N5819HW- 7- F	1
VCC | GND	Terminal Block,	J1	TEC_282841- 2	282841- 1	1

Comment	Description	Designator	Footprint	LibRef	Quantity
	2.54 mm, 2x1, Brass, TH				
	Header, 100mil, 2x1, Gold, TH	J2, J3, J4	Header, 100mil, 2x1, Gold, TH	HTSW- 102- 07- G- S_1	3
Header 3*1		P1, P2	Header, 100mil, 3x1, Gold, TH	Header 3*1	2
10K	10 K, 0603	R2	0603RC	Res3	1
0	0, 0603, 0	R3, R6	0603RC	Res3	2
1Meg	1 Meg, 0603	R5	0603RC	Res3	1
50mΩ/0805	50 mΩ/0805	R7	0805R	Res1	1
VCC	Test Point, Compact, Red, TH	TP1	Keystone5005/red	Keystone5005	1
VOUT	Test Point, Compact, Red, TH	TP2	Keystone5005/red	Keystone5005	1
EN/nFLP	Test Point, Compact, Red, TH	TP3	Keystone5005/red	Keystone5005	1
PWM	Test Point, Compact, Red, TH	TP4, TP5, TP6	Keystone5005/red	Keystone5005	3
	Test Point, Miniature, SMT	TP7, TP8	Keystone5015	5015	2
GND	Test Point, Compact, Black, TH	TP9, TP10	Keystone5005/ black	Keystone5006	2
VCC		TP11	TP_PIGTAIL	PIGTAIL	1
IN		TP12	TP_PIGTAIL	PIGTAIL	1
EN/nFLP		TP13	TP_PIGTAIL	PIGTAIL	1
OCP		TP14	TP_PIGTAIL	PIGTAIL	1
VOUT		TP15	TP_PIGTAIL	PIGTAIL	1
Rsense		TP16	TP_PIGTAIL	PIGTAIL	1
TPM44175		U1	SOT- 23- 6_L2.9W1.6- P0.95- LS2.8BR	TPM44175	1

Layout

Layout Example

Figures below show the location of external components as they appear on the PCB diagram.

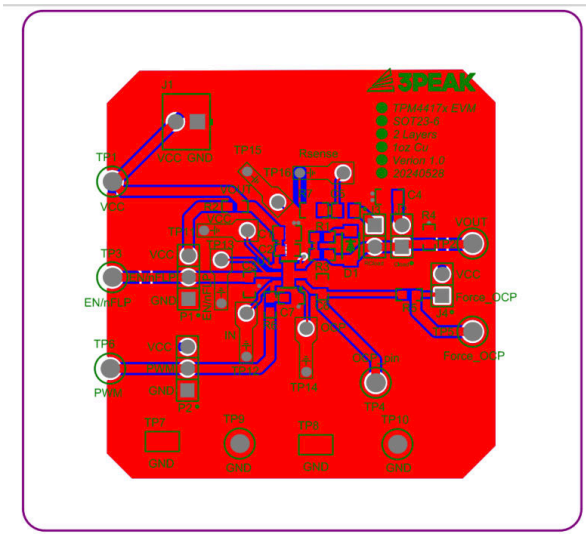


Figure 15. Top Layer

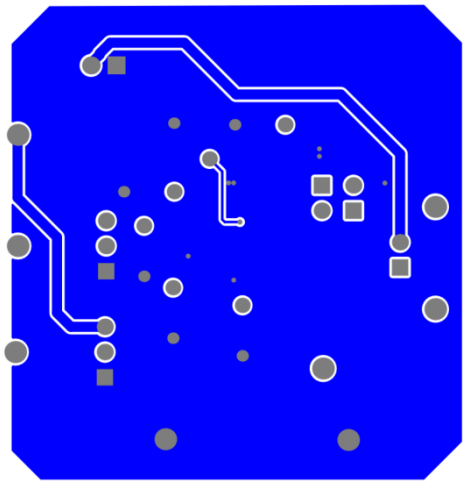
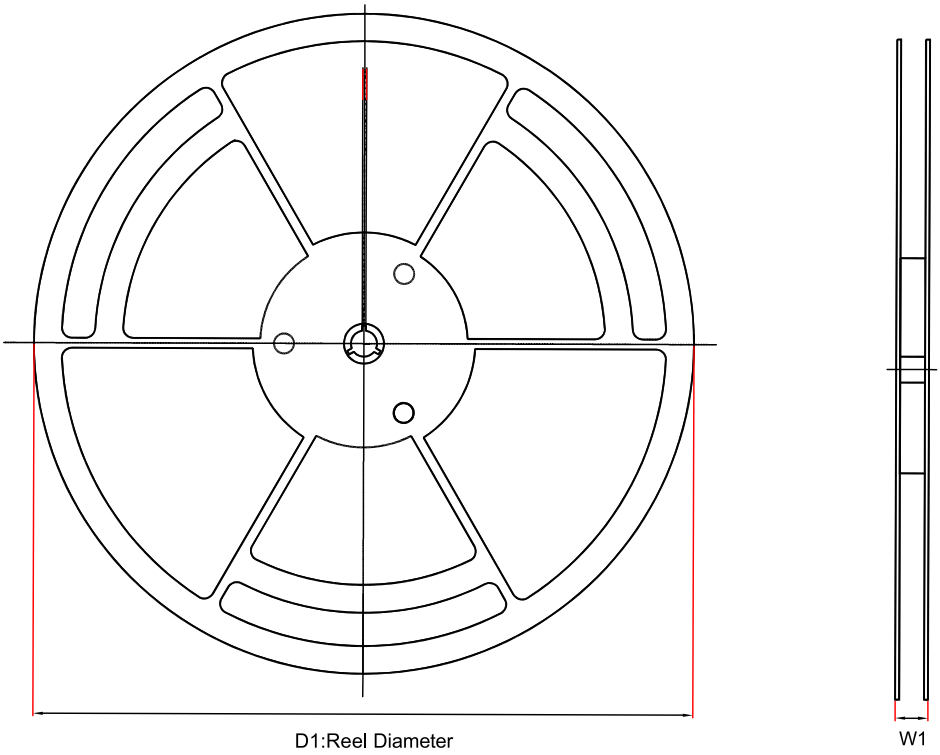
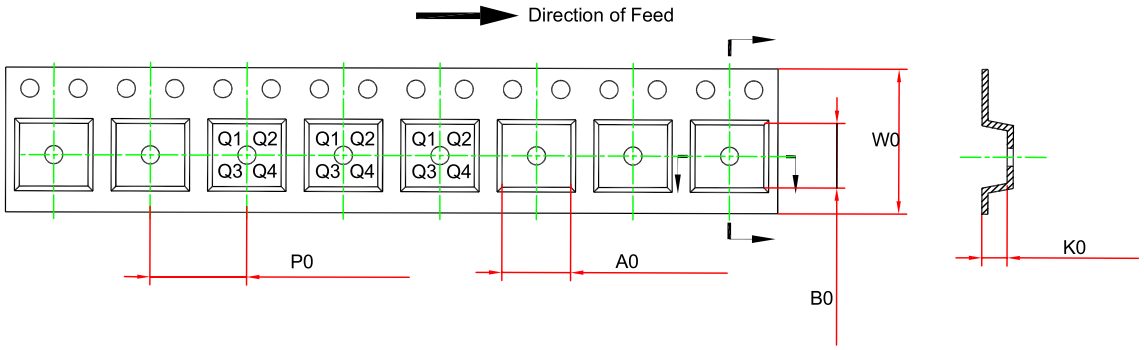


Figure 16. Bottom Layer

Tape and Reel Information



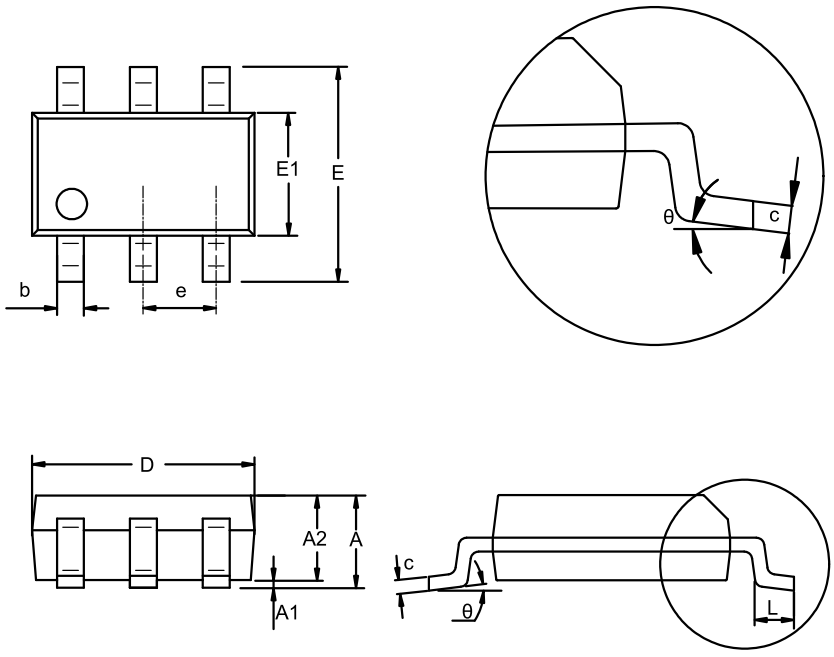


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM44175-S6TR	SOT23-6	180	12	3.3	3.2	1.4	4	8	Q3
TPM441750-S6TR	SOT23-6	180	12	3.3	3.2	1.4	4	8	Q3
TPM441751-S6TR	SOT23-6	180	12	3.3	3.2	1.4	4	8	Q3
TPM441752-S6TR	SOT23-6	180	12	3.3	3.2	1.4	4	8	Q3

Package Outline Dimensions

SOT23-6

Package Outline Dimensions S6T(SOT23-6-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.280	0.500	0.011	0.020
c	0.100	0.230	0.004	0.009
D	2.820	3.020	0.111	0.119
E	2.600	3.000	0.102	0.118
E1	1.500	1.720	0.059	0.068
e	0.950 BSC		0.037 BSC	
L	0.300	0.600	0.012	0.024
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.

Order Information

Order Number	Operating Ambient Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPM44175-S6TR	−40℃ to 125°C (1)	SOT23-6	475	MSL1	Tape and Reel,3000	Green
TPM441750-S6TR (2)	−40°C to 125°C (1)	SOT23-6	470	MSL1	Tape and Reel,3000	Green
TPM441751-S6TR (2)	−40°C to 125°C (1)	SOT23-6	471	MSL1	Tape and Reel,3000	Green
TPM441752-S6TR (2)	−40°C to 125°C (1)	SOT23-6	472	MSL1	Tape and Reel,3000	Green

(1) Ambient temperature indicates the device operation condition range. Application thermal behavior needs to be taken care of when operating in high-temperature scenarios.
(2) Contact 3PEAK representatives for more details.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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