Single Channel 5-A High-speed, Low-side Gate Driver

Features

- Industry-standard Pin Configuration
- 10-V to 40-V Single-Supply Range
- 5-A Peak Source and Sink-drive Current
- Inverting and noninverting inputs capable of with standing up to –5-V DC below ground
- TTL and CMOS Compatible Threshold
- Outputs Held Low during VDD-UVLO or Input Floating
- Low Propagation Delay (20-ns Typical)
- Fast Rise-and-fall Times (14-ns and 10-ns Typical)
- ESD Protection Exceeds JESD 22 – 6-kV HBM, 1.5-kV CDM
- Available in SOT23-5 Package

Applications

- Switched-mode Power Supplies
- DC-DC Converters
- Motor Control, Solar Inverters
- Gate & IGBT Drive

Description

The TPM27533 is a single-channel low-side gate driver for MOSFET, IGBT, and SiC power switches.

The TPM27533 family consists of single-channel, high-speed gate drivers designed for effective MOSFET, IGBT, and SiC power switch control. These drivers support up to 4.5 A sourcing and 5 A sinking through asymmetrical drive, with rail-to-rail capability and an ultra-fast propagation delay of 20 ns (typical). They are versatile, supporting enable, dual input, and inverting/non-inverting modes. The strong asymmetrical drive enhancesimmunity against parasitic Miller turn-on effects and helps reduce ground debouncing. Ideal for various applications, the TPM27533 gate drivers offer efficient and precise control of power switches.

Typical Application Circuit

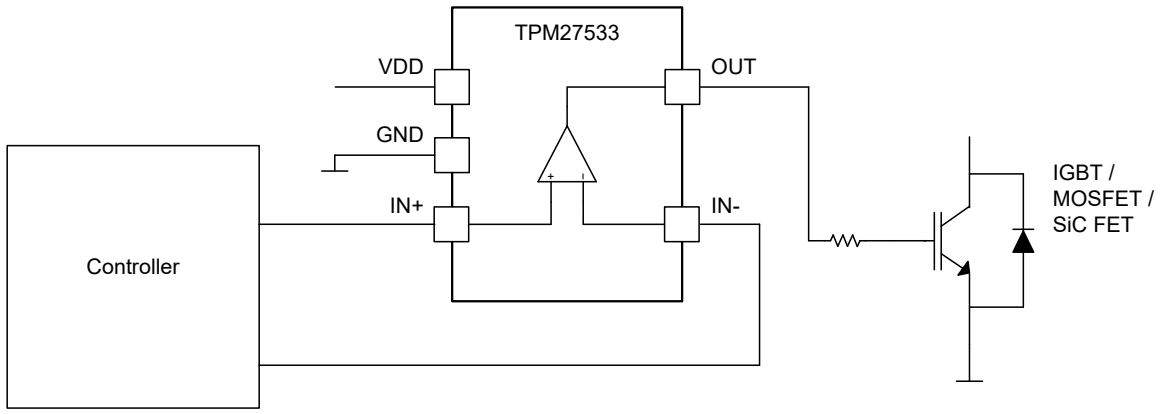


Table of Contents

Revision History

Date	Revision	Notes
2024-01-18	Rev A.0	Initial revision

Pin Configuration and Functions

TPM27533
SOT23-5
Top View

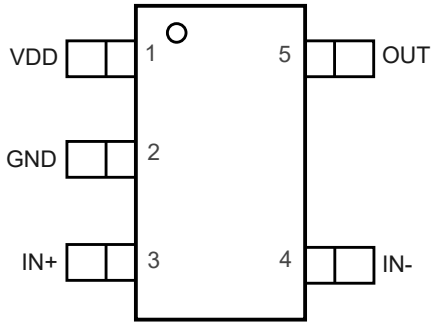


Table 1. Pin Functions: TPM27533

Pin	Name	I/O	Description
1	VDD	Power	Power Supply Input
2	GND	Ground	Device ground
3	IN+	Input	Logic non-inverting input. Internal resistor pulled down to ground.
4	IN-	Input	Logic inverting input. Internal resistor pulled up to the internal regulator.
5	OUT	Output	4.5-A Source, 5-A Sink Output

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
	Power Supply Voltage, VDD	–0.3	40	V
	Output Voltage Range OUT	–0.3	VDD + 0.3	V
		–2	VDD + 0.3 (200-ns pulse)	
	Input Voltage Range IN+, IN–	–5	27	V
	Continuous Output Channel Current	–300	300	mA
	Pulsed Output Channel Current (500 ns)	–5	5	A
	Operating Junction Temperature Range	–40	150	°C
T_{STG}	Storage Temperature Range	–65	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 300 mV beyond the power supply, the input current should be limited to less than 10 mA.
(3) Power dissipation and thermal limits must be observed.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±6	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter	Min	Max	Unit
Power Supply Voltage, VDD	10	36	V
Input Voltage Range IN+, IN-	−5	25	V
Operating Ambient Temperature Range	−40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOT23-5	89.1	52.0	°C/W

Electrical Characteristics

All test conditions: V_{DD} = 18 V, T_J = −40 °C to 150 °C, and 1-µF capacitor between V_{DD} and GND, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
$I_{DD(off)}$	Start-up Current	VDD = 7.0, IN+= GND， IN−-= VDD	100	200	300	µA
		VDD = 7.0, IN+= VDD， IN−= GND	100	217	300	
V_{ON}	Supply Under Voltage Lock Out Rising Threshold		8	8.9	9.8	V
V_{OFF}	Supply Under Voltage Lock Out Falling Threshold		7.3	8.3	9.1	V
V_{DD_H}	Supply Under Voltage Lock Out Hysteresis			0.6		V
V_{IN_H}	Input Signal High Threshold, IN+, IN-	Input high threshold, Output high for IN+; Output low for IN−	1.6	1.75	2	V
V_{IN_L}	Input Signal Low Threshold, IN+, IN-	Input low threshold, Output low for IN+; Output high for IN−	1	1.25	1.4	V
V_{IN_HYS}	Input Hysteresis			0.5		V
I_{OUT_SRC}	Output Peak Source Current	C_{LOAD} = 0.22 µF, F_{SW} = 1 kHz		5		A
I_{OUT_SINK}	Output Peak Sink Current	C_{LOAD} = 0.22 µF, F_{SW} = 1 kHz		8		A
V_{DD} – V_{OH}	Output High Voltage	I_{OUT} = −10 mA	60		200	mV
V_{OL}	Output Low Voltage	I_{OUT} = 100 mA	40		125	mV
R_{OH}	Output Pull-up Resistance, PMOS Pull-up only	I_{OUT} = −10 mA	6		20	Ω
R_{OL}	Output Pull-down Resistance	I_{OUT} = 100 mA	0.4		1.25	Ω
t_R	Output Rise-time	C_{LOAD} = 1.8 nF		15		ns
t_F	Output Fall-time	C_{LOAD} = 1.8 nF		7		ns
t_{PW}(1)	Minimal Pulse Width			15	25	ns
t_{UVLO_rec}	UVLO Recovery time		1	4.2	8	µs
t_{D1}	Input to Output Propagation Delay	C_{LOAD} = 1.8 nF, 5-V IN+ pulse to output rising edge delay		20		ns
t_{D2}	Input to Output Propagation Delay	C_{LOAD} = 1.8 nF, 5-V IN+ pulse to output falling edge delay		20		ns
t_{D3}	Input to Output Propagation Delay	C_{LOAD} = 1.8 nF, 5-V IN− pulse to output falling edge delay		20		ns
t_{D4}	Input to Output Propagation Delay	C_{LOAD} = 1.8 nF, 5-V IN− pulse to output rising edge delay		20		ns
T_{OTP}	Thermal protection threshold			165		°C

(1) Guaranteed by design

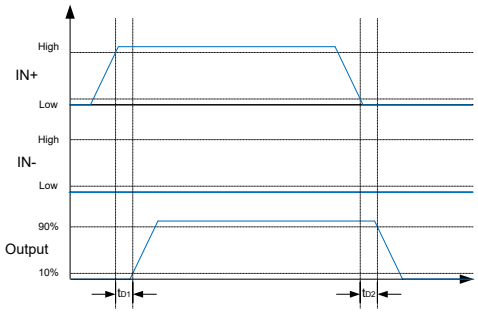


Figure 1. IN+ Timing Diagram

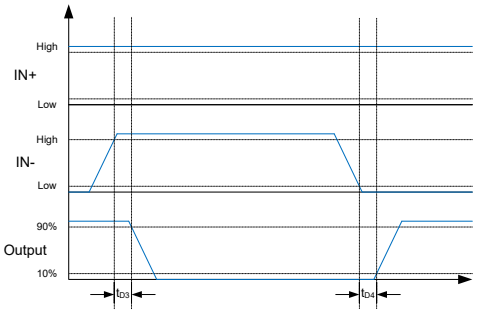


Figure 2. IN− Timing Diagram

Typical Performance Characteristics

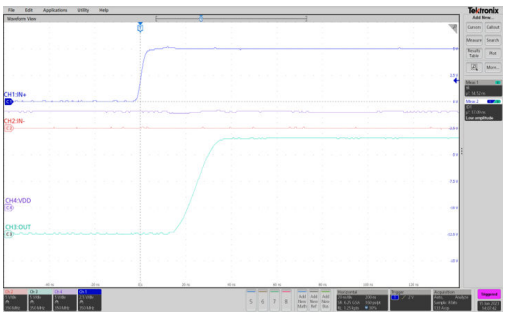


Figure 3. Rising Edge via IN+

V_{DD} = 18 V

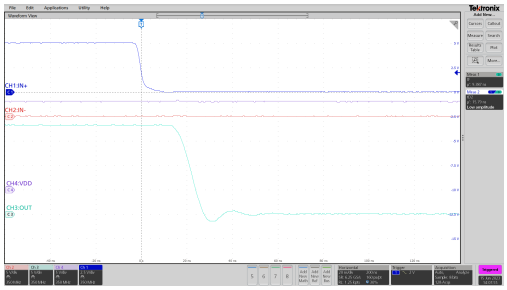


Figure 4. Falling Edge via IN+

V_{DD} = 18 V

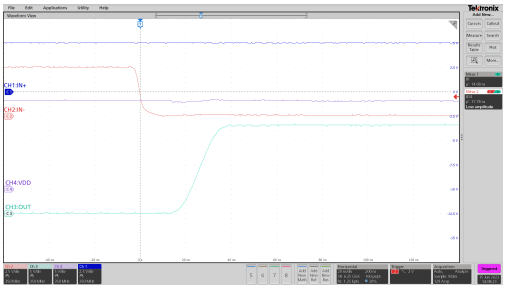


Figure 5. Rising Edge via IN−

V_{DD} = 18 V

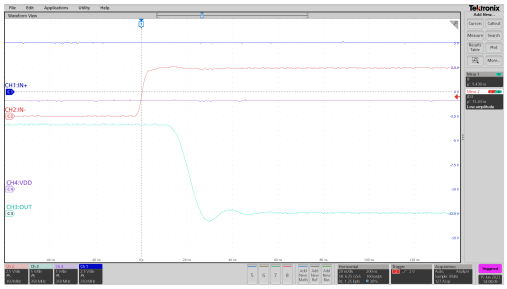


Figure 6. Falling Edge via IN−

V_{DD} = 18 V

Detailed Description

Overview

The TPM27533 family comprises single-channel, high-speed gate drivers designed to effectively drive MOSFET, IGBT, and SiC power switches with peak currents of up to 4.5 A for sourcing and 5 A for sinking. The strong sink capability in the asymmetrical drive enhances immunity against parasitic Miller turn-on effects. The device offers rail-to-rail drive capability and features an extremely small propagation delay, typically 20 ns, ensuring a rapid response. The input threshold is based on low-voltage TTL and CMOS-compatible logic, fixed and independent of the VDD supply voltage, with a 0.6-V typical hysteresis that provides excellent noise immunity.

Functional Block Diagram

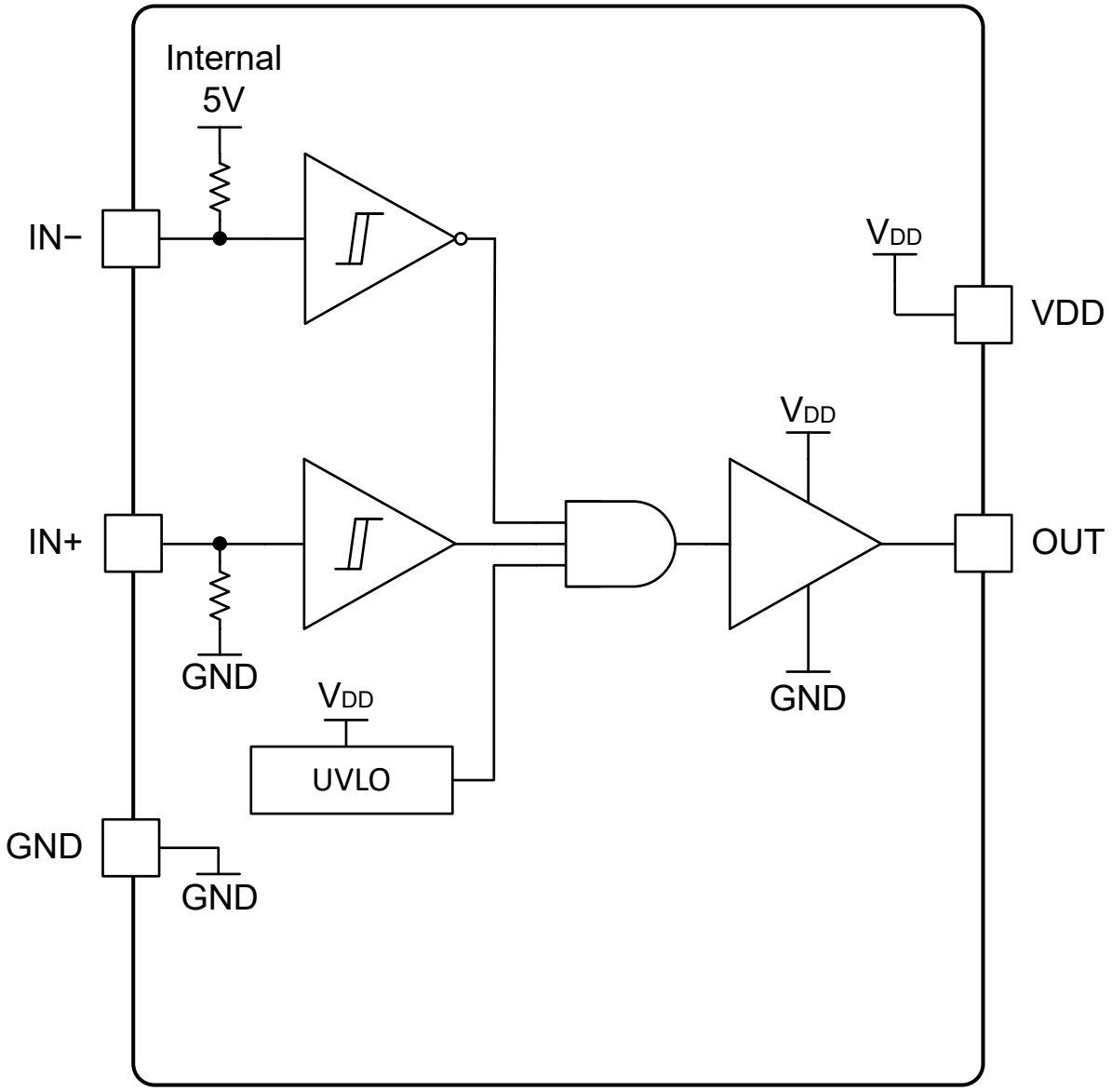


Figure 7. Functional Block Diagram

Feature Description

Supply and UVLO

The TPM27533 device has an internal UVLO protection feature on the VDD pin supply. It prevents the gate driver from operating at low supply voltages, ensuring acceptable power dissipation in the power switch. When in UVLO condition (VDD voltage below VON during power up or VDD voltage below VOFF during power down), all outputs are held LOW, regardless of the inputs. The UVLO threshold is typically 8.9 V with a 600-mV hysteresis, which prevents issues with noise or voltage droops during switching. The device's wide voltage range (10 V to 36 V) offers flexibility to drive various types of power switches, including Si MOSFETs, IGBTs, and emerging SiC FETs.

Channel Input

The device has a safety feature to keep the output low when the input pin is not connected. Use signals with short rise or fall times to avoid issues with slowly changing input signals or long traces. The input threshold hysteresis provides good noise immunity. To reduce EMI, add an external resistor between the driver output and the power device instead of delaying the input signal. Be cautious when dealing with high voltages or fast voltage changes on input or enable pins. In such cases, consider adding a series 150-Ω resistor for safety. The device can also handle negative voltages on inputs as low as -5V.

Output Stage

The TPM27533 device has an output stage design that provides high peak source current during critical turn-on transitions of power switches. It uses a hybrid pull-up structure with N-Channel and P-Channel MOSFETs to enable fast turn-on by briefly turning on the N-Channel MOSFET during state changes.

The device can deliver a 4.5-A source and up to a 5-A sink at VDD = 18 V, offering strong sink capability for low pull-down impedance. This boosts immunity against parasitic Miller turn-on effects in IGBT and FET power switches, especially in synchronous rectification applications.

The driver output swings between VDD and GND, providing rail-to-rail operation due to the low dropout of the output stage. It often eliminates the need for external Schottky diode clamps as the MOSFET body diodes offer low impedance to switching overshoots and undershoots, simplifying the design and enhancing efficiency in various applications.

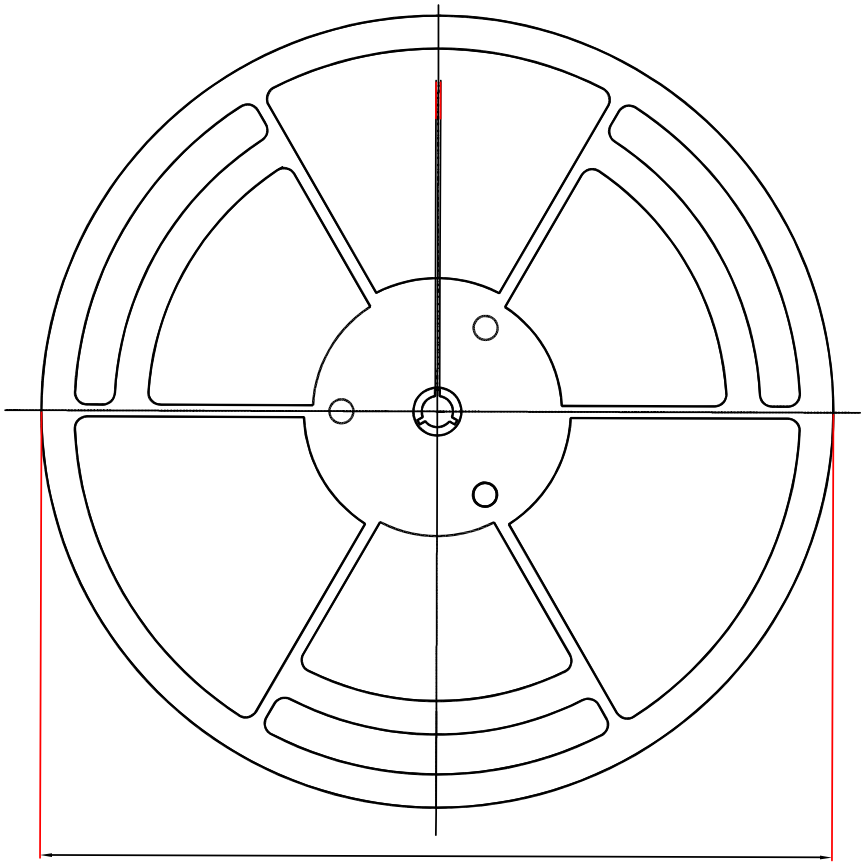
Active Pull-down

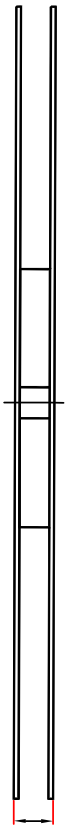
The TPM27533 incorporates an active pulldown feature to safeguard the OUT pin by clamping it to GND when the VDD supply is open. In such situations, the OUT pin is in a high-impedance state. The active pulldown feature prevents the output from being falsely turned on before the device is back under control. By actively pulling down the OUT pin to GND, potential issues caused by open VDD supply are avoided, ensuring the safe and reliable operation of the device.

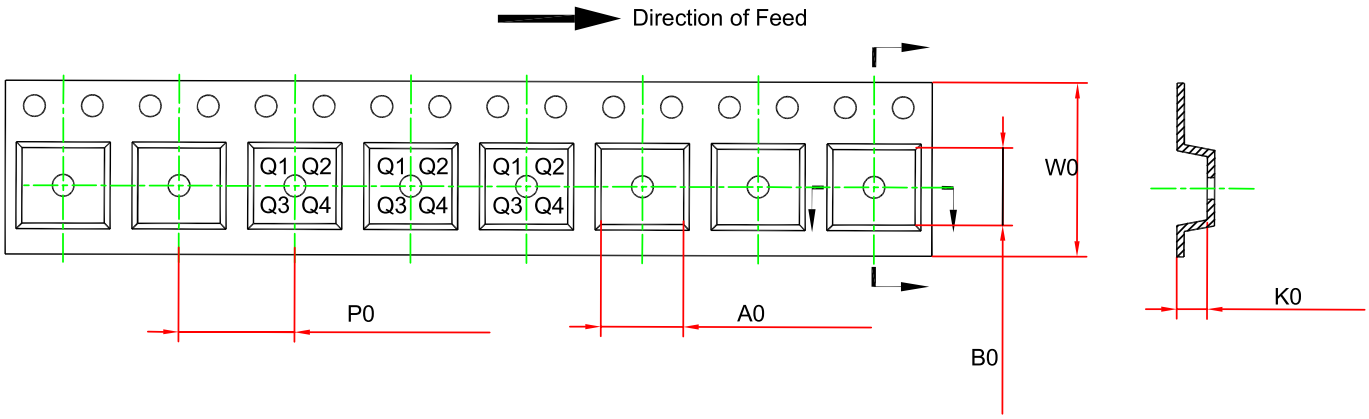
Over Temperature Protection

The TPM27533 incorporates a safeguard mechanism that reduces the output pulse width when the temperature exceeds 165°C. This feature is designed to protect the system from potential driver damage caused by overheating. However, it is essential to take appropriate measures to prevent the device from triggering over-temperature protection in the first place. Proper thermal management and operating within the specified temperature range are important to ensure the reliable and safe performance of the device.

Tape and Reel Information





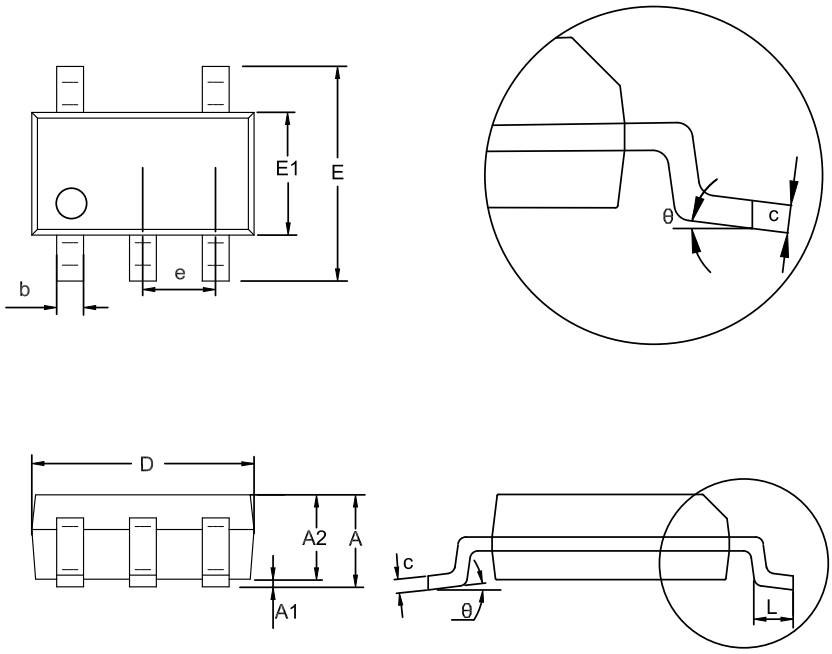


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM27533-S5TR	SOT23-5	180	12	3.3	3.25	1.4	4	8	Q3

Package Outline Dimensions

SOT23-5

Package Outline Dimensions S5T(SOT23-5-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.280	0.500	0.011	0.020
c	0.100	0.230	0.004	0.009
D	2.820	3.020	0.111	0.119
E	2.600	3.000	0.102	0.118
E1	1.500	1.720	0.059	0.068
e	0.950 BSC		0.037 BSC	
L	0.300	0.600	0.012	0.024
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Ambient Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPM27533-S5TR	-40 °C to 125 °C (1)	SOT23-5	533	1	Tape and Reel, 3000	Green

(1) Ambient temperature indicates device operation condition range. Application thermal behavior needs to be taken care of when operating in high-temperature scenarios.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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