
Single-Channel 5-A High-Speed Low-Side Gate Driver**Features**

- Industry-Standard Pin-Out
- 4.5-V to 23-V Single-Supply Range
- Single Channel 5-A Peak Source and Sink-Drive Current
- TTL and CMOS Compatible Threshold
- Outputs Held Low During VDD-UVLO or Input Floating
- Low Propagation Delay (13-ns Typical)
- Fast Rise and Fall Times (7-ns and 6-ns Typical)
- ESD Protection Exceeds JESD 22 – 6-kV HBM, 1.5-kV CDM
- Available in SOT23-5 Package

Applications

- Switched-Mode Power Supplies
- DC-DC Converters
- Motor Control, Solar Inverters, UPS
- Gate & IGBT Drive

Description

The TPM27517 is a single-channel low-side gate-driver for MOSFET, IGBT, and GaN power switches.

The high sourcing and sinking current capability of 5-A improves switching efficiencies by minimizing slew time and switching loss. The device supports a maximum 25-V supply voltage and -5-V input voltage, and improves system robustness, especially in noisy industrial applications. The ultra-low propagation delay allows applications with tight timing requirements.

A small SOT23-5 package assists with the design for high-density power supply.

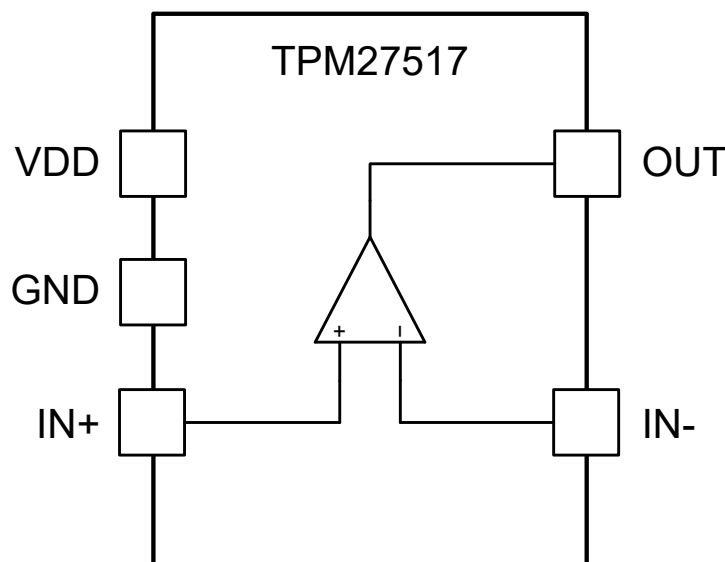
Typical Application Circuit

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Single-Channel 5-A High-Speed Low-Side Gate Driver**Revision History**

| Date | Revision | Notes |
|------------|----------|-----------------------------------|
| 2021-09-08 | Rev.A.0 | Initial released version |
| 2024-10-22 | Rev.A.1 | Updated to a new datasheet format |

Pin Configuration and Functions

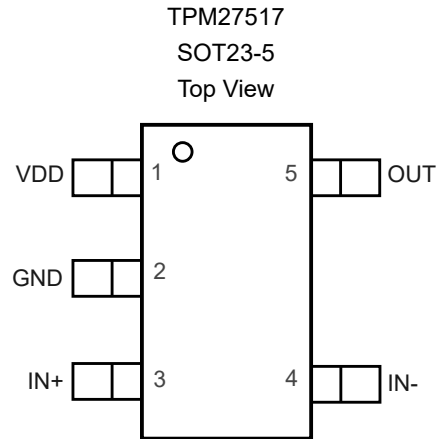


Table 1. Pin Function

| Pin No. | Name | I/O | Description |
|---------|------|--------|--------------------------------|
| 2 | GND | Ground | Ground. |
| 3 | IN+ | I | The logic non-inverting input. |
| 4 | IN- | I | The logic inverting input. |
| 5 | OUT | O | The channel output. |
| 1 | VDD | Power | The power supply input. |

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Specifications

Absolute Maximum Ratings ⁽¹⁾

| Parameter | | Min | Max | Unit |
|------------------|--|------|-----------------------|------|
| V _{DD} | Power Supply Voltage | -0.3 | 25 | V |
| OUT | Output Voltage Range | -0.3 | V _{DD} + 0.3 | V |
| | Output Voltage Range (200-ns Pulse) | -2 | V _{DD} + 0.3 | V |
| IN+, IN- | Input Voltage Range | -5 | 20 | V |
| | Continuous Output Channel Current OUT | -300 | 300 | mA |
| | Pulsed Output Channel Current OUT (500 ns) | -5 | 5 | A |
| T _J | Maximum Operating Junction Temperature | -40 | 150 | °C |
| T _{STG} | Storage Temperature Range | -65 | 150 | °C |
| T _L | Lead Temperature (Soldering, 10 sec) | | 260 | °C |

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
- (2) The inputs are protected by ESD-protection diodes to each power supply. If the input extends more than 300 mV beyond the power supply, the input current should be limited to less than 10 mA.
- (3) The power dissipation and thermal limits must be observed.

ESD, Electrostatic Discharge Protection

| Symbol | Parameter | Condition | Minimum Level | Unit |
|--------|--------------------------|---------------------------------------|---------------|------|
| HBM | Human Body Model ESD | ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±6 | kV |
| CDM | Charged Device Model ESD | ANSI/ESDA/JEDEC JS-002 ⁽²⁾ | ±1.5 | kV |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

| Parameter | | Min | Typ | Max | Unit |
|-----------------|-------------------------------------|-----|-----|-----|------|
| V _{DD} | Power Supply Voltage | 4.5 | | 23 | V |
| IN+, IN- | Input Voltage Range | 0 | | 20 | V |
| | Operating Ambient Temperature Range | -40 | | 125 | °C |

Thermal Information

| Package Type | θ _{JA} | θ _{Jc} | Unit |
|--------------|-----------------|-----------------|------|
| SOT23-5 | 89.1 | 52.0 | °C/W |

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Electrical Characteristics

All test conditions: $V_{DD} = 12\text{ V}$, $T_J = -40^\circ\text{C}$ to 150°C , $1\text{-}\mu\text{F}$ capacitor between V_{DD} and GND, unless otherwise noted.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|---|---|------|---------|------|---------------|
| $I_{DD(\text{off})}$ | Start-up Current | $V_{DD} = 3.4\text{ V}$, $\text{IN+} = \text{H}$, $\text{IN-} = \text{L}$ | | 40 | 100 | μA |
| | | $V_{DD} = 3.4\text{ V}$, $\text{IN+} = \text{L}$, $\text{IN-} = \text{H}$ | | 40 | 100 | |
| V_{ON} | Supply under Voltage Lock-out Rising Threshold | $T_J = 25^\circ\text{C}$ | 3.91 | 4.2 | 4.5 | V |
| | | $T_J = -40^\circ\text{C}$ to 150°C | 3.7 | 4.2 | 4.65 | |
| V_{OFF} | Supply under Voltage Lock-out Falling Threshold | $T_J = -40^\circ\text{C}$ to 150°C | 3.4 | 3.9 | 4.4 | V |
| V_{DD_H} | Supply under Voltage Lock-out Hysteresis | | 0.2 | 0.3 | 0.5 | V |
| V_{IN_H} | IN- High Threshold | IN- high threshold | | 1.9 | 2.3 | V |
| V_{IN_L} | IN- Low Threshold | IN- low threshold | 1 | 1.2 | | V |
| V_{IN_HYS} | IN- Hysteresis | | 0.7 | 0.9 | 1.1 | V |
| V_{IN+_H} | IN+ Signal High Threshold | IN+ high threshold | | 2.1 | 2.3 | V |
| V_{IN+_L} | IN+ Signal Low Threshold | IN+ low threshold | 1 | 1.2 | | V |
| V_{IN+_HYS} | IN+ Hysteresis | | 0.7 | 0.9 | 1.1 | V |
| I_{OUT} | Output Peak Current | $C_{LOAD} = 0.22\text{ }\mu\text{F}$, $F_{SW} = 1\text{ kHz}$ | | ± 5 | | A |
| $V_{DD} - V_{OH}$ | Output High Voltage | $I_{OUT} = -10\text{ mA}$ | | | 40 | mV |
| V_{OL} | Output Low Voltage | $I_{OUT} = 10\text{ mA}$ | | | 10 | mV |
| R_{OH} | Output Pull-up Resistance, PMOS Pull-up Only | $I_{OUT} = -10\text{ mA}$ | 1 | 1.6 | 3 | Ω |
| R_{OL} | Output Pull-Down Resistance | $I_{OUT} = 10\text{ mA}$ | 0.15 | 0.5 | 1 | Ω |
| t_R | Output Rise-Time | $C_{LOAD} = 1.8\text{ nF}$ | | 7 | 18 | ns |
| t_F | Output Fall-Time | $C_{LOAD} = 1.8\text{ nF}$ | | 6 | 10 | ns |
| t_{PW} | Minimal Pulse Width | | | 15 | 25 | ns |
| t_{D1} | IN+ to Output Propagation Delay | $C_{LOAD} = 1.8\text{ nF}$, 5-V IN+ pulse | 6 | 13 | 23 | ns |
| t_{D2} | IN+ to Output Propagation Delay | $C_{LOAD} = 1.8\text{ nF}$, 5-V IN+ pulse | 6 | 13 | 23 | ns |
| t_{D3} | IN- to Output Propagation Delay | $C_{LOAD} = 1.8\text{ nF}$, 5-V IN- pulse | 6 | 13 | 23 | ns |
| t_{D4} | IN- to Output Propagation Delay | $C_{LOAD} = 1.8\text{ nF}$, 5-V IN- pulse | 6 | 13 | 23 | ns |

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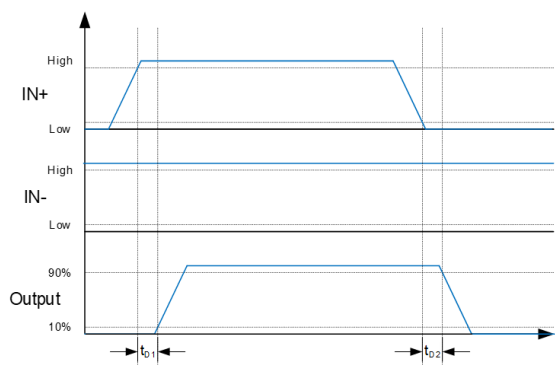


Figure 1. IN+ Timing Diagram

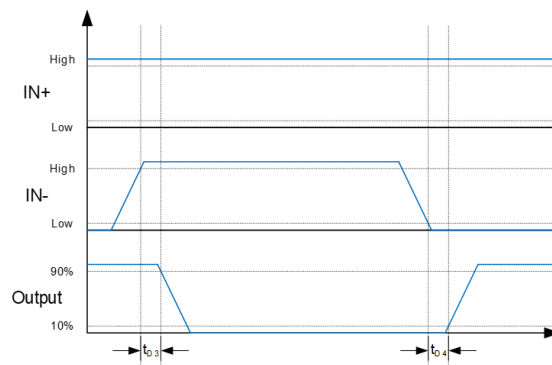


Figure 2. IN- Timing Diagram

Typical Performance Characteristics

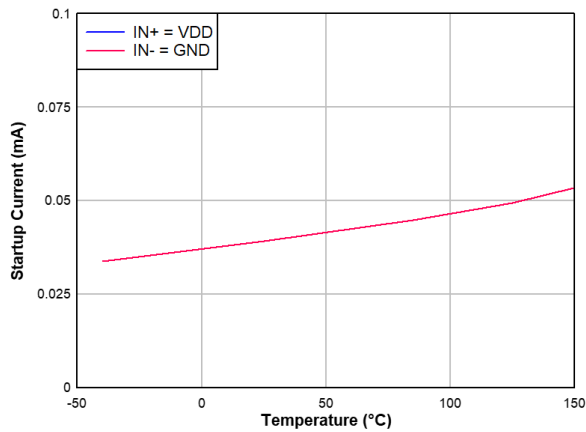


Figure 3. Start-up Current vs. Temperature

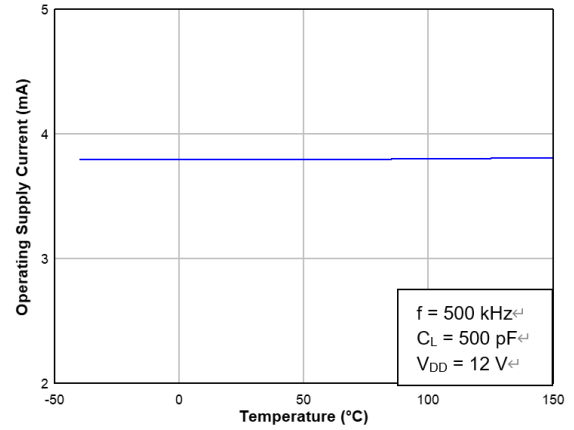


Figure 4. Operating Current vs. Ambient Temperature

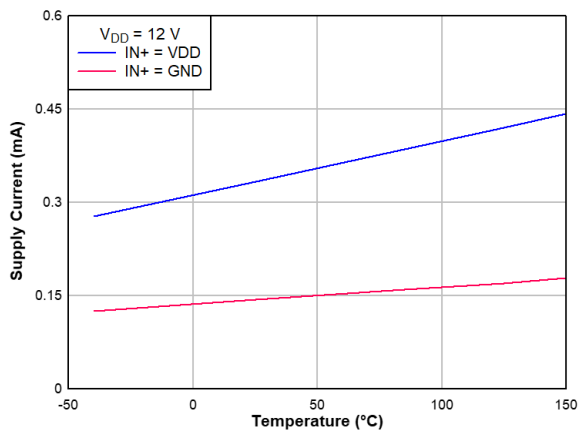


Figure 5. Supply Current vs. Temperature (On/Off)

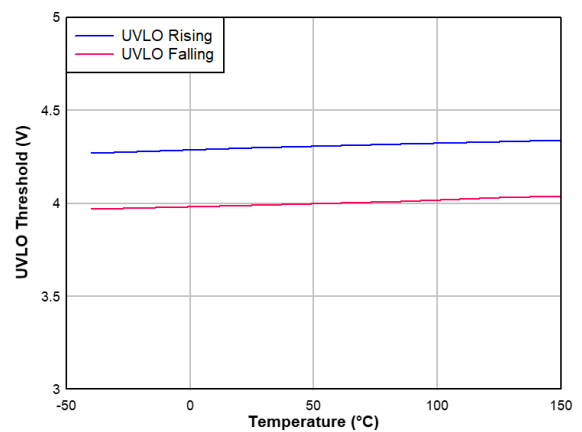


Figure 6. UVLO Threshold vs. Temperature

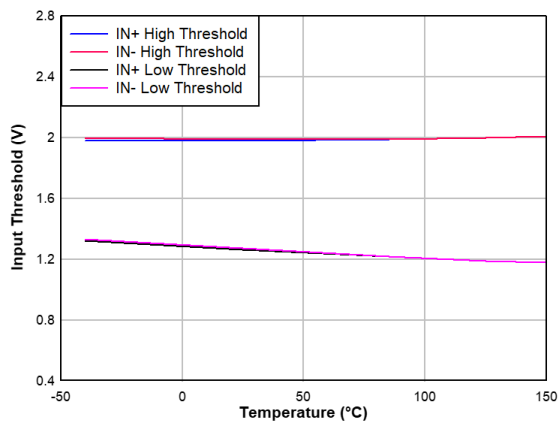


Figure 7. Input Threshold vs. Temperature

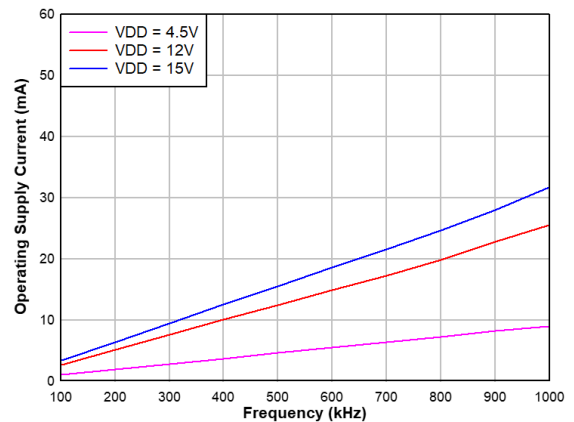


Figure 8. Operating Supply Current vs. Frequency

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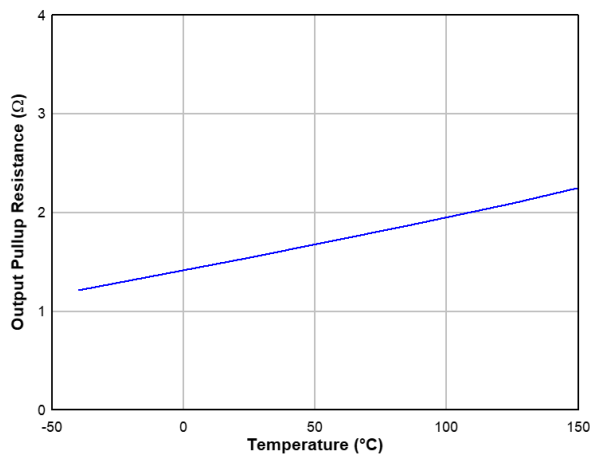


Figure 9. Output Pull-up Resistance vs. Temperature

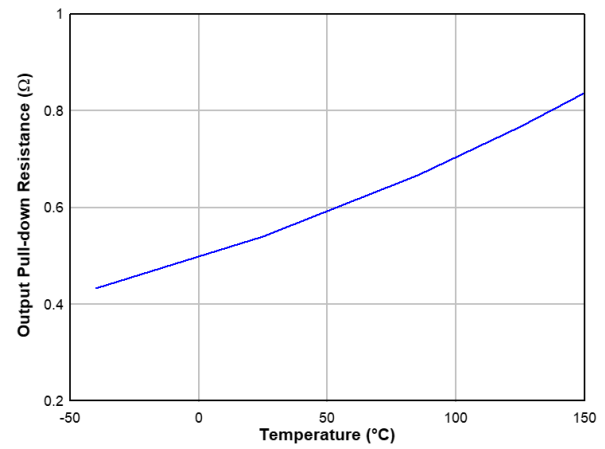


Figure 10. Output Pull-down Resistance vs. Temperature

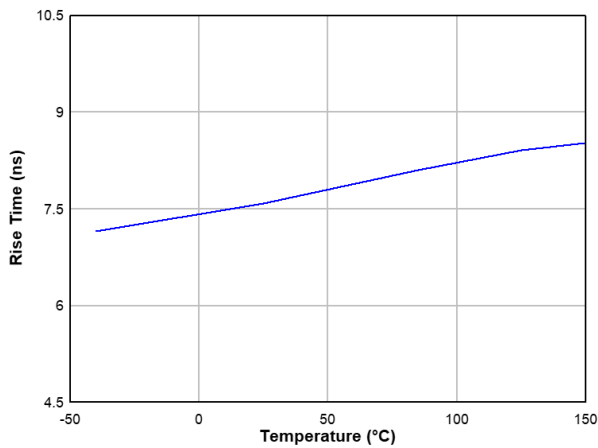


Figure 11. Rise-Time vs. Temperature

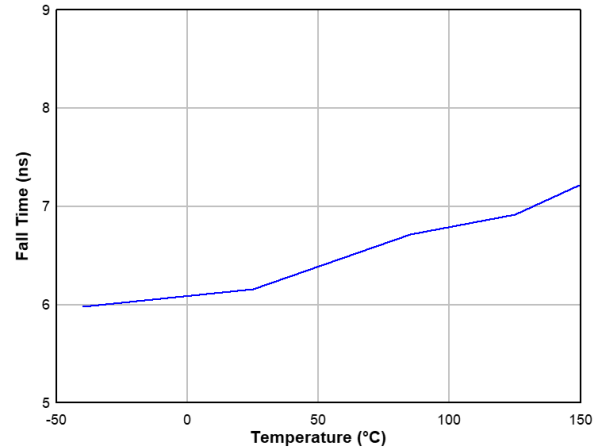


Figure 12. Fall-Time vs. Temperature

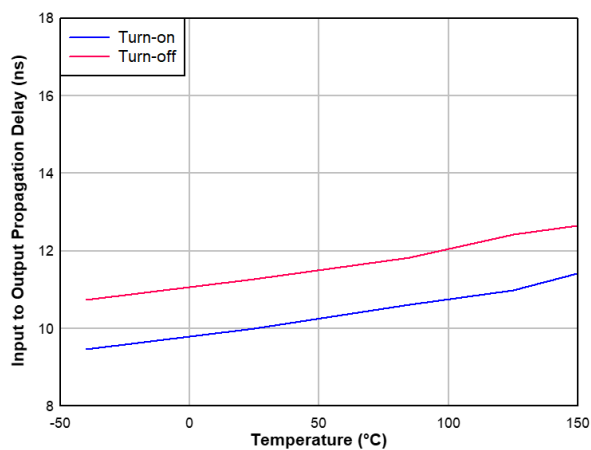


Figure 13. Input to Output Propagation Delay vs. Temperature

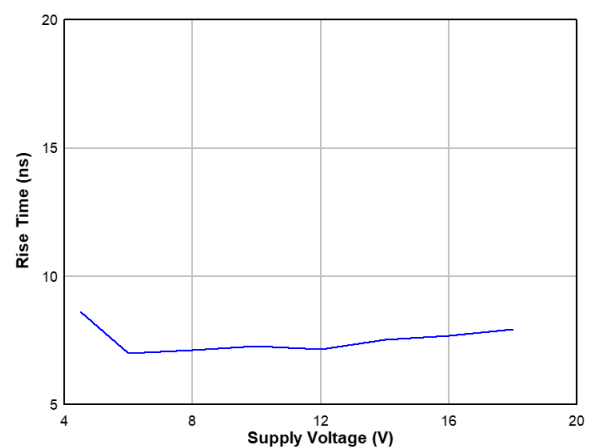


Figure 14. Rise-Time vs. Supply Voltage

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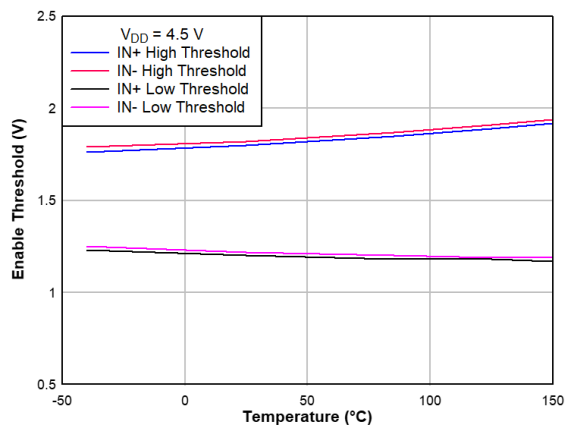


Figure 15. Enable Threshold vs. Temperature

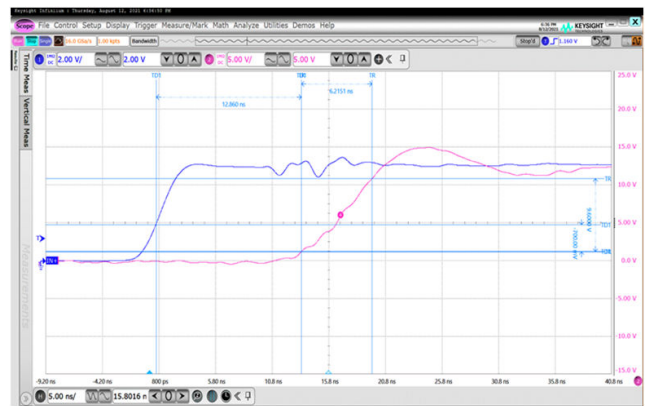


Figure 16. IN+ Rising Edge

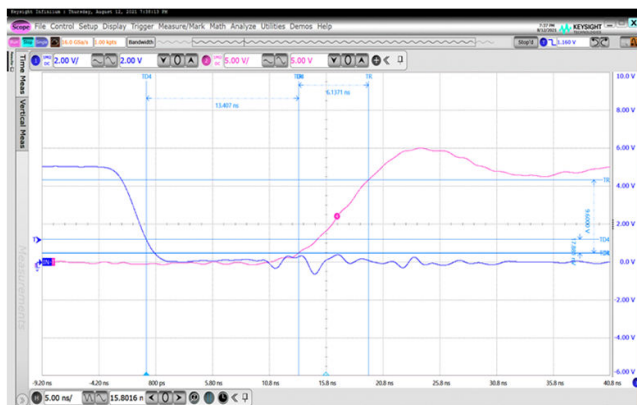


Figure 17. IN+ Falling Edge

Detailed Description

Overview

The TPM27517 single-channel low-side gate driver is designed for high-performance power supplies, motor controls, and inverters. Designed with the industrial standard pin-out and package, the TPM27517 accelerates the design process. With extended voltage ranges on the supply voltage and negative input voltage, the TPM27517 improves system-level reliability. Its 5-A strong driving capability improves the gate driver efficiency and lowers heat generation, especially in high-frequency switching applications.

Functional Block Diagram

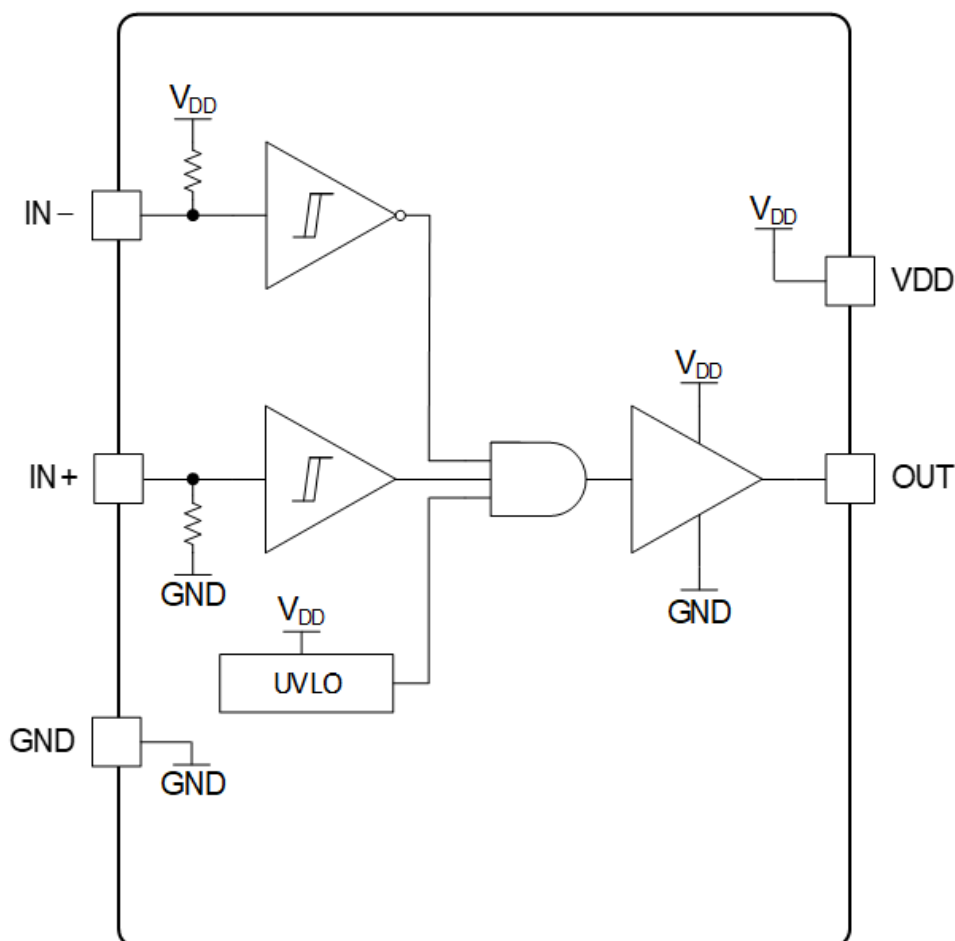


Figure 18. Functional Block Diagram

Feature Description

Low Propagation Delay Driver Output

The low-propagation-delay design allows the device to achieve industrial-leading low propagation delay between the device input and output. The low delay enhances driver performance in high-frequency switching regulators.

Single-Channel 5-A High-Speed Low-Side Gate Driver**Supply and UVLO**

The device monitors the supply voltage with under-voltage lock-out (UVLO). When the supply voltage is below the UVLO threshold, the output is held low in UVLO to avoid glitches during power rising and falling.

The quiescent current and operating current of the device are measured as shown in [Figure 5](#). The current is related to the internal quiescent current consumption as well as the output current. The output current can be calculated using the external transistor gate charge times switching frequency f_{sw} .

Channel Input

The input of the TPM27517 gate driver supports the TTL and CMOS input with threshold voltage independent of the supply voltage. The threshold is also designed as temperature-independent to support a wide range of ambient temperatures. The wide hysteresis enhances the system-level noise immunity. The integrated pull-down resistor sets the device in a low state when inputs are floating. Inputs can withstand DC -5 V, to improve robustness on ground bouncing.

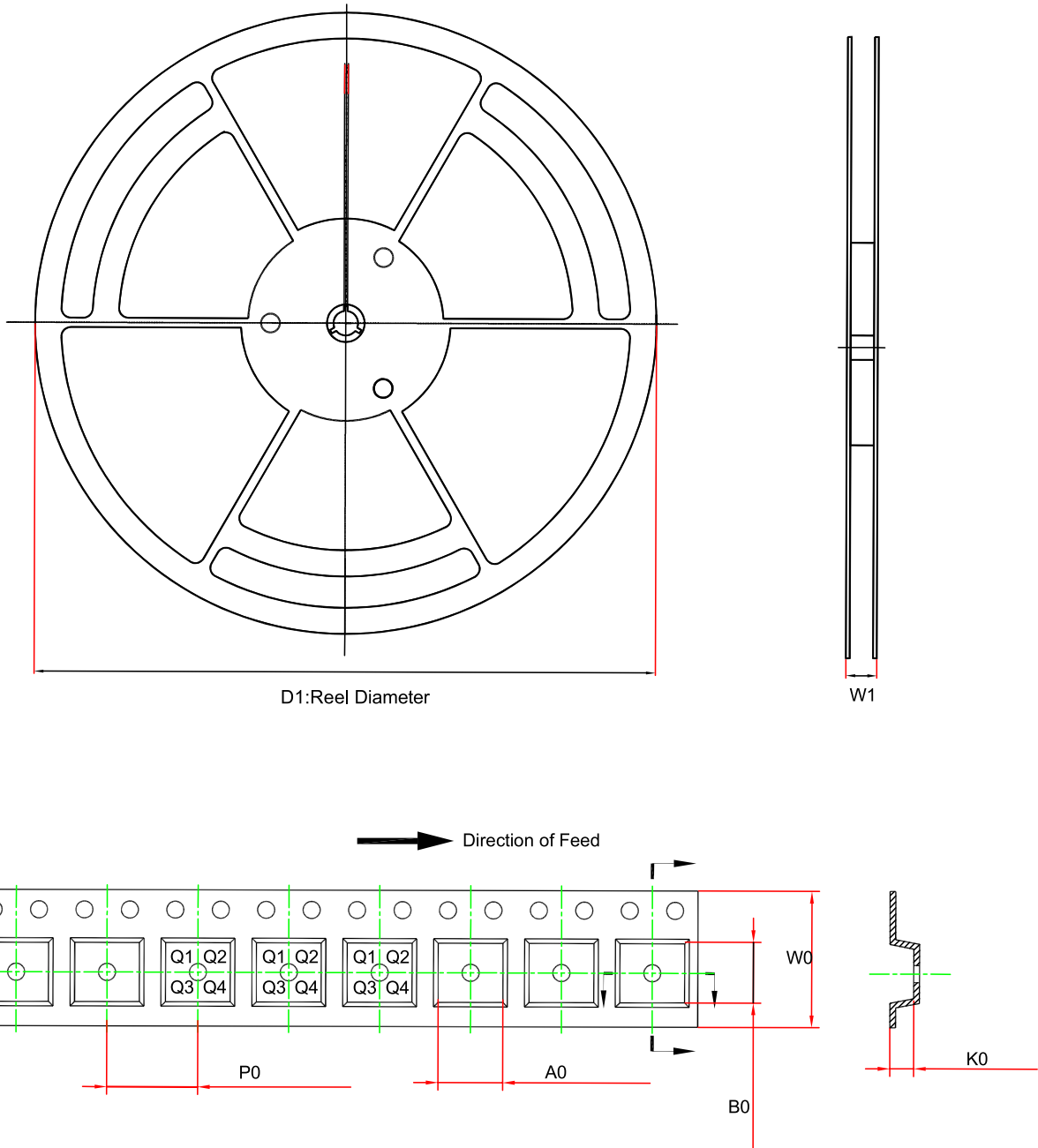
Output Stage

The output stage of the TPM27517 can deliver high current sourcing and sinking up to 5 A with low propagation delay.

Single-Channel 5-A High-Speed Low-Side Gate Driver**Application and Implementation****Note**

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Tape and Reel Information

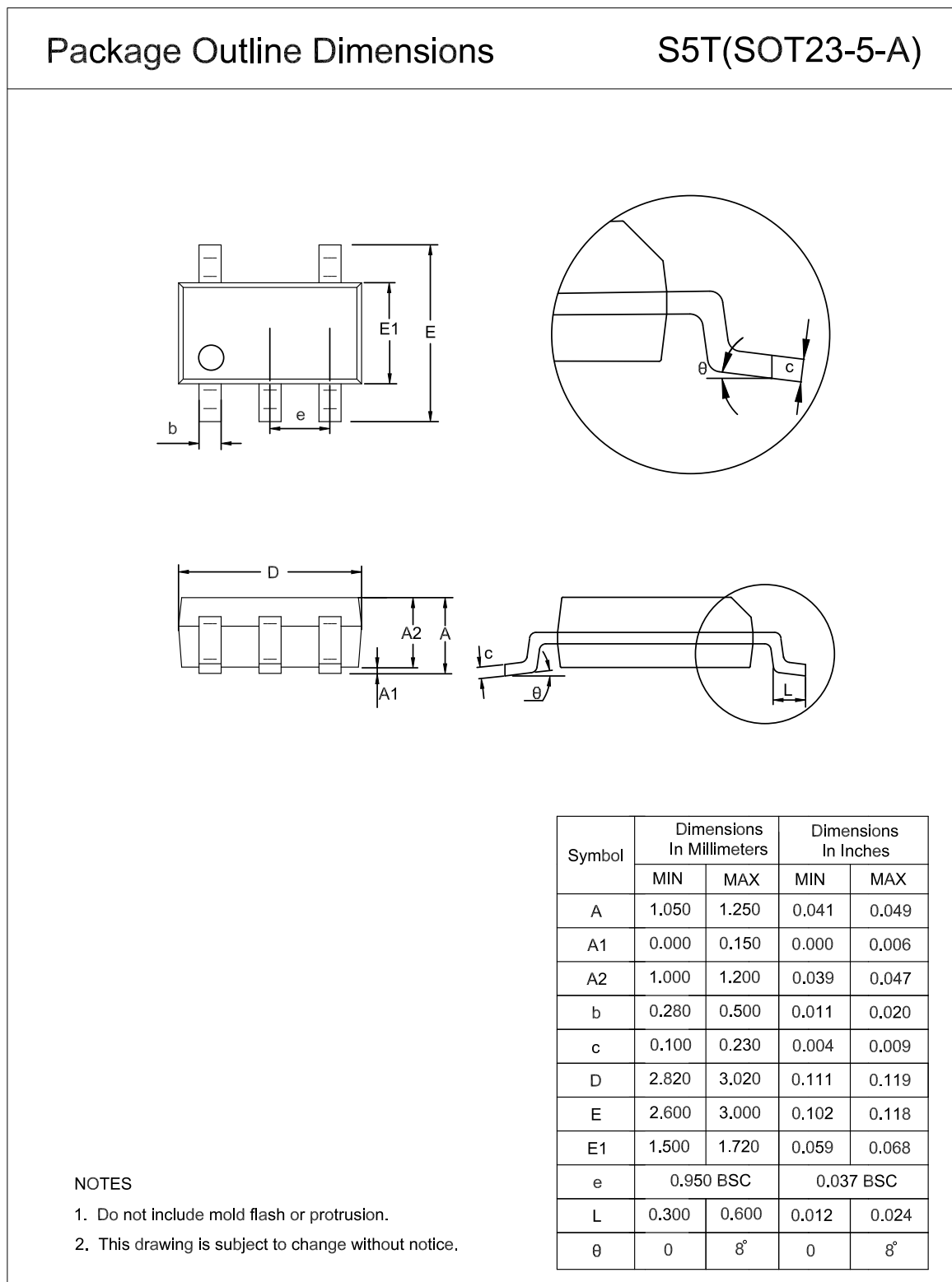


| Order Number | Package | D1 (mm) | W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | W0 (mm) | Pin1 Quadrant |
|----------------|---------|---------|---------|---------|---------|---------|---------|---------|---------------|
| TPM27517-S5TR | SOT23-5 | 180 | 12 | 3.3 | 3.25 | 1.4 | 4 | 8 | Q3 |
| TPM27517F-S5TR | SOT23-5 | 180 | 12 | 3.3 | 3.25 | 1.4 | 4 | 8 | Q3 |

Single-Channel 5-A High-Speed Low-Side Gate Driver

Package Outline Dimensions

SOT23-5



Order Information

| Order Number | Operating Temperature Range | Package | Marking Information | MSL | Transport Media, Quantity | Eco Plan |
|----------------|-----------------------------|---------|---------------------|-----|---------------------------|----------|
| TPM27517-S5TR | -40 to 125°C ⁽¹⁾ | SOT23-5 | M57 | 3 | Tape and Reel, 3000 | Green |
| TPM27517F-S5TR | -40 to 125°C ⁽¹⁾ | SOT23-5 | M57 | 3 | Tape and Reel, 3000 | Green |

(1) The ambient temperature indicates the operation condition range of the device. The application thermal behavior needs to be taken care of when operating in high-temperature scenarios.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

Single-Channel 5-A High-Speed Low-Side Gate Driver**IMPORTANT NOTICE AND DISCLAIMER**

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