Dual 2-A High-Speed, Low-Side Gate Driver

Features

- Industry-Standard Pin-out
- 4.5-V to 23-V Single-Supply Range
- Dual Independent Channels
- 2-A Peak Source and Sink-Drive Current
- Independent-Enable Function for Each Output
- TTL and CMOS Compatible Threshold
- Outputs Held Low during VDD-UVLO or Input Floating
- Low Propagation Delay (13-ns Typical)
- Fast Rise and Fall Times (7-ns and 6-ns Typical)
- <1-ns Typical Delay Matching Between Two Channels
- Two Outputs can be used in Parallel for Higher Drive Current
- ESD Protection Exceeds JESD 22 – 4-kV HBM, 1.5-kV CDM
- Available in SOP8 and DFN2X2-8 Packages

Applications

- Switched-Mode Power Supplies
- DC-DC Converters
- Motor Control, Solar Inverters
- Gate & IGBT Drive
- Piezo Driver

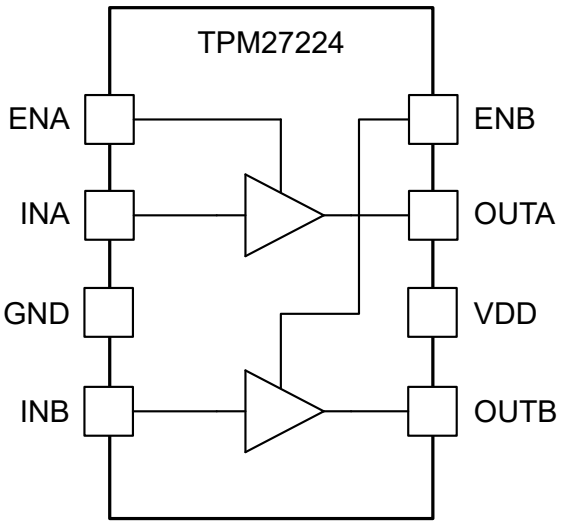
Description

The TPM2722x family is a series of dual-channel low-side gate drivers for MOSFET, IGBT, and GaN power switches.

High sourcing and sinking current capability of 2 A allows for improving switching efficiencies by minimizing slew time and switching loss. The device supports maximum 25-V supply voltage and −5 V DC input voltage capability, which improves system robustness, especially in noisy industrial applications. Ultra-low propagation delay and excellent matching between two channels are designed for applications with tight timing requirements.

The TPM2722x family consists of a set of gate drivers with different polarities, allowing customers to select based on application needs.

Typical Application Circuit



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Revision History

Date	Revision	Notes
2023-11-16	Rev.A.0	Initial released version
2024-03-11	Rev.A.1	Misc. correction

Pin Configuration and Functions

TPM27224
DFN2X2-8
Top View

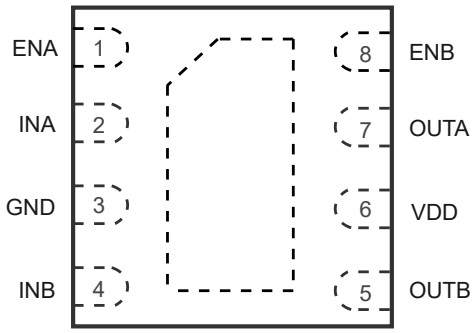


Table 1. Pin Functions: TPM27224

Pin	Name	I/O	Description
1	ENA	Input	Channel A Enable Input
8	ENB	Input	Channel B Enable Input
3	GND	Ground	Device Ground
2	INA	Input	Non-inverting Input
4	INB	Input	Non-inverting Input
7	OUTA	Output	Channel A Output
5	OUTB	Output	Channel B Output
6	VDD	Power	Power Supply Input

Specifications

Absolute Maximum Ratings(1)

Parameter		Min	Max	Unit
	Power Supply Voltage, VDD	–0.3	25	V
	Output Voltage Range OUTA, OUTB	–0.3	VDD + 0.3	V
		–2	VDD + 0.3 (200-ns pulse)	
	Input Voltage Range INA, INB, ENA, ENB	–5	20	V
	Pulsed Output Channel Current OUTA, OUTB (500 ns)	–2	2	A
	Operating Junction Temperature Range	–40	150	°C
T_{STG}	Storage Temperature Range	–65	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 300 mV beyond the power supply, the input current should be limited to less than 10 mA.
(3) Power dissipation and thermal limits must be observed.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter	Min	Max	Unit
Power Supply Voltage, VDD	4.5	23	V
Input Voltage Range INA, INB, ENA, ENB	0	20	V
Operating Ambient Temperature Range	–40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOP8	122.3	60.4	°C/W
DFN2X2-8	55	50	°C/W

Electrical Characteristics

All test conditions: V_{DD} = 18 V, T_J = −40 °C to 150 °C, and 1-µF capacitor between V_{DD} and GND, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
$I_{DD(off)}$	Start-up Current	V_{DD} = INA = INB = 3.4 V		54	80	µA
V_{ON}	Supply under Voltage Lock Out Rising Threshold	T_J = −40 °C – 150 °C	3.5	3.85	4.2	V
V_{OFF}	Supply Under Voltage Lock-out Falling Threshold	T_J = −40 °C – 150 °C	3.3	3.6	4	V
V_{DD_H}	Supply Under Voltage Lock-out Hysteresis			0.25		V
V_{EN_H}	Enable High Threshold	Enable high threshold		1.7	2.1	V
V_{EN_L}	Enable Low Threshold	Enable low threshold	1	1.15		V
V_{EN_HYS}	Enable Hysteresis			0.55		V
V_{IN_H}	Input Signal High Threshold	Input high threshold		1.7	2.1	V
V_{IN_L}	Input Signal Low Threshold	Input low threshold	1	1.15		V
V_{IN_HYS}	Input Hysteresis			0.55		V
I_{OUT}	Output Peak Current	C_{LOAD} = 0.22 µF, F_{SW} = 1 kHz		±2		A
R_{OH}	Output Pull-up Resistance, PMOS Pull-up only	I_{OUT} = −10 mA	3	6	10	Ω
R_{OL}	Output Pull-down Resistance	I_{OUT} = 10 mA	0.5	0.93	1.6	Ω
V_{OH}	Output Pull-up Voltage, PMOS pull-up only, V_{DD} – V_{OUT}	I_{OUT} = −10 mA			100	mV
V_{OL}	Output Pull-down Voltage	I_{OUT} = 10 mA	3		16	mV
t_R	Output Rise-Time	C_{LOAD}= 1 nF		9		ns
t_F	Output Fall-Time	C_{LOAD} = 1 nF		8		ns
t_M	Delay matching between OUTA and OUTB	INA = INB, OUTA and OUTB measured at 50%		1	4	ns
t_{D1}	Input to Output Propagation Delay	C_{LOAD} = 1 nF, 5-V INx pulse		18		ns
t_{D2}	Input to Output Propagation Delay	C_{LOAD} = 1 nF, 5-V INx pulse		14		ns
t_{D3}	Enable to Output Propagation Delay	C_{LOAD} = 1 nF, 5-V ENx pulse		18		ns
t_{D4}	Enable to Output Propagation Delay	C_{LOAD} = 1 nF, 5-V ENx pulse		14		ns

Typical Performance Characteristics

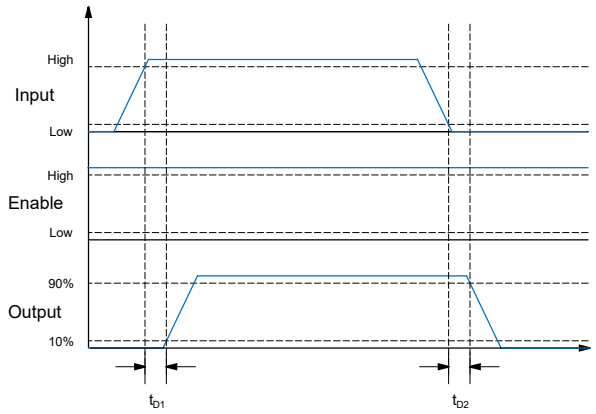


Figure 1. Input Timing Diagram

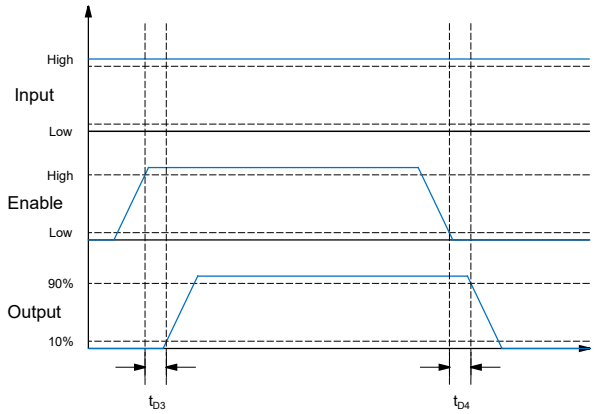


Figure 2. Enable Timing Diagram

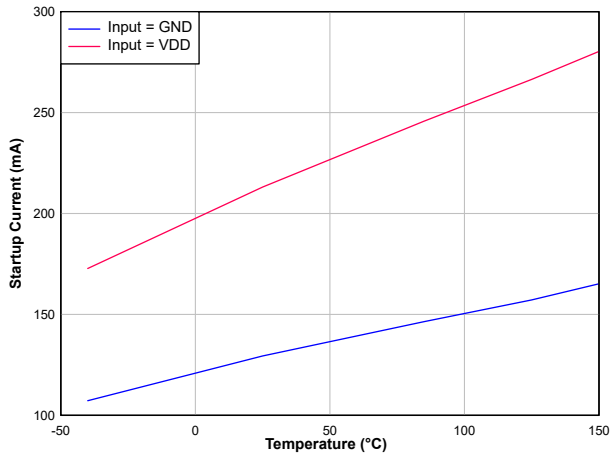


Figure 3. Quiescent Current vs. Temperature

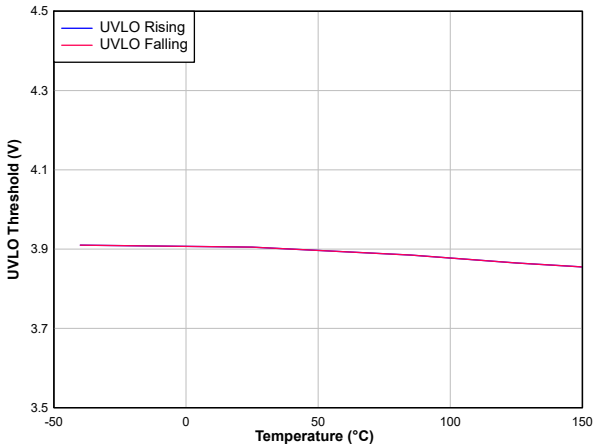


Figure 4. UVLO Threshold vs Temperature

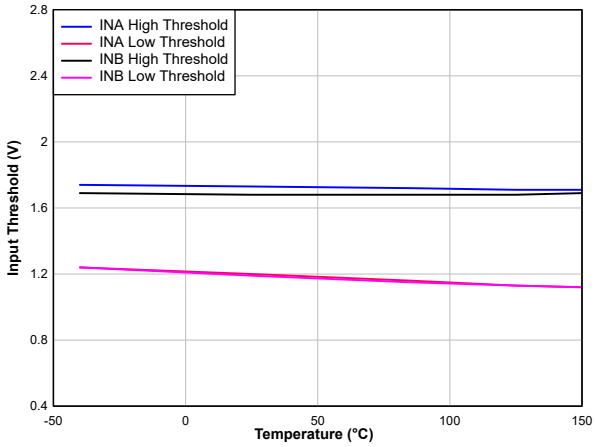


Figure 5. Input Threshold vs Temperature

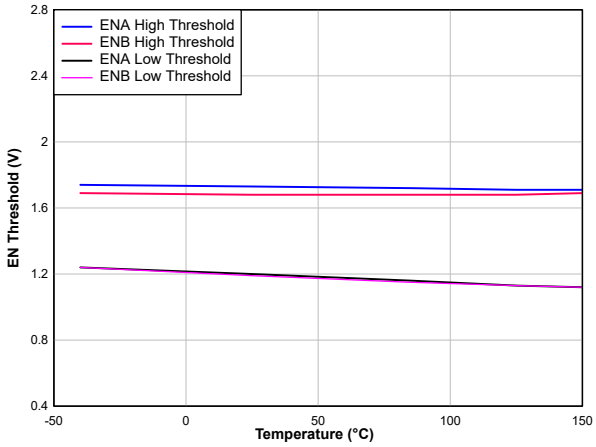


Figure 6. Enable Threshold vs Temperature

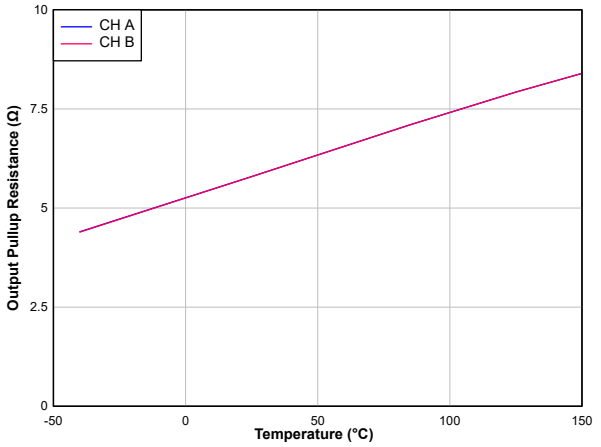


Figure 7. Output Pull-up Resistance vs Temperature

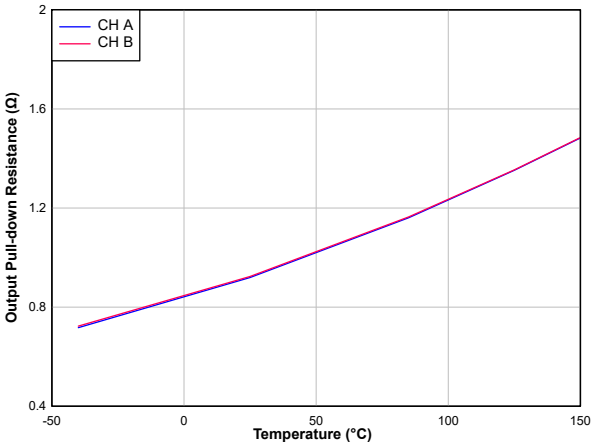


Figure 8. Output Pull-down Resistance vs Temperature

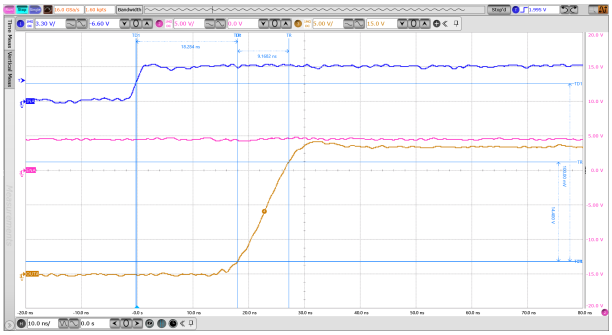


Figure 9. Channel A Rising Edge by INA

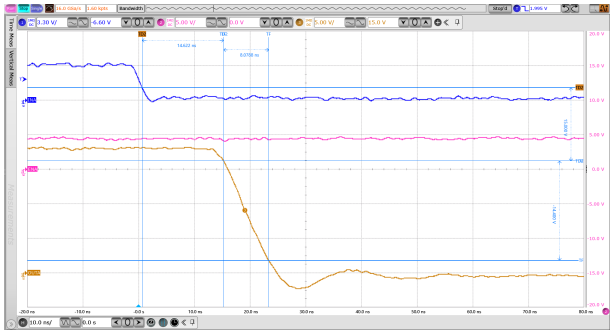


Figure 10. Channel A Falling Edge by INA

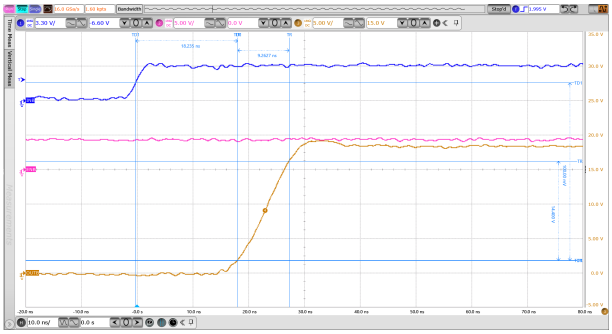


Figure 11. Channel B Rising Edge by INB

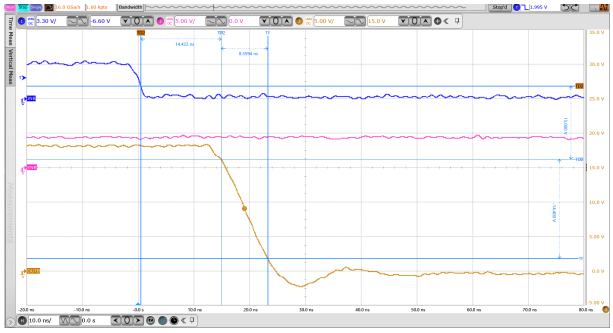


Figure 12. Channel B Falling Edge by INB

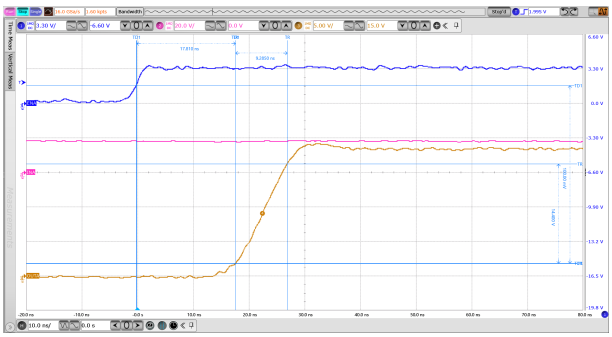


Figure 13. Channel A Rising Edge by ENA

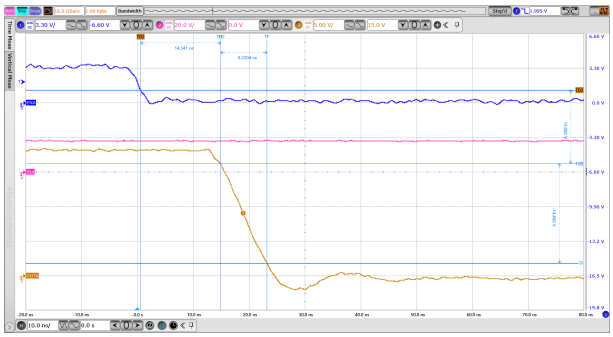


Figure 14. Channel A Falling Edge by ENA

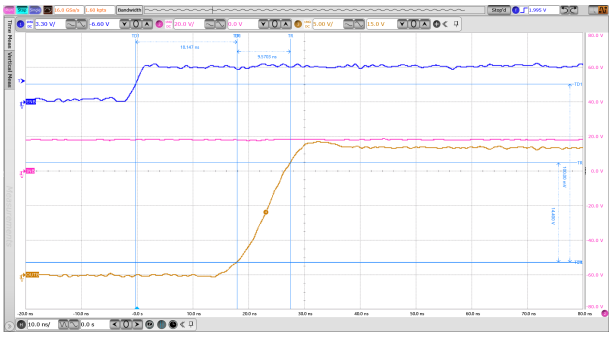


Figure 15. Channel B Rising Edge by ENB

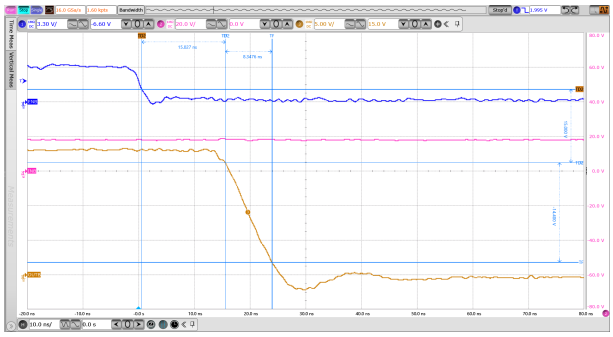


Figure 16. Channel B Falling Edge by ENB

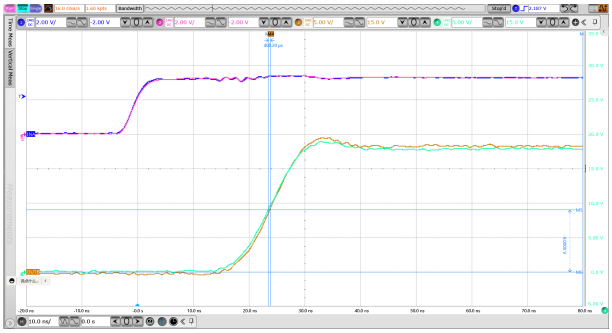


Figure 17. Channel Rising Edge Mismatch

VDD = 4.5 V

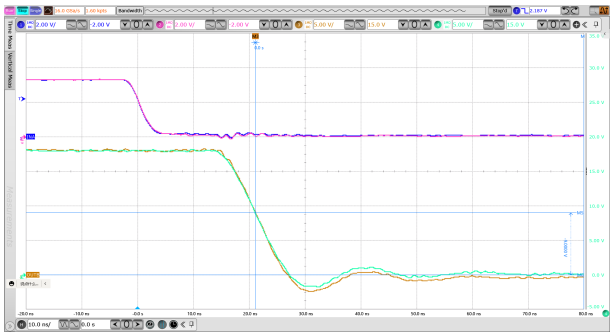


Figure 18. Channel Falling Edge Mismatch

Detailed Description

Overview

The TPM27224 series of dual-channel low-side gate drivers are designed for high-performance power supplies, motor controls, and inverters. Designed with industrial standard pin-out and package, the TPM27224 accelerates design process. With extended voltage ranges of supply voltage and negative input voltage on inputs, the TPM27224 improves system-level reliability. 2-A driving capability improves gate driver efficiency and lowers heat generation, especially in high-frequency switching applications.

Functional Block Diagram

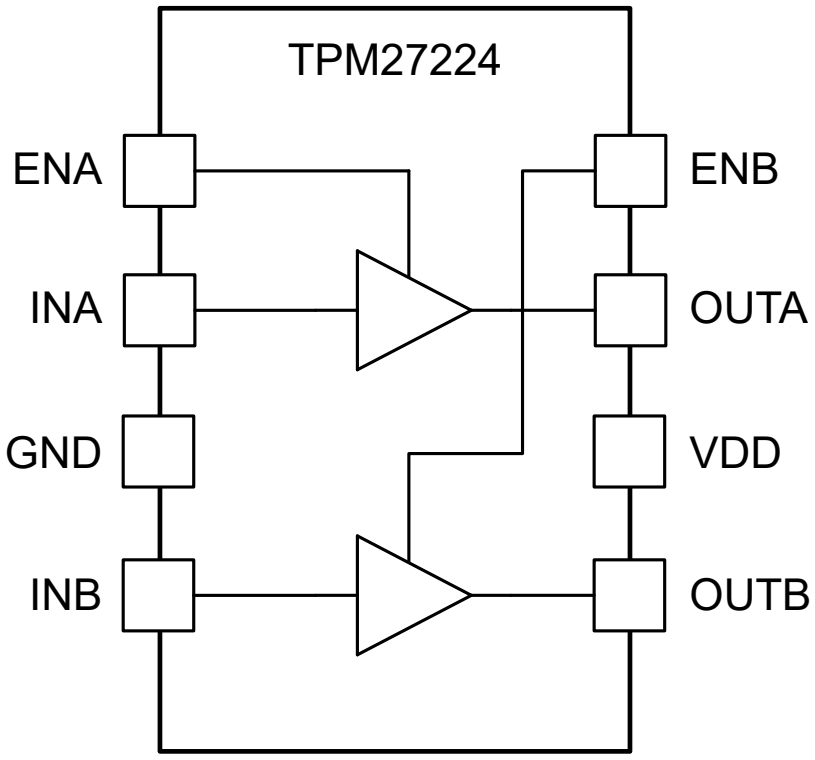


Figure 19. Functional Block Diagram

Feature Description

Low Propagation Delay Driver Outputs

The low-propagation-delay design allows the device to achieve industrial leading low propagation delay between inputs and outputs. The low delay enhances driver performance in high-frequency switching regulators. Matching between two channels is optimized to support parallel driving. 3PEAK recommends tying IN1 and IN2 locally together with a high input slew rate, to avoid shoot-through between the two well-matched channels. Capacitors are not recommended on IN1 and IN2 nodes when used in parallel.

Supply and UVLO

The device monitors supply voltage with under-voltage lock-out (UVLO). When the supply voltage is below the UVLO threshold, the outputs are held low in UVLO to avoid glitches during power rising and falling.

The device quiescent current and operating current are measured as shown in Figure 5. The current is related to internal quiescent current consumption as well as the output current. The output current can be calculated using external transistor gate charge times switching frequency f_{sw}.

Channel Input

The input of the TPM27224 gate drivers supports TTL and CMOS input with threshold voltage independent of the supply voltage. The threshold is also designed as temperature independent to support a wide range of ambient temperatures. Wide hysteresis enhances system-level noise immunity. The integrated pull-up and pull-down resistors set the device state when inputs are floating. EN supports the NC connection with the help of internal pull-up resistors.

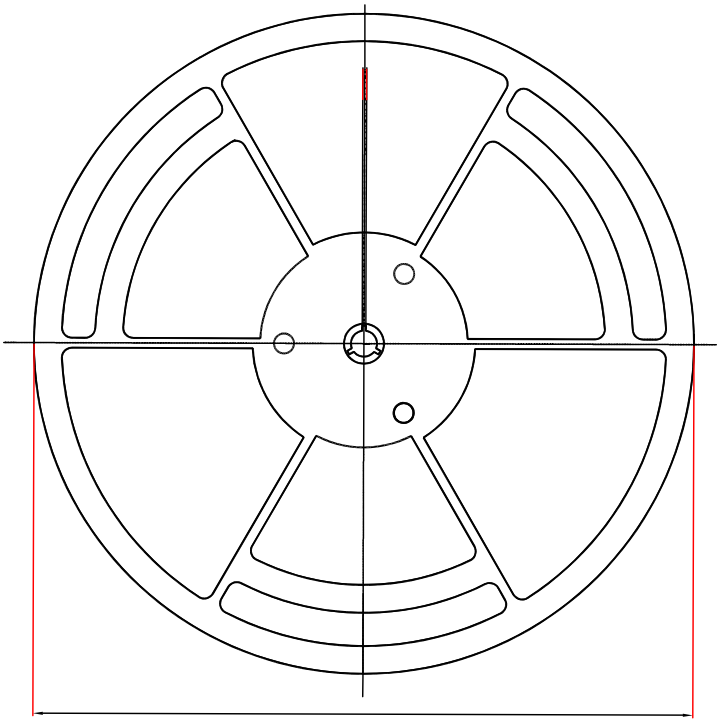
Inputs can withstand DC −5 V, to improve robustness on ground bouncing.

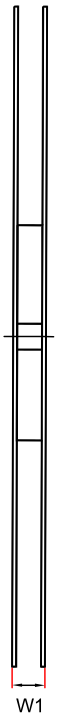
Output Stage

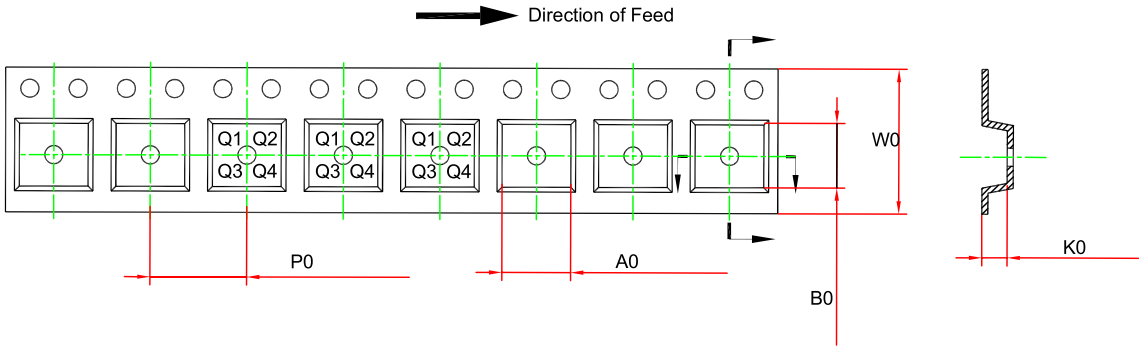
The TPM27224 output stage is able to deliver high-current sourcing and sinking up to 2-A with low-propagation delay. The delay matching between dual channels is also optimized within 1-ns.

In the case of higher output driving capabilities needed, the TPM27224 allows paralleling the dual channel to achieve a higher driving current. In this case, it is recommended to use a high slew rate on IN1 and IN2 and connect IN1 and IN2 to avoid shoot through between channels.

Tape and Reel Information





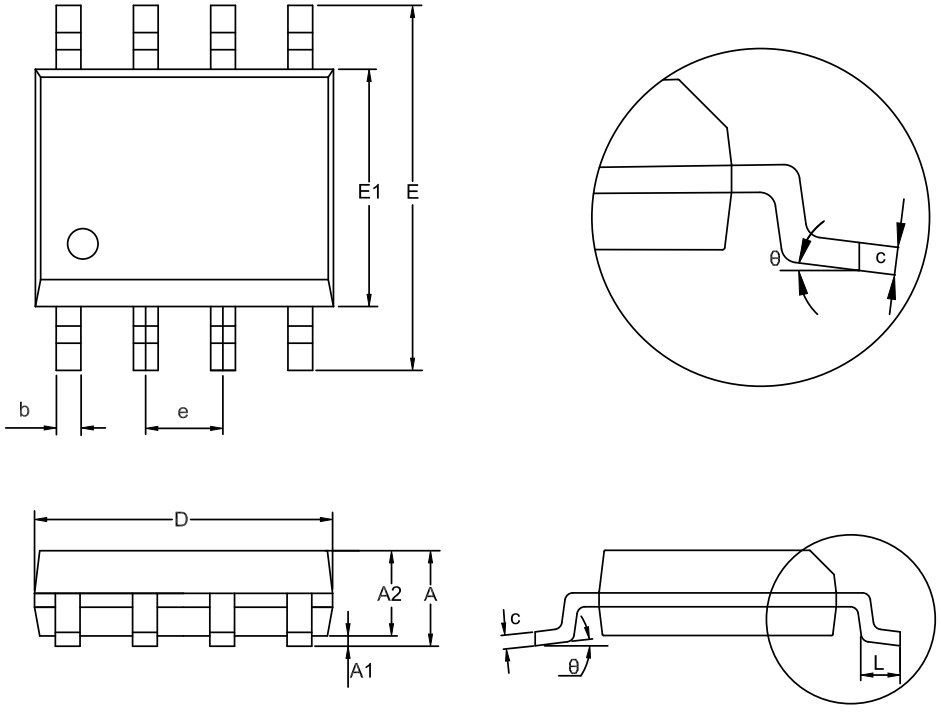


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM27224-SO1R	SOP8	330.0	17.6	6.5	5.4	2.0	8.0	12.0	Q1
TPM27224-DF4R	DFN2X2-8	180.0	12.5	2.3	2.3	1.1	4.0	8.0	Q2

Package Outline Dimensions

SOP8

Package Outline Dimensions SO1(SOP-8-A)



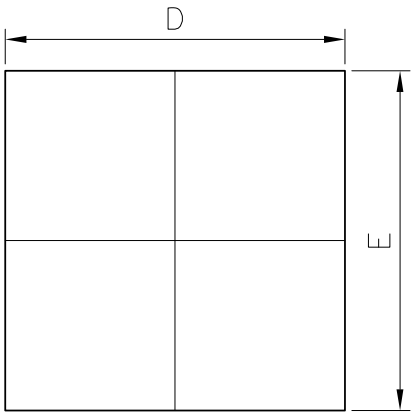
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.550	0.049	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.000	0.016	0.039
θ	0	8°	0	8°

NOTES

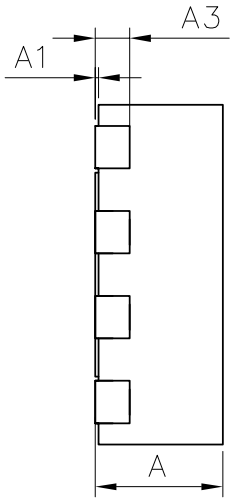
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

DFN2X2-8-G

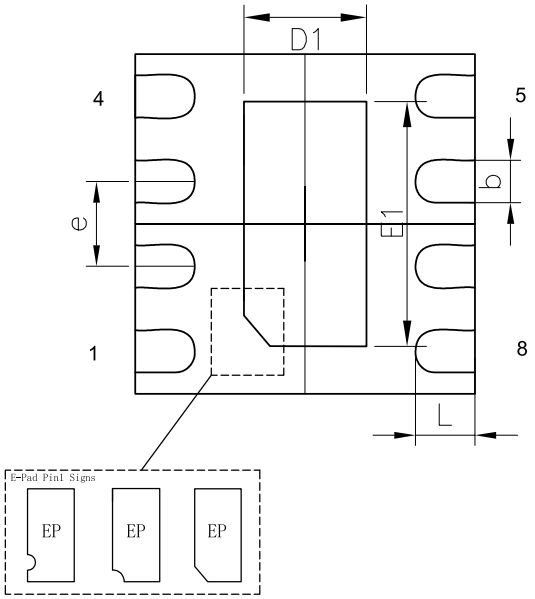
Package Outline Dimensions DFJ(DFN2X2-8-G)



Top View



Side View



Bottom View

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.031	0.035
A1	0.000	0.050	0.000	0.002
b	0.180	0.300	0.007	0.012
A3	0.150	0.250	0.006	0.010
D	1.900	2.100	0.075	0.083
D1	0.750	0.850	0.030	0.033
E	1.900	2.100	0.075	0.083
E1	1.550	1.650	0.061	0.065
e	0.500 BSC		0.020BSC	
L	0.250	0.350	0.010	0.014

Order Information

Order Number	Operating Ambient Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPM27224-SO1R	-40 °C to 125 °C (1)	SOP8	224	3	Tape and Reel, 4000	Green
TPM27224-DF4R	-40 °C to 125 °C (1)	DFN2X2-8	224	3	Tape and Reel, 3000	Green

(1) Ambient temperature indicates device operation condition range. Application thermal behavior needs to be taken care of when operating in high-temperature scenarios.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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