120-V Supply, 4-A Peak, High-frequency HS and LS Gate Driver

Features

- Drives Both High-side and Low-side N-Channel MOSFET with Independent Inputs
- 4-A Peak Output Source and Sink Current Capability
- Max Bootstrap Supply Voltage up to 120 V
- Wide Supply Rail from 7 V to 20 V
- Integrated Bootstrap Diode
- TTL/CMOS Compatible Input, −10-V to 20-V Input Capability
- 20-ns Propagation Delay Times
- 2-ns Delay Matching
- 7-ns Rise and 4.5-ns Fall Time with 1000-pF Load
- 15-ns Input Deglitching Time
- 20-ns Minimum Pulse Width
- Supply Rail Under-Voltage Lockout (UVLO)
- Operation from −40°C to 150ºC
- Available in SOP8, ESOP8, DFN4X4-8 and DFN4X4-10 Packages

Applications

- Power Supplies for Telecom, Datacom, and Data Centers
- Half-Bridge and Full-Bridge Converters
- Push-Pull Converters
- High-Voltage Synchronous-Buck Converters
- 48-V Fan Driver

Description

The TPM2721x MOSFET drivers are pin-to-pin compatible with industrial-standard 100-V half-bridge drivers. They are designed to control two N-channel MOSFETs in half-bridge or synchronous-buck configurations. They have higher peak currents at 4 A for both pull-up and pull-down, and lower resistance at 0.9 Ω. This helps drive bigger MOSFETs with less switching loss. They can handle −10 VDC input directly, which is stronger and lets them connect to the gate-drive transformers without external diodes. The drivers work with any supply voltage up to 20 V.

Both high-side and low-side driver stages have an under-voltage lockout that forces outputs low if the supply voltage drops below the set threshold. An integrated bootstrap diode eliminates the need for an external diode in many setups, saving space and reducing costs. The TPM27211 comes in various packages, ESOP8, DFN4X4-10, DFN4X4-8, DFN3X3-8, etc, suitable for high-density designs.

Typical Application Circuit

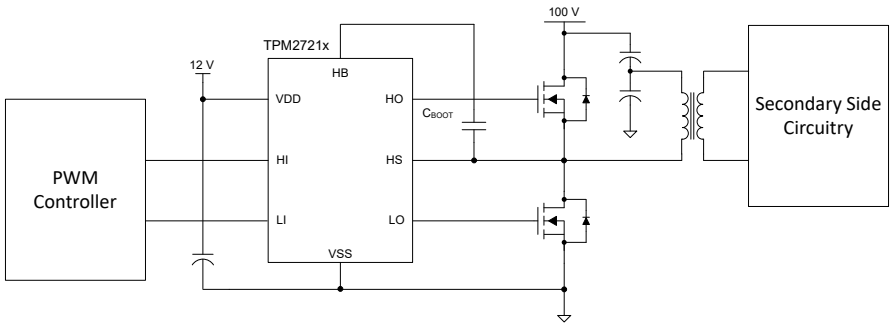


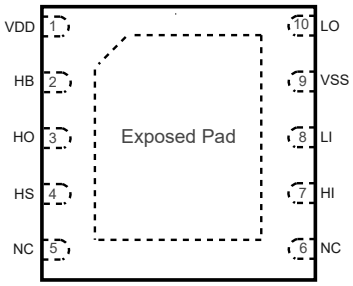
Table of Contents

Revision History

Date	Revision	Notes
2025-07-22	Rev.A.0	Initial release.

Pin Configuration and Functions

TPM27211-DF9R
DFN4X4-10
Top View



TPM27211-DFMR
DFN4X4-8
Top View

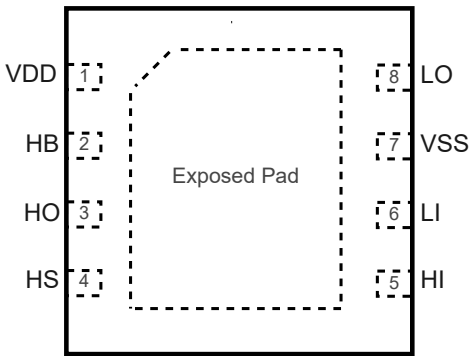
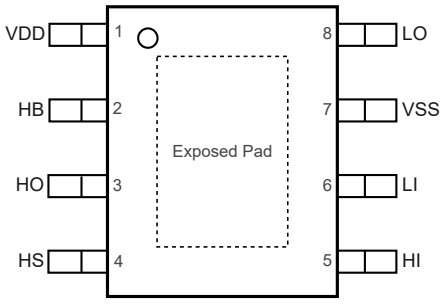


Table 1. Pin Functions

Pin No.		Name	I/O	Description
TPM27211-DF9R	TPM27211-DFMR			
1	1	VDD	P	The low-side gate driver in the TPM27211 requires a positive supply, which should be decoupled to the VSS with a typical capacitor value of 1 μF to ensure stable operation. If an external boot diode is used, its anode should be connected to this pin.
2	2	HB	P	The high-side bootstrap supply in the TPM27211 includes an integrated bootstrap diode with an external bootstrap capacitor. Attach the positive terminal of this capacitor to the HB pin, with a typical recommendation of 0.1 μF for the HB bypass capacitor, mainly determined by characteristics of the high-side MOSFET. When an external bootstrap diode is used, its cathode should be connected to this pin.
3	3	HO	O	The high-side output of the TPM27211. This pin should be connected directly to the gate of the high-side power MOSFET or to one terminal of an external gate resistor if used.
4	4	HS	P	The high-side source connection on the TPM27211 should be connected to the source of the high-side power MOSFET. The negative side of the bootstrap capacitor should be attached to this pin.
5	n/a	NC	NC	Not connected
6	n/a	NC	NC	Not connected.
7	5	HI	I	High-side driver logic input, TTL compatible. Floating logic low.
8	6	LI	I	Low-side driver logic input, TTL compatible. Floating logic low.
9	7	VSS	GND	Supply ground.

Pin No.		Name	I/O	Description
TPM27211-DF9R	TPM27211-DFMR			
10	8	LO	O	Low-side driver output. The low-side output of the TPM27211 should be connected directly to the gate of the low-side power MOSFET or to one terminal of an external gate resistor if used.
Exposed Pad	Exposed Pad	EP	G	Exposed Pad. Recommend to connect to GND

TPM27211-ES1R
ESOP8
Top View



TPM27211-SO1R
SOP8
Top View

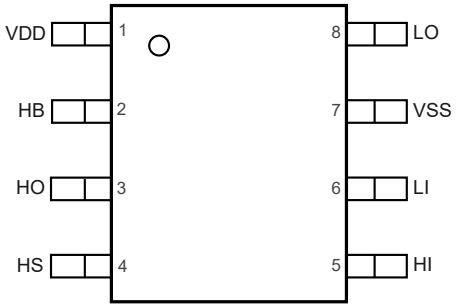


Table 2. Pin Functions

Pin No.		Name	I/O	Description
ESOP8	SOP8			
1	1	VDD	P	The low-side gate driver in the TPM27211 requires a positive supply, which should be decoupled to the VSS with a typical capacitor value of 1 μF to ensure stable operation. If an external boot diode is used, its anode should be connected to this pin.
2	2	HB	P	The high-side bootstrap supply in the TPM27211 includes an integrated bootstrap diode with an external bootstrap capacitor. Attach the positive terminal of this capacitor to the HB pin, with a typical recommendation of 0.1 μF for the HB bypass capacitor, mainly determined by characteristics of the high-side MOSFET. When an external bootstrap diode is used, its cathode should be connected to this pin.
3	3	HO	O	The high-side output of the TPM27211. This pin should be connected directly to the gate of the high-side power MOSFET or to one terminal of an external gate resistor if used.
4	4	HS	P	The high-side source connection on the TPM27211 should be connected to the source of the high-side power MOSFET. The negative side of the bootstrap capacitor should be attached to this pin.
5	5	HI	I	High-side driver logic input, TTL compatible. Floating logic low.
6	6	LI	I	Low-side driver logic input, TTL compatible. Floating logic low.
7	7	VSS	GND	Supply ground.
8	8	LO	O	Low-side driver output. The low-side output of the TPM27211 should be connected directly to the gate of the low-side power MOSFET or to one terminal of an external gate resistor if used.
Exposed Pad	n/a	EP	G	Exposed Pad. Recommend to connect to GND

Specifications

Absolute Maximum Ratings

All test conditions: over operating free-air temperature, unless otherwise noted. (1)

Parameter		Min	Max	Unit
Supply Voltage	V_{DD}	−0.3	20	V
Input Voltage	HI, LI	−10	20	V
Output Voltage	LO (DC)	−0.3	V_{DD} + 0.3	V
Output Voltage	LO (Pulse < 100 ns) (3)	−2	V_{DD} + 0.3	V
Bootstrap Voltage	HB	−0.3	120	V
High-Side Voltage	HB-HS	−0.3	26	V
Output Voltage	HO (DC)	V_{HS} − 0.3	V_{HB} + 0.3	V
Output Voltage	HO (Pulse < 100 ns) (3)	V_{HS} − 2	V_{HB} + 0.3	V
High-Side MOSFET Source Voltage	HS (DC)	−8	120	V
High-Side MOSFET Source Voltage	HS (Pulse < 300 ns) (3)	−12	120	V
High-Side MOSFET Source Voltage	HS (Pulse < 100 ns) (3)	−18	120	V
T_J	Maximum Operating Junction Temperature (2)	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) The IC includes over-temperature protection to protect the device during overload conditions. The junction temperature exceeds 150°C when the over-temperature protection is active. Continuous operation above the specified maximum operating junction temperature reduces lifetime.
(3) Values are verified by characterization and are not production-tested.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Min	Max	Unit
V_{ESD}	Human Body Model ESD (HBM)	per ANSI-JEDEC-JS-001-2014 specification, all pins (1)	−2	2	kV
	Charged Device Model ESD (CDM)	per ANSI-JEDEC-JS-002-2014 specification, all pins (1)	−1	1	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specifications.

Recommended Operating Conditions

Over-operating free-air temperature range unless otherwise noted

Parameter		Min	Typ	Max	Unit
V_{DD}	Supply Voltage Range	7	12	16	V
$V_{HI,LI}$	Driver Input Voltage Range	−10		VDD + 0.3	V
V_{HS}	Voltage on HS (DC)	−8		100	V
	Voltage on HS (pulse width < 100 ns)	−12		110	
V_{LO}	Voltage on LO	0		V_{DD}+ 0.3	V
V_{HO}	Voltage on HO	V_{HS}		V_{HB}+ 0.3	V
V_{SR}	Slew Rate on HS			50	V/ns
V_{HB}	Voltage on HB	V_{HS} +7, VDD −1		V_{HS} +16, 115	V
I_{BST}	Transient Internal Bootstrap Diode Current			2	A
T_J	Operating Junction Temperature	−40		150	°C

Thermal Information

Parameter	$R_{\theta JA}$	$R_{\theta JC}$	Unit
DFN4X4-8	35	41	°C/W
DFN4X4-10	35	41	°C/W
ESOP8	34.66	42.92	°C/W
SOP8	105	51	°C/W

Electrical Characteristics

All test conditions: V_{DD} = 12 V, T_J = −40°C~150°C, typical values are tested under 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply Currents						
I_{DD}	VDD Quiescent Current	V_{HI} = V_{LI} = 0	200	334	500	μA
I_{DDO}	VDD Operating Current	f_{SW} = 500 kHz, C_{Load} = 0 nF	1.5	2.46	4.5	mA
I_{HB}	HB Quiescent Current	V_{HI} = V_{LI} = 0	90	138	410	μA
I_{HBO}	HB Operating Current	f_{SW} = 500 kHz, C_{Load} = 0 nF	1.6	2.75	3.8	mA
I_{HBS}	HB to VSS Quiescent Current	V_{HS} = V_{HB} = 110 V			1	μA
I_{HBSO}	HB to VSS Operating Current	f_{SW} = 500 kHz, C_{Load} = 0 nF	0.05	0.51	0.95	mA
Inputs						
$V_{HI, LI,\_R}$	Input Logic High Threshold		1.8	2.1	2.4	V
V_{HI, LI_F}	Input Logic Low Threshold		0.8	1.14	1.5	V
V_{HI, LI_Hys}	Hysteresis			0.96		V
Undervoltage Protection (UVLO)						
V_{DDR}	VDD Rising Threshold		6.1	6.55	6.85	V
V_{DDF}	VDD Falling Threshold		5.7	6.15	6.5	V
V_{DDHYS}	VDD Threshold Hysteresis			0.33		V
V_{HBR}	HB Rising Threshold		5.3	5.78	6.17	V
V_{HBF}	HB Falling Threshold		4.9	5.27	5.7	V
V_{HBHYS}	HB Threshold Hysteresis			0.38		V
LO Gate Driver						
V_{LOH}	Output High Voltage	I_{OUT} = −100 mA, V_{LOH} = V_{DD} − V_{LO}	50	108	220	mV
V_{LOL}	Output Low Voltage	I_{OUT} = 100 mA	18	36	70	mV
I_{LOSRC}	Output Source Peak Current	C_{Load} = 10 nF, V_{LO} = 0 V		3.5		A
I_{LOSINK}	Output Sink Peak Current	C_{Load} = 10 nF, V_{LO} = 12 V		6.5		A
R_{LOH}	Output Pull High Resistance	I_{OUT} = −100 mA	0.5	1	2.2	Ω
R_{LOL}	Output Pull Low Resistance	I_{OUT} = 100 mA	0.18	0.4	0.7	Ω
HO Gate Driver						
V_{HOH}	Output High Voltage	I_{OUT}= −100 mA, V_{HOH} = V_{HB} − V_{HO}	50	104	220	mV
V_{HOL}	Output Low Voltage	I_{OUT} = 100 mA	20	41	75	mV
I_{HOSRC}	Output Source Peak Current	C_{Load} = 10 nF, V_{HO} = 0 V		3.5		A
I_{HOSINK}	Output Sink Peak Current	C_{Load} = 10 nF, V_{HO} = 12 V		6.5		A
R_{HOH}	Output Pull High Resistance	I_{OUT} = −100 mA	0.5	1	2.2	Ω
R_{HOL}	Output Pull Low Resistance	I_{OUT} = 100 mA	0.2	0.4	0.75	Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Bootstrape Diode						
V_{FL}	Low Current Forward Voltage	I_{VDD} − HB = 100 uA	0.8	1.266	2.1	V
V_{FH}	High Current Forward Voltage	I_{VDD} – HB = 100 mA	1.4	1.899	2.8	V
R_D	Dynamic Resistance			3.998	10	Ω
Output Rise and Fall Time						
T_{DLFF}	VLI falling to VLO falling	C_{Load} = 10 pF		27.6		ns
T_{DHFF}	VHI falling to VHO falling	C_{Load} = 10 pF		29.4		ns
T_{DLRR}	VLI rising to VLO rising	C_{Load} = 10 pF		29.2		ns
T_{DHRR}	VHI rising to VHO rising	C_{Load} = 10 pF		29.4		ns
T_R	LO, HO Rise Time	C_{Load} = 1.8 nF		10.94		ns
T_F	LO, HO Fall Time	C_{Load} = 1.8 nF		5.63		ns
Delay Matching						
T_{MON}	HO OFF to LO ON			2		ns
T_{MOFF}	LO OFF to HO ON			2		ns
Miscellaneous						
T_{MIN_ON}	Minimum Input Pulse Width			9		ns
$T_{IN\_Deglitch}$	Input Deglitch Time			15		ns

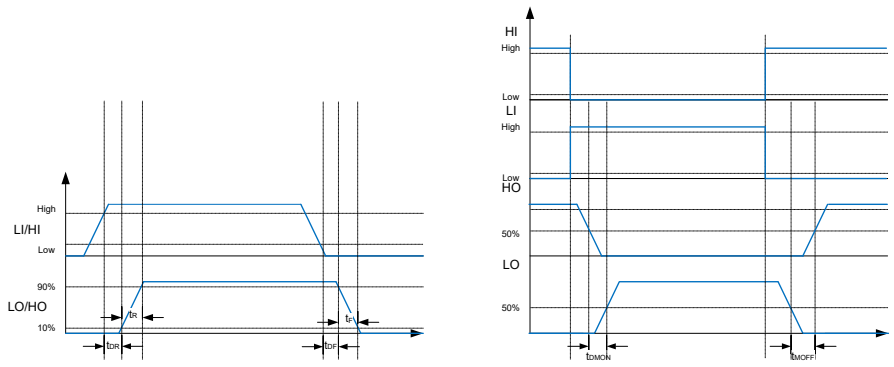
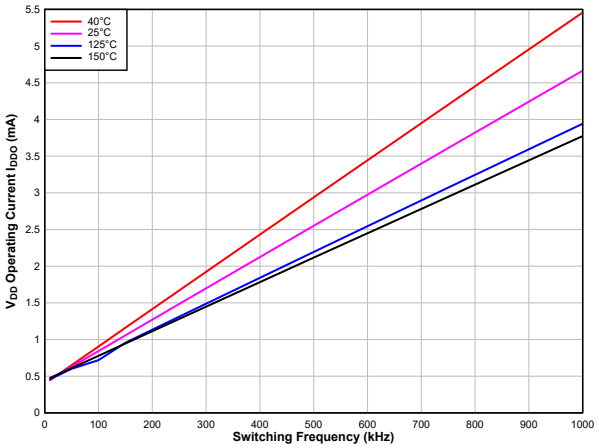


Figure 1. Timing Diagram

Typical Performance Characteristics

All test conditions: V_{DD} = V_{HB} = 12 V, V_{HS} = V_{SS} = 0 V, no load on outputs, unless otherwise noted.



C_L = 0 F, V_{DD} = V_{HB} = 12 V

Figure 2. I_{DD} Operating Current vs. Frequency

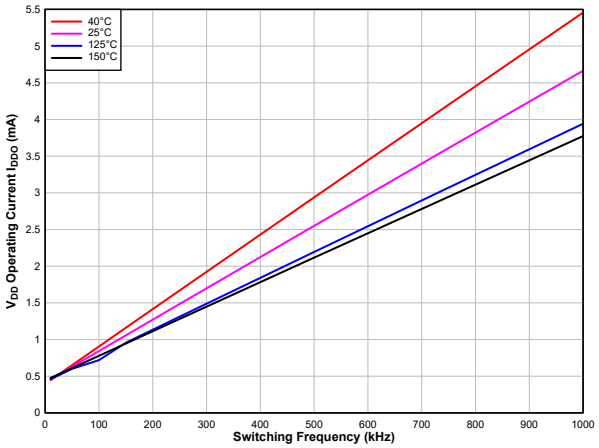


Figure 3. Boot Voltage Operating Current vs. Frequency

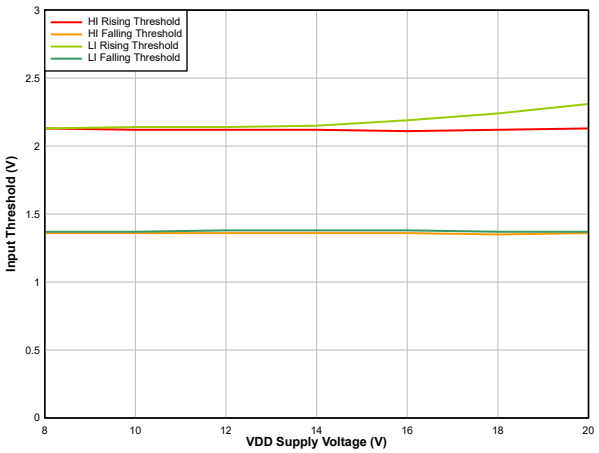


Figure 4. Input Threshold vs. Supply Voltage

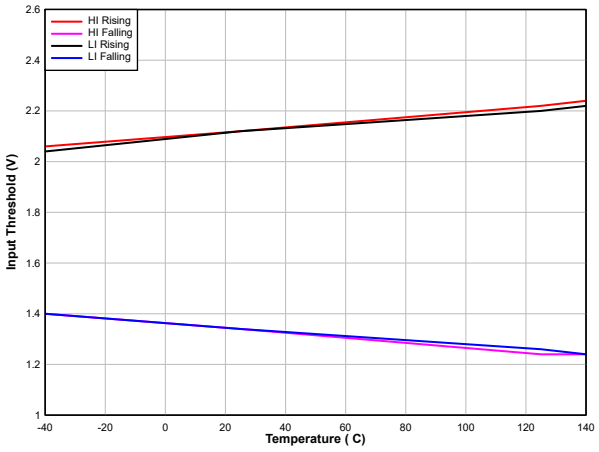


Figure 5. Input Threshold vs. Temperature

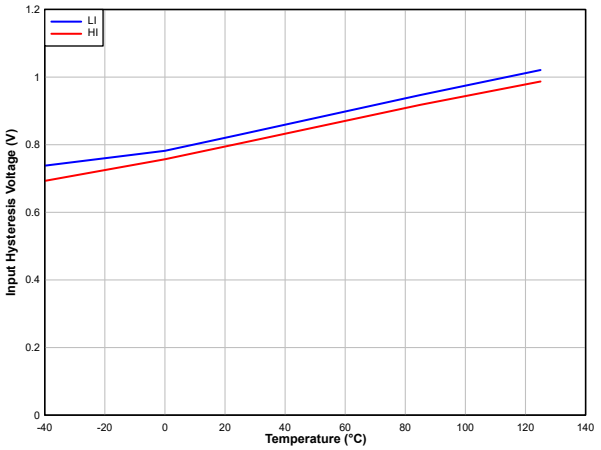


Figure 6. Input Hysteresis vs. Temperature

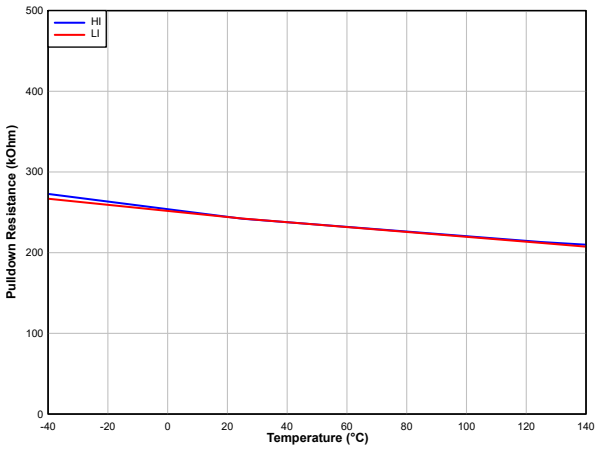
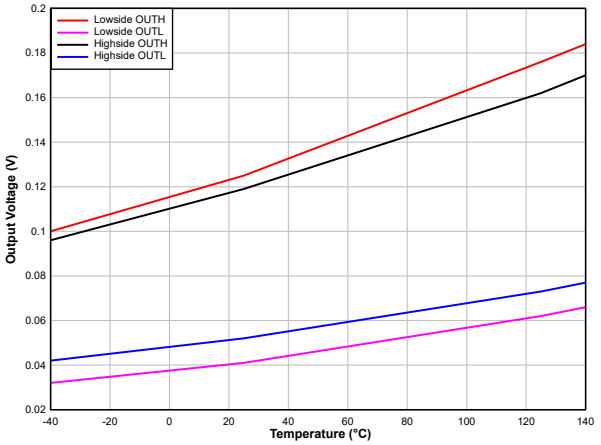


Figure 7. Input Resistance vs. Temperature



I_{OUT} = 100 mA

Figure 8. Output Voltage vs. Temperature

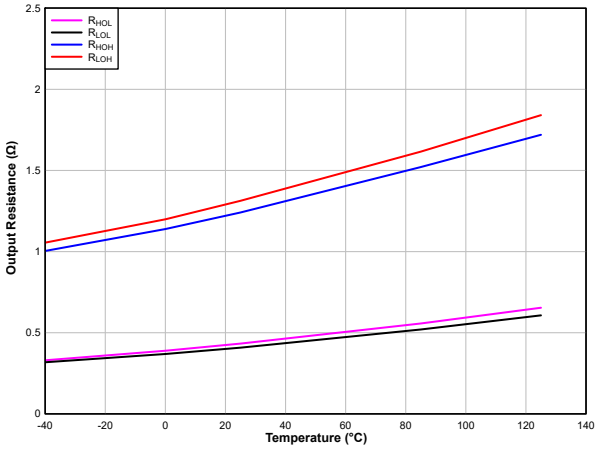


Figure 9. Driver Output Resistance vs. Temperature

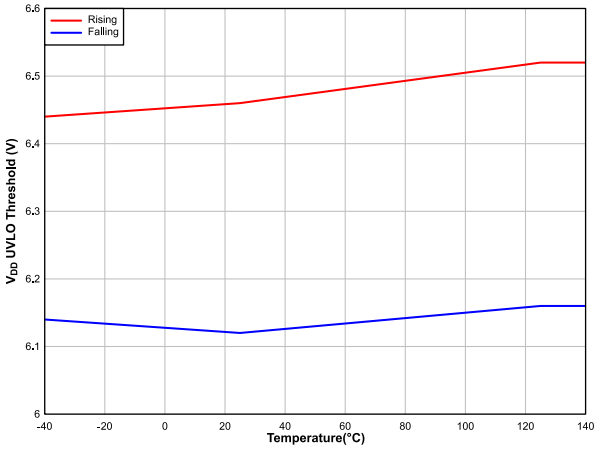


Figure 10. V_{DD} UVLO Threshold vs. Temperature

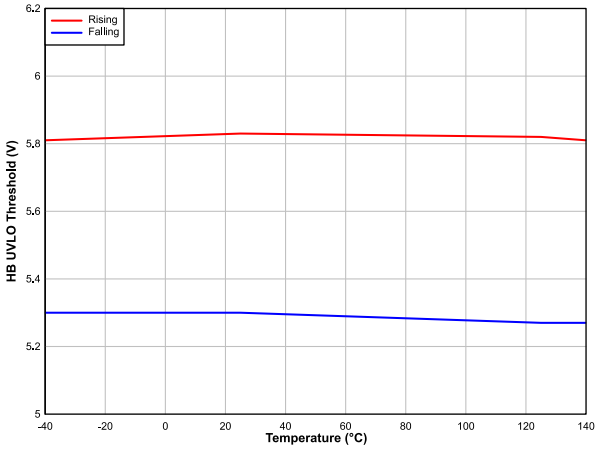


Figure 11. HB UVLO Threshold vs. Temperature

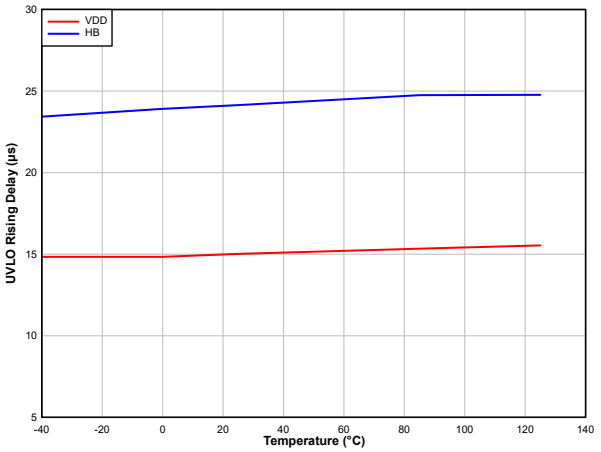


Figure 12. UVLO Rising Delay vs. Temperature

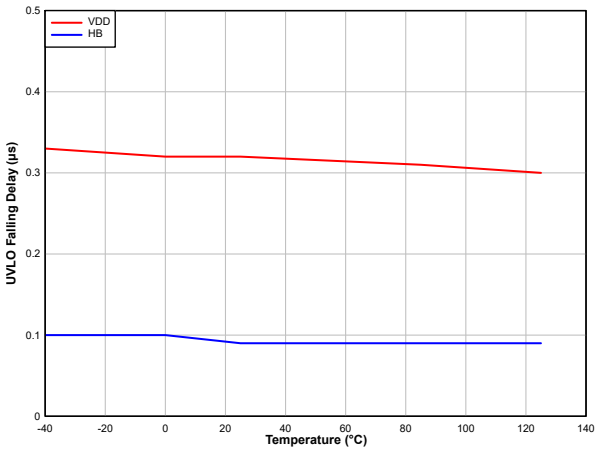


Figure 13. UVLO Falling Delay vs. Temperature

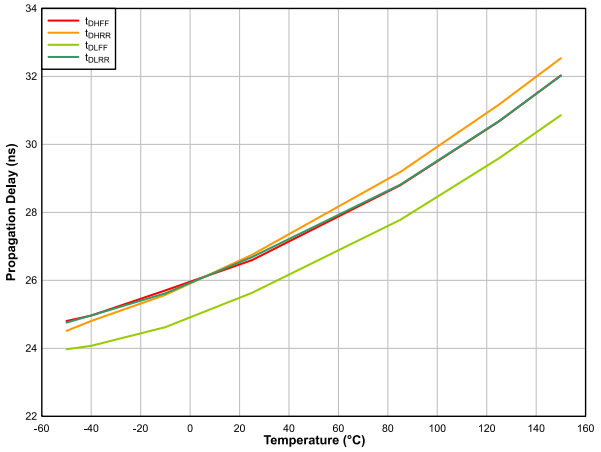


Figure 14. Propagation Delays vs. Temperature

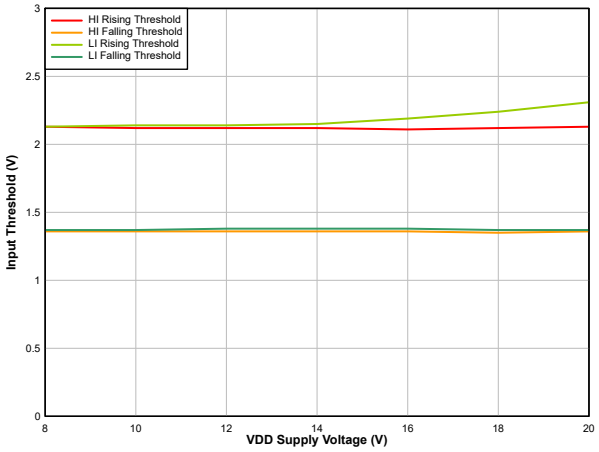


Figure 15. Propagation Delay vs. Supply Voltage

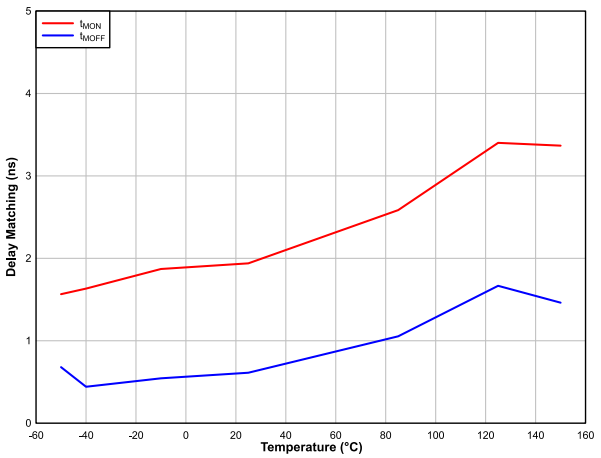


Figure 16. Delay Matching vs. Temperature

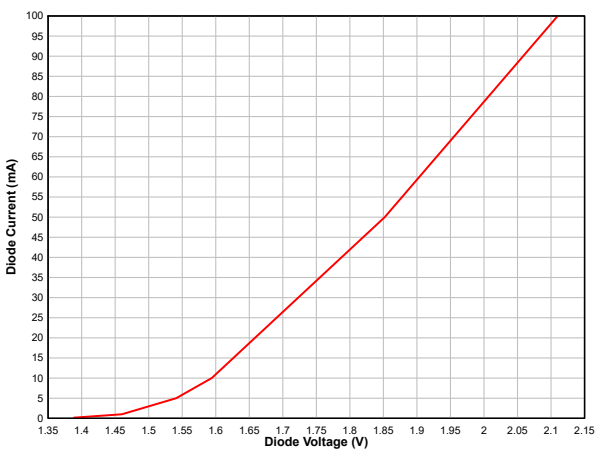


Figure 17. Diode Current vs. Diode Voltage

Detailed Description

Overview

The TPM27211 is a high-side and low-side MOSFET driver, featuring independent inputs for each side, providing ultimate flexibility in controlling application signals. It includes an integrated boot diode for the bias supply of the high-side driver and is compatible with TTL logic inputs. The high-side driver operates in reference to the switch node (HS), typically connected to the source of the high-side MOSFET and the drain of the low-side MOSFET. The low-side driver is grounded at VSS. Key functions include input stages, under-voltage lockout (UVLO) protection, level shifting, the integrated boot diode, and output driver stages.

Table 3. The TPM27211 Device Logic

HI	LI	HO	LO
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H

Functional Block Diagram

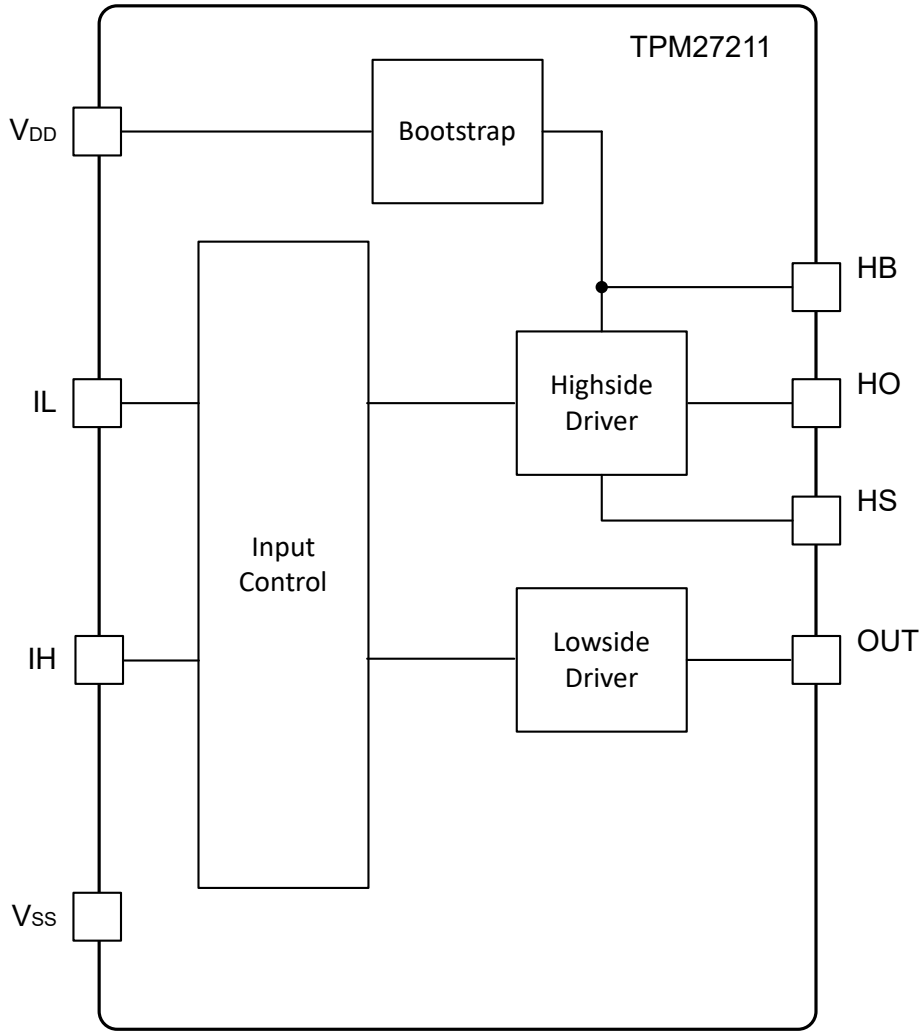


Figure 18. Functional Block Diagram

Feature Description

Under-Voltage Lockout (UVLO)

The gate driver incorporates under-voltage lockout (UVLO) protection for the bias supplies of both the high-side and low-side drivers, ensuring that the operation stops when voltages fall below the critical thresholds. The V_{DD} UVLO safeguards the entire system by disabling both drivers if V_{DD} is below 7.0 V, with a re-enabling threshold at 7.5 V, while the V_{HB} UVLO specifically targets the high-side driver, engaging if the V_{HB} to V_{HS} differential is below 6.7 V and re-enabling at 7.8 V. These features provide a reliable and stable operation with hysteresis to prevent oscillation around the threshold points.

Input Stage

The TPM27211 features input stages that facilitate PWM signal interfacing with specific characteristics. It is designed with a pseudo-CMOS input structure offering significant hysteresis and compatibility with various PWM controllers. The TPM27211

has a nominal impedance of 70 kΩ with the same capacitance of approximately 2 pF and a pull-down resistance to ground of 70 kΩ. It provides a more standard logic-level input with a rising threshold at 2.3 V and a falling threshold at 1.6 V.

The TPM27211 input stage withstands the negative voltage as low as −10 V to improve system robustness.

Bootstrap Diode

The TPM27211 drivers include an integrated boot diode for generating the high-side bias voltage. This diode has its anode connected to V_{DD} and its cathode connected to V_{HB}. The V_{HB} capacitor which is linked to both the HB and HS pins, is recharged during each switching cycle when the HS pin goes to the ground. The boot diode is designed to offer fast recovery, low resistance, and a voltage rating margin, ensuring efficient and dependable performance.

Output Stages

The output stages of the driver serve as the link to the power MOSFETs in the power train. They are designed for high efficiency, with characteristics, such as high slew rate, minimal resistance, and the ability to handle high peak currents, ensuring that the power MOSFETs switch effectively. The low-side output stage operates with a reference from V_{DD} to V_{SS}, while the high-side output stage is referenced between V_{HB} and V_{HS}.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

Driver Power Dissipation

The power dissipation of the gate driver consists of two parts: quiescent power (P_{DC}) and switching power (P_G).

The DC component of power loss in the driver is given by:

$$P_{DC} = I_Q \times V_{DD} \quad (1)$$

Where:

I_Q represents the quiescent current of the driver. This current is used to power all the internal circuits.

The power P_G is lost in the resistive components of the circuit during the MOSFET/IGBT switching transitions. Approximately half of this power is expended when the load capacitor charges on turn-on, and the other half is lost when the load capacitor discharges on turn-off. Without the use of an external gate resistor between the driver and the MOSFET/IGBT, the entire P_G is dissipated within the driver package itself. However, by incorporating external gate-drive resistors, the power dissipation is distributed between the internal resistance of the driver and the external gate resistors, effectively sharing the thermal load.

$$P_G = Q_g \times V_{DD} \times f_{SW} \quad (2)$$

Where:

- Q_g is the gate charge of the power device;
- f_{SW} is the switching frequency;
- V_{DD} is the supply voltage.

If R_G is applied between the driver and the gate of the power device to slow down the power device transition, the power dissipation of the driver is shown below:

$$P_G = \frac{1}{2} \times Q_g \times V_{DD} \times f_{SW} \times \left(\frac{R_{OL}}{R_{OL} + R_G} + \frac{R_{OH}}{R_{OH} + R_G} \right) \quad (3)$$

where

- R_{OH} is the equivalent pull-up resistance of the TPM27211;
- R_{OL} is the pull-down resistance of the TPM27211;
- R_G is the gate resistance between the driver output and the gate of the power device.

Typical Application

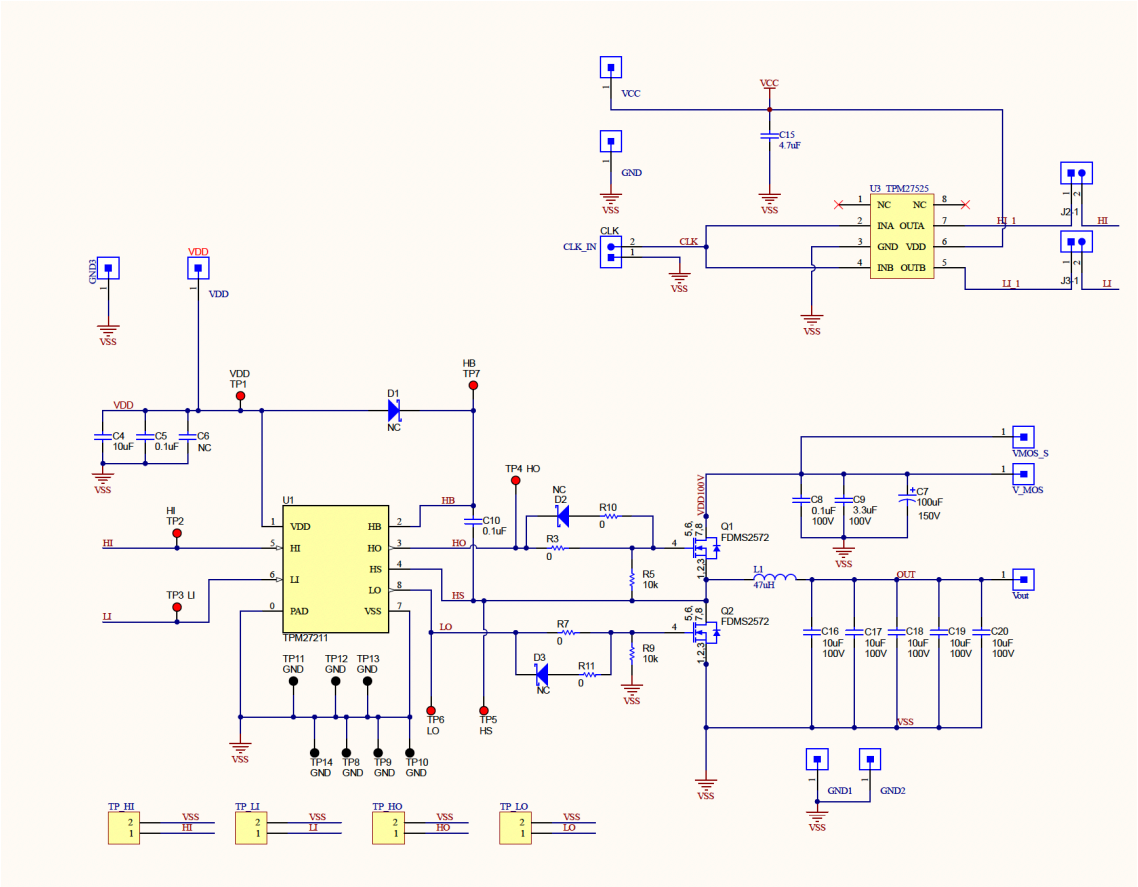
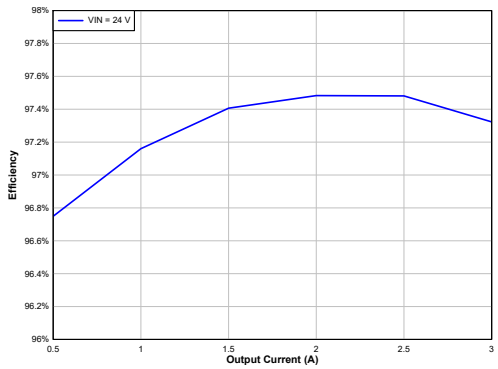
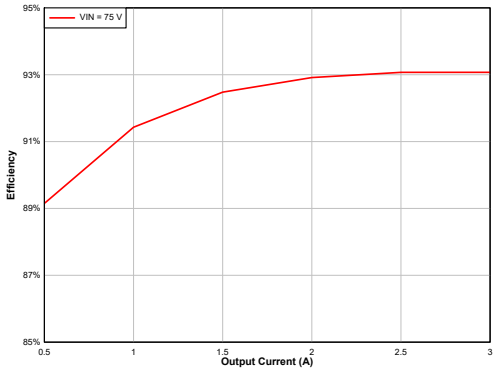


Figure 19. Typical Application



V_{IN} = 24 V, V_{OUT} = 12 V， V_{DD} = 12 V, *f* = 300 kHz

Figure 20. Efficiency



V_{IN} = 75 V, V_{OUT} = 12V, V_{DD} = 12 V, *f* = 300 kHz

Figure 21. Efficiency

Layout

Layout Guideline

- For the voltage mode input driver, a low ESR and ESL capacitor should be placed close to VCC and VEE pins, and make the loop from VCC to VEE small.
- For the current mode input driver, a low ESR and ESL capacitor should be placed close to the cathode and anode pins.
- To ensure isolation performance between the primary and secondary sides, avoid placing any PCB traces or copper below the driver device. A PCB cutout or groove is recommended to increase the creepage distance.
- To enhance thermal performance, a PCB copper connected with VCC and VEE is recommended to be enlarged.
- Use the Kelvin source to decouple the power loop and driver loop.

Layout Example

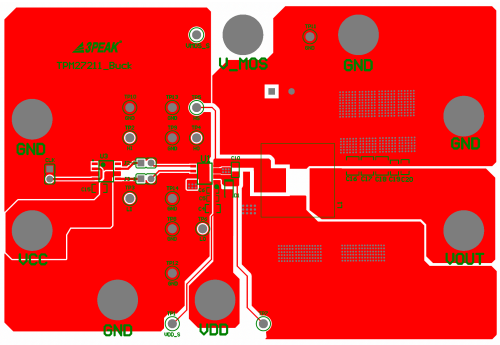


Figure 22. Top Layer

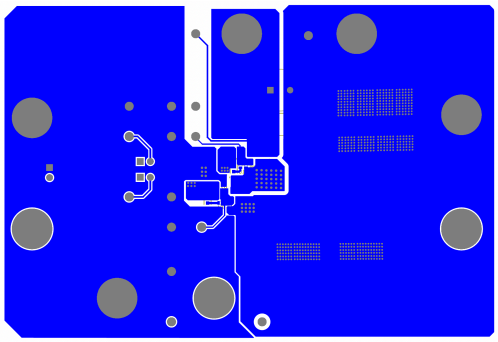


Figure 23. Bottom Layer

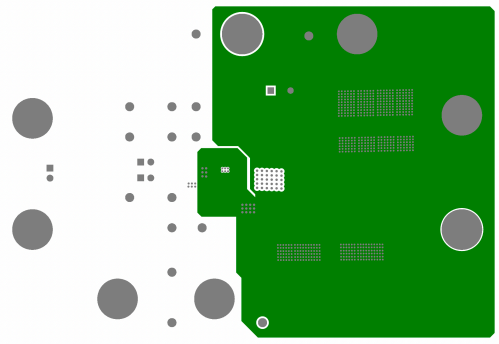


Figure 24. M1 Layer

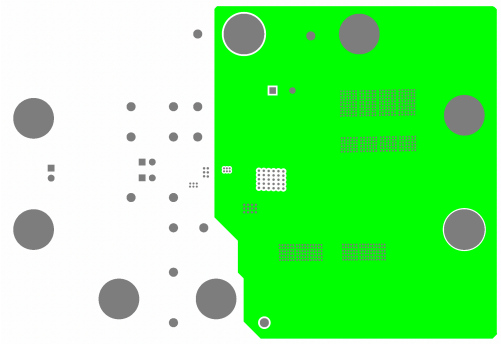
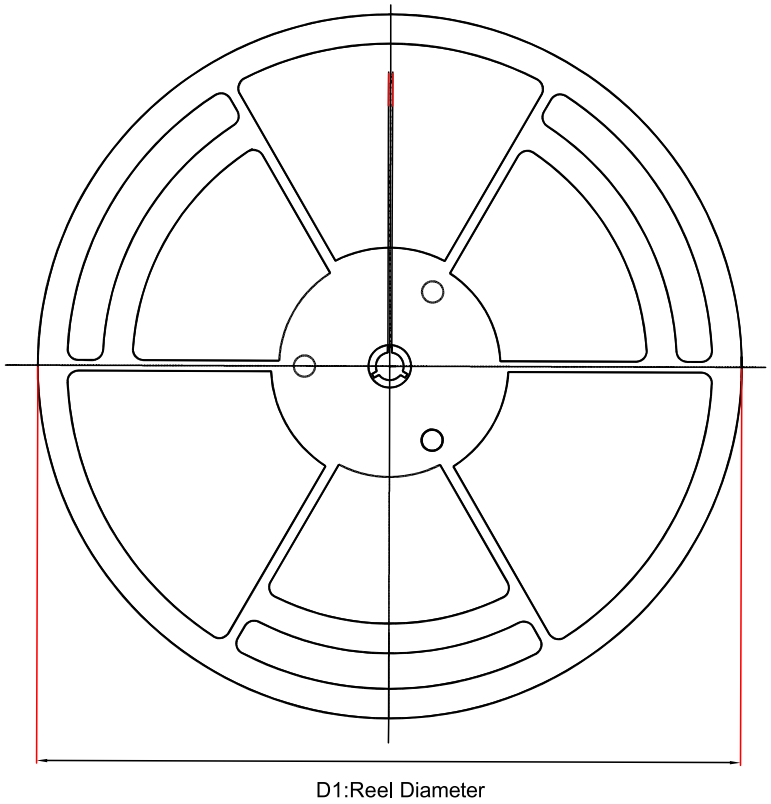
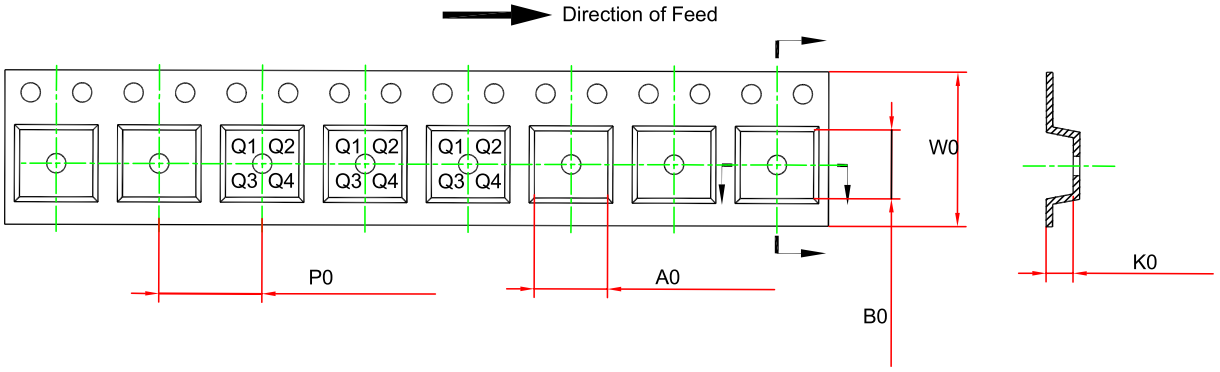


Figure 25. M2 Layer

Tape and Reel Information



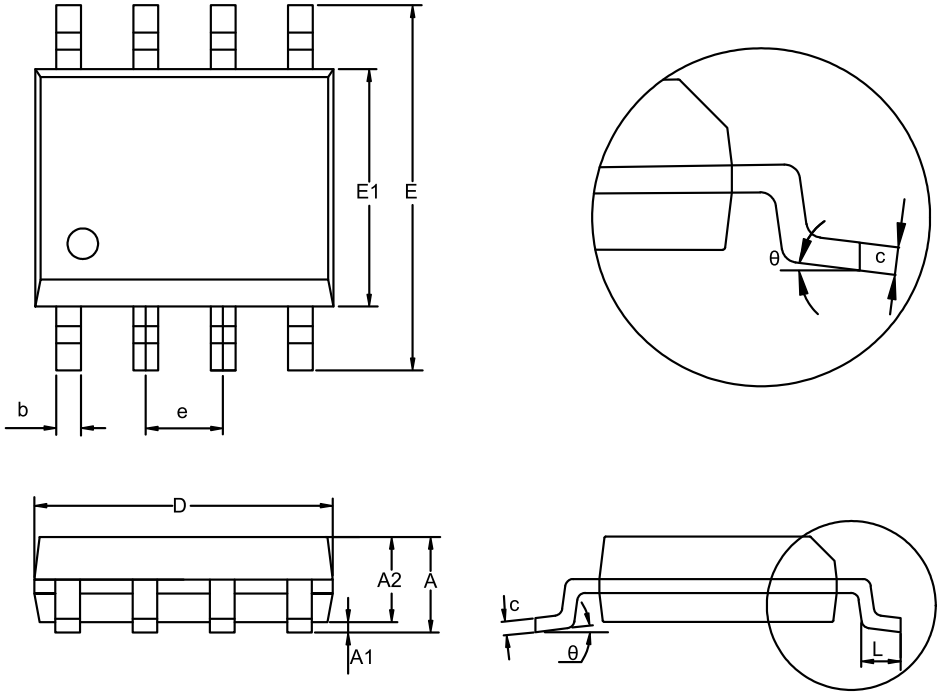


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM27211-ES1R	ESOP8	330	17.6	6.4	5.4	2.1	8	12	Q1
TPM27211-SO1R	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TPM27211-DFMR	DFN4X4-8	330	17.6	4.3	4.3	1.1	8	12	Q2
TPM27211-DF9R	DFN4X4-10	330	17.6	4.3	4.3	1.1	8	12	Q2

Package Outline Dimensions

ESOP8

Package Outline Dimensions ES1(ESOP-8-F)



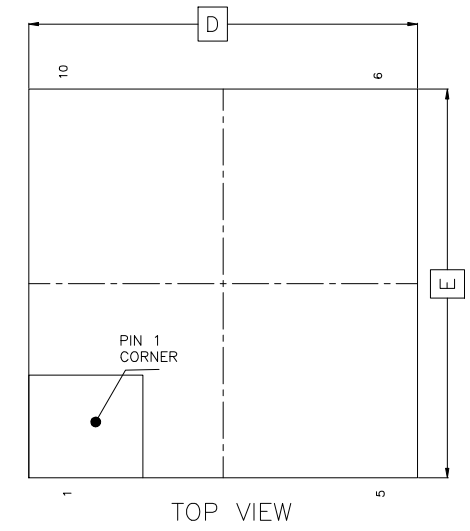
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	2.850	3.250	0.112	0.128
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
E2	1.950	2.360	0.077	0.093
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0	8°	0	8°

NOTES

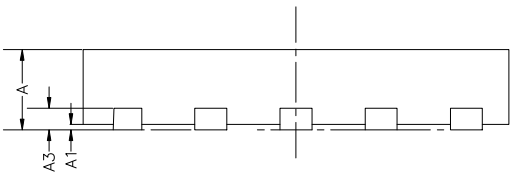
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

DFN4X4-10

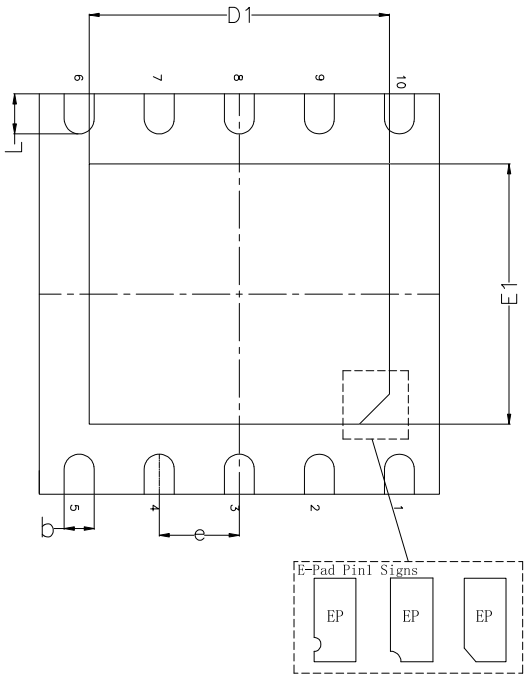
Package Outline Dimensions DF9(DFN4X4-10-A)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

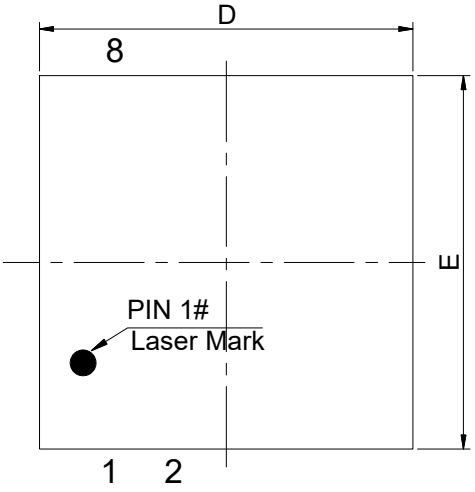
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.250	0.350	0.010	0.014
A3	0.150	0.250	0.006	0.010
D	3.900	4.100	0.154	0.161
D1	2.950	3.050	0.116	0.120
E	3.900	4.100	0.154	0.161
E1	2.550	2.650	0.100	0.104
e	0.800 BSC		0.031 BSC	
L	0.350	0.450	0.014	0.018

NOTES

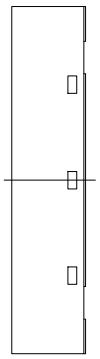
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

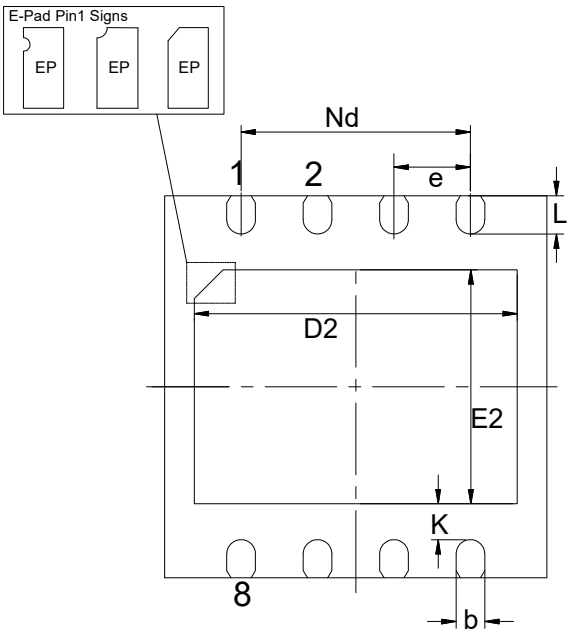
DFN4X4-8

Package Outline Dimensions DN4(DFN4X4-8-C)

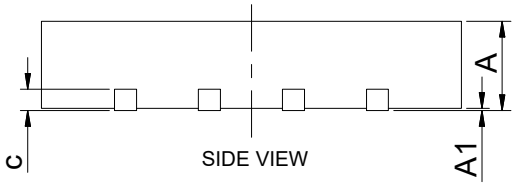


TOP VIEW





BOTTOM VIEW



SIDE VIEW

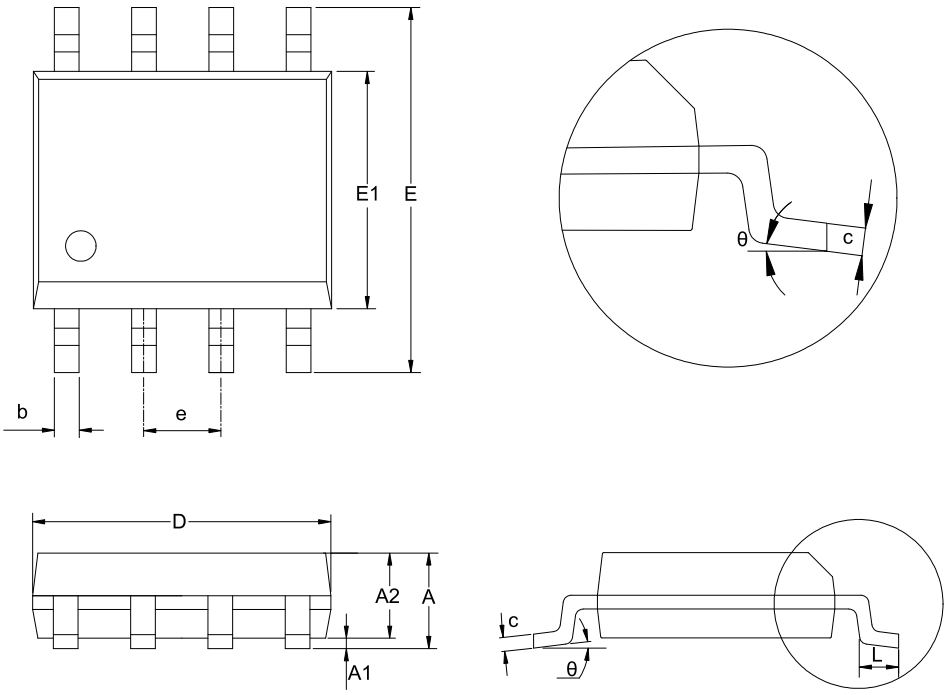
NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.031	0.035
A1	0.000	0.050	0.000	0.002
b	0.250	0.350	0.010	0.014
c	0.203 REF		0.008 REF	
D	3.900	4.100	0.154	0.161
E	3.900	4.100	0.154	0.161
D2	3.280	3.480	0.129	0.137
E2	2.350	2.550	0.093	0.100
e	0.800 BSC		0.031 BSC	
L	0.350	0.450	0.014	0.018
Nd	2.400 BSC		0.094 BSC	
K	0.375 REF		0.015 REF	

SOP8

Package Outline Dimensions SO1(SOP-8-B)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	1.550	0.049	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.000	0.016	0.039
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPM27211-ES1R	−40 to 125°C	ESOP8	27211	MSL1	Tape and Reel, 4000	Green
TPM27211-SO1R (1)	−40 to 125°C	SOP8	27211	MSL1	Tape and Reel,4000	Green
TPM27211-DF9R (1)	−40 to 125°C	DFN4X4-10	27211	MSL3	Tape and Reel,3000	Green
TPM27211-DFMR	−40 to 125°C	DFN4X4-8	27211	MSL1	Tape and Reel,3000	Green

(1) Contact 3PEAK sales representatives for more information.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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