4.5-A / 5-A, Opto-Compatible 1CH Isolated Gate Driver

Features

- Single-Channel Isolated Gate Driver with Optocoupler-Compatible Input
- 4.5-A Source/5-A Sink Peak Output Current with Rail-to-Rail Output
- 14-V to 40-V Output Driver Supply Voltage
- 8-V and 12-V V_{CC} UVLO Options
- 5.7-V Reverse Polarity Voltage Handling Capability on Input Stage
- Ultra-Fast Output Driving
  - 105-ns Propagation Delay
  - 25-ns Delay Matching
  - 35-ns Pulse Width Distortion
- 5-kV_{RMS} Reinforced Isolation Rating
- ±150-kV/μs Common-Mode Transient Immunity (CMTI)
- Industrial Standard Wide-Body WSOP6 Package
- Operating Ambient Temperature T_A −40°C to +125°C
- Safety-Related Certifications: (In progress)
  - VDE Reinforced Insulation according to DIN VDE V 0884-11: 2017-01
  - 5.7-kV_{RMS} Isolation Rating per UL 1577
  - CSA Certification per IEC 60950-1, IEC 62368-1, and IEC 60601-1 End Equipment Standards
  - TÜV Certification according to EN 60950-1 and EN 61010-1
  - CQC Certification per GB4943.1-2011

Applications

- Industrial Motor-Control Drives
- Industrial Power Supplies, UPS
- Solar Inverters
- Induction Heating

Description

The TPM23513 driver is a single-channel isolated gate driver for IGBTs, MOSFETs, and SiC MOSFETs. Its input is optocoupler compatible with the industrial standard wide-body WSOP6 package. Its driving capability can support a 4.5-A source and 5-A sink current. The output stage can withstand high voltages up to 40 V and supports the latest generation of IGBT and SiC-based applications.

The TPM23513 device provides high electromagnetic immunity and low emissions at low power consumption. Its isolation channel is separated by a double-capacitive silicon dioxide (SiO2) insulation barrier. 3PEAK proprietary galvanic isolation technology supports 150 kV/μs common-mode transient immunity (CMTI), which is critical especially for SiC applications. The TPM23513 input stage emulates an opto-diode with the enhanced noise immunity. Its enhanced reliability can support high-power industrial applications.

Typical Application Circuit

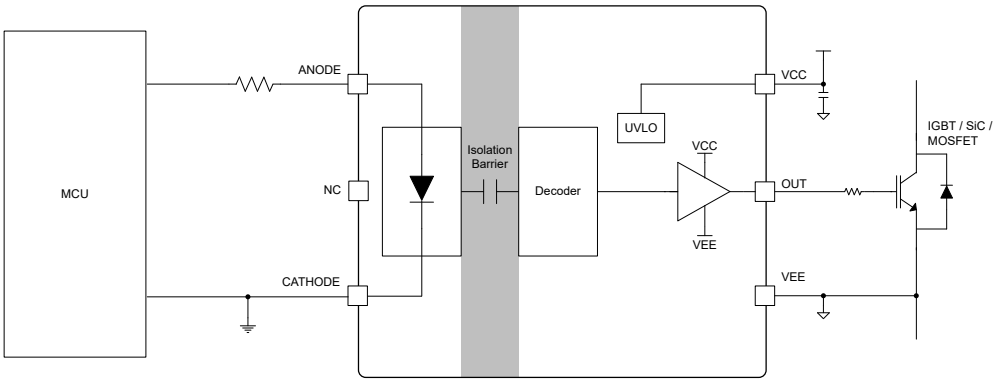


Table of Contents

Product Family Table

Order Number	UVLO Threshold (V)	Package
TPM23513-SOER	12.5	WSOP6
TPM23513B-SOER (1)	8.5	WSOP6
TPM23513-SOER-S	12.5	WSOP6
TPM23513B-SOER-S (1)	8.5	WSOP6

(1) Contact sales representatives for more details.

Revision History

Date	Revision	Notes
2023-12-04	Rev A.0	Initial release
2024-05-15	Rev A.1	Updated MSL Level and Isolation Parameters

Pin Configuration and Functions

TPM23513
WSOP6
Top View

Table 1. Pin Functions: TPM23513

Pin		I/O	Description
No.	Name		
1	ANODE	I	Emulated diode anode input
2	NC	-	No Connection
3	CATHODE	O	Emulated diode cathode input
4	VEE	P	Output power ground
5	VOUT	O	Gate driver output
6	VCC	P	Output power supply

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Input Voltage	Reverse Input Voltage, CATHODE – ANODE		8.25	V
	Average Transient Input Current, $I_{F(AVG)}$		25	mA
	Peak Transient Input Current, $I_{F(TRAN)}$		1	A
Output Voltage	Output Supply Voltage, V_{CC} − V_{EE}	−0.3	40	V
	V_{OUT}	V_{EE} − 0.3	V_{CC} + 0.3	V
T_J	Maximum Junction Temperature	−40	150	°C
T_A	Operating Ambient Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.
(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
V_{CC} – V_{EE}	Output Supply Voltage (TPM23513 12V UVLO)	14	40	V
V_{CC} – V_{EE}	Output Supply Voltage (TPM23513B 8V UVLO)	10	40	V
V_{OUT}	Output Voltage	V_{EE}	V_{CC}	V
$I_{F(ON)}$	Input Diode Forward Current, on-state	7	16	mA
$V_{F(OFF)}$	Input Diode Forward Voltage, off-state	−6	0.9	V
T_J	Junction Temperature	−40	150	°C
T_A	Operating Ambient Temperature	−40	125	°C

Safety Limiting Values

Parameter		Test Conditions	Min	Typ	Max	Unit
I_S	Safety input, output, or supply current	R_{QJA} = 120 °C/W, V_I = 15 V, T_J = 150 °C, T_A = 25 °C			50	mA
		R_{QJA} = 120 °C/W, V_I = 30 V, T_J = 150 °C, T_A = 25 °C			25	
P_S	Safety input, output, or total power	R_{QJA} = 120 °C/W, T_J = 150 °C, T_A = 25 °C			750	mW
T_S	Maximum safety temperature				150	°C

Insulation Specifications

Parameter		Conditions	Value	Unit
CLR	External Clearance	Shortest terminal-to-terminal distance through air	> 8.5	mm
CPG	External Creepage	Shortest terminal-to-terminal distance across the package surface	> 8.5	mm
DTI	Distance through the Insulation	Minimum internal gap (internal clearance)	> 22	μm
CTI	Comparative Tracking Index		> 600	V
	Material Group		I	
	Installation Classification	For Rated Mains Voltage ≤ 300 V_{RMS}	I-III	
	Pollution Degree		2	
	Climate Category		40/125/21	
C_{IO}	Isolation Capacitance	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	0.5	pF
R_{IO}	Isolation Resistance	V_{IO} = 500 V, T_A = 25 °C	> 10^9	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125 °C	> 10^{10}	
		V_{IO} = 500 V, T_A = 150 °C	> 10^{11}	
V_{IORM}	Maximum Repetitive Isolation Voltage	AC voltage (bipolar)	1500	V_{PK}
V_{IOWM}	Maximum Working Isolation Voltage	AC voltage; TDDB Test	1060	V_{RMS}
		DC voltage	1500	V_{DC}
V_{IOTM}	Maximum Transient Isolation Voltage	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production)	8000	V_{PK}
V_{IOSM}	Maximum Surge Isolation Voltage	Test method per IEC 62368-1, 1.2/50 μs waveform, V_{TEST} = 1.3 × V_{IOSM}(qualification) = 11700v	9000	V_{PK}
V_{ISO}	UL 1577 Withstand Isolation Voltage	V_{TEST} = V_{ISO} = 5700 V_{RMS}, t = 60 s (in qualification), V_{TEST} = 1.2 × V_{ISO}- 6840 V_{RMS} ， t = 1 s (100% in production)	5700	V_{RMS}
q_{pd}	Apparent Charge	Method a, After Input/Output safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10 s	≤ 5	pC
		Method a, After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10 s	≤ 5	
		Method b1; At routine test (100% production) and preconditioning (type test), V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1 s	≤ 5	

(1) All pins on each side of the barrier tied together create a two-terminal device.

Electrical Characteristics

All test conditions: V_{CC} − V_{EE} = 14 to 40 V, V_{EE}referred as GND, T_A = −40°C to 125°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Input						
I_{FTH_R}	Input Forward Threshold Current, Rising Edge	V_{OUT} > 5 V	1.1	3.6	4.8	mA
V_F	Input Forward Voltage	I_F = 10 mA	1.8	2.05	2.4	V
V_{FTH_F}	Input Threshold Voltage, falling edge	V_{OUT} < 5 V	0.9	1.4	1.9	V
$\Delta V_F/\Delta T$	Input Forward Voltage, Temperature Coefficient	I_F = 10 mA		0.9		mV/°C
V_R	Input Reverse Breakdown Voltage	I_R = 10 μA	8.25			V
C_{IN}	Input Parasitic Capacitance	F = 0.5 MHz		15		pF
Output						
I_{OH}	Output Source Peak Current (1)	I_F = 10 mA, V_{CC} = 15 V, C_{LOAD} = 0.18 μF, V_{CC} = 0.18 μF, t_{pw} < 10 μs		4.5		A
I_{OL}	Output Sink Peak Current (1)	I_F = 10 mA, V_{CC} = 15 V, C_{LOAD} = 0.18 μF, V_{CC} = 0.18 μF, t_{pw} < 10 μs		5		A
V_{OH}	Output Voltage, V_{CC} − V_{OUT}	OUT = H, I_{OUT} = −20 mA	70	180	360	mV
V_{OL}	Output Voltage, V_{OUT} − V_{EE}	OUT = L, I_{OUT} = 20 mA		12	25	mV
I_{CC_H}	Output Quiescent Current, OUT = H	OUT = H, I_{OUT} = 0 mA	0.8	1.53	2.4	mA
I_{CC_L}	Output Quiescent Current, OUT = L	OUT = L, I_{OUT} = 0 mA	0.8	1.50	2.4	mA
Under Voltage Lockout, TPM23513 (12-V UVLO Version)						
V_{UVLO_R}	Under Voltage Lock-out Threshold, Rising Edge	OUT = H	11	12.5	13.9	V
V_{UVLO_F}	Under Voltage Lock-out Threshold, Falling Edge		10	11.5	12.9	V
V_{UVLO_HYS}	UVLO Hysteresis			1		V
Under Voltage Lockout, TPM23513B (8-V UVLO Version)						
V_{UVLO_R}	Under Voltage Lock-out Threshold, Rising Edge	OUT = H	7.8	8.95	9.8	V
V_{UVLO_F}	Under Voltage Lock-out Threshold, Falling Edge		7.05	8.35	9.2	V
V_{UVLO_HYS}	UVLO Hysteresis			0.57		V

(1) Guranteed by design

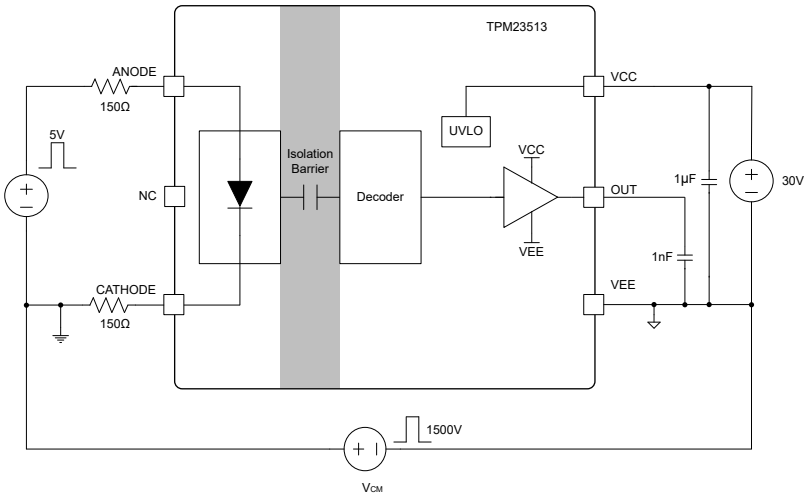
Timing Characteristics

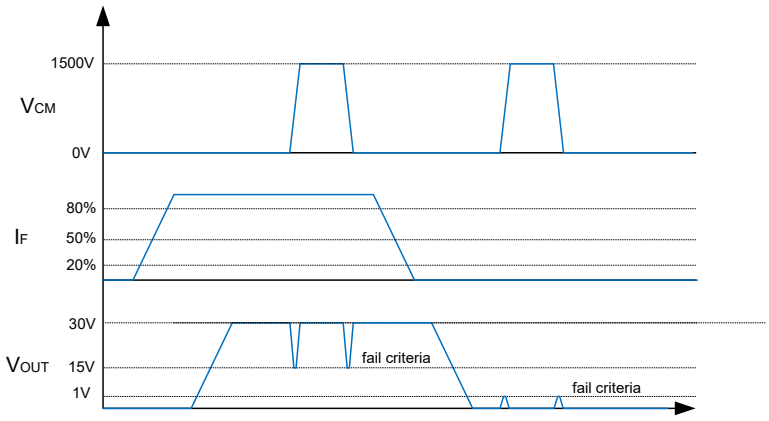
Parameter		Test Conditions	Min	Typ	Max	Unit
t_r	Output Rise Time (1)	F_{SW} = 20 kHz, (50% Duty Cycle) V_{CC} = 15 V		8.2	28	ns
t_f	Output Fall Time (1)			6.5	25	ns
t_{PLH}	Propagation Delay, Low to High			54.9	105	ns
t_{PHL}	Propagation Delay, High to Low			47.4	105	ns
t_{PWD}	Pulse Width Distortion $\|t_{PHL} - t_{PLH}\|$		-35	9.35	35	ns
$t_{sk(pp)}$	Part-to-Part Skew in Propagation Delay between any Two Parts (1)	F_{SW} = 20 kHz, (50% Duty Cycle) V_{CC} = 15 V, I_F = 10 mA			25	ns
t_{UVLO_rec}	UVLO Recovery Delay	V_{CC} Rising from 0 V to 15 V		28.8	47	μs
$CMTI_H$	Common-mode Transient Immunity (Output High)(1)	I_F= 10 mA, V_{CM} = 1500 V, VCC = 30 V, T_A = 25 °C	150			kV/μs
$CMTI_L$	Common-mode Transient Immunity (Output Low)(1)	V_F= 0 V, V_{CM} = 1500 V, VCC = 30 V, T_A = 25 °C	150			kV/μs

(1) Guranteed by design

Parameter Measurement

Driver Parameter

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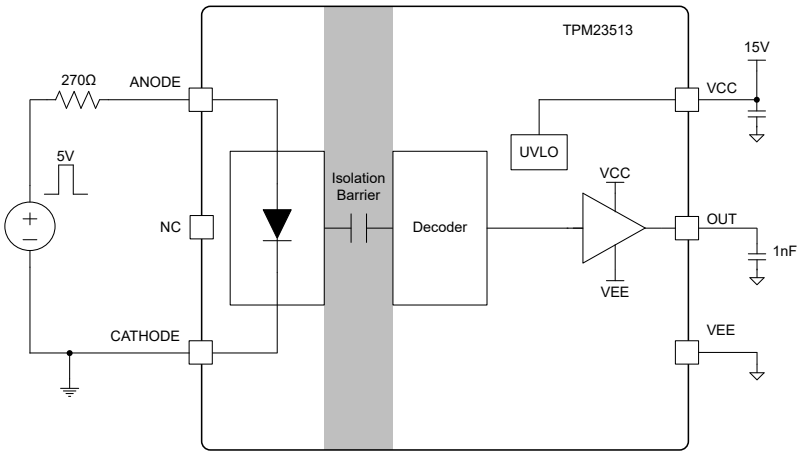
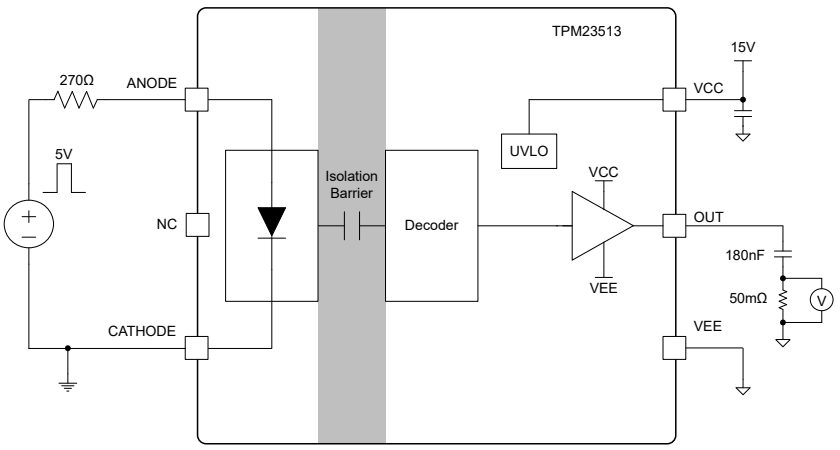
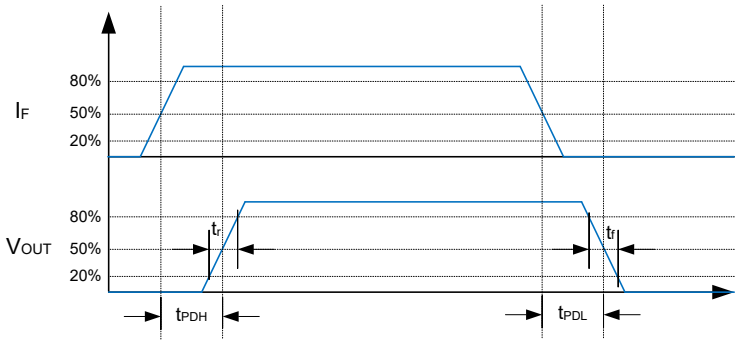
VCM
0V
80%
IF
50%
20%
30V
VOUT
15V
1V
fail criteria
fail criteria


TPM23513
15V
270Ω
ANODE
VCC
UVLO
5V
VCC
Isolation Barrier
NC
Decoder
OUT
1nF
VEE
CATHODE
VEE


TPM23513
15V
270Ω
ANODE
VCC
UVLO
5V
VCC
Isolation Barrier
NC
Decoder
OUT
180nF
50mΩ
V
VEE
CATHODE
VEE


IF
80%
50%
20%
VOUT
80%
50%
20%
tr
tf
tPDH
tPDL

Typical Performance Characteristics

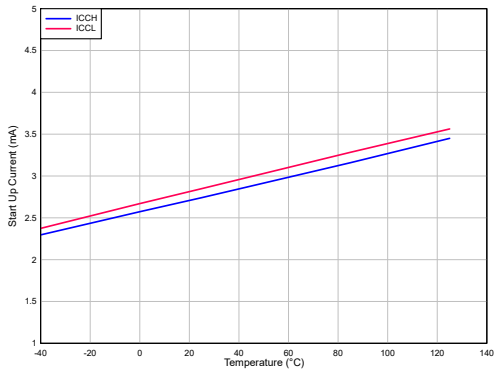


Figure 1. Start-up Current vs. Temperature

V_{CC} = 15 V

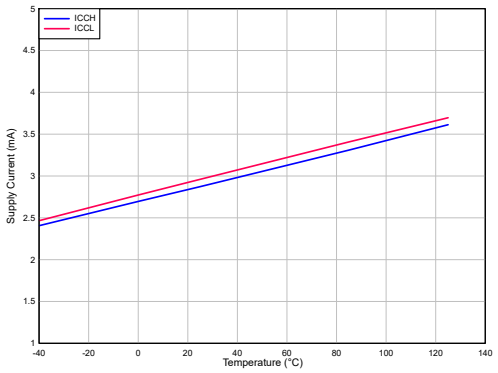


Figure 2. Start-up Current vs. Temperature

V_{CC} = 30 V

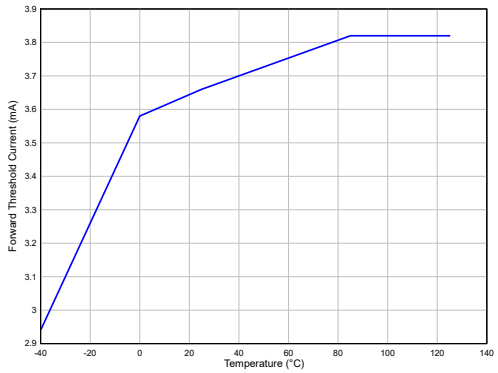


Figure 3. Forward Threshold Current vs. Temperature

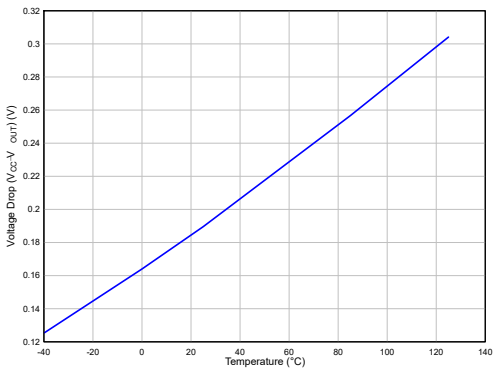


Figure 4. VOH Voltage Drop vs. Temperature

I_{OUT} = 20mA

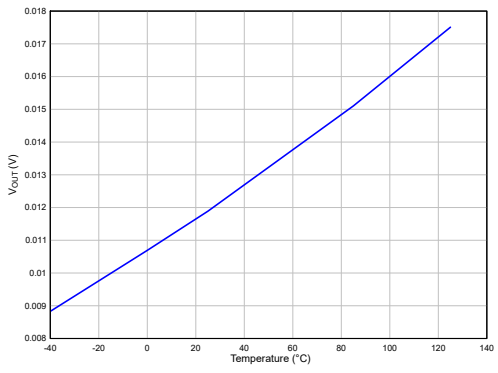


Figure 5. VOL Voltage Drop vs. Temperature

I_{OUT} = −20mA

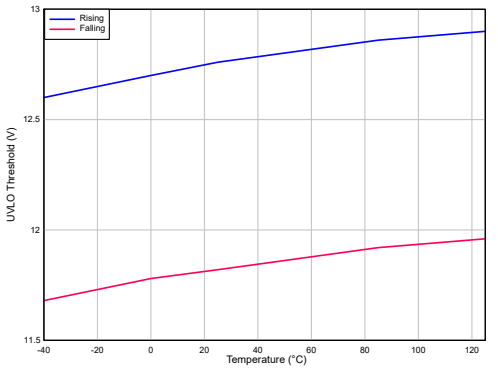


Figure 6. UVLO Threshold vs. Temperature

12-V UVLO Version

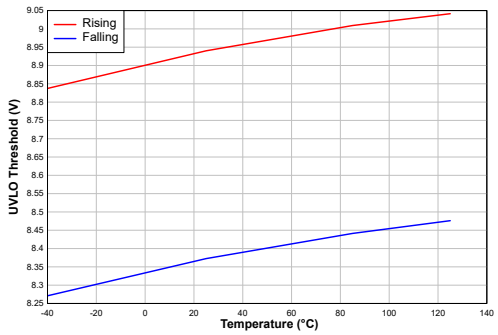


Figure 7. UVLO Threshold vs. Temperature

8-V UVLO Version

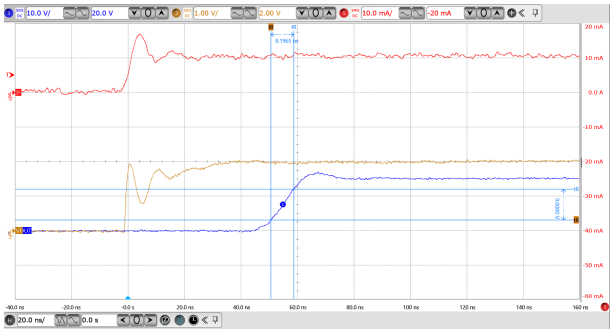


Figure 8. Output Rising Edge

Figure 9. Output Falling Edge

Detailed Description

Overview

The TPM23513 is a single-channel isolated gate driver for MOSFETs, IGBTs, and SiC FETs with optocoupler compatible input stage which is an emulated diode. It has 40-V maximum operating driver voltage, which is especially suitable for high-power fast-transient IGBT / SiC applications.

The TPM23513 is designed to replace optocoupler gate driver with industry standard wide-body 6-pin package WSOP6, with more than 8.5-mm creepage and clearance to withstand over 1060-V_{RMS}working voltage, reinforced isolation, and 5.7-$kV_{RMS}$for 60s and a surge rating of 8-k V_{PK}. 3PEAK proprietary isolation technology supports common-mode transient immunity of greater than 150 kV/μs.

Functional Block Diagram

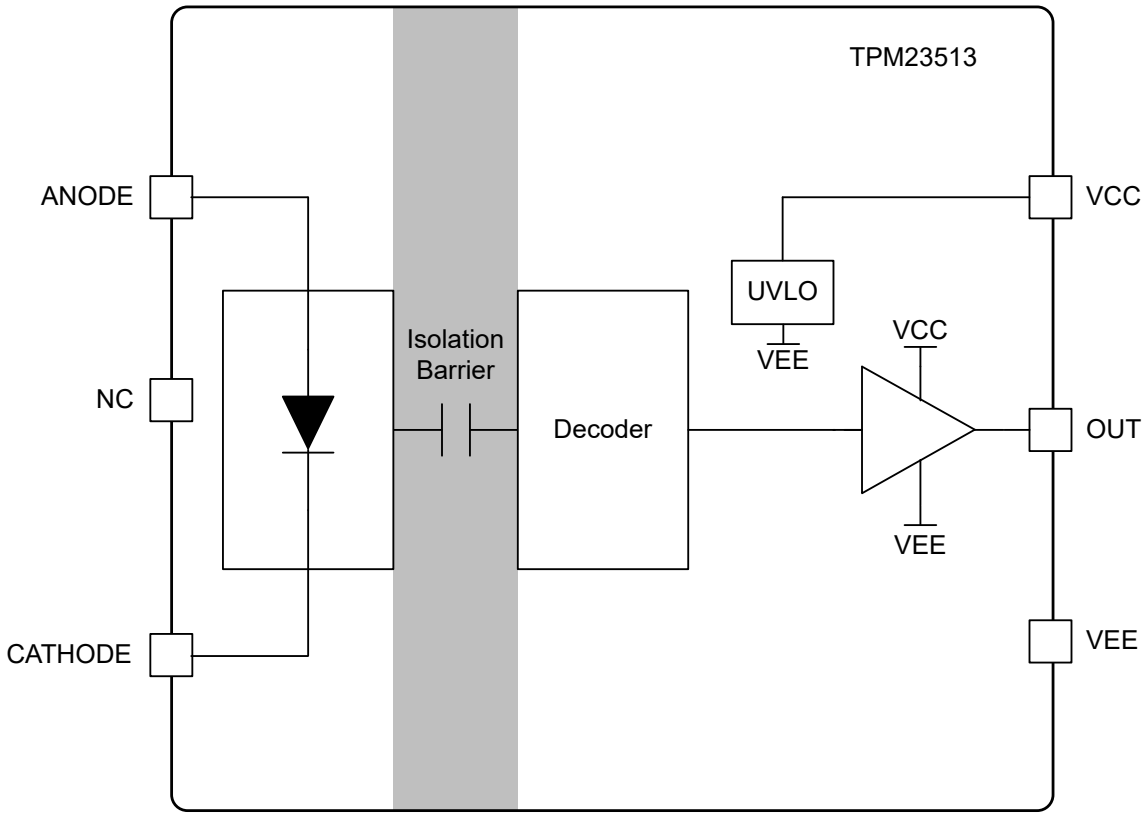


Figure 10. Functional Block Diagram

Feature Description

Emulated Diode Input

The input stage of TPM23513 is an emulated diode input to be pin-to-pin compatible with optocoupler input. Working like an opto-diode, when the current flows from ANODE and CATHODE, the forward voltage drop between ANODE and CATHODE is typical 2.1 V. An external resistor can be placed on the ANODE side or the CATHODE side or both to limit the current. 3PEAK recommends that the forward current should be from 7 mA to 30 mA. When the input current is higher than the threshold current I_{FTH_R}, the TPM23513 internal isolation transmitter starts to send CMTI-optimized high-frequency On-Off-Keying(OOK) signals through the double-capacitive silicon dioxide (SiO_2) isolation layer. 3PEAK proprietary isolation technology provides high CMTI performance against fast dV/dt scenarios, which is especially useful for latest generation applications like SiC FETs.

Decoder & Output Stage

The high-frequency signal is converted by the decoder via double-capacitive insulation barrier as the output stage's input. The rail-to-rail output stage provides high-peak current during the output slewing. The output V_{CC} supports maximum 40-V input.

The TPM23513 output stage is able to deliver high current sourcing up to 4.5 A and sinking up to 5.5 A with low propagation delay.

Protection

Under-Voltage Lock Out (UVLO)

The device has UVLO feature to monitor voltage between V_{CC} and V_{EE} to prevent under-driven working conditions. When V_{CC} rises above UVLO rising threshold, the output follows device input; when V_{CC} falls below UVLO falling threshold longer than deglitch timer, the device gets into UVLO protection and holds output low. The UVLO has hysteresis of $UVLO_{HYS}$ to prevent power supply noises during switching.

3PEAK provides 2 UVLO options, 12-V UVLO option TPM23513 and 8-V UVLO option TPM23513B.

Active Pulldown

The output stage has an under-voltage lock-out feature to protect the output driver from malfunction during low-voltage operation. When V_{CC} is lower than the UVLO threshold, the output will be driven low. When V_{CC} is higher than the UVLO threshold, the output will be operated according to the input bias state. When V_{CC} is unbiased, the output will be pulled lower to 2 V to avoid false turning on.

Short Circuit Clamping

The device has short-circuit clamping feature to clamp driver output voltage and protect IGBT/MOSFET gatefrom over-voltage breakdown or degradation. The short-circuit can withstand 500-mA for 10 µs and continuous current of 20 mA. In case of higher current conduction is required, 3PEAK recommends to use external Schottky diodes in parallel.

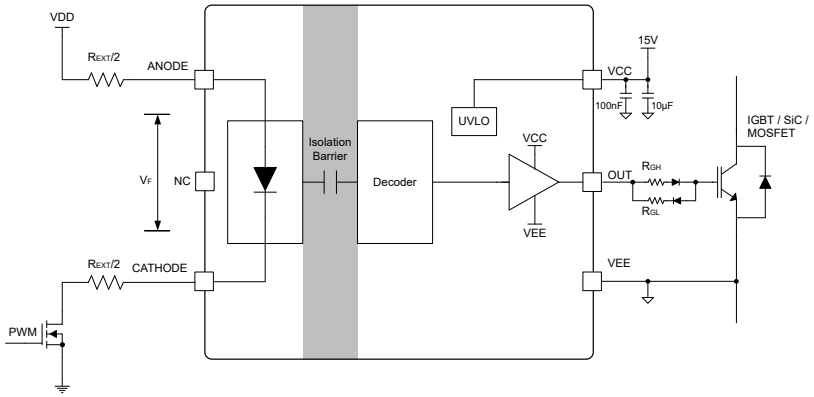
Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

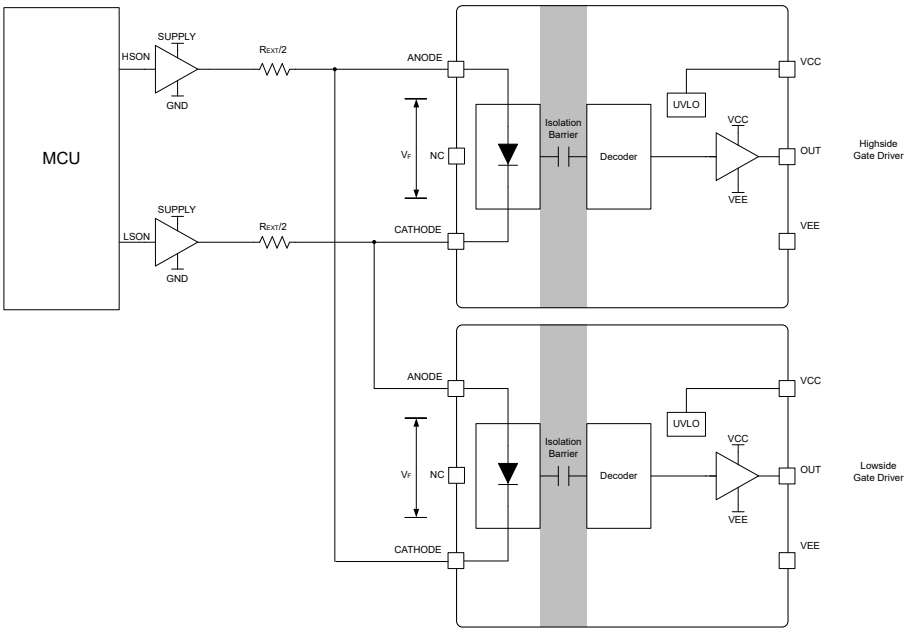
Typical Application

The TPM23513 supports pin-to-pin replacement of common opto-coupler based gate drivers. Serial resistor is added to the input path to limit current between 7 mA and 25 mA.

Lowside NMOS Driving Stage



Half-bridge Driver with interlock



For most half-bridge driver applications, 2 pcs of TPM23513 can be used with MCU interlock feature, and prevent shoot-through since the input will reject when LSON and HSON are both at high state or at low state. The reverse input voltage between ANODE and CATHODE can be as high as SUPPLY voltage, 3PEAK recommends supply voltage is set below 5.5V considering 6.5V input reverse breakdown voltage.

Input Resistor

Common MCU cannot supply large enough current to turn on the input diode. 3PEAK recommends to use an NMOS FET to drive with current limiting resistors. Serial resistor is used to limit diode current as below equation, 3PEAK recommends to use R_{EXT} between 200Ω and 300Ω.

$$R_{EXT} = \frac{V_{SUPPLY} - V_F}{I_F} - R_{BUFFER}$$

10-μF VCC capacitor and 100-nF decoupling capacitor should be placed close to device VCC node.

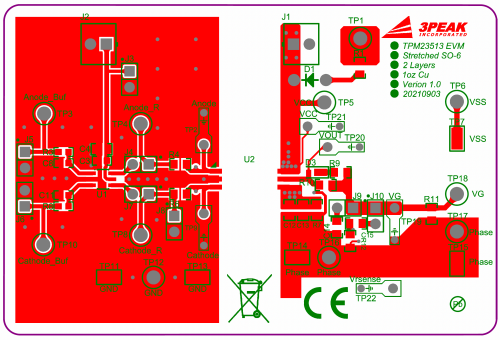
Power supply between VCC and VEE must be greater than UVLO. 3PEAK recommends 15V and above. In case of negative shutdown voltage is needed, 3PEAK recommend to seperate VEE from IGBT emitter / MOSFET source node. and tie VEE to negative voltage with reference to IGBT emitter / MOSFET source node. Total VCC-VEE should be smaller than 40V.

Layout

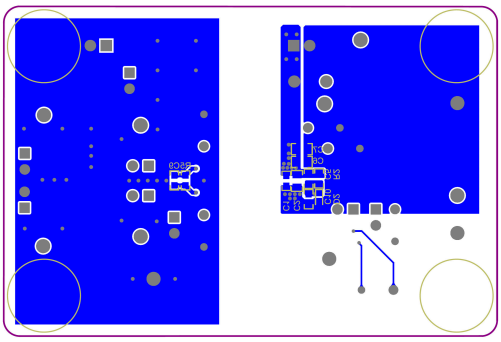
Layout Guideline

- For voltage mode input drivers, a low ESR and ESL capacitor should be placed close to the VCC and VEE pins, and the loop from VCC to VEE should be made small.
- For current mode input drivers, a low ESR and ESL capacitor should be placed close to the Cathode and Anode pins.
- To minimize the inductance of the drive circuit loop, the driver should be placed closely with the transistor.
- The Miller clamp trace should be directly connected to the transistor's gate, and the trace should be kept short.
- To ensure isolation between the primary and secondary sides, avoid placing any PCB traces or copper directly below the driver device. A PCB cutout or groove is recommended to increase the creepage distance.
- To enhance thermal performance, it is recommended to enlarge the PCB copper connected to VCC and VEE.

Layout Recommendations

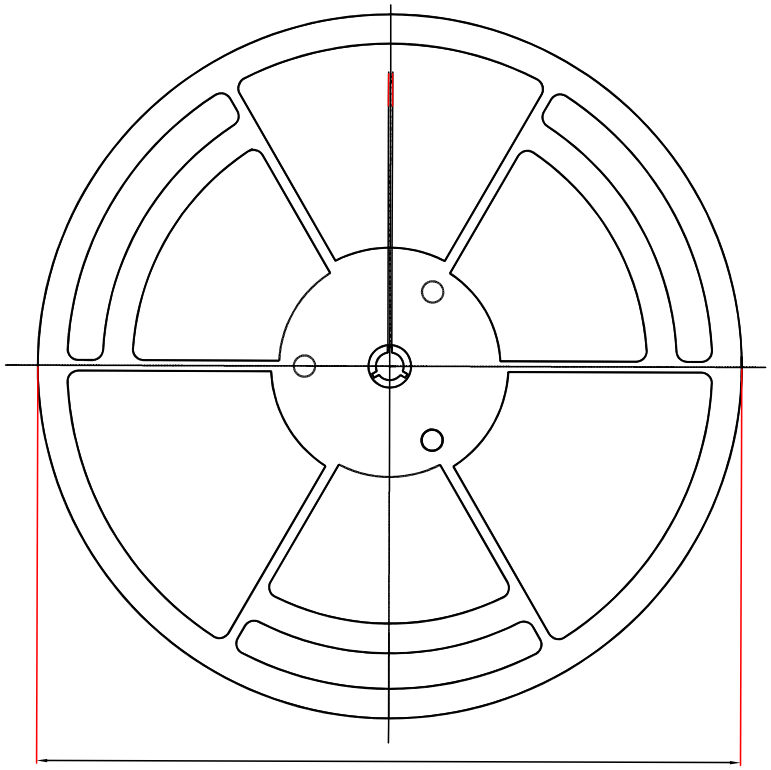


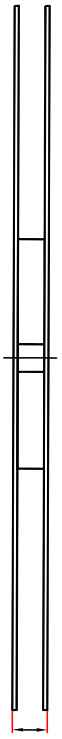
Top Layer

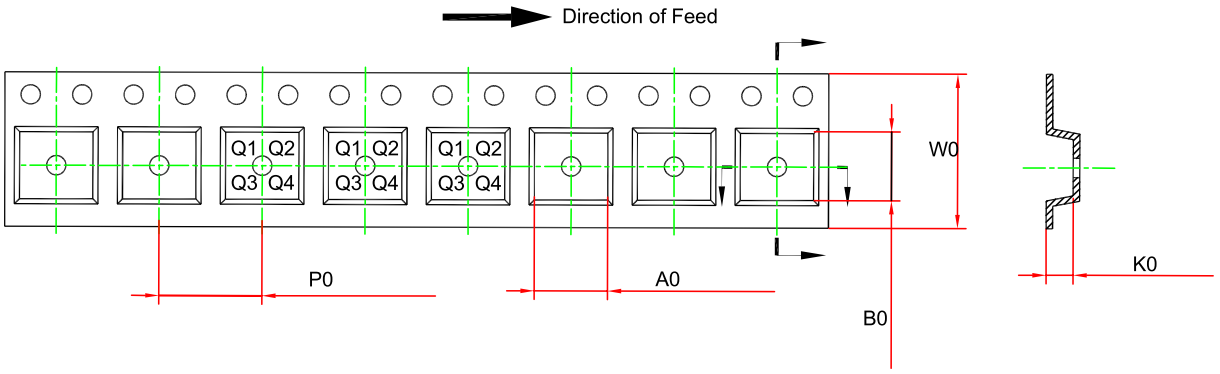


Bottom Layer

Tape and Reel Information





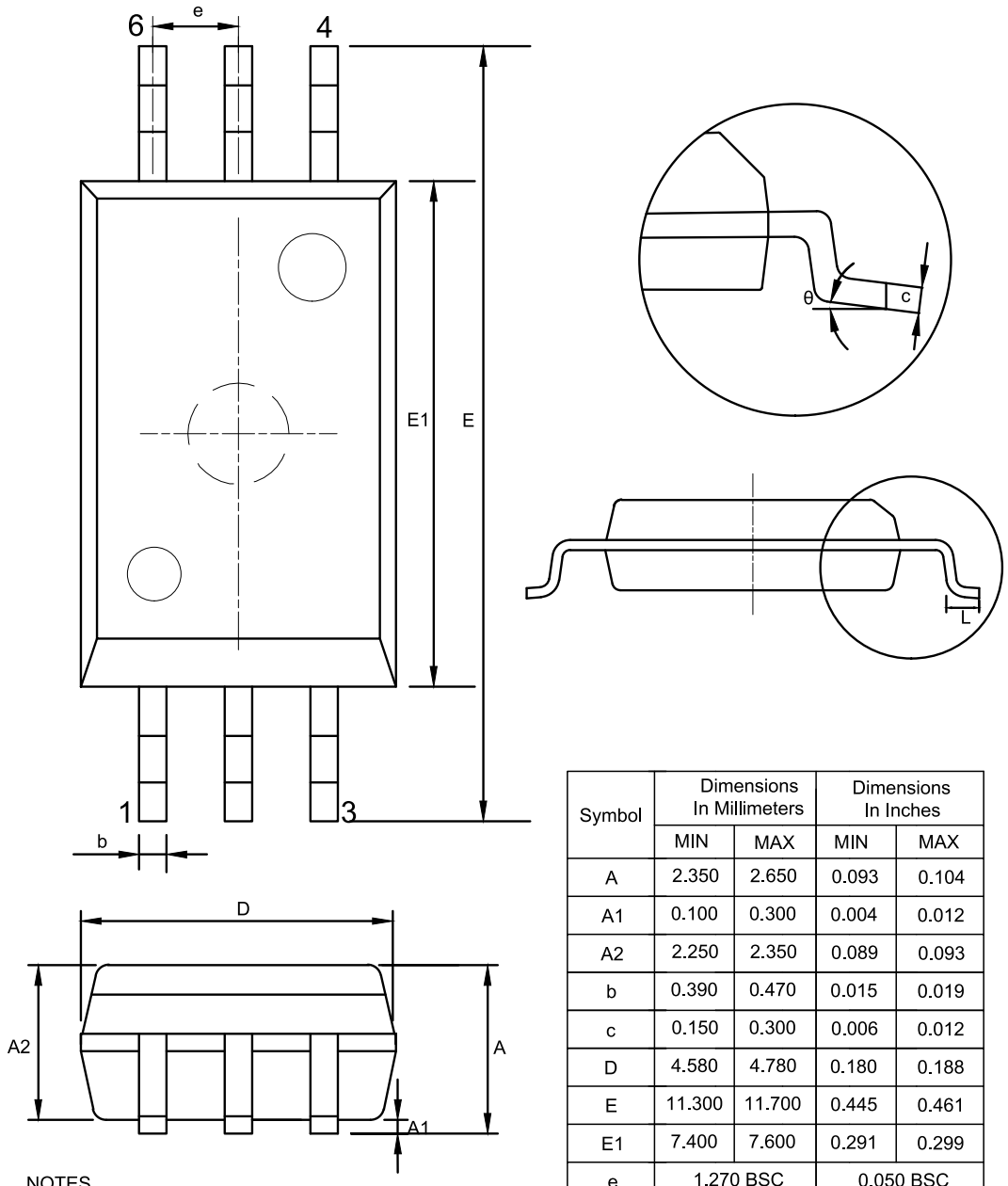


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM23513-SOER	WSOP6	330	21.6	11.95	5.2	3	16	16	Q1
TPM23513B-SOER	WSOP6	330	21.6	11.95	5.2	3	16	16	Q1
TPM23513-SOER-S	WSOP6	330	21.6	11.95	5.2	3	16	16	Q1

Package Outline Dimensions

WSOP6

Package Outline Dimensions SOE(WSOP-6-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	2.350	2.650	0.093	0.104
A1	0.100	0.300	0.004	0.012
A2	2.250	2.350	0.089	0.093
b	0.390	0.470	0.015	0.019
c	0.150	0.300	0.006	0.012
D	4.580	4.780	0.180	0.188
E	11.300	11.700	0.445	0.461
E1	7.400	7.600	0.291	0.299
e	1.270 BSC		0.050 BSC	
L	0.500	1.000	0.020	0.039
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Ambient Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPM23513-SOER	−40 to 125°C	WSOP6	M513	3	1000	Green
TPM23513B-SOER	−40 to 125°C	WSOP6	M513B	3	1000	Green
TPM23513-SOER-S	−40 to 125°C	WSOP6	M513	3	1000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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Performance Information. Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

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