4.1-A Source, 6.4-A Sink, 5-kV$_{RMS}$ Dual-Channel Isolated Gate Driver

Features

- Automotive AEC-Q100 Grade 1 (TPM2155xQ)
- Dual-Channel Isolated Gate Drivers with TTL/CMOS-Compatible Inputs
- Available with Disable (TPM21550x) or Enable (TPM21551x) Input Variants
- 4.1-A Source/6.4-A Sink Peak Output Current with Rail-to-Rail Output
- 35-V Output Driver Supply Voltage
- 5-V Input VCCI Range to Interface
- 4-V, 6-V, 8-V, 12-V, and 18-V V_{DD} UVLO Options
- Programmable Overlap and Dead Time
- Ultra-Fast Output Driving
  - 33-ns Typical Propagation Delay
  - 12-ns Typical Minimum Pulse Width
  - 4-ns Delay Matching
  - 6-ns Pulse Width Distortion
- 5-kV$_{RMS}$ Reinforced Isolation Rating
- ±150-V/ns Common-Mode Transient Immunity (CMTI)
- Industrial Standard Wide-Body WSOP14 / WSOP16 Package
- TPM2155xQ : AEC-Q100 Qualified for Automotive Applications
  - Grade 1 : −40°C to +125°C
- Safety-Related Certifications:
  - CQC Certification per GB4943.1-2022
  - CB Certification per IEC 62368-1:2023
  - 5-kV$_{RMS}$ Isolation Rating per UL 1577
  - DIN EN IEC 60747-17(VDE 0884-17): 2021-10

Applications

- Automotive On-board Charge, DCDC Converters
- Automotive Compressor, Thermal Management System
- Isolated Converters in DC-DC and AC-DC Power Supplies
- Server, Telecom, IT, and Industrial Infrastructures
- Motor Drive and DC-to-AC Solar Inverters
- Solar Inverters, Battery, and Energy Storage

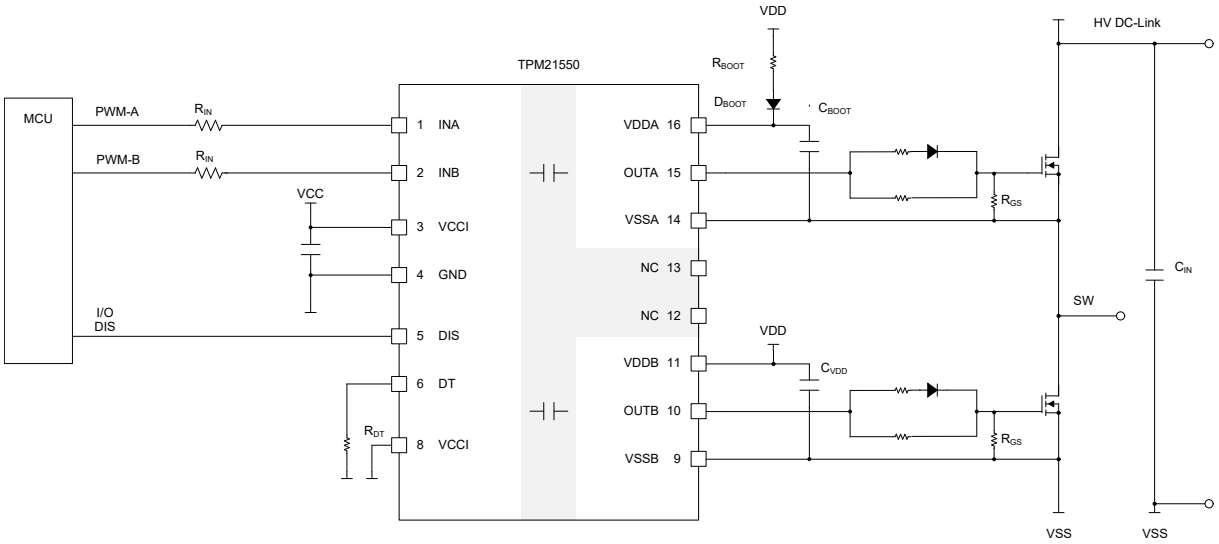
Description

The TPM21550 series consists of isolated dual-channel gate drivers that feature 4.1-A source and 6.4-A sink peak current. These drivers are specifically designed to power MOSFETs, IGBTs, and SiC MOSFETs, with ultra-low propagation delay and minimal pulse-width distortion.

The input side of the TPM21550 series is isolated from its two output drivers by a reinforced isolation barrier rated at 5 kVRMS, providing a typical of 150-V/ns common-mode transient immunity (CMTI). Additionally, the two secondary-side drivers feature internal functional isolation, enabling a working voltage of up to 1500 V_{DC}.

Each driver within the series offers flexible configuration options, functioning as either two low-side drivers, two high-side drivers, or as a half-bridge driver with a programmable dead time. For safety, a dedicated control pin shuts down both outputs. The TPM21550x variant uses an active-high DIS pin with an internal pull-up; pulling DIS low enables normal operation, and leaving it open shuts down both outputs. The TPM21551x variant uses an active-high EN pin with an internal pull-down; pulling EN high enables normal operation, and leaving it open shuts down both outputs. Both variants include a fail-safe mechanism that forces both outputs low on a primary-side logic failure.

Typical Application Circuit



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Product Family Table

Order Number	UVLO Rising Threshold (V)	Package	Quality Grade
TPM21550A-SOBR	6	WSOP16	Industrial
TPM21550B-SOBR	8.3	WSOP16	Industrial
TPM21550C-SOBR	12.5	WSOP16	Industrial
TPM21550D-SOBR (1)	17.7	WSOP16	Industrial
TPM21550E-SOBR	4.15	WSOP16	Industrial
TPM21551A-SOBR	6	WSOP16	Industrial
TPM21551B-SOBR	8.3	WSOP16	Industrial
TPM21551C-SOBR	12.5	WSOP16	Industrial
TPM21551D-SOBR (1)	17.7	WSOP16	Industrial
TPM21551E-SOBR	4.15	WSOP16	Industrial
TPM21550A-SOGR	6	WSOP14	Industrial
TPM21550B-SOGR	8.3	WSOP14	Industrial
TPM21550C-SOGR	12.5	WSOP14	Industrial
TPM21550D-SOGR (1)	17.7	WSOP14	Industrial
TPM21550E-SOGR	4.15	WSOP14	Industrial
TPM21551A-SOGR	6	WSOP14	Industrial
TPM21551B-SOGR	8.3	WSOP14	Industrial
TPM21551C-SOGR	12.5	WSOP14	Industrial
TPM21551D-SOGR (1)	17.7	WSOP14	Industrial
TPM21551E-SOGR	4.15	WSOP14	Industrial
TPM21550AQ-SOBR-S (1)	6	WSOP16	Automotive
TPM21550BQ-SOBR-S	8.3	WSOP16	Automotive
TPM21550CQ-SOBR-S	12.5	WSOP16	Automotive
TPM21551AQ-SOBR-S (1)	6	WSOP16	Automotive
TPM21551BQ-SOBR-S (1)	8.3	WSOP16	Automotive
TPM21551CQ-SOBR-S (1)	12.5	WSOP16	Automotive
TPM21550AQ-SOGR-S (1)	6	WSOP14	Automotive
TPM21550BQ-SOGR-S	8.3	WSOP14	Automotive
TPM21550CQ-SOGR-S	12.5	WSOP14	Automotive
TPM21551AQ-SOGR-S (1)	6	WSOP14	Automotive
TPM21551BQ-SOGR-S (1)	8.3	WSOP14	Automotive
TPM21551CQ-SOGR-S (1)	12.5	WSOP14	Automotive

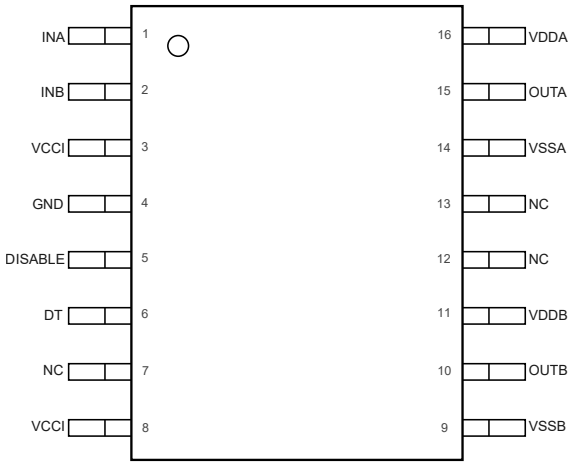
(1) Contact 3PEAK representatives for more information.

Revision History

Date	Revision	Notes
2026-06-10	A0	Initial Revision.
2026-08-25	A1	• Updated Typical Application, Layout Recommendations • Updated the certificate status • Updated the CLR and CPG in the insulation specifications • Updated the ESD table The actucal product remains unchanged.

Pin Configuration and Functions

TPM21550
WSOP16
Top View



TPM21550
WSOP14
Top View

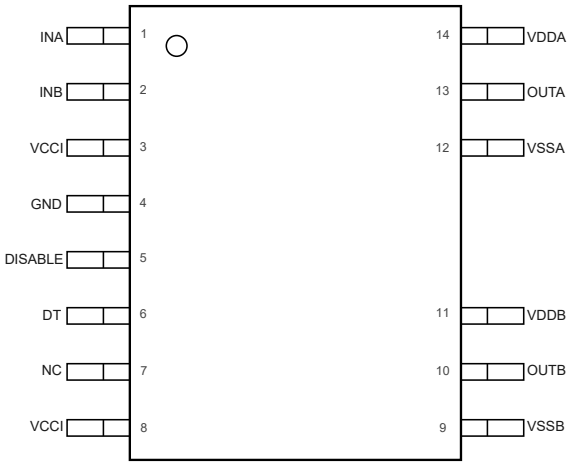


Table 1. Pin Functions: TPM21550x (DISABLE)

Name	No.		I/O	Description
	WSOP16	WSOP14		
INA	1	1	I	Input for A Channel, TTL/CMOS input threshold, pulled down internally. If unused, connect this pin to ground for better noise resistance.
INB	2	2	I	Input for B Channel, TTL/CMOS input threshold, pulled down internally. If unused, connect this pin to ground for better noise resistance.
VCCI	3	3	P	Primary side supply voltage. Internally connected to PIN 8. Use a low ESR/ESL capacitor close to the device to decouple the ground for stable operation.
GND	4	4	P	Primary side GND. All signals on the primary side are referenced to this ground connection.
DISABLE	5	5	I	DISABLE input (active-high). When held high or left open, both outputs are forced low; outputs follow INA/INB only when DISABLE is held low. Internally pulled up so the device defaults to shutdown if the pin is left floating. Tie directly to GND, or drive low from a microcontroller, to enable normal operation. For remote microcontroller drive, add a 1-nF bypass capacitor close to this pin.
DT	6	6	I	Deadtime control input. Programmable dead-time control input. Tie DT to VCCI to disable dead-time interlock (overlap mode). Place a resistor R_{DT} in the range 1 kΩ to 100 kΩ between DT and GND to set the programmable dead time. When DT is not tied to VCCI, an internal op-amp clamps the DT pin to 0.8 V, so the source current flowing out of DT through R_{DT} to GND

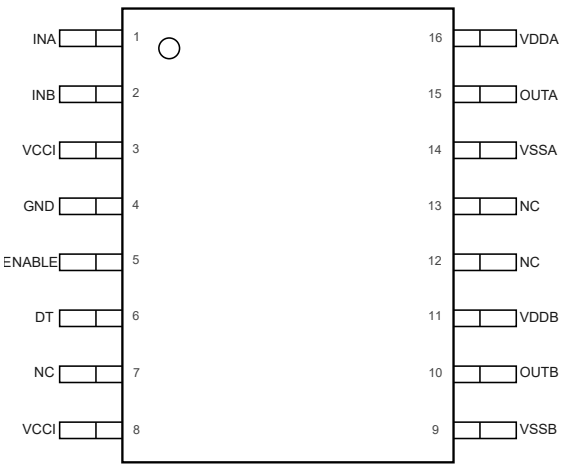
Name	No.		I/O	Description
	WSOP16	WSOP14		
				equals 0.8 V / R_{DT}; this current programs the dead time. A bypass capacitor on DT is optional; if used, a value larger than 1 nF is recommended.
NC	7	7	NC	Not connected
VCCI	8	8	P	Primary side supply voltage. Internally connected to PIN 3. Use a low ESR/ESL capacitor close to the device to decouple the ground for stable operation.
VSSB	9	9	P	Channel B secondary ground. Ground reference for secondary side B channel.
OUTB	10	10	O	Channel B secondary output. Connect this pin to the gate terminal of the MOSFET, IGBT, GaN HEMT, or SiC FET in the B channel.
VDDB	11	11	P	Channel B secondary power. Use a low ESR/ESL capacitor close to the device to decouple the ground for stable operation.
NC	12	n/a	NC	Not connected
NC	13	n/a	NC	Not connected
VSSA	14	12	P	Channel A secondary ground. Ground reference for secondary side A channel.
OUTA	15	13	O	Channel A secondary output. Connect this pin to the gate terminal of the MOSFET, IGBT, GaN HEMT, or SiC FET in the A channel.
VDDA	16	14	P	Channel A secondary power. Use a low ESR/ESL capacitor close to the device to decouple the ground for stable operation.

Table 2. Pin Functions: TPM21551x (ENABLE)

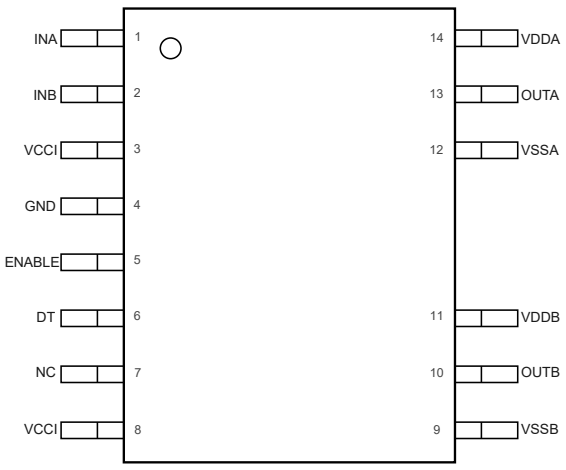
Name	No.		I/O	Description
	WSOP16	WSOP14		
INA	1	1	I	Input for A Channel, TTL/CMOS input threshold, pulled down internally. If unused, connect this pin to ground for better noise resistance.
INB	2	2	I	Input for B Channel, TTL/CMOS input threshold, pulled down internally. If unused, connect this pin to ground for better noise resistance.
VCCI	3	3	P	Primary side supply voltage. Internally connected to PIN 8. Use a low ESR/ESL capacitor close to the device to decouple the ground for stable operation.
GND	4	4	P	Primary side GND. All signals on the primary side are referenced to this ground connection.
ENABLE	5	5	I	ENABLE input (active-high). When held high, the device follows INA/INB; when held low or left open, both outputs are forced low. Internally pulled down so the device is disabled by default if the pin is left floating. Tie to VCCI, or drive high from a microcontroller, to enable the device. For remote microcontroller drive, add a 1-nF bypass capacitor close to this pin.
DT	6	6	I	Deadtime control input. Programmable dead-time control input. Tie DT to VCCI to disable dead-time interlock (overlap mode). Place a resistor R_{DT} in

Name	No.		I/O	Description
	WSOP16	WSOP14		
				the range 1 kΩ to 100 kΩ between DT and GND to set the programmable dead time. When DT is not tied to VCCI, an internal op-amp clamps the DT pin to 0.8 V, so the source current flowing out of DT through R_{DT} to GND equals 0.8 V / R_{DT}; this current programs the dead time. A bypass capacitor on DT is optional; if used, a value larger than 1 nF is recommended.
NC	7	7	NC	Not connected
VCCI	8	8	P	Primary side supply voltage. Internally connected to PIN 3. Use a low ESR/ESL capacitor close to the device to decouple the ground for stable operation.
VSSB	9	9	P	Channel B secondary ground. Ground reference for secondary side B channel.
OUTB	10	10	O	Channel B secondary output. Connect this pin to the gate terminal of the MOSFET, IGBT, GaN HEMT, or SiC FET in the B channel.
VDDB	11	11	P	Channel B secondary power. Use a low ESR/ESL capacitor close to the device to decouple the ground for stable operation.
NC	12	n/a	NC	Not connected
NC	13	n/a	NC	Not connected
VSSA	14	12	P	Channel A secondary ground. Ground reference for secondary side A channel.
OUTA	15	13	O	Channel A secondary output. Connect this pin to the gate terminal of the MOSFET, IGBT, GaN HEMT, or SiC FET in the A channel.
VDDA	16	14	P	Channel A secondary power. Use a low ESR/ESL capacitor close to the device to decouple the ground for stable operation.

TPM21551
WSOP16
Top View



TPM21551
WSOP14
Top View



Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Input Voltage	Input bias Pin Supply Voltage, VCCI refer to GND	−0.3	6	V
	Input Signal Voltage, INA, INB, DISABLE, refer to GND	−0.3	VCCI + 0.3	V
	Input Signal Negative Transient Voltage, INA, INB, DISABLE, refer to GND, 50-ns pulse	−5		V
	Input Signal Voltage, DT refer to GND	−0.3	VCCI + 0.3	V
Output Voltage	Output Supply Voltage, V_{DDA} − V_{SSA}, V_{DDB} − V_{SSB}	−0.3	35	V
	OUTA to VSSA, OUTB to VSSB	−0.3	V_{DDx} + 0.3	V
	OUTA to VSSA, OUTB to VSSB, transient for 200 ns	−2	V_{DDx} + 0.3	V
	Channel-to-Channel Voltage, VSSA-VSSB, VSSB-VSSA	−1850	1850	V
T_J	Maximum Junction Temperature	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.
(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Table 3. TPM2155x

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Table 4. TPM2155xQ

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	AEC Q100-002 (1)	±2	kV
CDM	Charged Device Model ESD	AEC Q100-011	±1.5	kV

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

Recommended Operating Conditions

Parameter		Min	Max	Unit
V_{CCI} – GND	Primary Side Supply Voltage	3	5.5	V
V_{DDA} – V_{SSA} V_{DDB} – V_{SSB} –	Output Supply Voltage (18-V UVLO)	18.3	33	V
	Output Supply Voltage (12-V UVLO)	13.1	33	V
	Output Supply Voltage (8-V UVLO)	8.8	33	V
	Output Supply Voltage (6-V UVLO)	6.4	33	V
	Output Supply Voltage (4-V UVLO)	4.4	33	V
T_J	Junction Temperature	−40	150	°C
T_A	Operating Ambient Temperature	−40	125	°C

Safety Limiting Values

Parameter		Test Conditions	Min	Typ	Max	Unit
P_D	Safety Input, Output, or Total Power	V_{CCI} = 18 V, $V_{DDA/B}$ = 12 V, INA/B = 3.3 V, 3 MHz 50% duty cycle square wave 1-nF load			1.05	W
P_{DA} P_{DB}	Power Dissipation by Each Output Driver				0.5	W
P_I	Power Dissipation by Primary Side				0.05	W
I_S	Safety Output Supply Current	$R_{\theta JA}$ = 70°C/W, VDDA/B = 12 V, T_A = 25°C, T_J = 150°C			70	mA
		$R_{\theta JA}$ = 70°C/W, VDDA/B = 25 V, T_A = 25°C, T_J = 150°C			35	mA
P_S	Safety Supply Power, INPUT	$R_{\theta JA}$ = 70°C/W, T_A = 25°C, T_J = 150°C			50	mW
	Safety Supply Power, DRIVER A				900	mW
	Safety Supply Power, DRIVER B				900	mW
	Safety Supply Power, Total				1850	mW
T_S	Maximum Safety Temperature				150	°C

Insulation Specifications

Parameter		Conditions	Value	Unit
CLR	External Clearance	Shortest terminal-to-terminal distance through air	> 8	mm
CPG	External Creepage	Shortest terminal-to-terminal distance across the package surface	> 8	mm
DTI	Distance through the Insulation	Minimum internal gap (internal clearance)	> 21	μm
CTI	Comparative Tracking Index		> 600	V
	Material Group		I	
	Installation Classification per IEC 60664-1	For Rated Mains Voltage ≤ 600 V_{RMS}	I-IV	
		For Rated Mains Voltage ≤ 1000 V_{RMS}	I-III	
	Pollution Degree		2	
	Climate Category		40/125/21	
C_{IO}	Isolation Capacitance	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	1.2	pF
R_{IO}	Isolation Resistance	V_{IO} = 500 V, T_A = 25 °C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125 °C	> 10^{11}	
		V_{IO} = 500 V, T_A = 150 °C	> 10^9	
V_{IORM}	Maximum Repetitive Isolation Voltage	AC voltage (bipolar)	1500	V_{PK}
V_{IOWM}	Maximum Working Isolation Voltage	AC voltage; TDDB Test	1060	V_{RMS}
		DC voltage	1500	V_{DC}
V_{IOTM}	Maximum Transient Isolation Voltage	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production)	7070	V_{PK}
V_{IOSM}	Maximum Surge Isolation Voltage	V_{TEST} = 1.3 × V_{IOSM}; tested in oil (qualification test); 1.2/50-μs waveform per IEC 62368-1	7692	V_{PK}
V_{ISO}	UL 1577 Withstand Isolation Voltage	V_{TEST} = V_{ISO} = 5000 V_{RMS}, t = 60 s (in qualification), V_{TEST} = 1.2 × V_{ISO}- 6000 V_{RMS}, t = 1 s (100% in production)	5000	V_{RMS}
q_{pd}	Apparent Charge	Method a, After Input/Output safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10 s	≤ 5	pC
		Method a, After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10 s	≤ 5	
		Method b1; At routine test (100% production) and preconditioning (type test), V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1 s	≤ 5	

(1) All pins on each side of the barrier tied together create a two-terminal device.

Electrical Characteristics

V_{VCCI} = 5 V, 0.1-µF capacitor from VCCI to GND; V_{DDA} = V_{DDB} = 15 V, 1.0-µF capacitor from each V_{DDx} to the corresponding V_{SSx}; DT pin floating; DISABLE = GND (TPM21550x) or ENABLE = VCCI (TPM21551x); C_L = 0 pF; T_J = −40°C to +150°C unless otherwise noted. Typical values are at T_J = 25°C.

Parameter		Conditions	Min	Typ	Max	Unit
Supply						
I_{VCCI}	VCCI Quiescent Current	VINA = 0 V, VINB = 0 V		0.9	2	mA
I_{VDDA},I_{VDDB}	VDDA and VDDB Quiescent Current	VINA = 0 V, VINB = 0 V, VDD = 15 V		0.9	2.5	mA
I_{VCCI}	VCCI Operating Current	*f* = 500 kHz, current per channel, C_{OUT} = 100 pF		2.2	3.2	mA
I_{VDDA},I_{VDDB}	VDDA and VDDB Operating Current	*f* = 500 kHz, current per channel, C_{OUT} = 100 pF, VDD = 15V		2.3	3.2	mA
V_{VCCI_ON}	Rising Threshold		2.55	2.7	2.85	V
V_{VCCI_OFF}	Falling Threshold VCCI_OFF		2.35	2.5	2.65	V
V_{VCCI_HYS}	Threshold Hysteresis			0.2		V
Input						
VINAH, VINBH,	Input High Voltage VDISH		1.6	1.8	2.1	V
VINAL, VINBL, VDISL	Input Low Voltage		0.8	1.0	1.3	V
VINA_HYS, VINB_HYS, VDIS_HYS	Input Hysteresis			0.7		V
VINA, VINB	Negative Transient, ref to GND, 50 ns pulse		−5			V
R_{INx}	INA, INB Pull-Down Resistance	INx = 3.3 V	50	102.2	185	kΩ
R_{DIS}	DIS Pull-Up Resistance (TPM21550x)	DIS = GND	50	100	185	kΩ
R_{EN}	EN Pull-Down Resistance (TPM21551x)	EN = 3.3 V	50	100	185	kΩ
Output UVLO - 6V						
V_{VDDA_ON}, V_{VDDB_ON}	Rising Threshold VDDA_ON, VDDB_ON		5.7	6	6.3	V
V_{VDDA_OFF}, VVDDB_OFF	Falling Threshold VDDA_OFF, VDDB_OFF		5.4	5.7	6	V

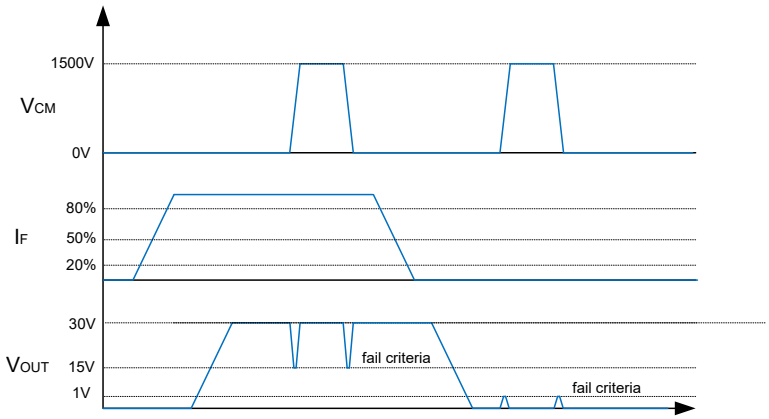
Parameter		Conditions	Min	Typ	Max	Unit
V_{VDDA_HYS}, V_{VDDB_HYS}	Threshold Hysteresis			0.3		V
Output UVLO - 8V						
V_{VDDA_ON}, V_{VDDB_ON}	Rising Threshold VDDA_ON, VDDB_ON		7.9	8.3	8.7	V
V_{VDDA_OFF}, V_{VDDB_OFF}	Falling Threshold VDDA_OFF, VDDB_OFF		7.5	7.8	8.1	V
V_{VDDA_HYS}, V_{VDDB_HYS}	Threshold Hysteresis			0.5		V
Output UVLO - 12V						
V_{VDDA_ON}, V_{VDDB_ON}	Rising Threshold VDDA_ON, VDDB_ON		12	12.5	12.95	V
V_{VDDA_OFF}, V_{VDDB_OFF}	Falling Threshold VDDA_OFF, VDDB_OFF		11.1	11.6	12.0	V
V_{VDDA_HYS}, V_{VDDB_HYS}	Threshold Hysteresis			0.9		V
Output UVLO - 18V						
V_{VDDA_ON}, V_{VDDB_ON}	Rising Threshold VDDA_ON, VDDB_ON		17.1	17.7	18.2	V
V_{VDDA_OFF}, V_{VDDB_OFF}	Falling Threshold VDDA_OFF, VDDB_OFF		16.1	16.7	17.0	V
V_{VDDA_HYS}, V_{VDDB_HYS}	Threshold Hysteresis			1		V
Output UVLO - 4V						
V_{VDDA_ON}, V_{VDDB_ON}	Rising Threshold VDDA_ON, VDDB_ON		4	4.15	4.26	V
V_{VDDA_OFF}, V_{VDDB_OFF}	Falling Threshold VDDA_OFF, VDDB_OFF		3.65	3.79	3.9	V
V_{VDDA_HYS}, V_{VDDB_HYS}	Threshold Hysteresis			0.4		V
Output						
V_{OUTPD}	Output Active Pull down on OUTx	I_{OUT} = 200mA ,V_{DDx} = OPEN	1.3	1.8	2.1	V
I_{OA+}, I_{OB+}	Peak Output Source Current	C_{VDD} = 10 μF, C_{LOAD} = 0.18 μF, f = 1 kHz		4.1		A
I_{OA-}, I_{OB-}	Peak Output Sink Current	C_{VDD} = 10 μF, C_{LOAD} = 0.18 μF, f = 1 kHz		6.4		A
R_{OHA}, R_{OHB}	Output Resistance at High State	I_{OUT} = −10 mA, R_{OHA}, R_{OHB}		5		Ω
R_{OLA}, R_{OLB}	Output Resistance at Low State	I_{OUT} = 10 mA		0.55		Ω

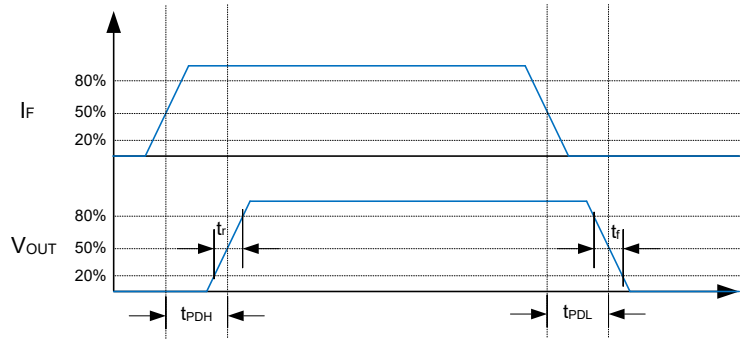
Parameter		Conditions	Min	Typ	Max	Unit
V_{OHA}, V_{OHB}	Output Voltage at High State, VDD − VOUT	V_{VDDA}, V_{VDDB} = 15 V, I_{OUT} = −10 mA	40	80	150	mV
V_{OLA}, V_{OLB}	Output Voltage at Low State	V_{VDDA}, V_{VDDB} = 15 V, I_{OUT} = 10 mA		12	25	mV
Timing						
t_{DEAD}	Dead Time(1)	DT floating or Pull DT pin to VCCI	Determined by INA and INB			
		DT pull down to GND, R_{DT} < 0.15 kΩ		15	20	ns
		R_{DT} = 10 kΩ	86	100	112	ns
		R_{DT} = 20 kΩ	167	187	203	ns
		R_{DT} = 50 kΩ	399	441	487	ns
t_{RISE}	Output Rise Time, 20% to80% measured points (1)	VDD = 12V, COUT = 1.8 nF		8.8	16	ns
	Output Rise Time, 20% to 80% measured points (1)	VDD = 25V, COUT = 1.8 nF		12		ns
t_{FALL}	Output Fall Time, 90% to 10% measured points (1)	VDD = 12V, COUT = 1.8 nF		7.4	13	ns
	Output Fall Time, 90% to 10% measured points (1)	VDD = 25V, COUT = 1.8 nF		10.7		ns
t_{PWmin}	Minimum Pulse Width (1)	Output off for less than minimum, COUT = 0 pF	7	12	25	ns
t_{PDHL}	Propagation Delay from INx to OUTx Falling Edges			32.9		ns
t_{PDLH}	Propagation Delay from INx to OUTx Rising Edges			33.2		ns
t_{PDHL}	Propagation Delay from DIS to OUTx Falling Edges			43		ns
t_{PDLH}	Propagation Delay from DIS to OUTx Rising Edges			40.6		ns
t_{PWD}(1)	Pulse Width Distortion |tPDLH – tPDHL| (1)			0.7	6	ns
t_{DM} (1)	Propagation Delays Matching between VOUTA, VOUTB (1)	f = 100 kHz		0.5	4	ns
t_{VDD+} to OUT VDDA, VDDB	Power-up Delay Time: UVLO Rise to OUTA, OUTB (1)	INA or INB tied to VCCI		9.7	15	µs
t_{VDD-} to OUT VDDA, VDDB	Power-down Delay Time: UVLO Falling to OUTA, OUTB (1)	INA or INB tied to VCCI	0.3	1	2	µs

Parameter		Conditions	Min	Typ	Max	Unit
t_{Vcc+} to OUT	VCC UVLO on Delay		18	45	95	μs
t_{Vcc-} to OUT	VCC UVLO off Delay			1.2	7	μs
|CMTI|	Common Mode Transient Immunity	V_{CM} = 1500 V	150			V/ns

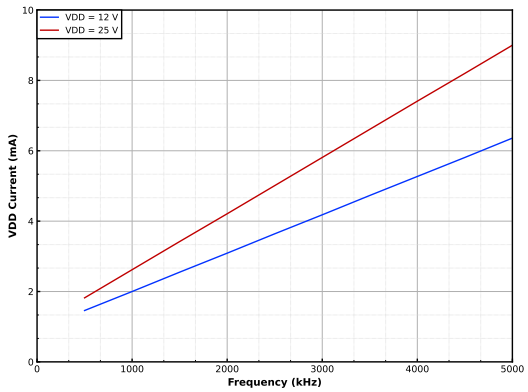
(1) Guaranteed by design

Parameter Measurement



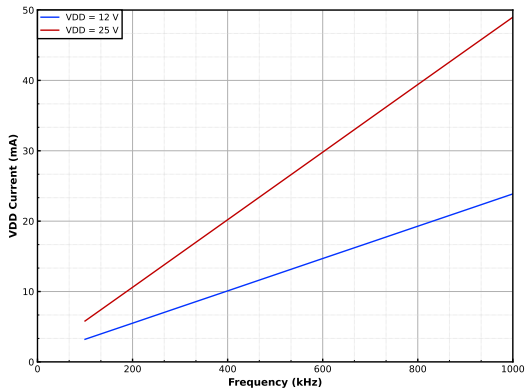


Typical Performance Characteristics



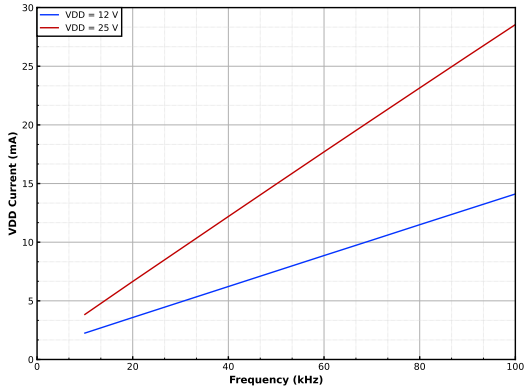
No Load, VDD = 12 V or 25 V

Figure 1. VDDx Current Consumption vs. Frequency



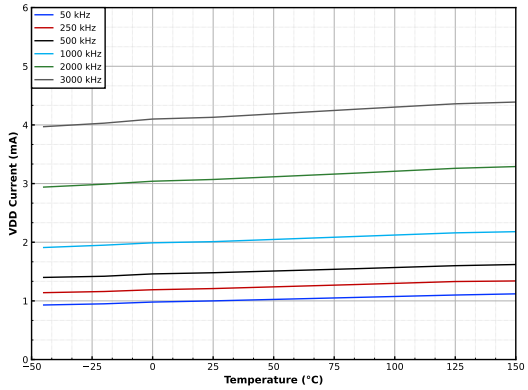
1.8-nF Load, VDD = 12 V or 25 V

Figure 2. VDDx Current Consumption vs. Frequency



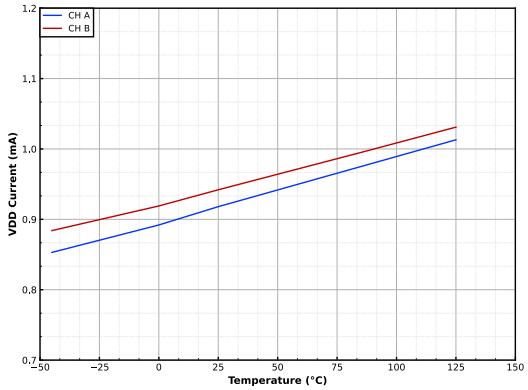
10-nF Load, VDD = 12 V or 25 V

Figure 3. VDDx Current Consumption vs. Frequency



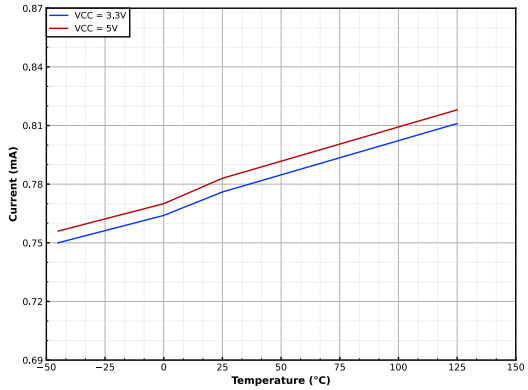
VCC = 5 V, VDD = 12 V, no load

Figure 4. VDDx Current Consumption vs. Temperature



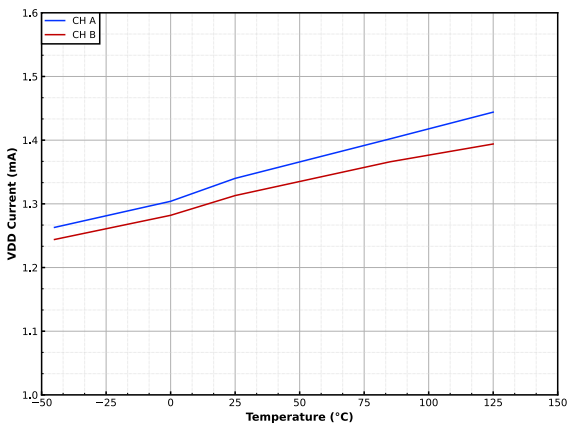
No load, input low, no switching, VDD = 12 V

Figure 5. VDDx Quiescent Current vs. Temperature



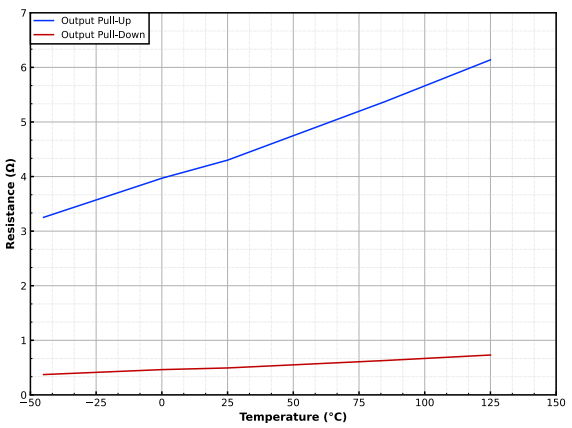
No load, input high & low, no switching

Figure 6. VCCI Current Consumption vs. Temperature



VCC = 5 V, VDD = 12 V, no load, *f* = 500 kHz

Figure 7. VDDx Switching Current vs. Temperature



VDD = 12 V, no load

Figure 8. Output Resistance vs. Temperature

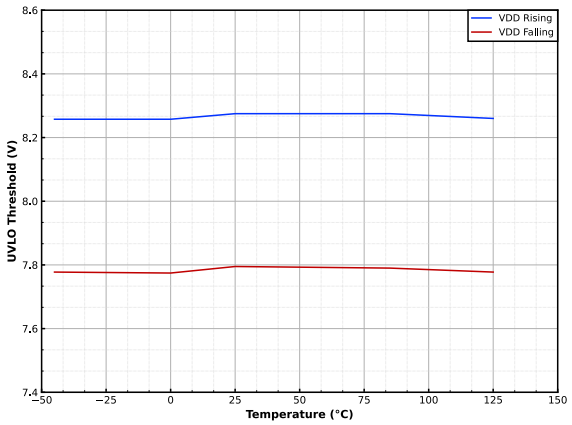


Figure 9. VDD 8 V UVLO Threshold vs. Temperature

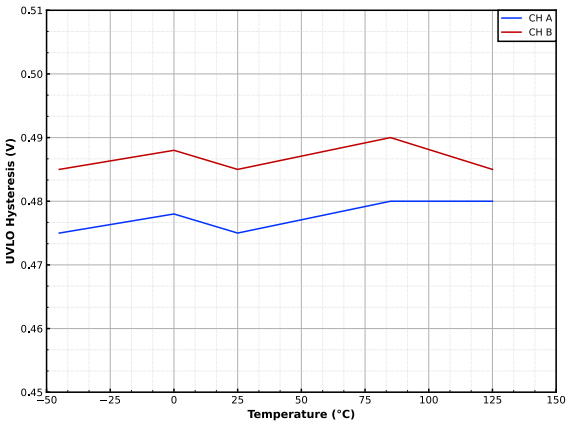


Figure 10. VDD 8 V UVLO Hysteresis vs. Temperature

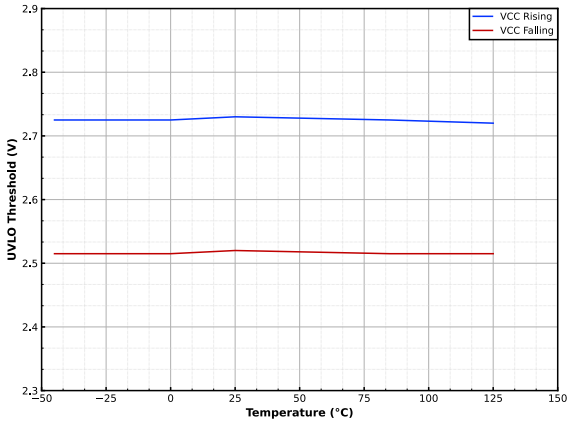


Figure 11. VCC UVLO Threshold vs. Temperature

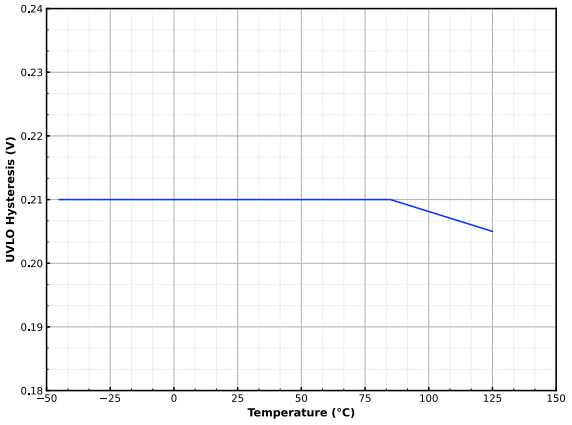


Figure 12. VCC UVLO Hysteresis vs. Temperature

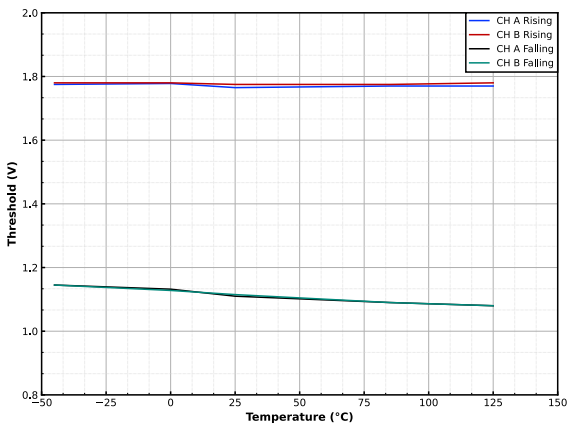


Figure 13. IN/DIS Threshold vs. Temperature

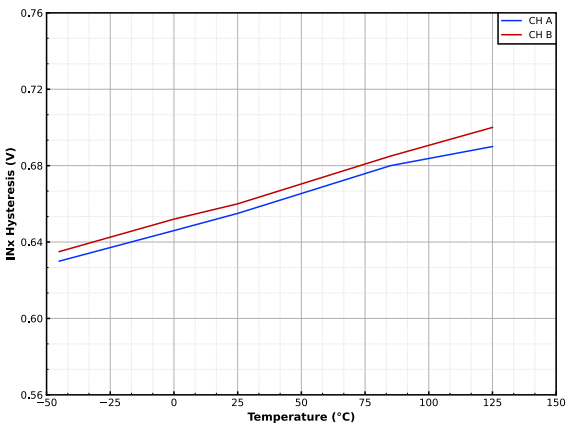


Figure 14. IN/DIS Hysteresis vs. Temperature

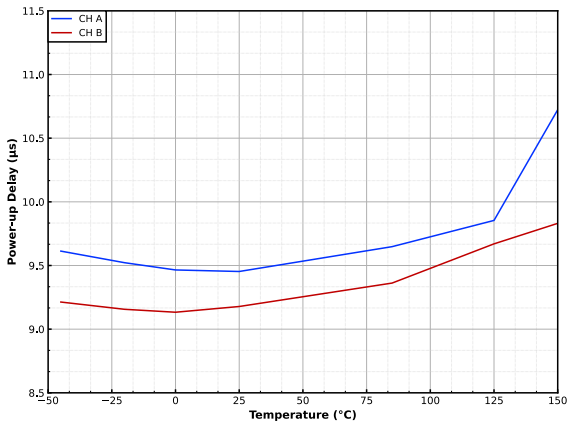


Figure 15. VDD UVLO Power-up Delay vs. Temperature

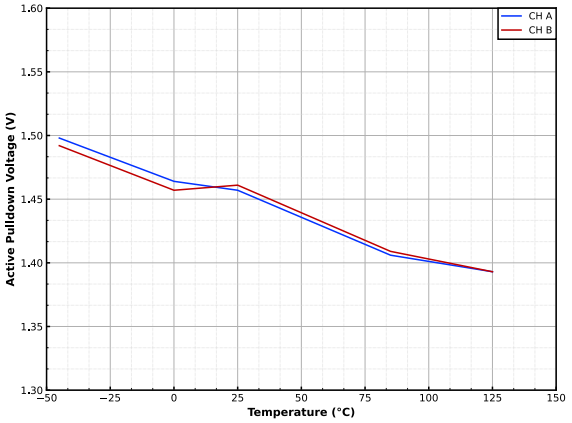


Figure 16. Active Pulldown Voltage vs. Temperature

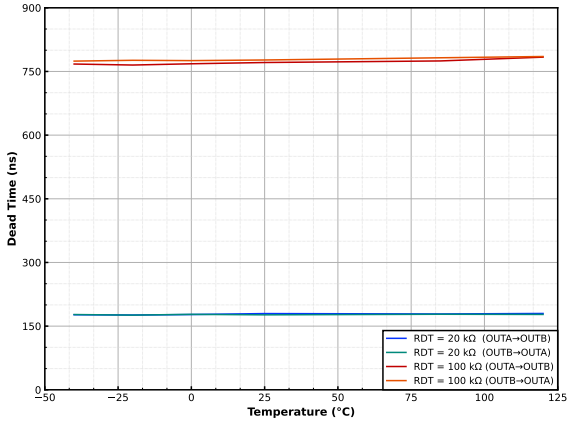


Figure 17. Deadtime vs. Temperature

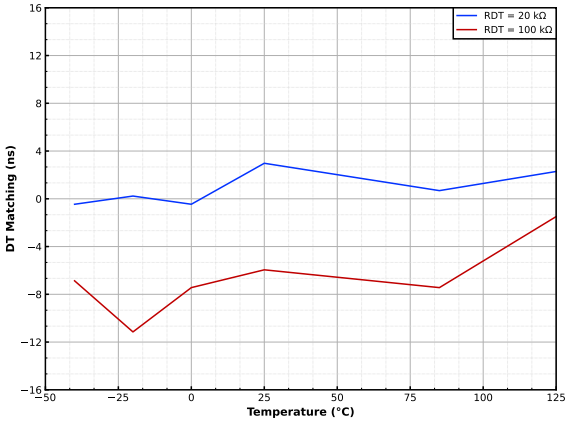
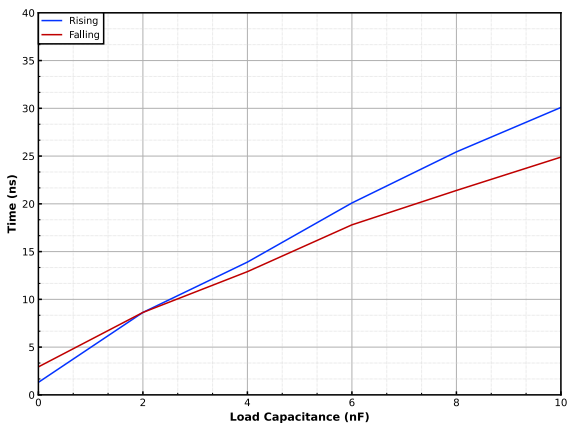
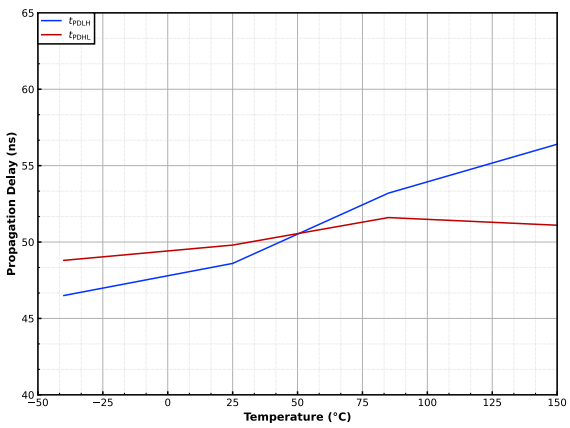


Figure 18. Deadtime Mismatch vs. Temperature



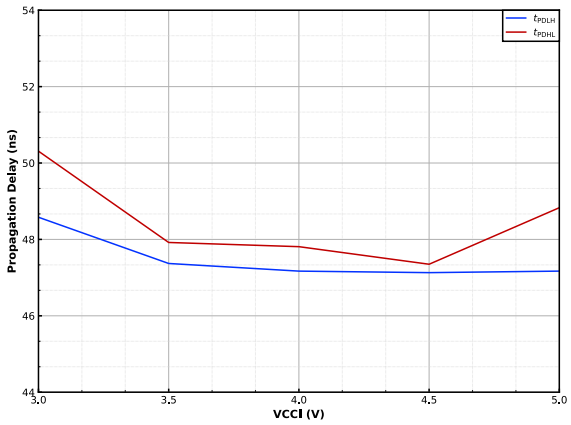
VDD = 12 V, VCCI = 5 V, Channel B

Figure 19. Rising and Falling Time vs. Load



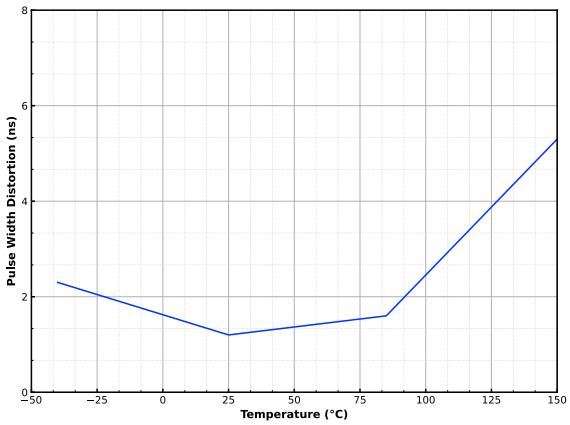
VDD = 12 V, VCCI = 5 V, Channel B

Figure 20. Propagation Delay vs. Temperature



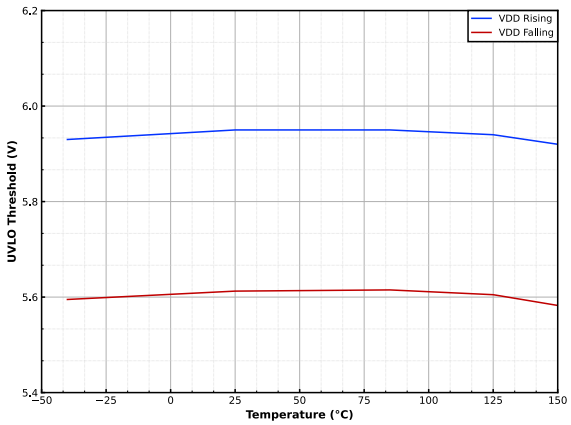
VDD = 12 V, TA = 25 °C, Channel B

Figure 21. Propagation Delay vs. VCCI



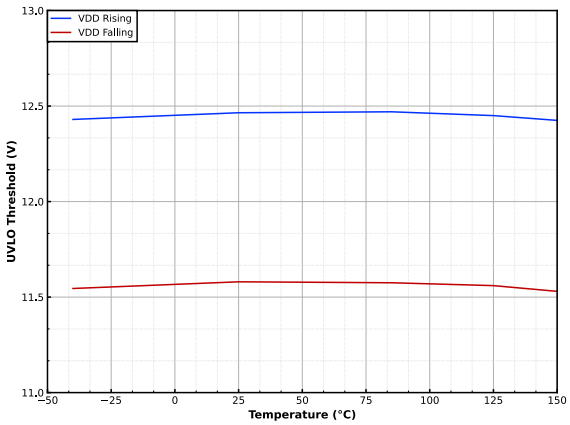
VDD = 12 V, VCCI = 5 V, Channel B

Figure 22. Pulse Width Distortion vs. Temperature



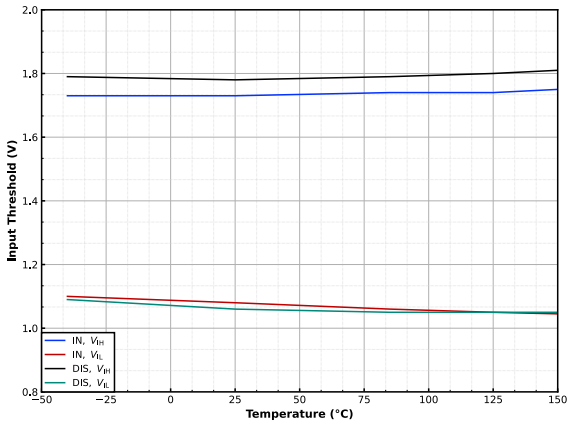
VCCI = 5 V

Figure 23. VDD UVLO Threshold vs. Temperature (6.3 V Variant)



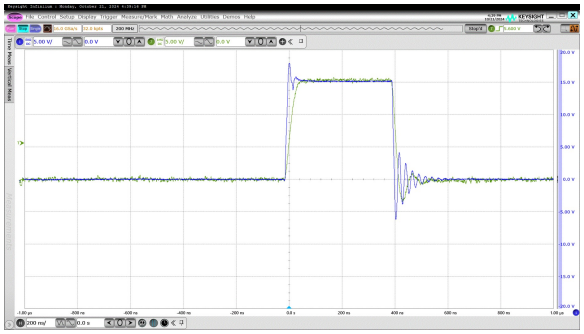
VCCI = 5 V

Figure 24. VDD UVLO Threshold vs. Temperature (13 V Variant)



VDD = 12 V, VCCI = 5 V

Figure 25. IN/DIS Input Threshold vs. Temperature



CH: 1-nF Load; CH2 10-nF Load

Figure 26. Typical Output Waveform

Detailed Description

Overview

The TPM21550 family of dual gate drivers is designed for high-performance power transistor switching. These drivers act as an isolated bridge between controllers and transistor gates, ensuring efficient and reliable operation. With their ability to adapt to various power supply and motor systems, as well as support for different transistors, including GaN HEMT, IGBT, and SiC MOSFETs, the TPM21550 family offers versatility and flexibility. Advanced features such as programmable dead time control and voltage protection enhance system safety and stability. Whether used with digital or analog controllers, the TPM21550 family provides a robust solution for power transistor driving needs.

Functional Block Diagram

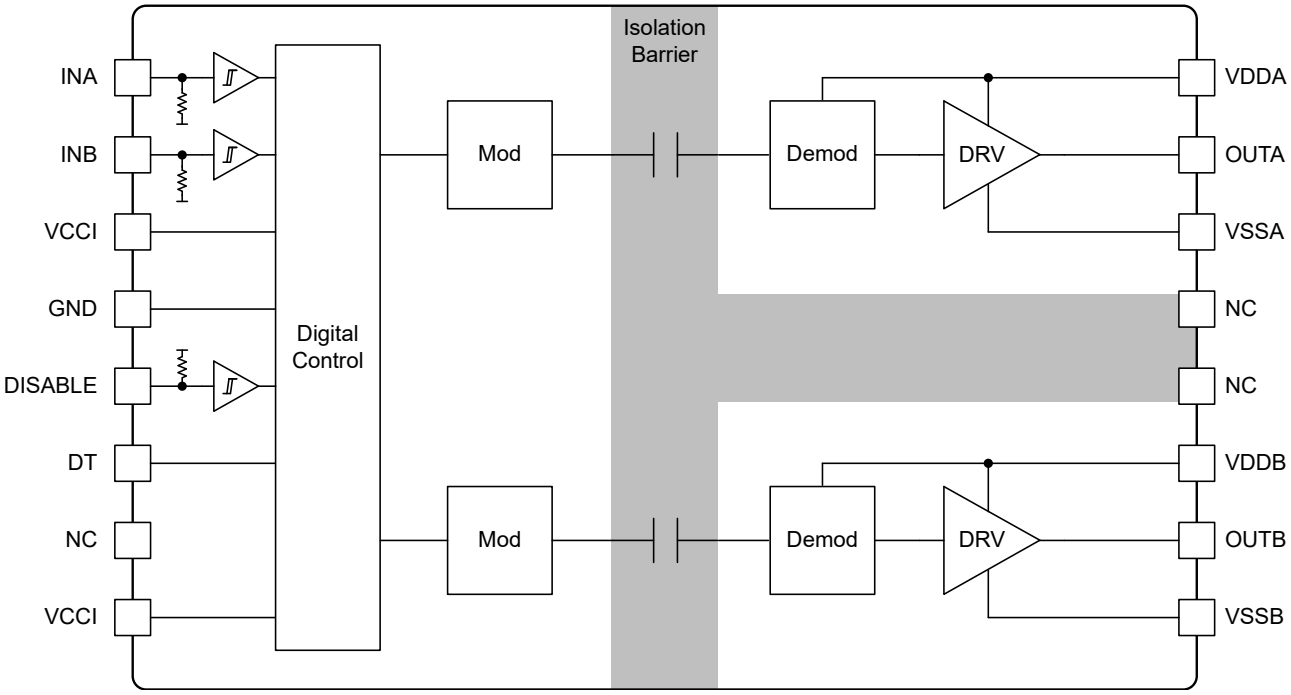


Figure 27. TPM21550x (DISABLE Variant) — WSOP16

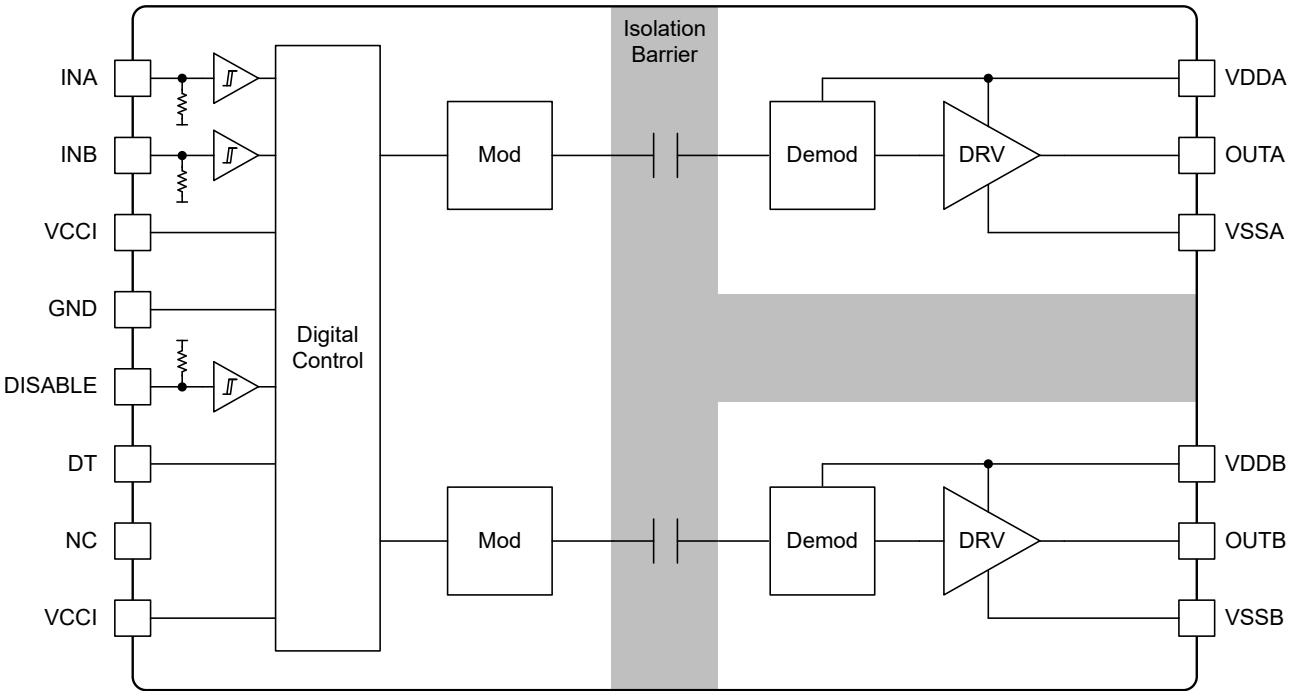


Figure 28. TPM21550x (DISABLE Variant) — WSOP14

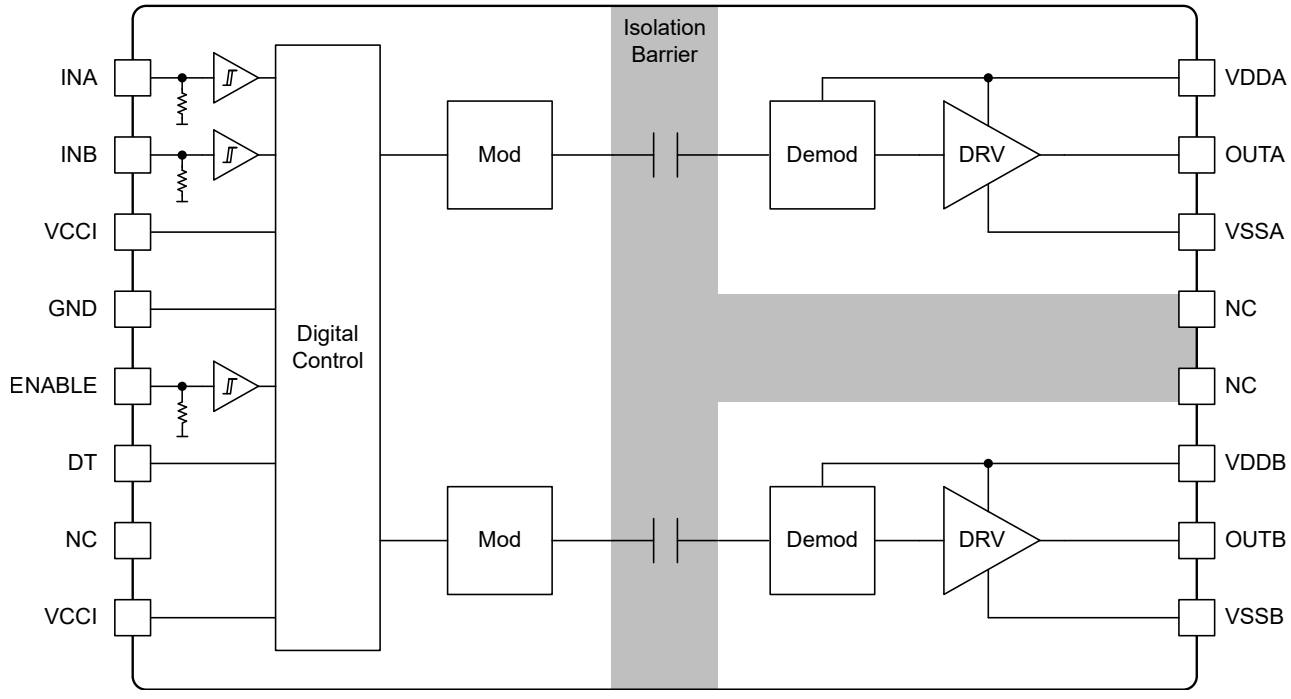


Figure 29. TPM21551x (ENABLE Variant) — WSOP16

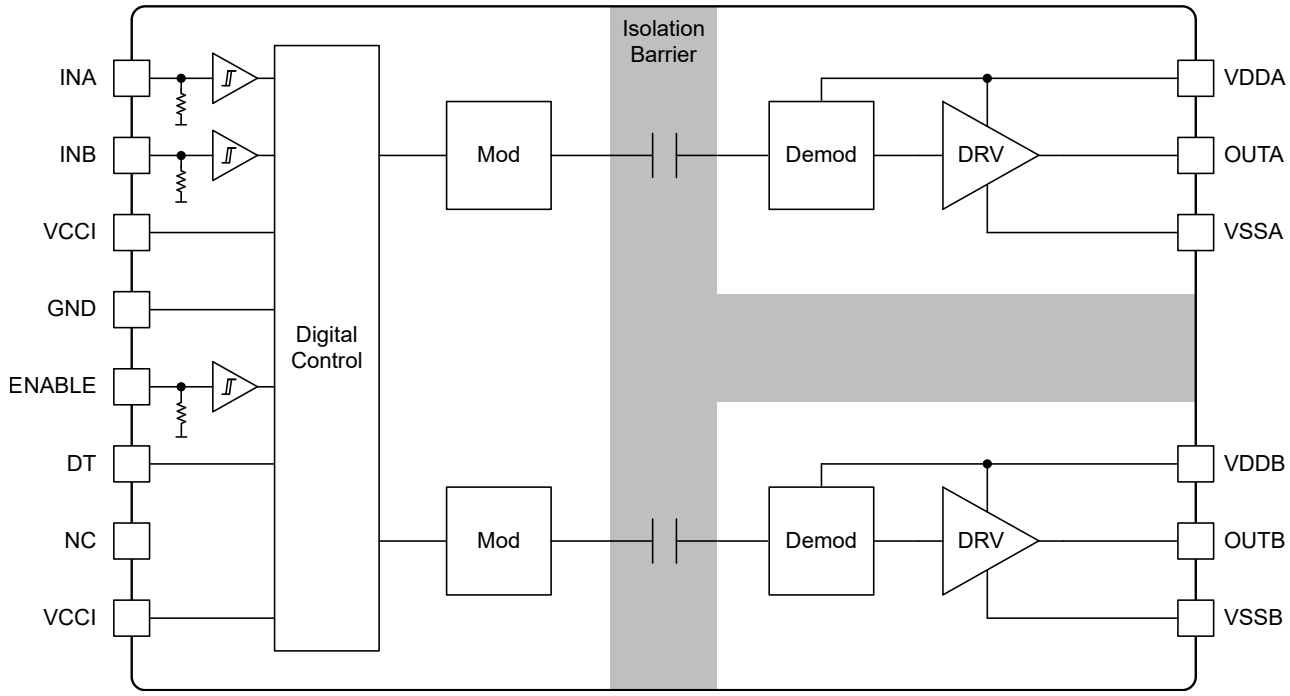


Figure 30. TPM21551x (ENABLE Variant) — WSOP14

Feature Description

Supply and UVLO

The TPM21550 family of gate drivers features internal undervoltage lock-out (UVLO) protection on both the supply circuit and the input side. This UVLO function ensures reliable operation by monitoring VDD and VCCI voltages.

For the VDD supply circuit, if the bias voltage falls below a certain threshold (V_{VDD_ON} at the rising edge or V_{VDD_OFF} at the falling edge), the UVLO protection activates, holding the affected output low regardless of the input pin status. This prevents potential damage or malfunction due to insufficient bias voltage.

Additionally, the TPM21550 family incorporates an active clamp circuit that keeps the driver outputs low when the output stages are in an unbiased or UVLO condition. This clamp circuit limits the voltage rise on the driver outputs, effectively clamping them to the threshold voltage of the lower NMOS device, typically around 2 V, when no bias power is available.

To enhance stability and prevent chatter caused by ground noise from the power supply, the VDD UVLO protection in the TPM21550 family includes a hysteresis feature (V_{VDD_HYS}). This hysteresis also allows the device to tolerate small drops in bias voltage that may occur during switching operations or sudden increases in operating current consumption.

The input side of the TPM21550 family has a UVLO protection feature that monitors the VCCI voltage. The device remains inactive until the VCCI voltage exceeds a certain threshold (V_{VCCI_ON}) during start-up. Once operational, if the VCCI voltage drops below another threshold (V_{VCCI_OFF}), the output does not follow inputs and holds low regardless of the input pin status. This input UVLO also includes hysteresis (V_{VCCI_HYS}) for stable operation.

Table 5. TPM21550x VCCI UVLO Logic Table

CONDITION	INPUTS		OUTPUTS	
	INA	INB	OUTA	OUTB
VCCI-GND < V_{VCCI_ON} during device start up	H	L	L	
VCCI-GND < V_{VCCI_ON} during device start up	L	H	L	L

CONDITION	INPUTS		OUTPUTS	
	INA	INB	OUTA	OUTB
VCCI-GND < V_{VCCI_ON} during device start up	H	H	L	L
VCCI-GND < V_{VCCI_ON} during device start up	L	L	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	H	L	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	L	H	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	H	H	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	L	L	L	L

Table 6. TPM21550x VDD UVLO Logic Table

CONDITION	INPUTS		OUTPUTS	
	INA	INB	OUTA	OUTB
VDD-VSS < V_{VDD_ON} during device start up	H	L	L	L
VDD-VSS < V_{VDD_ON} during device start up	L	H	L	L
VDD-VSS < V_{VDD_ON} during device start up	H	H	L	L
VDD-VSS < V_{VDD_ON} during device start up	L	L	L	L
VDD-VSS < V_{VDD_OFF} after device start up	H	L	L	L
VDD-VSS < V_{VDD_OFF} after device start up	L	H	L	L
VDD-VSS < V_{VDD_OFF} after device start up	H	H	L	L
VDD-VSS < V_{VDD_OFF} after device start up	L	L	L	L

The TPM21550 family input pins (INA, INB, and DISABLE / ENABLE) use TTL/CMOS-compatible input thresholds, fully isolated from the VDD supply. The typical V_{INx_H} = 1.8 V and V_{INx_L} = 1.0 V allow direct drive from 3.3-V microcontrollers. A typical 0.7-V input hysteresis improves noise immunity.

To guarantee a defined logic state when a pin is left floating, the TPM21550 family integrates internal bias resistors (typically 100 kΩ) on every logic input. INA and INB are internally pulled down, so an unused input defaults to logic low. The DIS pin (TPM21550x) is internally pulled up, so leaving DIS open shuts down both outputs by default. The EN pin (TPM21551x) is internally pulled down, so leaving EN open also shuts down both outputs. 3PEAK still recommends explicitly tying every control pin to its active level for best noise immunity.

The isolation between the input circuitry and the output drivers within the TPM21550 family provides flexibility for different applications. The amplitude of the input signal can exceed or fall below the VDD voltage, provided it remains within the manufacturer's recommended operating limits. Crucially, the voltage amplitude of signals applied to the INA or INB pins must never surpass the VCCI voltage. This inherent flexibility facilitates seamless integration with a wide range of control signal sources, empowering users to select the most appropriate VDD voltage for their specific gate driver requirements.

Disable Pin (TPM21550x): Driving the DIS pin high or leaving it open shuts down both outputs simultaneously. Pulling the DIS pin low allows the TPM21550x to operate normally. The DIS pin includes an internal pull-up, so the device defaults to shutdown when DIS is left floating.

Enable Pin (TPM21551x): Driving the EN pin low or leaving it open shuts down both outputs simultaneously. Pulling the EN pin high allows the TPM21551x to operate normally. The EN pin includes an internal pull-down, so the device defaults to shutdown when EN is left floating.

DT Pin Configurations: Shorting the DT pin directly to VCCI disables the dead-time interlock function. 3PEAK does not recommend placing a series resistor between VCCI and the DT pin; a direct connection ensures robust operation. When R_{DT} is connected from DT to GND to program the dead time, an internal op-amp clamps the DT pin to 0.8 V; the resulting source current flowing out of the DT pin through R_{DT} equals 0.8 V / R_{DT}, and this current sets the programmable dead time.

Table 7. TPM21550x Input Logic Table

INPUTS		DISABLE	OUTPUTS		NOTE
INA	INB		OUTA	OUTB	
L	L	L	L	L	If programmable deadtime is used, output transitions occur after the dead time expires.
L	H	L	L	H	
H	L	L	H	L	
H	H	L	L	L	DT is programmed with R_{DT}
H	H	L	H	H	DT is left open or DT pin pulled up to VCCI
Left Open	Left Open	Left Open	L	L	–
X	X	H or Left Open	L	L	–

Table 8. TPM21551x Input Logic Table

INPUTS		ENABLE	OUTPUTS		NOTE
INA	INB		OUTA	OUTB	
X	X	L or Left Open	L	L	ENABLE is internally pulled down. When ENABLE is Low or left open, both outputs are disabled and held Low regardless of INA/INB. When ENABLE is High, the device follows the standard INA/INB input logic (see Input Logic Table above).
L	L	H	L	L	
L	H	H	L	H	
H	L	H	H	L	
H	H	H	H	H	
Left Open	Left Open	H	L	L	Inputs pulled down internally.

Output Stage

The TPM21550 family features an enhanced output stage designed to optimize power switch turn-on transitions, particularly during the critical Miller plateau region.

Both outputs of the TPM21550 family are capable of delivering robust 4.1-A peak source and 6.4-A peak sink current pulses. The output voltage operates rail-to-rail between VDD and VSS, with minimal dropout. This design enhances the overall performance and reliability of the gate drivers in demanding applications.

Output Stage UVLO

Each output channel monitors its own driver supply (V_{DDA}−V_{SSA} for OUTA, V_{DDB}−V_{SSB} for OUTB) with an independent undervoltage lockout (UVLO). The two channels operate in parallel: a UVLO event on one channel forces only that channel's output low without disturbing the other channel.

The TPM21550 family is offered in five UVLO threshold options to match the gate-charge requirements of common power switches. Each option specifies a rising threshold V_{VDDx_ON}, a falling threshold V_{VDDx_OFF}, and a fixed hysteresis V_{VDDx_HYS} = V_{VDDx_ON} − V_{VDDx_OFF}. The hysteresis prevents chatter from gate-drive supply ripple and from the inrush transient that occurs when the output begins switching at full gate charge. Refer to the Electrical Characteristics table for the exact threshold values of each option.

Output Stage UVLO behavior:

- **Start-up:** While V_{DDx}−V_{SSx} is below V_{VDDx_ON}, the corresponding output is held low through an active clamp regardless of the input pin state. The output is released to follow the input only after the supply rises above V_{VDDx_ON}.

- **Run-time brown-out:** If the supply later collapses below V_{VDDx_OFF}, the output is forced low and the active clamp re-engages. Normal operation resumes only after the supply recovers above V_{VDDx_ON} (one full hysteresis above the falling threshold).
- **Active clamp during unbiased state:** When neither V_{DDx} nor V_{SSx} is biased, an internal clamp pulls OUTx toward V_{SSx} and limits the OUTx voltage to roughly the V_{th} of the lower NMOS device (typically 2 V). This prevents shoot-through in the external power switch when only the bus rail is present.
- **Power-up delay:** After $V_{DDx}-V_{SSx}$ crosses V_{VDDx_ON}, the output begins to follow the input after t_{VDD+} (see Electrical Characteristics).

Output Stage UVLO is independent of the VCCI UVLO on the input side. The two protections are layered: a VCCI UVLO event holds both outputs low through the digital path before any signal reaches the isolation barrier, while a per-channel Output Stage UVLO acts locally on the output side after the barrier. As a result, an output is released to follow its input only when both (a) VCCI is above V_{VCCI_ON}, and (b) the corresponding $V_{DDx}-V_{SSx}$ is above V_{VDDx_ON}. See the TPM21550x VDD UVLO Logic Table for the per-input/per-output truth table during a VDD UVLO event.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPM21550 is an isolated dual-channel gate driver. The device delivers 4.1-A peak source current and 6.4-A peak sink current. The device drives MOSFETs, IGBTs, and SiC MOSFETs in high-voltage power-conversion stages.

The reinforced isolation barrier rated at 5 kVRMS separates INA, INB, and DIS from OUTA and OUTB. The common-mode transient immunity reaches 150 V/ns typical. The secondary-side functional isolation supports up to 1500 VDC working voltage between OUTA and OUTB.

Each channel operates as a low-side driver, a high-side driver, or as part of a half-bridge. The DT pin programs the dead time with an external resistor. The DIS pin forces both outputs low for fault shutdown.

Typical Application

Typical Application

The figure below shows the typical application schematic of the TPM21550 driving a half-bridge power stage.

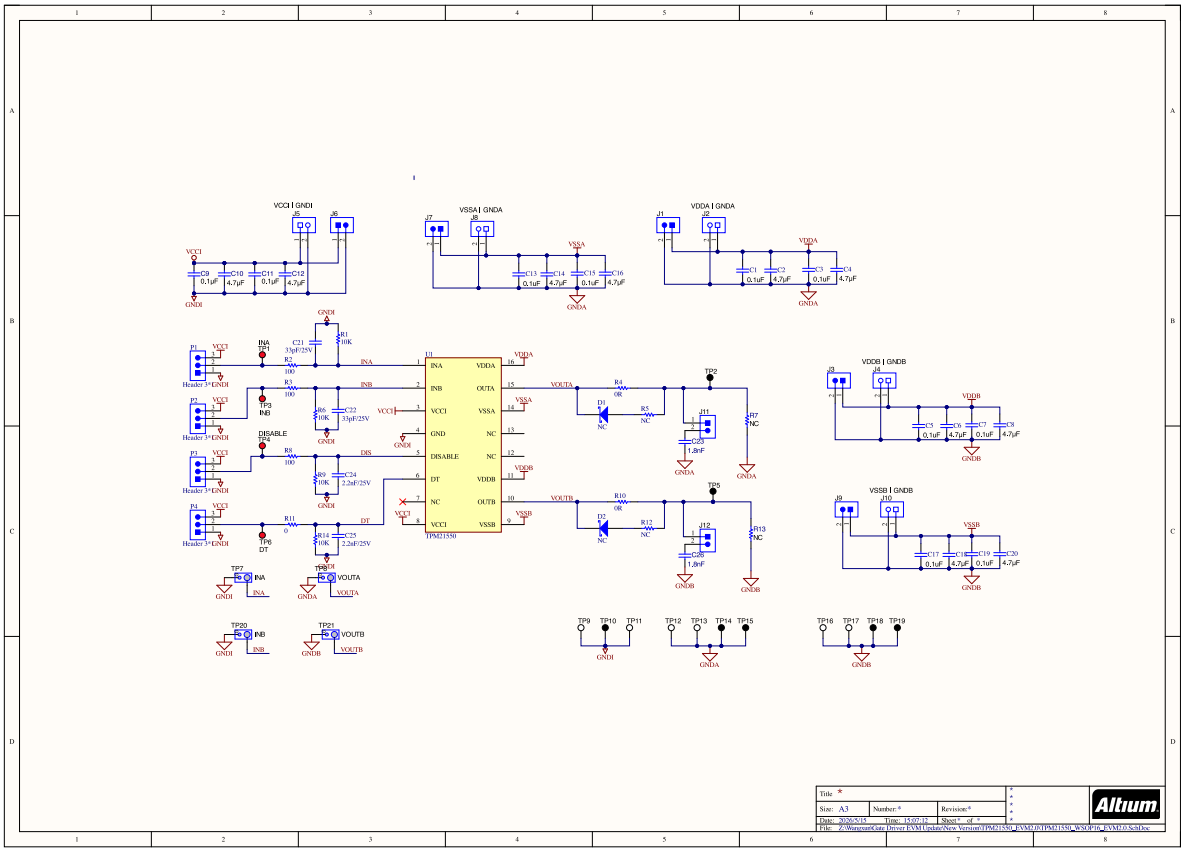


Figure 31. Typical Application Circuit

Design Requirements

The system specifies VCCI at 5 V on the logic side. The system specifies VDD at 15 V on the gate-drive side. The switching frequency is 100 kHz. The power switches are SiC MOSFETs in a half-bridge.

Target dead time between OUTA and OUTB is 100 ns. The input signals swing from 0 V to 3.3 V from a microcontroller.

Detailed Design Procedure

Place one 100-nF ceramic capacitor between VCCI and GND. Place one 1-µF ceramic capacitor between VDD and VSS. Locate each capacitor within 2 mm of the supply pin.

Select the dead-time resistor RDT to set the target dead time. Connect RDT between the DT pin and VSS. Tie DT to VCCI when no dead time is needed.

Drive INA and INB from the microcontroller PWM outputs. Tie DIS low or leave DIS open during normal operation. Pull DIS high to force OUTA and OUTB low during fault shutdown.

Route OUTA and OUTB with short, wide traces to the MOSFET gates. Keep the gate-drive loop area small. Use a separate return trace from each MOSFET source back to VSS.

Application Performance Plots

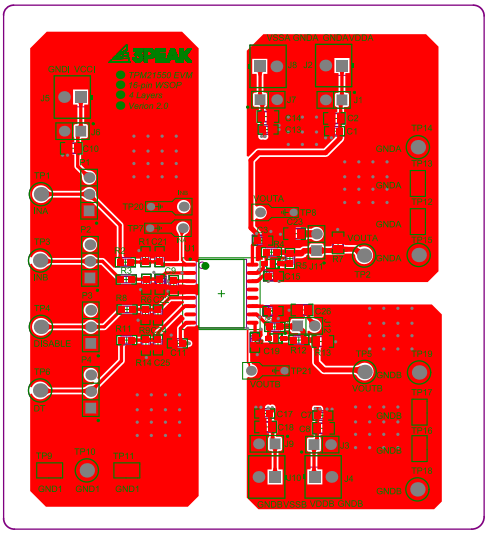
Refer to the Typical Performance Characteristics section for propagation delay, rise time, fall time, and quiescent current waveforms measured in the recommended application configuration.

Layout

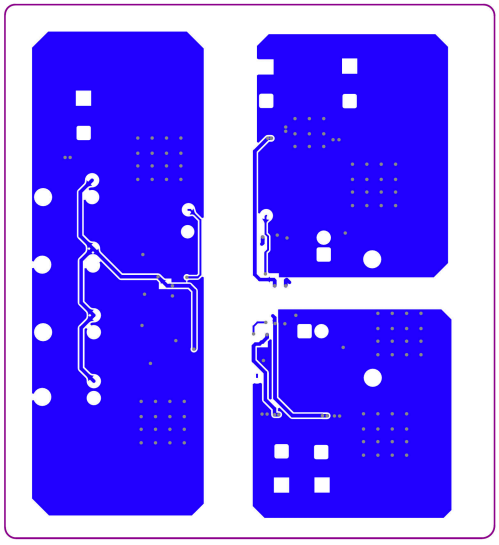
Layout Guideline

- Place low-ESR / low-ESL ceramic decoupling capacitors as close to the device as possible — between VCCI and GND on the primary side, and between VDDA–VSSA / VDDB–VSSB on each secondary channel — to support high transient currents during gate switching. Keep each decoupling loop area small.
- To minimize the inductance of the drive circuit loop, the driver should be placed close to the transistor.
- The Miller clamp trace should be directly connected to the gate of the transistor, and the trace should be kept short.
- To ensure isolation between the primary and secondary sides, avoid placing any PCB traces or copper directly below the driver device. A PCB cutout or groove is recommended to increase the creepage distance.
- To enhance thermal performance, enlarge the PCB copper area connected to VDDA / VSSA / VDDB / VSSB and add multiple thermal vias to the inner power planes.

Layout Recommendations

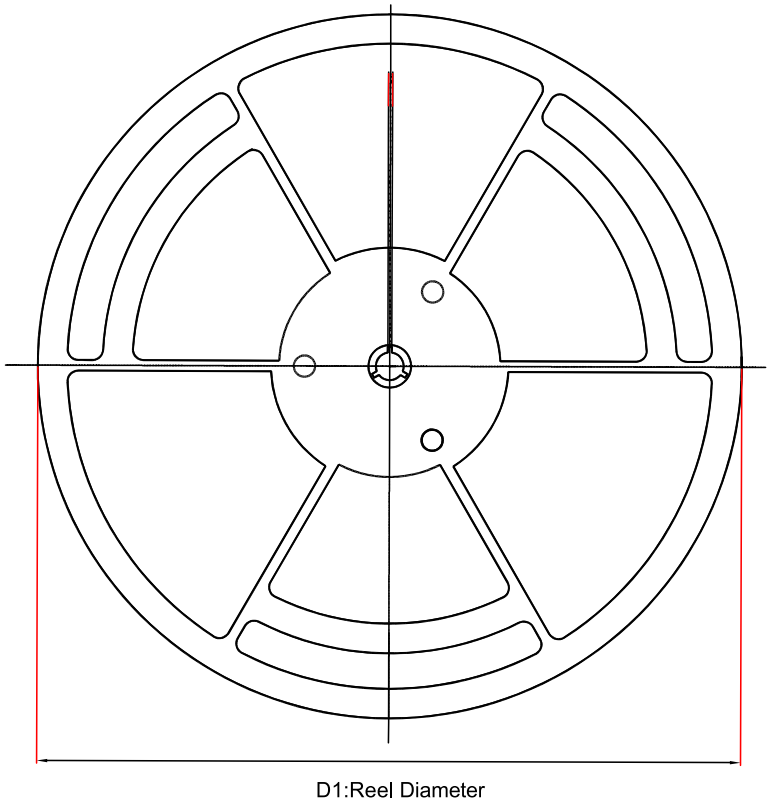


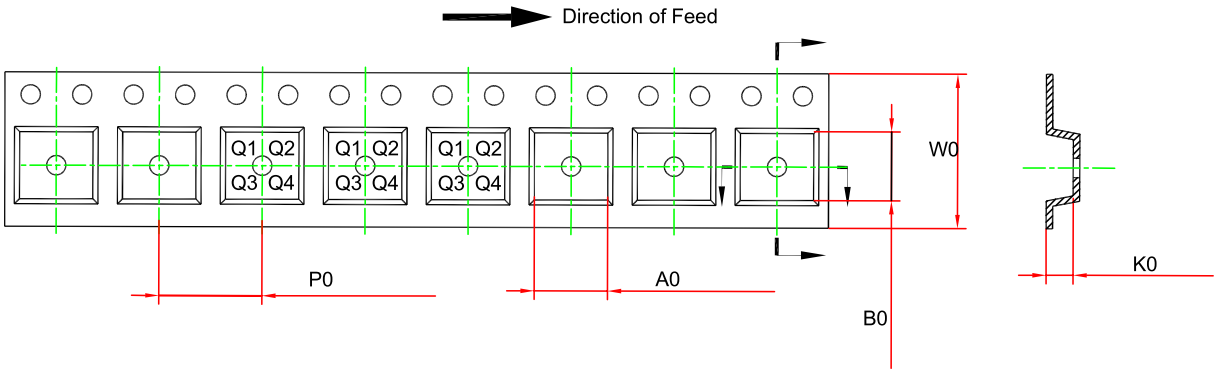
Top Layer



Bottom Layer

Tape and Reel Information





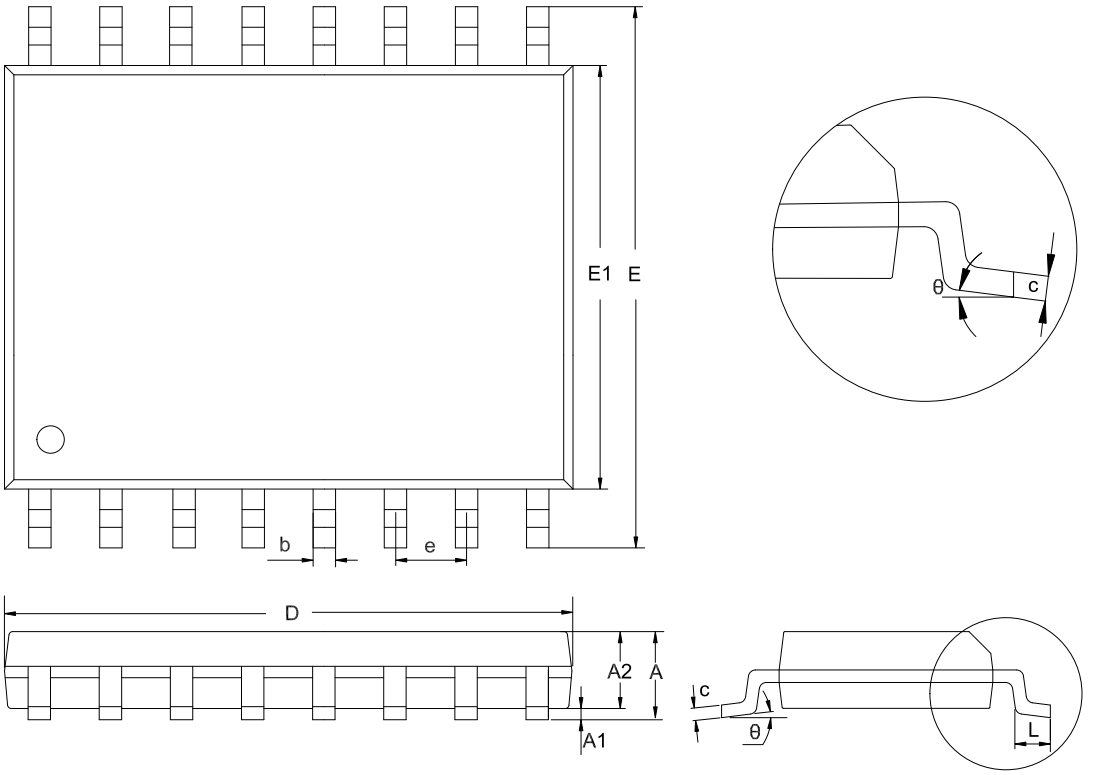
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM21550A-SOBR	WSOP16	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21550B-SOBR	WSOP16	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21550C-SOBR	WSOP16	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21550D-SOBR	WSOP16	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21550E-SOBR	WSOP16	330	21.6	10.9	10.8	3.1	12	16	Q1

Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM21551A-SOBR	WSOP16	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21551B-SOBR	WSOP16	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21551C-SOBR	WSOP16	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21551D-SOBR	WSOP16	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21551E-SOBR	WSOP16	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21550A-SOGR	WSOP14	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21550B-SOGR	WSOP14	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21550C-SOGR	WSOP14	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21550D-SOGR	WSOP14	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21550E-SOGR	WSOP14	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21551A-SOGR	WSOP14	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21551B-SOGR	WSOP14	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21551C-SOGR	WSOP14	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21551D-SOGR	WSOP14	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21551E-SOGR	WSOP14	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21550AQ-SOBR-S	WSOP16	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21550BQ-SOBR-S	WSOP16	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21550CQ-SOBR-S	WSOP16	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21551AQ-SOBR-S	WSOP16	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21551BQ-SOBR-S	WSOP16	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21551CQ-SOBR-S	WSOP16	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21550AQ-SOGR-S	WSOP14	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21550BQ-SOGR-S	WSOP14	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21550CQ-SOGR-S	WSOP14	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21551AQ-SOGR-S	WSOP14	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21551BQ-SOGR-S	WSOP14	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM21551CQ-SOGR-S	WSOP14	330	21.6	10.9	10.8	3.1	12	16	Q1

Package Outline Dimensions

WSOP16

Package Outline Dimensions SOB(WSOP-16-A)



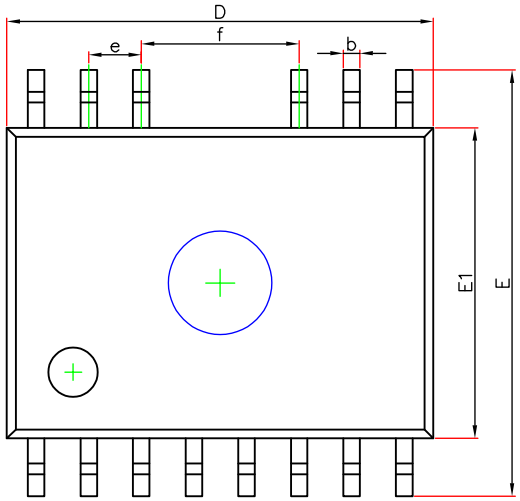
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	2.350	2.650	0.093	0.104
A1	0.100	0.300	0.004	0.012
A2	2.250	2.350	0.089	0.093
b	0.350	0.450	0.014	0.018
c	0.200	0.290	0.008	0.011
D	10.100	10.500	0.398	0.413
E	10.100	10.600	0.398	0.417
E1	7.300	7.700	0.287	0.303
e	1.270 BSC		0.050 BSC	
L	0.500	0.850	0.020	0.033
θ	0	8°	0	8°

NOTES

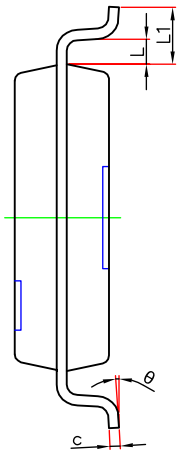
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

WSOP14

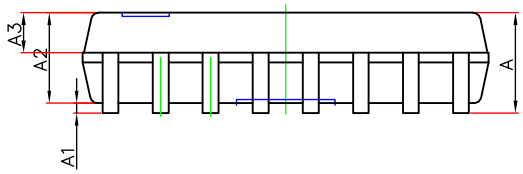
Package Outline Dimensions — SOG (WSOP-14-A)



TOP VIEW



SIDE VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	-	2.650	-	0.104
A1	0.100	0.300	0.004	0.012
A2	2.250	2.350	0.089	0.093
A3	0.970	1.070	0.038	0.042
b	0.350	0.430	0.014	0.017
c	0.250	0.290	0.010	0.011
D	10.200	10.400	0.402	0.409
e	1.270 BSC		0.050 BSC	
E	10.100	10.500	0.398	0.413
E1	7.400	7.600	0.291	0.299
f	3.810 BSC		0.150 BSC	
L	0.550	0.850	0.022	0.033
L1	1.400 REF		0.060 REF	
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Ambient Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPM21550A-SOBR	−40 to 125°C	WSOP16	M550A	3	Tape and Reel, 1500	Green
TPM21550B-SOBR	−40 to 125°C	WSOP16	M550B	3	Tape and Reel, 1500	Green
TPM21550C-SOBR	−40 to 125°C	WSOP16	M550C	3	Tape and Reel, 1500	Green
TPM21550D-SOBR (1)	−40 to 125°C	WSOP16	M550D	3	Tape and Reel, 1500	Green
TPM21550E-SOBR (1)	−40 to 125°C	WSOP16	M550E	3	Tape and Reel, 1500	Green
TPM21551A-SOBR (1)	−40 to 125°C	WSOP16	M551A	3	Tape and Reel, 1500	Green
TPM21551B-SOBR (1)	−40 to 125°C	WSOP16	M551B	3	Tape and Reel, 1500	Green
TPM21551C-SOBR (1)	−40 to 125°C	WSOP16	M551C	3	Tape and Reel, 1500	Green
TPM21551D-SOBR (1)	−40 to 125°C	WSOP16	M551D	3	Tape and Reel, 1500	Green
TPM21551E-SOBR (1)	−40 to 125°C	WSOP16	M551E	3	Tape and Reel, 1500	Green
TPM21550A-SOGR	−40 to 125°C	WSOP14	M550A	3	Tape and Reel, 1500	Green
TPM21550B-SOGR	−40 to 125°C	WSOP14	M550B	3	Tape and Reel, 1500	Green
TPM21550C-SOGR	−40 to 125°C	WSOP14	M550C	3	Tape and Reel, 1500	Green
TPM21550D-SOGR (1)	−40 to 125°C	WSOP14	M550D	3	Tape and Reel, 1500	Green
TPM21550E-SOGR (1)	−40 to 125°C	WSOP14	M550E	3	Tape and Reel, 1500	Green
TPM21551A-SOGR (1)	−40 to 125°C	WSOP14	M551A	3	Tape and Reel, 1500	Green
TPM21551B-SOGR (1)	−40 to 125°C	WSOP14	M551B	3	Tape and Reel, 1500	Green
TPM21551C-SOGR (1)	−40 to 125°C	WSOP14	M551C	3	Tape and Reel, 1500	Green
TPM21551D-SOGR (1)	−40 to 125°C	WSOP14	M551D	3	Tape and Reel, 1500	Green
TPM21551E-SOGR (1)	−40 to 125°C	WSOP14	M551E	3	Tape and Reel, 1500	Green

Order Number	Operating Ambient Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPM21550AQ-SOBR-S (1)	−40 to 125°C	WSOP16	M550A	3	Tape and Reel, 1500	Green
TPM21551AQ-SOBR-S (1)	−40 to 125°C	WSOP16	M551A	3	Tape and Reel, 1500	Green
TPM21550BQ-SOBR-S	−40 to 125°C	WSOP16	M550B	3	Tape and Reel, 1500	Green
TPM21551BQ-SOBR-S (1)	−40 to 125°C	WSOP16	M551B	3	Tape and Reel, 1500	Green
TPM21550CQ-SOBR-S (1)	−40 to 125°C	WSOP16	M550C	3	Tape and Reel, 1500	Green
TPM21551CQ-SOBR-S (1)	−40 to 125°C	WSOP16	M551C	3	Tape and Reel, 1500	Green
TPM21551CQ-SOGR-S (1)	−40 to 125°C	WSOP14	M551C	3	Tape and Reel, 1500	Green
TPM21550AQ-SOGR-S (1)	−40 to 125°C	WSOP14	M550A	3	Tape and Reel, 1500	Green
TPM21551AQ-SOGR-S (1)	−40 to 125°C	WSOP14	M551A	3	Tape and Reel, 1500	Green
TPM21550BQ-SOGR-S	−40 to 125°C	WSOP14	M550B	3	Tape and Reel, 1500	Green
TPM21551BQ-SOGR-S (1)	−40 to 125°C	WSOP14	M551B	3	Tape and Reel, 1500	Green
TPM21550CQ-SOGR-S (1)	−40 to 125°C	WSOP14	M550C	3	Tape and Reel, 1500	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

(1) Contact 3PEAK representatives for more information

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