4.2-A Source, 7.8-A Sink, 5.7-kV$_{RMS}$ Dual-Channel Isolated Gate Driver

Features

- Automotive Grade 1 (TPM21520Q)
- Dual-Channel Isolated Gate Drivers with TTL/CMOS-Compatible Inputs
- 4.2-A Source/7.8-A Sink Peak Output Current with Rail-to-Rail Output
- 30-V Output Driver Supply Voltage
- 3-V to 20-V Input VCCI Range to Interface
- 5-V, 8-V, 10-V, and 12-V V_{DD} UVLO Options
- 5-V Reverse Polarity Voltage Handling Capability on Input Stage
- Programmable Overlap and Dead Time
- Ultra-Fast Output Driving
  - 30-ns Propagation Delay
  - 10-ns Minimum Pulse Width
  - 5-ns Delay Matching
  - 6-ns Pulse Width Distortion
- 5.7-kV$_{RMS}$ Reinforced Isolation Rating
- ±125-kV/μs Common-Mode Transient Immunity (CMTI)
- Industrial Standard Wide-Body WSOP16 Package
- Operating Ambient Temperature T_A: −40°C to +125°C
- Safety-Related Certifications: (In progress)
  - CQC Certification per GB4943.1-2022 (in progress)
  - CB Certification per IEC 62368-1:2023 (in progress)
  - 5.7-kV$_{RMS}$ Isolation Rating per UL 1577 (in progress)
  - CSA Component Acceptance Notice 5A (in progress)
  - DIN EN IEC 60747-17(VDE 0884-17): 2021-10 (in progress)

Applications

- Automotive On-board Charge, DCDC Converters
- Automotive Compressor, Thermal Management System
- Isolated Converters in DC-DC and AC-DC Power Supplies
- Server, Telecom, IT, and Industrial Infrastructures
- Motor Drive and DC-to-AC Solar Inverters
- Solar Inverters, Battery, and Energy Storage

Description

The TPM21520 series consists of isolated dual-channel gate drivers that feature 4.2-A source and 7.8-A sink peak current. These drivers are specifically designed to power MOSFETs, IGBTs, and SiC MOSFETs, with ultra-low propagation delay and minimal pulse-width distortion.

The input side of the TPM21520 series is isolated from its two output drivers by a reinforced isolation barrier rated at 5.7 kVRMS, providing a typical of 125-V/ns common-mode transient immunity (CMTI). Additionally, the two secondary-side drivers feature internal functional isolation, enabling a working voltage of up to 1500 V_{DC}.

Each driver within the series offers flexible configuration options, functioning as either two low-side drivers, two high-side drivers, or as a half-bridge driver with a programmable dead time. For safety measures, a dedicated disable pin is included. When the pin is set to high, both outputs are simultaneously shut down. Leaving this pin open or grounding, it allows for normal operation. Furthermore, the system incorporates a fail-safe mechanism that forces both outputs to go low in the event of a primary-side logic failure.

Typical Application Circuit

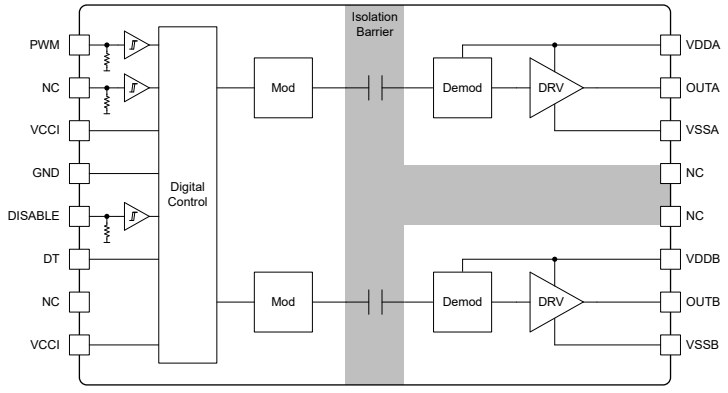


Table of Contents

Product Family Table

Order Number	UVLO Threshold (V)	Package	Quality Grade
TPM21520-SOBR	12.5	WSOP16	Industrial
TPM215201-SOBR	8.5	WSOP16	Industrial
TPM215202-SOBR	5	WSOP16	Industrial
TPM215203-SOBR (1)	10	WSOP16	Industrial

(1) Contact sales representatives for more details.

Revision History

Date	Revision	Notes
2025-04-14	Rev.A.0	Initial release
2025-05-08	Rev.A.1	Misc correction

Pin Configuration and Functions

TPM21520
WSOP16
Top View

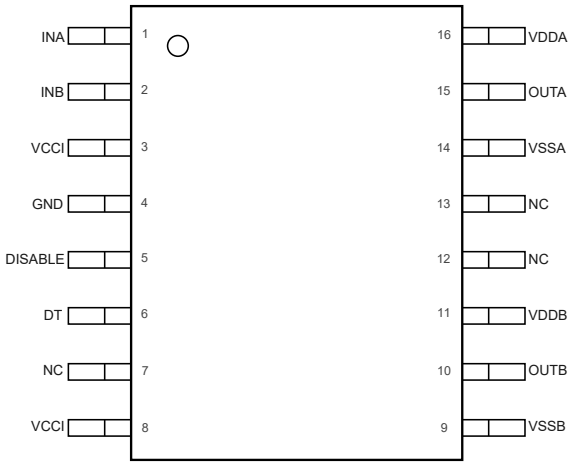


Table 1. Pin Functions: TPM21520x

Pin		I/O	Description
No.	Name		
1	INA	I	Input for A Channel, TTL/CMOS input threshold, pulled down internally. If unused, connect this pin to ground for better noise resistance.
2	INB	I	Input for B Channel, TTL/CMOS input threshold, pulled down internally. If unused, connect this pin to ground for better noise resistance.
3	VCCI	P	Primary side supply voltage. Internally connected to PIN 8. Use a low ESR/ESL capacitor close to the device to decouple the ground for stable operation.
4	GND	P	Primary side GND. All signals on the primary side are referenced to this ground connection.
5	DISABLE	I	Device disable. Internally pulled down. For better noise resistance, tie it to ground if unused. If connecting to a distant microcontroller, use a 1-nF capacitor near the DISABLE pin for bypassing.
6	DT	I	Deadtime control input. Programmable deadtime between output signals. Connect DT to VCCI for no delay, or use a resistor (500 Ω to 500 kΩ) between DT and GND to adjust the delay. Add a 2.2-nF or larger ceramic capacitor next to the resistor and avoid leaving the DT pin unconnected.
7	NC	NC	Not connected
8	VCCI	P	Primary side supply voltage. Internally connected to PIN 3. Use a low ESR/ESL capacitor close to the device to decouple the ground for stable operation.
9	VSSB	P	Channel B secondary ground. Ground reference for secondary side B channel.

Pin		I/O	Description
No.	Name		
10	OUTB	O	Channel B secondary output. Connect this pin to the gate terminal of the MOSFET, IGBT, GaN HEMT, or SiC FET in the A channel.
11	VDDB	P	Channel B secondary power. Use a low ESR/ESL capacitor close to the device to decouple the ground for stable operation.
12	NC	NC	Not connected
13	NC	NC	Not connected
14	VSSA	P	Channel A secondary ground. Ground reference for secondary side A channel.
15	OUTA	O	Channel A secondary output. Connect this pin to the gate terminal of the MOSFET, IGBT, GaN HEMT, or SiC FET in the A channel.
16	VDDA	P	Channel A secondary power. Use a low ESR/ESL capacitor close to the device to decouple the ground for stable operation.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Input Voltage	Input bias Pin Supply Voltage, VCCI refer to GND	−0.3	25	V
	Input Signal Voltage, INA, INB, DISABLE, refer to GND	−5	VCCI + 0.3	V
	Input Signal Voltage, DT refer to GND	−0.3	VCCI + 0.3	V
Output Voltage	Output Supply Voltage, V_{DDA} − V_{SSA}, V_{DDB} − V_{SSB}	−0.3	30	V
	OUTA to VSSA, OUTB to VSSB	− 0.3	V_{DDx} + 0.3	V
	OUTA to VSSA, OUTB to VSSB, transient for 200 ns	− 2	V_{DDx} + 0.3	V
	Channel-to-Channel Voltage, VSSA-VSSB, VSSB-VSSA	−1500	1500	V
T_J	Maximum Junction Temperature	−40	150	°C
T_A	Operating Ambient Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.
(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
V_{CCI} – GND	Primary Side Supply Voltage	3	20	V
V_{DDA} – V_{EEA} V_{DDB} – V_{EEB} –	Output Supply Voltage (12-V UVLO)	13.5	28	V
	Output Supply Voltage (10-V UVLO)	11.5	28	V
	Output Supply Voltage (8-V UVLO)	9.2	28	V
	Output Supply Voltage (5-V UVLO)	6.5	28	V
T_J	Junction Temperature	−40	150	°C
T_A	Operating Ambient Temperature	−40	125	°C

Safety Limiting Values

Parameter		Test Conditions	Min	Typ	Max	Unit
P_D	Safety Input, Output, or Total Power	V_{CCI} = 18 V, $V_{DDA/B}$ = 12 V, INA/B = 3.3 V, 3 MHz 50% duty cycle square wave 1-nF load			1.05	W
P_{DA} P_{DB}	Power Dissipation by Each Output Driver				0.5	W
P_I	Power Dissipation by Primary Side				0.05	W
I_S	Safety Output Supply Current	$R_{\theta JA}$ = 70°C/W, VDDA/B = 12 V, T_A = 25°C, T_J = 150°C			70	mA
		$R_{\theta JA}$ = 70°C/W, VDDA/B = 25 V, T_A = 25°C, T_J = 150°C			35	mA
P_S	Safety Supply Power, INPUT	$R_{\theta JA}$ = 70°C/W, T_A = 25°C, T_J = 150°C			50	mW
	Safety Supply Power, DRIVER A				900	mW
	Safety Supply Power, DRIVER B				900	mW
	Safety Supply Power, Total				1850	mW
T_S	Maximum Safety Temperature				150	°C

Insulation Specifications

Parameter		Conditions	Value	Unit
CLR	External Clearance	Shortest terminal-to-terminal distance through air	> 8	mm
CPG	External Creepage	Shortest terminal-to-terminal distance across the package surface	> 8	mm
DTI	Distance through the Insulation	Minimum internal gap (internal clearance)	> 21	μm
CTI	Comparative Tracking Index		> 600	V
	Material Group		I	
	Installation Classification per IEC 60664-1	For Rated Mains Voltage ≤ 600 V_{RMS}	I-IV	
		For Rated Mains Voltage ≤ 1000 V_{RMS}	I-III	
	Pollution Degree		2	
	Climate Category		40/125/21	
C_{IO}	Isolation Capacitance	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	1.2	pF
R_{IO}	Isolation Resistance	V_{IO} = 500 V, T_A = 25 °C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125 °C	> 10^{11}	
		V_{IO} = 500 V, T_A = 150 °C	> 10^9	
V_{IORM}	Maximum Repetitive Isolation Voltage	AC voltage (bipolar)	1700	V_{PK}
	Maximum working Isolation Voltage	AC voltage (sine wave); time dependent dielectric breakdown (TDDB)	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IOWM}	Maximum Working Isolation Voltage	AC voltage; TDDB Test	1060	V_{RMS}
		DC voltage	1500	V_{DC}
V_{IOTM}	Maximum Transient Isolation Voltage	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production)	8000	V_{PK}
V_{IOSM}	Maximum Surge Isolation Voltage	Test method per IEC 62368-1, 1.2/50 μs waveform, V_{TEST} = 1.3 × V_{IOSM}(qualification) = 10000 v	7692	V_{PK}
V_{ISO}	UL 1577 Withstand Isolation Voltage	V_{TEST} = V_{ISO} = 5700 V_{RMS}, t = 60 s (in qualification), V_{TEST} = 1.2 × V_{ISO}- 6840 V_{RMS} ， t = 1 s (100% in production)	5700	V_{RMS}
q_{pd}	Apparent Charge	Method a, After Input/Output safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10 s	≤ 5	pC
		Method a, After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10 s	≤ 5	

Parameter		Conditions	Value	Unit
		Method b1; At routine test (100% production) and preconditioning (type test), V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1 s	≤ 5	

(1) All pins on each side of the barrier tied together create a two-terminal device.

Electrical Characteristics

All test conditions: V_{DDA} = V_{DDB} = 15 V, V_{SSA} and V_{SSB} referred as GND, T_A = −40°C to 125°C, unless otherwise noted. Typical value is tested at V_{DDA} = V_{DDB} = 15 V.

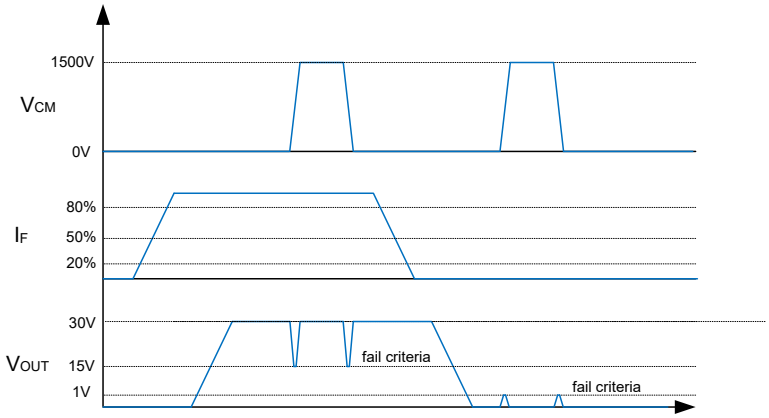
Parameter		Conditions	Min	Typ	Max	Unit
Supply						
I_{VCCI}	VCCI Quiescent Current	VINA = 0 V, VINB = 0 V		1.5	2	mA
I_{VDDA},I_{VDDB}	VDDA and VDDB Quiescent Current	VINA = 0 V, VINB = 0 V, VDD = 15 V		1.25	2.5	mA
I_{VCCI}	VCCI Operating Current	*f* = 500 kHz, current per channel, C_{OUT} = 100 pF		2.0		mA
I_{VDDA},I_{VDDB}	VDDA and VDDB Operating Current	*f* = 500 kHz, current per channel, C_{OUT} = 100 pF, VDD = 15V		2.5		mA
V_{VCCI_ON}	Rising Threshold		2.55	2.7	2.85	V
V_{VCCI_OFF}	Falling Threshold VCCI_OFF		2.35	2.5	2.68	V
V_{VCCI_HYS}	Threshold Hysteresis			0.2		V
Input						
VINAH, VINBH,	Input High Voltage VDISH		1.6	1.7	1.9	V
VINAL, VINBL, VDISL	Input Low Voltage		1.15	1.3	1.45	V
VINA_HYS, VINB_HYS, VDIS_HYS	Input Hysteresis			0.4		V
VINA, VINB	Negative Transient, ref to GND, 50 ns pulse		–5			V
Output UVLO - 5V						
V_{VDDA_ON}, V_{VDDB_ON}	Rising Threshold VDDA_ON, VDDB_ON		5.58	5.78	6.1	V
V_{VDDA_OFF}, VVDDB_OFF	Falling Threshold VDDA_OFF, VDDB_OFF		5.3	5.58	5.9	V
V_{VDDA_HYS}, V_{VDDB_HYS}	Threshold Hysteresis			0.2		V
Output UVLO - 8V						
V_{VDDA_ON}, V_{VDDB_ON}	Rising Threshold VDDA_ON, VDDB_ON		8.3	8.7	9.2	V

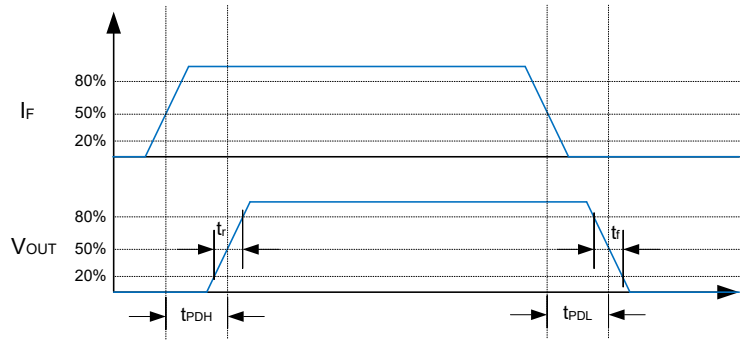
Parameter		Conditions	Min	Typ	Max	Unit
V_{VDDA_OFF}, V_{VDDB_OFF}	Falling Threshold VDDA_OFF, VDDB_OFF		7.8	8.2	8.7	V
V_{VDDA_HYS}, V_{VDDB_HYS}	Threshold Hysteresis			0.5		V
Output UVLO - 12V						
V_{VDDA_ON}, V_{VDDB_ON}	Rising Threshold VDDA_ON, VDDB_ON		13	13.6	14	V
V_{VDDA_OFF}, V_{VDDB_OFF}	Falling Threshold VDDA_OFF, VDDB_OFF		12.2	12.8	13.2	V
V_{VDDA_HYS}, V_{VDDB_HYS}	Threshold Hysteresis			0.8		V
Output						
V_{OUTPD}	Output Active Pull down on OUTx	I_{OUT} = 0.1*$I_{OUT(L)}$,V_{DDx} = OPEN		2.4		V
I_{OA+}, I_{OB+}	Peak Output Source Current	C_{VDD} = 10 µF, C_{LOAD} = 0.18 µF, f = 1 kHz		4.2		A
I_{OA-}, I_{OB-}	Peak Output Sink Current	C_{VDD} = 10 µF, C_{LOAD} = 0.18 µF, f = 1 kHz		7.8		A
R_{OHA}, R_{OHB}	Output Resistance at High State	I_{OUT} = –10 mA, T_A = 25°C, R_{OHA}, R_{OHB}		5		Ω
R_{OLA}, R_{OLB}	Output Resistance at Low State	I_{OUT} = 10 mA, T_A = 25°C		0.55		Ω
V_{OHA}, V_{OHB}	Output Voltage at High State	V_{VDDA}, V_{VDDB} = 15 V, I_{OUT} = –10 mA, T_A = 25°C		14.95		V
V_{OLA}, V_{OLB}	Output Voltage at Low State	V_{VDDA}, V_{VDDB} = 15 V, I_{OUT} = 10 mA, T_A = 25°C		5.5		mV
Timing						
t_{DEAD}	Dead Time	Pull DT pin to VCCI	Determined by INA and INB			
		DF pin floating	0.8		15	ns
		R_{DT} = 20 kΩ	160	200	240	ns
t_{RISE}	Output Rise Time, 20% to 80% measured points	COUT = 1.8 nF		6	16	ns
t_{FALL}	Output Fall Time, 90% to 10% measured points	COUT = 1.8 nF		7	12	ns
t_{PWmin}	Minimum Pulse Width	Output off for less than minimum, COUT = 0 pF			20	ns
t_{PDHL}	Propagation Delay from INx to OUTx Falling Edges			30		ns
t_{PDLH}	Propagation Delay from INx to OUTx Rising Edges			30		ns
t_{PWD}(1)	Pulse Width Distortion |tPDLH – tPDHL|				6	ns

Parameter		Conditions	Min	Typ	Max	Unit
t_{DM} (1)	Propagation Delays Matching between VOUTA, VOUTB	f = 100 kHz			5	ns
t_{VDD+} to OUT VDDA, VDDB	Power-up Delay Time: UVLO Rise to OUTA, OUTB.	INA or INB tied to VCCI		8	12	μs

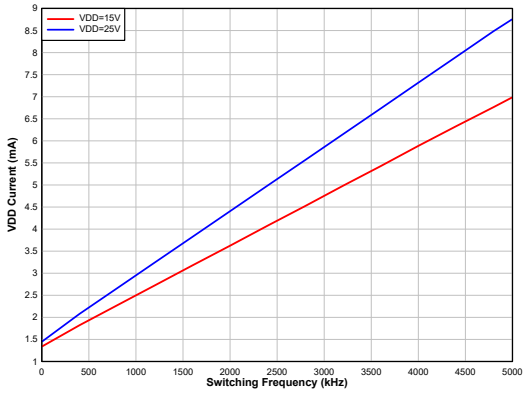
(1) Guaranteed by design

Parameter Measurement



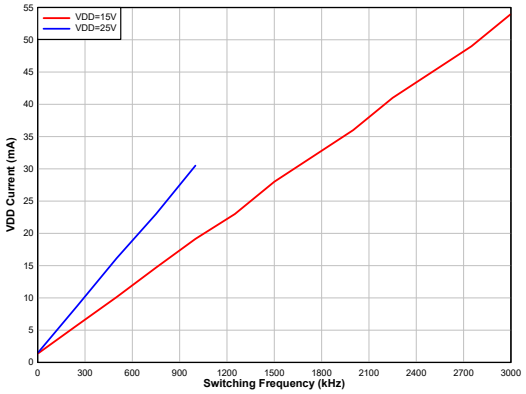


Typical Performance Characteristics



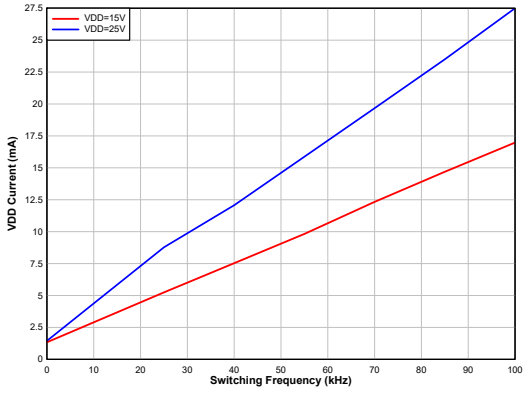
No Load, VDD = 15 V or 25 V

Figure 1. VDDx Current Consumption vs. Frequency



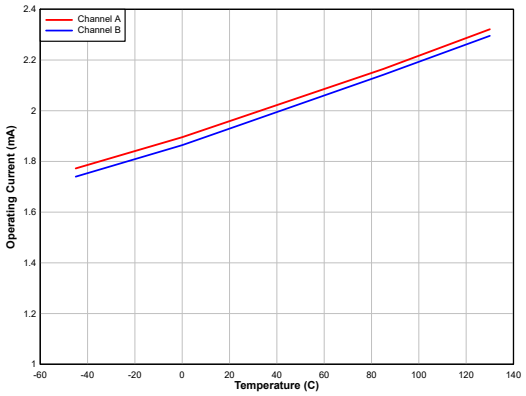
1-nF Load, VDD = 15 V or 25 V

Figure 2. VDDx Current Consumption vs. Frequency



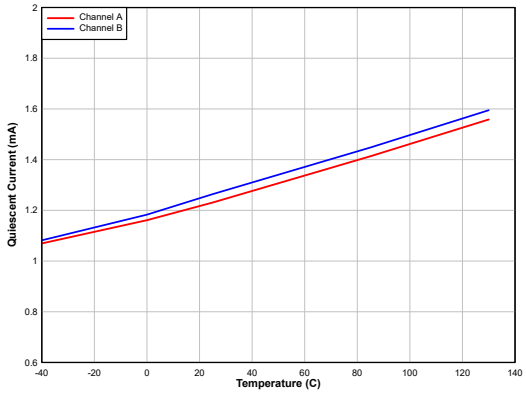
10-nF Load, VDD = 15 V or 25 V

Figure 3. VDDx Current Consumption vs. Frequency



No Load, VDD = 15 V, *f* = 500 kHz

Figure 4. VDDx Current Consumption vs. Temperature



No load, input low, no switching, VDD = 15 V

Figure 5. VDDx Quiescent Current Consumption vs. Temperature

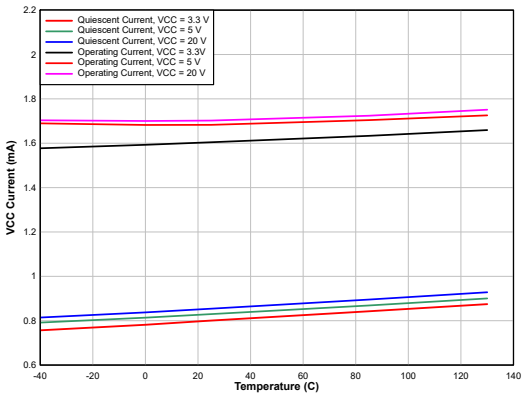
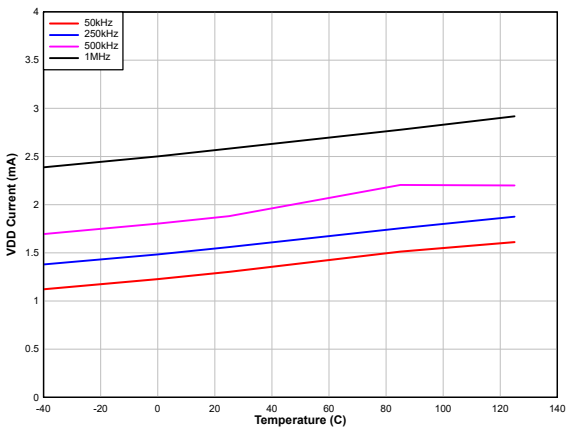


Figure 6. VCCI Current Consumption vs. Temperature



No load, input low, VDD = 15 V

Figure 7. VDDx Switching Current Consumption vs. Temperature

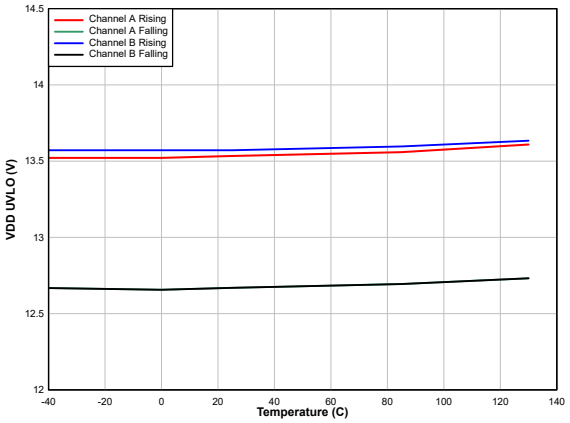


Figure 8. VDD 12-V UVLO Threshold vs. Temperature

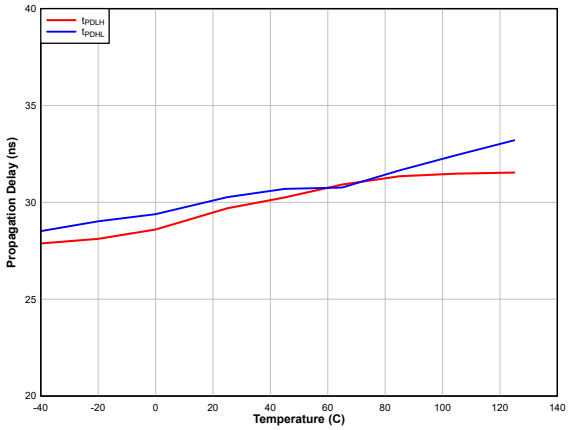


Figure 9. Propagation Delay vs. Temperature

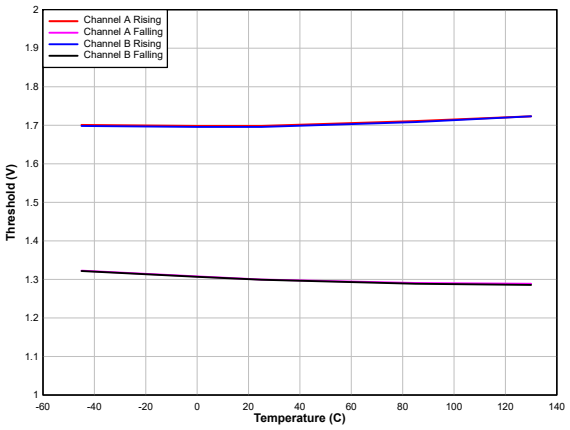


Figure 10. INx/DISABLE Threshold vs. Temperature

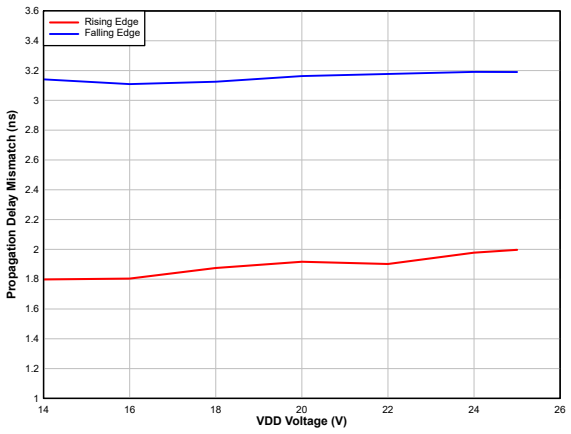


Figure 11. Propagation Delay Matching (t_{DM}) vs. VDD

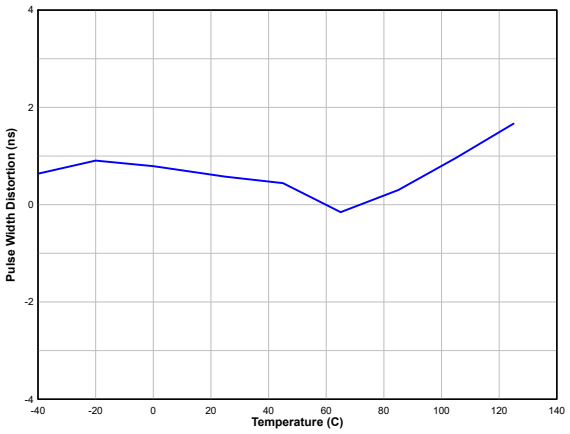
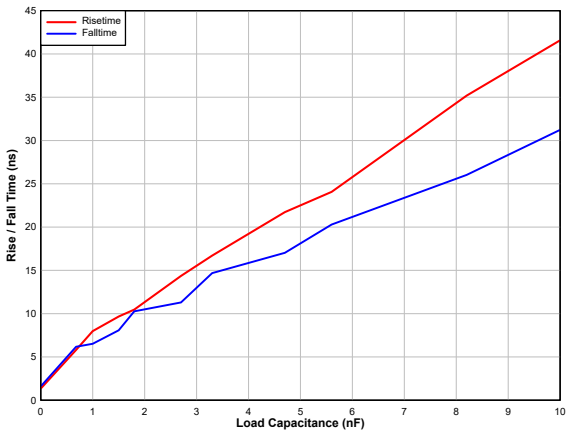
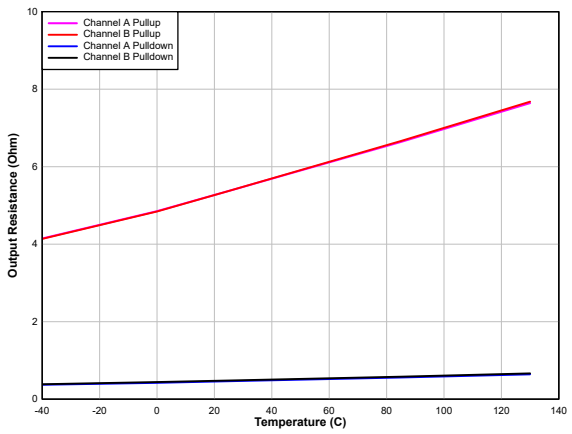


Figure 12. Pulse Width Distortion vs. Temperature



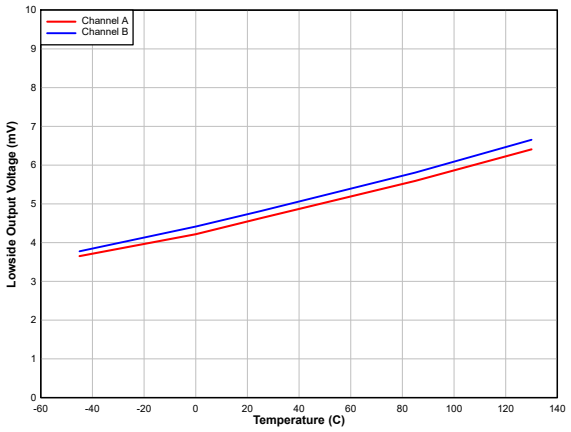
VDD = 12 V

Figure 13. Rise and Fall Time vs. Load Capacitance



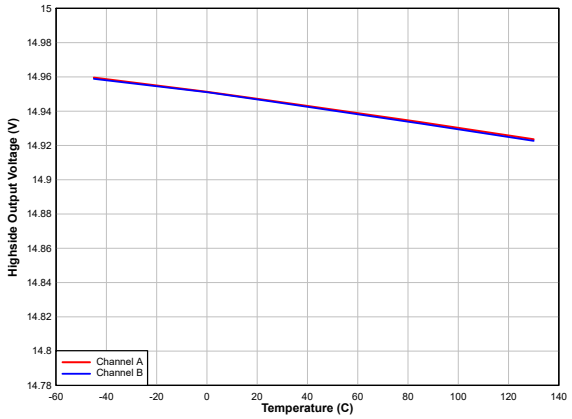
VDD = 12 V

Figure 14. Output Resistance vs. Temperature



VDD = 15 V, I_{OUT} = 10 mA

Figure 15. VOL vs. Temperature



VDD = 15 V, I_{OUT} = −10 mA

Figure 16. VOH vs. Temperature

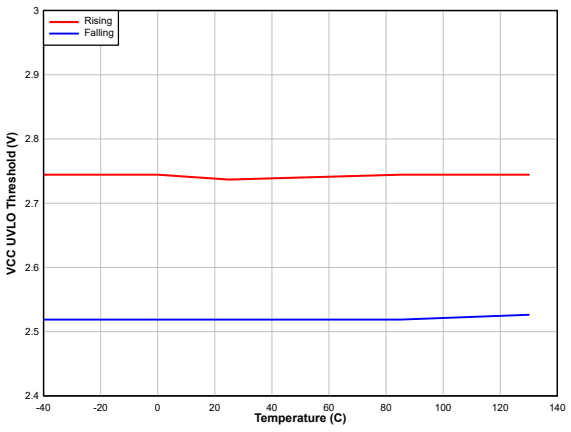


Figure 17. VCC UVLO Threshold vs. Temperature

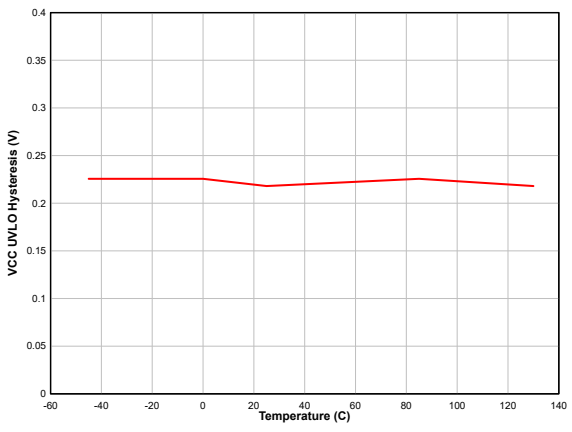


Figure 18. VCC UVLO Hysteresis vs. Temperature

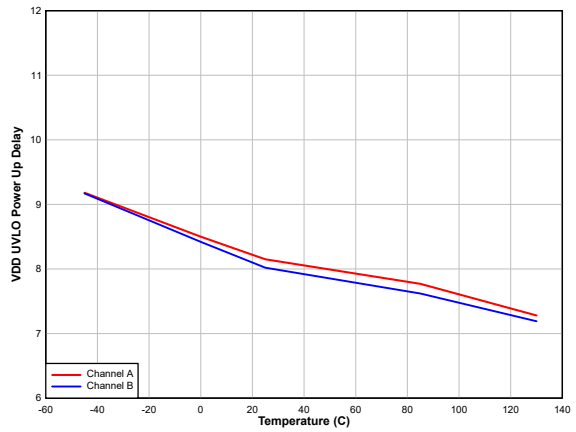


Figure 19. VDD UVLO Delay vs. Temperature

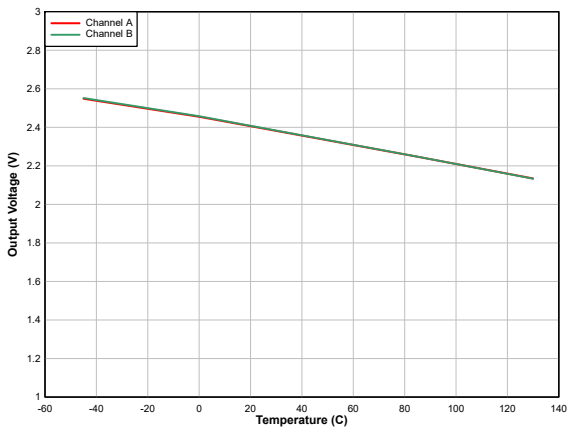


Figure 20. Active Pulldown Voltage vs. Temperature

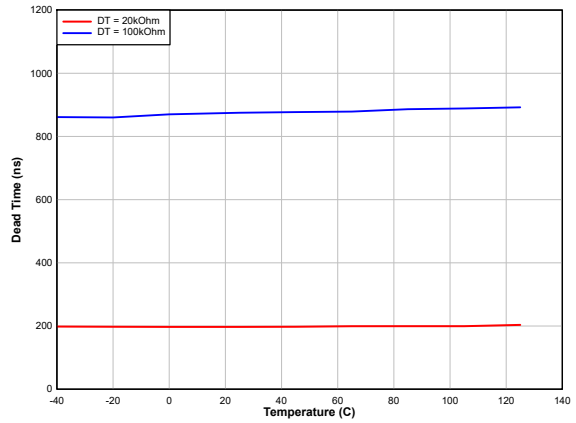


Figure 21. Dead Time vs. Temperature

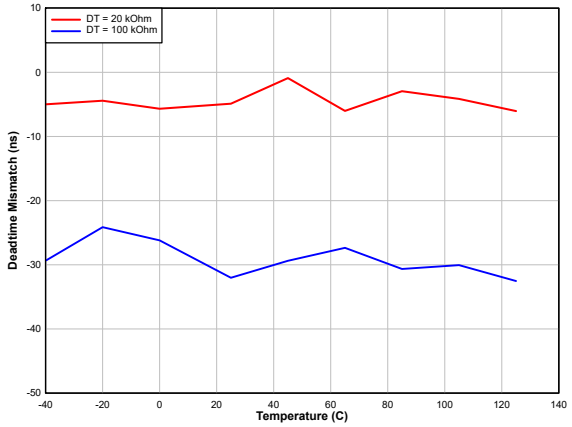
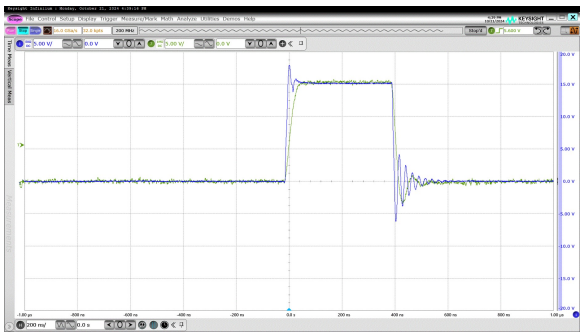


Figure 22. Dead Time Mismatch vs. Temperature



CH: 1-nF Load; CH2 10-nF Load

Figure 23. Typical Output Waveform

Detailed Description

Overview

The TPM21520 family of dual gate drivers is designed for high-performance power transistor switching. These drivers act as an isolated bridge between controllers and transistor gates, ensuring efficient and reliable operation. With their ability to adapt to various power supply and motor systems, as well as support for different transistors, including GaN HEMT, IGBT, and SiC MOSFETs, the TPM21520 family offers versatility and flexibility. Advanced features such as programmable dead time control and voltage protection enhance system safety and stability. Whether used with digital or analog controllers, the TPM21520 family provides a robust solution for power transistor driving needs.

Functional Block Diagram

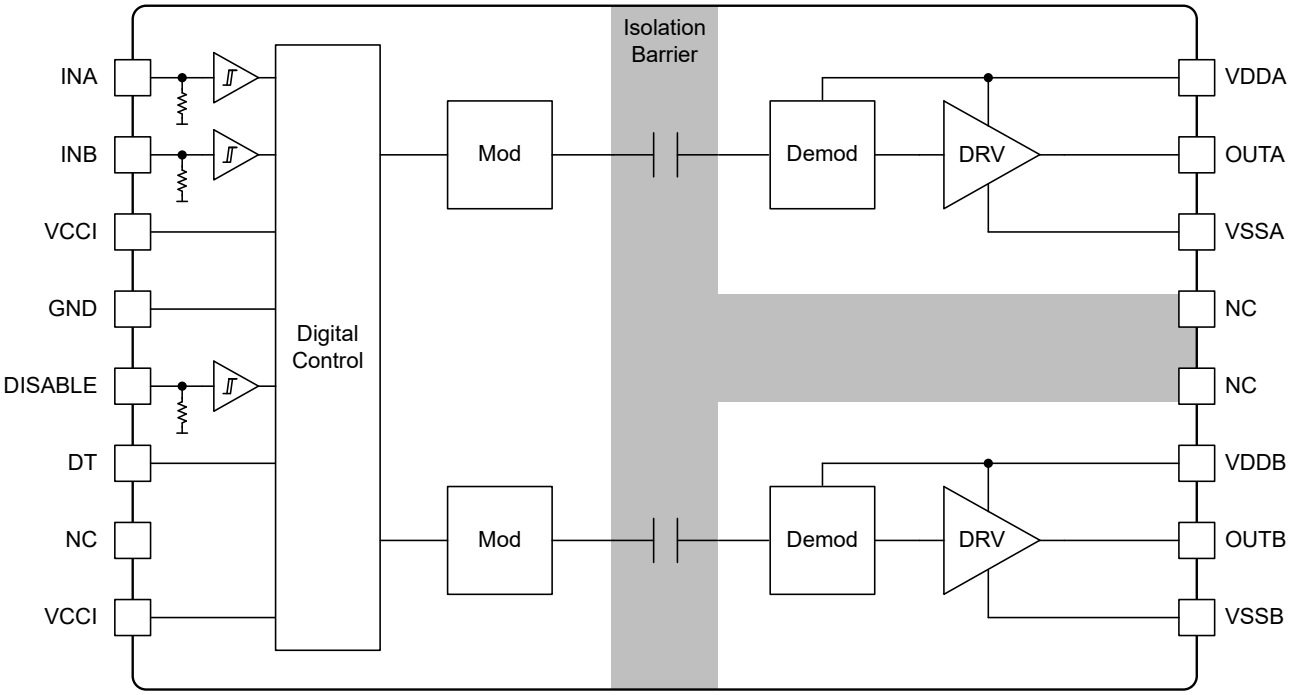


Figure 24. Functional Block Diagram

Feature Description

Supply and UVLO

The TPM21520 family of gate drivers features internal undervoltage lock-out (UVLO) protection on both the supply circuit and the input side. This UVLO function ensures reliable operation by monitoring VDD and VCCI voltages.

For the VDD supply circuit, if the bias voltage falls below a certain threshold (V_{VDD_ON} at the rising edge or V_{VDD_OFF} at the falling edge), the UVLO protection activates, holding the affected output low regardless of the input pin status. This prevents potential damage or malfunction due to insufficient bias voltage.

Additionally, the TPM21520 family incorporates an active clamp circuit that keeps the driver outputs low when the output stages are in an unbiased or UVLO condition. This clamp circuit limits the voltage rise on the driver outputs, effectively clamping them to the threshold voltage of the lower NMOS device, typically around 2 V, when no bias power is available.

To enhance stability and prevent chatter caused by ground noise from the power supply, the VDD UVLO protection in the TPM21520 family includes a hysteresis feature (V_{VDD_HYS}). This hysteresis also allows the device to tolerate small drops in bias voltage that may occur during switching operations or sudden increases in operating current consumption.

The input side of the TPM21520 family has a UVLO protection feature that monitors the VCCI voltage. The device remains inactive until the VCCI voltage exceeds a certain threshold (V_{VCCI_ON}) during start-up. Once operational, if the VCCI voltage drops below another threshold (V_{VCCI_OFF}), the output does not follow inputs and holds low regardless of the input pin status. This input UVLO also includes hysteresis (V_{VCCI_HYS}) for stable operation.

Table 2. TPM21520x VCCI UVLO Logic Table

CONDITION	INPUTS		OUTPUTS	
	INA	INB	OUTA	OUTB
VCCI-GND < V_{VCCI_ON} during device start up	H	L	L	
VCCI-GND < V_{VCCI_ON} during device start up	L	H	L	L
VCCI-GND < V_{VCCI_ON} during device start up	H	H	L	L
VCCI-GND < V_{VCCI_ON} during device start up	L	L	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	H	L	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	L	H	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	H	H	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	L	L	L	L

Table 3. TPM21520x VDD UVLO Logic Table

CONDITION	INPUTS		OUTPUTS	
	INA	INB	OUTA	OUTB
VDD-VSS < V_{VDD_ON} during device start up	H	L	L	L
VDD-VSS < V_{VDD_ON} during device start up	L	H	L	L
VDD-VSS < V_{VDD_ON} during device start up	H	H	L	L
VDD-VSS < V_{VDD_ON} during device start up	L	L	L	L
VDD-VSS < V_{VDD_OFF} after device start up	H	L	L	L
VDD-VSS < V_{VDD_OFF} after device start up	L	H	L	L
VDD-VSS < V_{VDD_OFF} after device start up	H	H	L	L
VDD-VSS < V_{VDD_OFF} after device start up	L	L	L	L

The TPM21520 family of gate drivers incorporates TTL and CMOS-compatible input pins, specifically INA, INB, and DIS, which maintain complete isolation from the VDD supply voltage. These pins are characterized by a high threshold voltage (V_{INAH}) of 1.8 V and a low threshold voltage of 1 V, facilitating seamless integration with logic-level control signals originating from devices such as 3.3-V microcontrollers. Additionally, the input pins exhibit a substantial hysteresis of 0.8 V, significantly enhancing noise immunity and ensuring robust operational stability.

To guarantee reliable device performance, the TPM21520 family incorporates internal pull-down resistors, typically rated at 200 kΩ, which serve to automatically drive any unused input pins to a low voltage state. Nonetheless, it is still recommended to manually ground any unused input pins for optimal device operation.

The isolation between the input circuitry and the output drivers within the TPM21520 family provides flexibility for different applications. The amplitude of the input signal can exceed or fall below the VDD voltage, provided it remains within the manufacturer's recommended operating limits. Crucially, the voltage amplitude of signals applied to the INA or INB pins must

never surpass the VCCI voltage. This inherent flexibility facilitates seamless integration with a wide range of control signal sources, empowering users to select the most appropriate VDD voltage for their specific gate driver requirements.

Table 4. Input Logic Table

INPUTS		DISABLE	OUTPUTS		NOTE
INA	INB		OUTA	OUTB	
L	L	L or Left Open	L	L	If programmable deadtime is used, output transitions occur after the dead time expires.
L	H	L or Left Open	L	H	
H	L	L or Left Open	H	L	
H	H	L or Left Open	L	L	DT is left open or programmed with R_{DT}
H	H	L or Left Open	H	H	DT pin pulled up to VCCI
Left Open	Left Open	L or Left Open	L	L	–
X	X	H	L	L	–

Output Stage

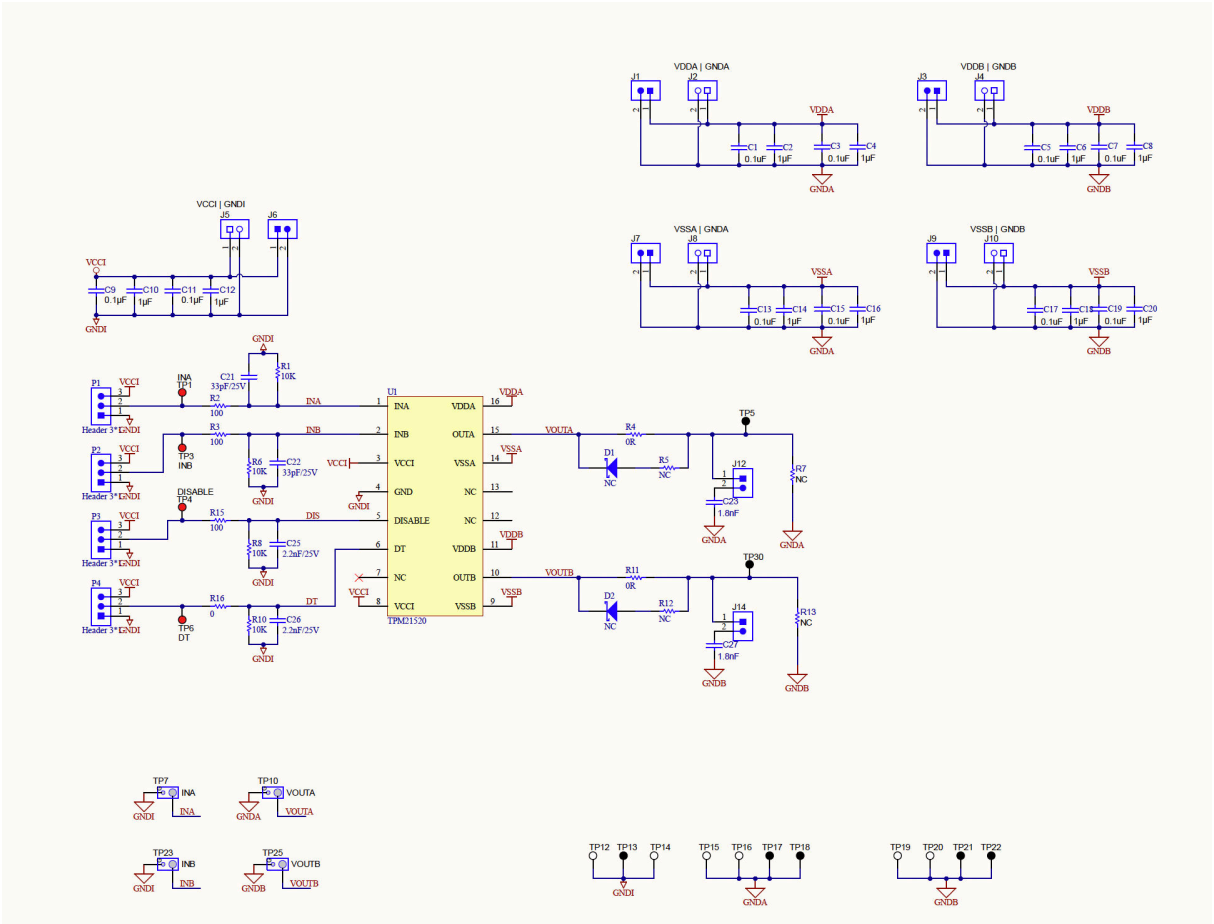
The TPM21520 family features an enhanced output stage designed to optimize power switch turn-on transitions, particularly during the critical Miller plateau region.

Both outputs of the TPM21520 family are capable of delivering robust 4.2-A peak source and 7.8-A peak sink current pulses. The output voltage operates rail-to-rail between VDD and VSS, with minimal dropout. This design enhances the overall performance and reliability of the gate drivers in demanding applications.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Typical Application

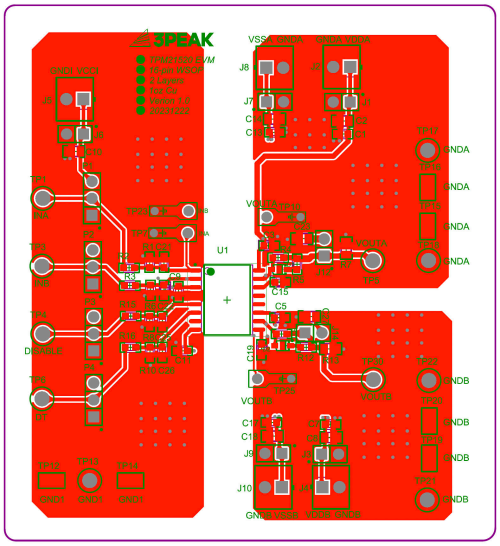


Layout

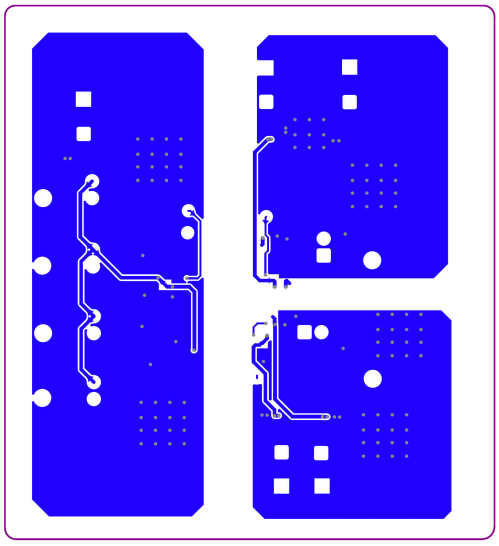
Layout Guideline

- For voltage mode input drivers, a low ESR and ESL capacitor should be placed close to the VCC and VEE pins, and the loop from VCC to VEE should be small.
- For current mode input drivers, a low ESR and ESL capacitor should be placed close to the Cathode and Anode pins.
- To minimize the inductance of the drive circuit loop, the driver should be placed close to the transistor.
- The Miller clamp trace should be directly connected to the gate of the transistor, and the trace should be kept short.
- To ensure isolation between the primary and secondary sides, avoid placing any PCB traces or copper directly below the driver device. A PCB cutout or groove is recommended to increase the creepage distance.
- To enhance thermal performance, it is recommended to enlarge the PCB copper connected to VCC and VEE.

Layout Recommendations

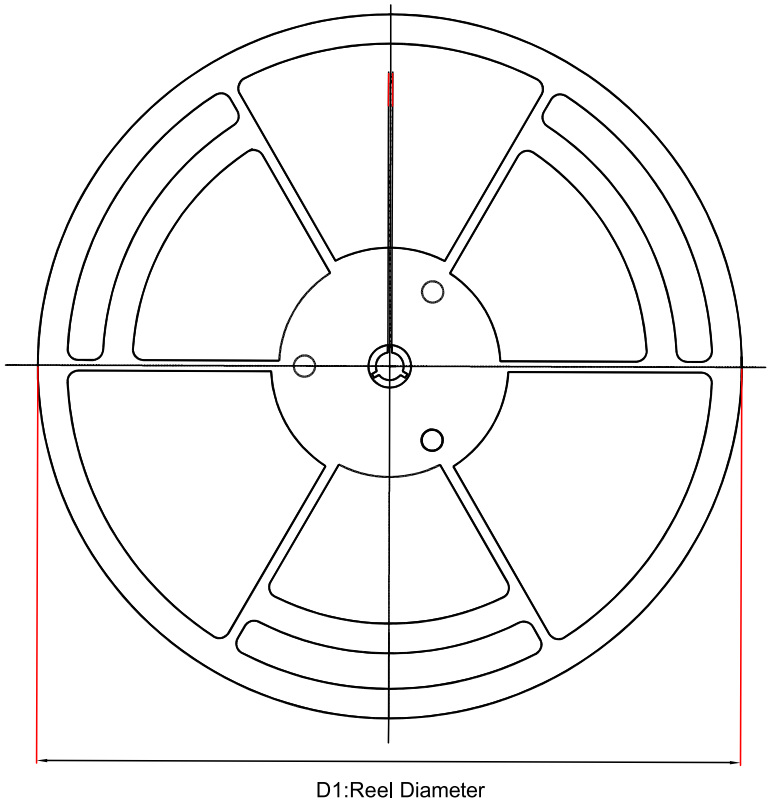


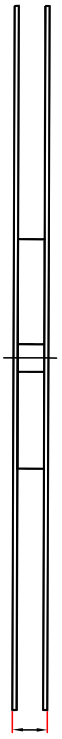
Top Layer

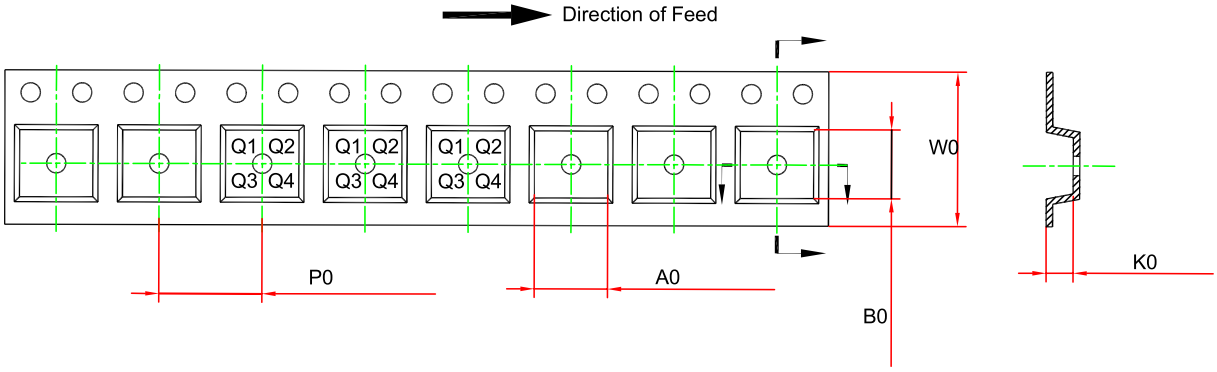


Bottom Layer

Tape and Reel Information







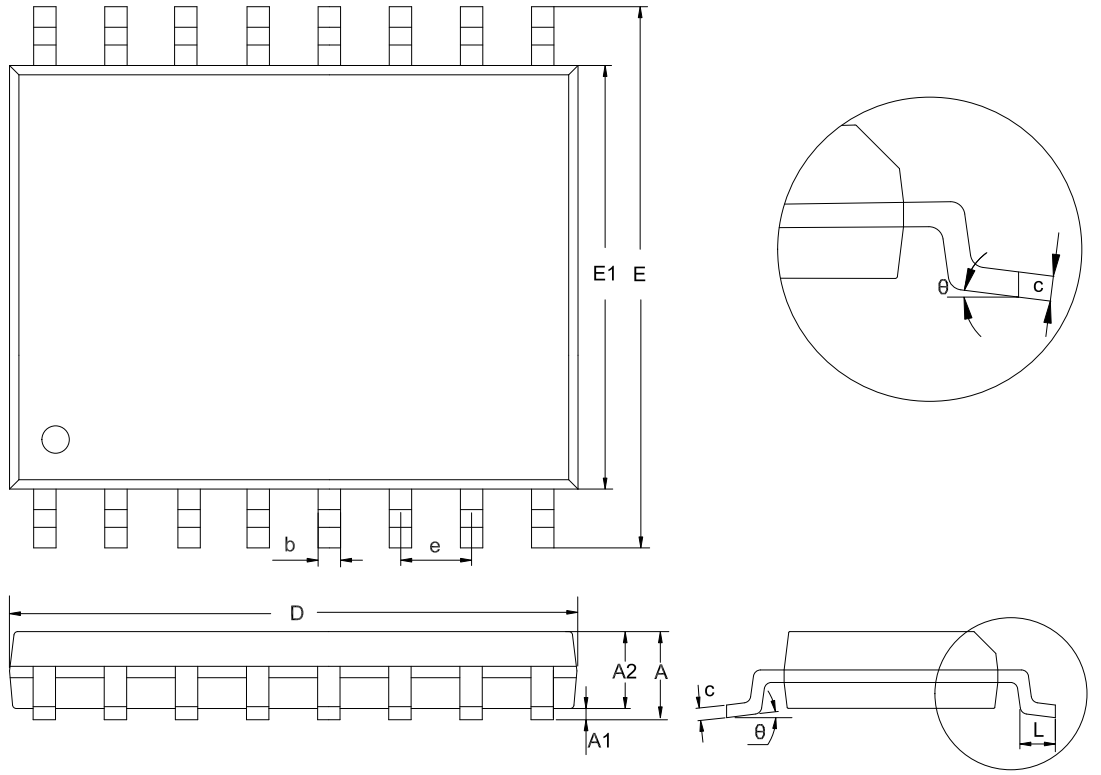
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM21520-SOBR	WSOP16	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM215201-SOBR	WSOP16	330	21.6	10.9	10.8	3.1	12	16	Q1
TPM215202-SOBR	WSOP16	330	21.6	10.9	10.8	3.1	12	16	Q1

Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM215203-SOBR	WSOP16	330	21.6	10.9	10.8	3.1	12	16	Q1

Package Outline Dimensions

WSOP16

Package Outline Dimensions SOB(WSOP-16-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	2.350	2.650	0.093	0.104
A1	0.100	0.300	0.004	0.012
A2	2.250	2.350	0.089	0.093
b	0.350	0.450	0.014	0.018
c	0.200	0.290	0.008	0.011
D	10.100	10.500	0.398	0.413
E	10.100	10.600	0.398	0.417
E1	7.300	7.700	0.287	0.303
e	1.270 BSC		0.050 BSC	
L	0.500	0.850	0.020	0.033
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Ambient Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPM21520-SOBR	−40 to 125°C	WSOP16	M2520	3	Tape and Reel, 1500	Green
TPM215201-SOBR	−40 to 125°C	WSOP16	M2521	3	Tape and Reel, 1500	Green
TPM215202-SOBR	−40 to 125°C	WSOP16	M2522	3	Tape and Reel, 1500	Green
TPM215203-SOBR (1)	−40 to 125°C	WSOP16	M2523	3	Tape and Reel, 1500	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

(1) Contact 3PEAK representatives for more information

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