150-V, 0.3-Ω DrMOS with 100% Duty Cycle Support

Features

- 7-V to 150-V Input Voltage for MOSFET
- 3.0-V to 6.0-V Device Power Supply Range
- 15-A Source and Sink Pulse Current Capability
- Internal Charge Pump Supporting 100% Duty Cycle Operation
- 10-ns Deglitch Time for Logic Input
- 40-ns Propagation Delay Time
- 3-V/ns Rising and Falling Slew Rate
- Over Current Protection
- Short Circuit Protection
- Operating T_J Temperature Range from −40°C to +125°C
- Available in an 8-pin SOP Package

Applications

- High-Current Driver for Capacitive Load
- High-Voltage Converter
- Piezo Driver

Description

The TPM1525 is a monolithic half-bridge power stage with built-in 150-V MOSFETs and drivers. The device can source and sink 15-A pulse current with up to 150-V input power supply voltage.

The TPM1525 offers 10-ns deglitch time for logic input. The dead time is optimized to minimize the propagation delay time. The rising and falling time is well controlled to optimize the EMI performance.

The TPM1525 provides over-current protection and short-circuit protection for output.

With an internal charge pump, the TPM1525 supports a 100% duty cycle that maintains the high side MOSFET at on-state when the logic input level at the IN pin is at the high level.

The TPM1525 is available in an 8-pin SOP package.

Typical Application Circuit

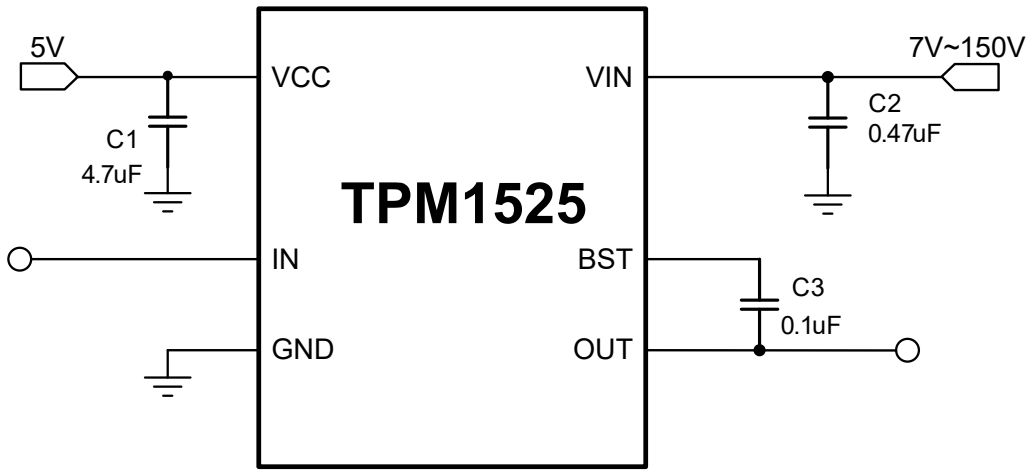


Table of Contents

Revision History

Date	Revision	Notes
2023-02-23	Rev A.0	Initial release
2023-11-02	Rev A.1	Updated typical V_{CC} quiescent current to 180 μA Updated thermal shutdown protection threshold to 160℃ Updated maximum recommended operating V_{IN} to 140 V Corrected typo

Pin Configuration and Functions

TPM1525
SOP8
Top View

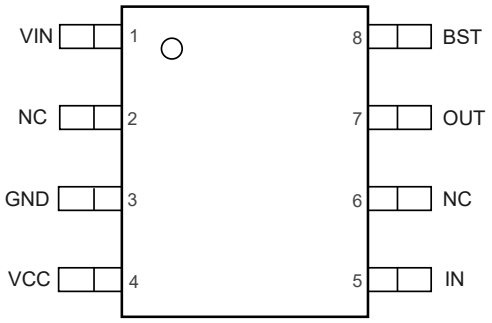


Table 1. Pin Functions: TPM1525

Pin		I/O	Description
No.	Name		
1	VIN	P	Power supply for power stage MOSFETs.
2, 6	NC	-	No connection pins.
3	GND	GND	Power ground of the device.
4	VCC	P	Power supply for the device and the low side MOSFET driver.
5	IN	I	Logic input.
7	OUT	O	Output of the device. It is connected to the source of the high-side NMOS FET and the drain of the low-side NMOS FET.
8	BST	I	Bootstrap pin. Power supply for the high-side MOSFET driver. A ceramic capacitor of 0.1 μF is required between the BST pin and the OUT pin.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Voltage range at terminals	VIN, OUT	−0.3	150	V
	BST	OUT − 0.3	OUT + 6.0	V
	VCC, IN	−0.3	6.0	V
T_J	Maximum Junction Temperature	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.
(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
V_{HBM}	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	2000	V
V_{CDM}	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
V_{IN}	Power Supply for Power Stage MOS FETs	7	140	V
V_{CC}	Power Supply for Device	3.0	5.5	V
T_J	Junction Temperature Range	–40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOP8	122.3	60.4	°C/W

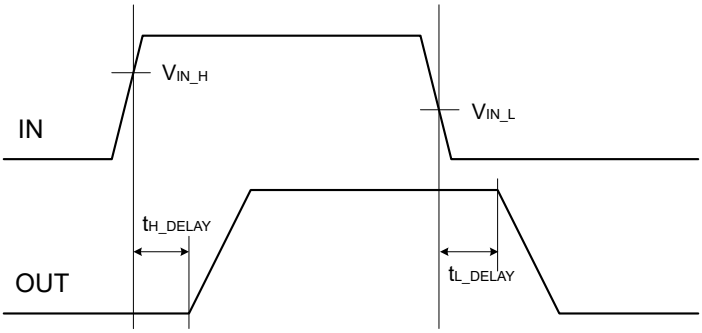
Electrical Characteristics

All test conditions: V_{IN} = 120 V, V_{CC} = 5 V, T_J = −40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C.

Parameter		Conditions	Min	Typ	Max	Unit
Supply Voltage and Current						
V_{VIN}	Supply Voltage Range For Power Stage		7		140	V
V_{VIN_UVLO}	Under Voltage Lockout of V_{IN}	VIN rising	5.5	6.0	6.5	V
V_{VIN_HYS}	V_{IN} UVLO Hysteresis			200		mV
V_{CC}	Supply Voltage Range for Device		3.0		5.5	V
I_{CC}	Operating Quiescent Current from VCC	No switching, the IN pin is at logic high or low level		180		μA
V_{CC_UVLO}	Under Voltage Lockout of V_{CC}	VCC rising	2.6	2.8	3.0	V
V_{CC_HYS}	V_{CC} UVLO Hysteresis		50	100	200	mV
Power MOS FET						
R_{DSON_HS}	On Resistance of High-Side NMOS FET			310		mΩ
R_{DSON_LS}	On Resistance of Low-Side NMOS FET			320		mΩ
Logic Input						
V_{IN_H}	IN Logic High Threshold				1.5	V
V_{IN_L}	IN Logic Low Threshold		0.4			V
V_{IN_HYS}	IN Threshold Hysteresis		300	500		mV
R_{IN}	Internal Pull-Down Resistance at the IN Pin			100		kΩ
Hiccup Protection						
t_{DET} (1)	Over-Current Detection Time			10		μs
t_{HICCUP} (1)	Hiccup Duration Time			100		ms
Timing						
t_{H_DELAY} (1)	IN High to OUT High Delay	From logic input high threshold to OUT starts rising		40		ns
t_{L_DELAY} (1)	IN Low to OUT Low Delay	From logic input low threshold to OUT starts falling		40		ns
t_{RISING} (1)	OUT Rising Time	V_{IN} = 120 V, C_{LOAD} = 3 nF, 10% to 90%		40		ns
$t_{FALLING}$ (1)	OUT Falling Time	V_{IN} = 120 V, C_{LOAD} = 3 nF, 90% to 10%		40		ns
Junction Temperature Protection						
T_{SD} (1)	Thermal Shutdown Protection Threshold	T_J rising		160		ºC
T_{SD_HYS} (1)	Thermal Shutdown Hysteresis	T_J falling below T_{SD}		20		ºC

(1) Guaranteed by design and sample characterization. Not tested in production.

Timing Block Diagram



Typical Performance Characteristics

All test conditions are at V_{CC} = 5 V, T_A = +25°C, unless otherwise noted.

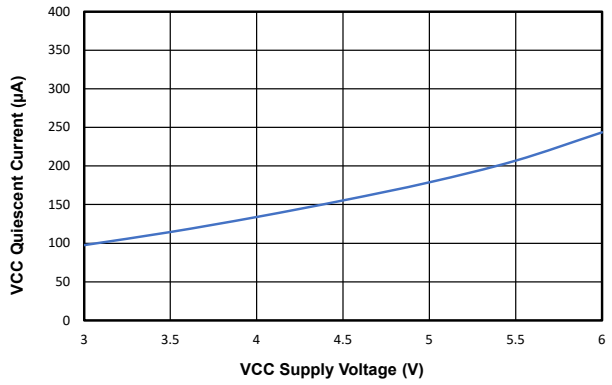


Figure 1. VCC Quiescent Current vs. VCC

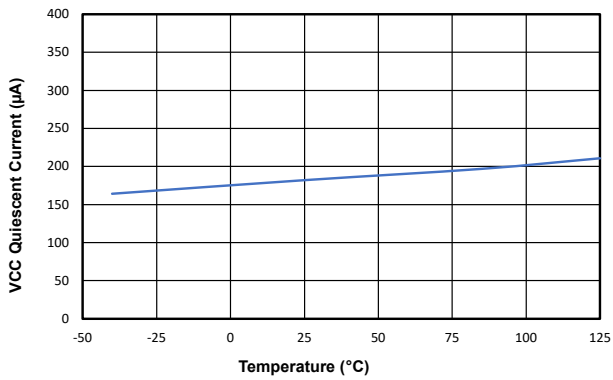


Figure 2. VCC Quiescent Current vs. Temperature

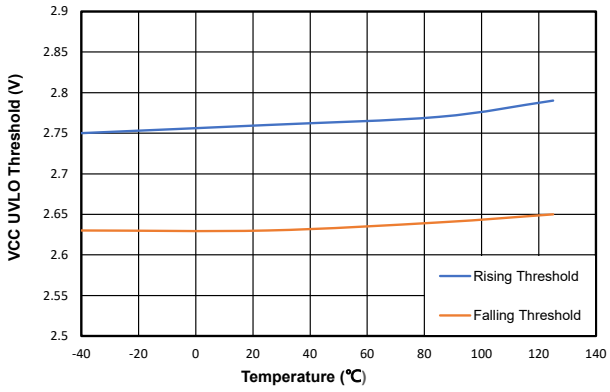


Figure 3. VCC UVLO Threshold vs. Temperature

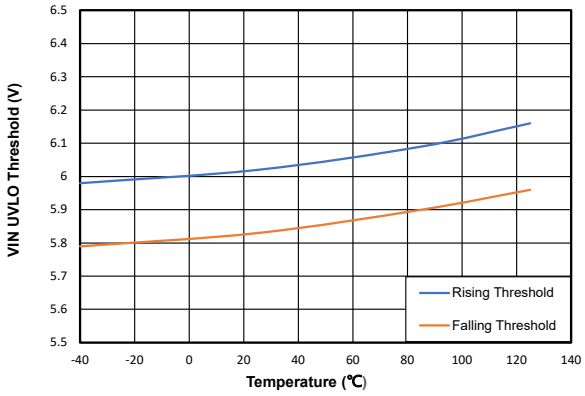
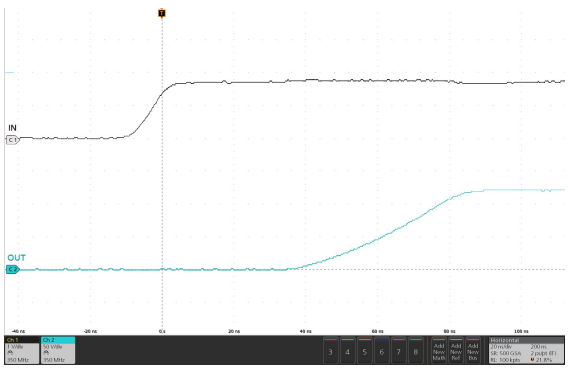
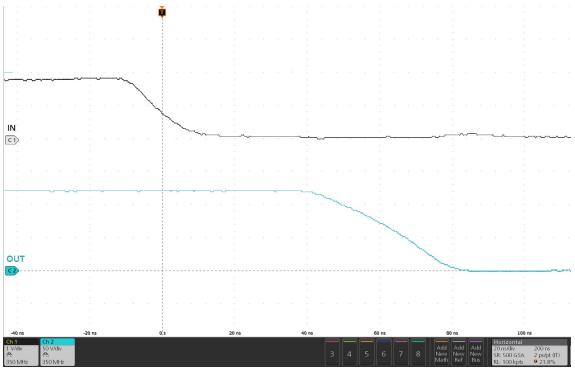


Figure 4. VIN UVLO Threshold vs. Temperature



V_{VIN} = 120 V, C_{LOAD} = 3 nF

Figure 5. OUT Rising Waveform



V_{VIN} = 120 V, C_{LOAD} = 3 nF

Figure 6. OUT Falling Waveform

Detailed Description

Overview

The TPM1525 is a monolithic half-bridge power stage with built-in 150-V MOSFETs and drivers. The device is supplied by the VCC pin and the VIN pin. The TPM1525 accepts a logic PWM signal at the IN pin and outputs the power at the OUT pin. The power MOSFETs of the TPM1525 can source and sink 15-A pulse current. The rising and falling slew rate at the OUT pin is well controlled during switching. With an internal charge pump, the TPM1525 supports 100% duty cycle PWM input signal thus the high-side MOSFET can be always at on state and the output can be maintained at the VIN voltage.

The TPM1525 is designed to drive a capacitive load such as RF PIN diode and piezo transducer. The TPM1525 also can be power stage in a high-voltage DC/DC converter.

Functional Block Diagram

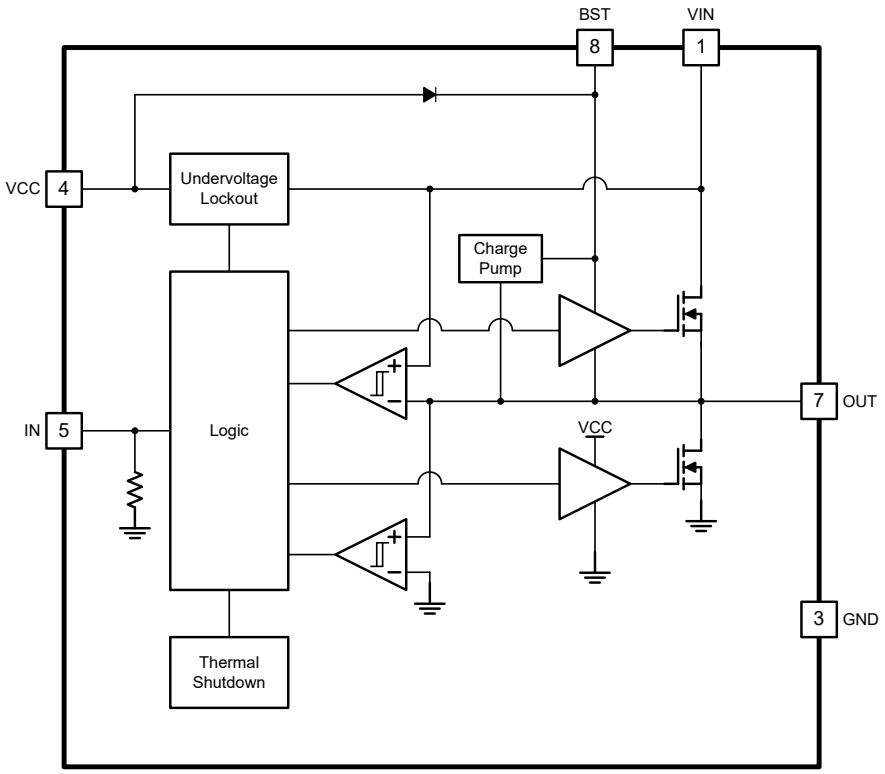


Figure 7. Functional Block Diagram

Feature Description

Power Supply Under-Voltage Lockout

The TPM1525 has two power supply inputs. VCC is the power supply for the internal control circuits and drivers. VIN is the power supply for the internal charge pump and the high-side power MOSFET. Both power supplies have under-voltage lockout thresholds. If one power supply voltage is below its threshold, the device is disabled. In the UVLO state, the high-side power MOSFET is turned off and the low-side power MOSFET is turned on. The voltage at the OUT pin is zero volt regardless of the input voltage level at the IN pin.

Boot Strap Capacitor and Internal Charge Pump

The TPM1525 uses a boost strap capacitor between the OUT pin and the BST pin. The boost strap capacitor is charged to the VCC voltage when the OUT pin is zero volt. When the logic level at the IN pin switches to a high voltage, the boot strap capacitor supplies the high-side driver and turns on the high-side power MOSFET. Afterwards, the internal charge pump starts working to supply the high-side driver and maintain the voltage of the boot strap capacitor.

Current Limit and Output Short-Circuit Protection

The TPM1525 has current limit for both sinking and sourcing. The typical current limit is 20 A. If the load is a large capacitor or the OUT pin is short to a DC voltage or ground, the sinking or sourcing current may reach the current limit.

The TPM1525 sets a duration time of typical 10 μs to avoid over heat on the device. Once the sinking or sourcing current reaches 20 A for 10 μs, the TPM1525 goes into hiccup short-circuit protection. Both high-side MOSFET and low-side MOSFET are turned off for 100 ms. After 100 ms, the TPM1525 resumes the output at the OUT pin.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPM1525 is a monolithic power stage to drive capacitive load or for synchronous buck applications. The device integrates high-performance gate drivers and two power MOSFETs. The TPM1525 accepts a logic PWM signal at the IN pin to drive high-side and low-side MOSFETs. The device controls the slew rate and optimizes the dead time during switching.

Typical Application

The TPM1525 can be used to drive a high-voltage RF PIN diode in wireless infrastructure. The PIN diode is a capacitive load and needs to be turned on and off quickly. The Figure 8 is the typical application circuit. The R1 is to limit the DC current through the PIN diode when the PIN diode is turned on.

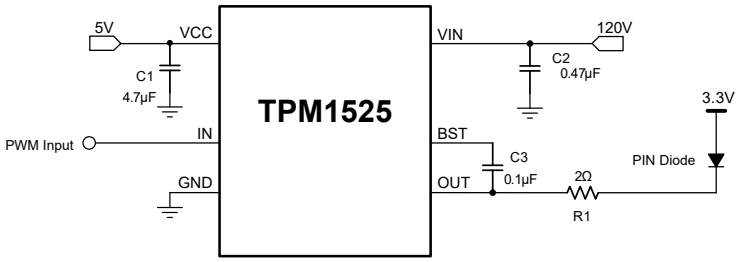


Figure 8. PIN Diode Drive Circuit

System Example

The TPM1525 can be the power stage of a high-voltage synchronous buck converter. The Figure 9 is the typical application. The buck controller outputs logic PWM signal to the IN pin of the TPM1525. The TPM1525 outputs the power PWM signal to the LC filter to generate the desired DC voltage.

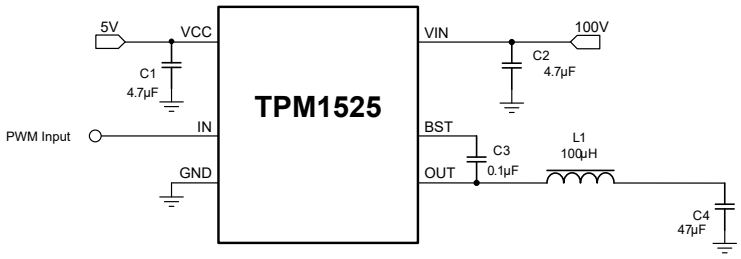


Figure 9. Power Stage of the 100-V Synchronous Buck Converter

Layout

Layout Guideline

Since the TPM1525 can work with up to 150-V high-supply voltage connecting to the VIN pin, cares must be taken to have enough separating space between the low-voltage PCB wires and the high-voltage PCB wires. Place the decoupling capacitor as close to the VIN pin as possible to minimize the parasitic inductance from the decoupling capacitor to the OUT pin. When working with a pure capacitive load, the high-voltage slew rate at the OUT pin may generate voltage overshoot and undershoot at the load because of the parasitic inductance from the OUT pin to the load. In this situation, a resistor may be added in the path to minimize the voltage overshoot and undershoot as shown in the Figure 8.

Layout Example

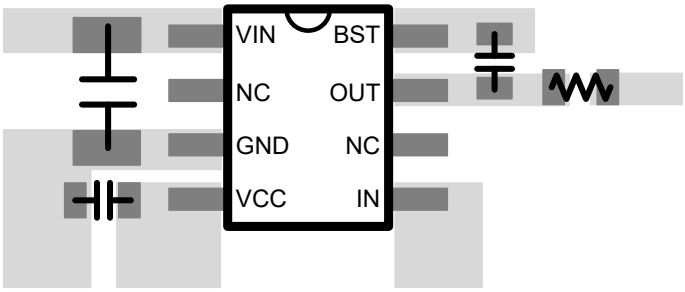
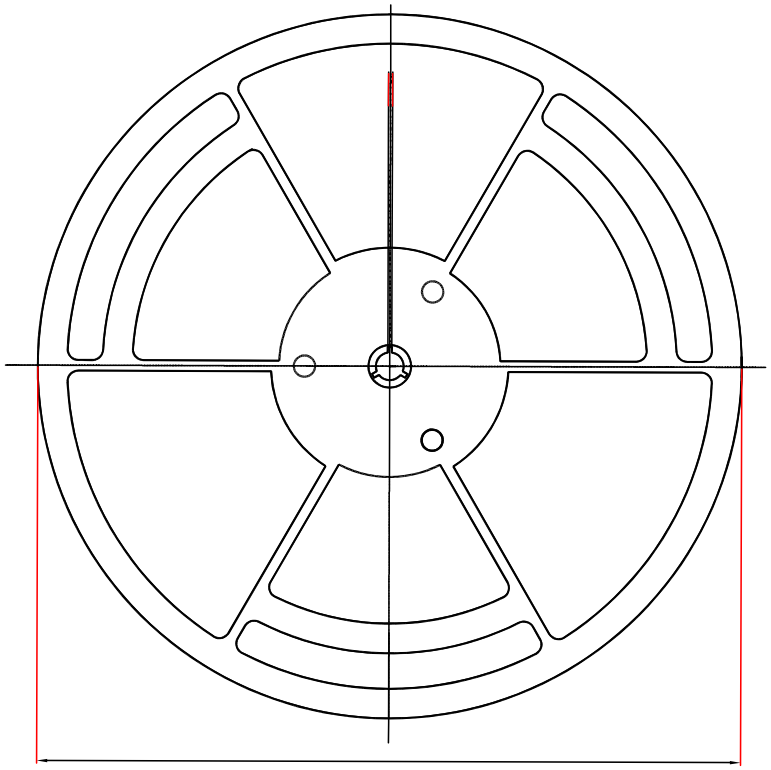
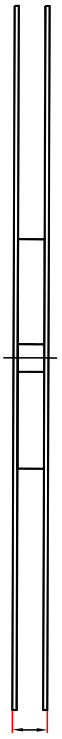
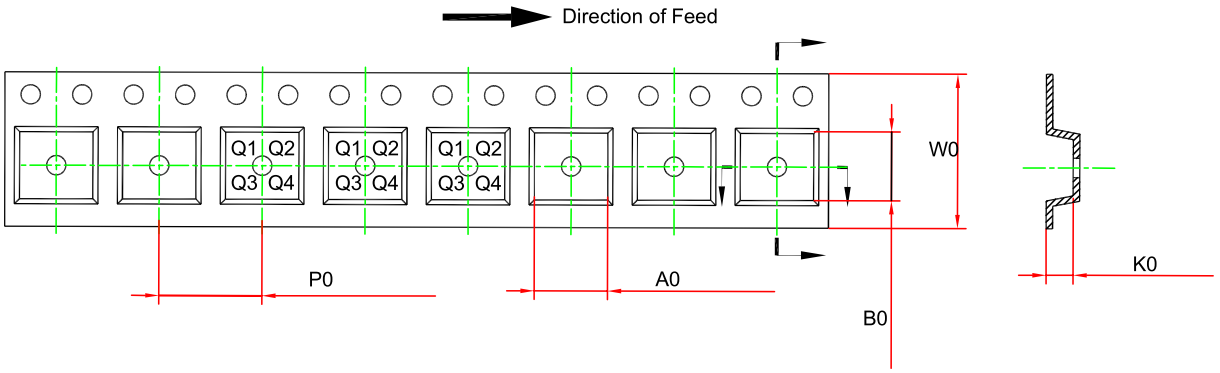


Figure 10. PCB Layout Example

Tape and Reel Information





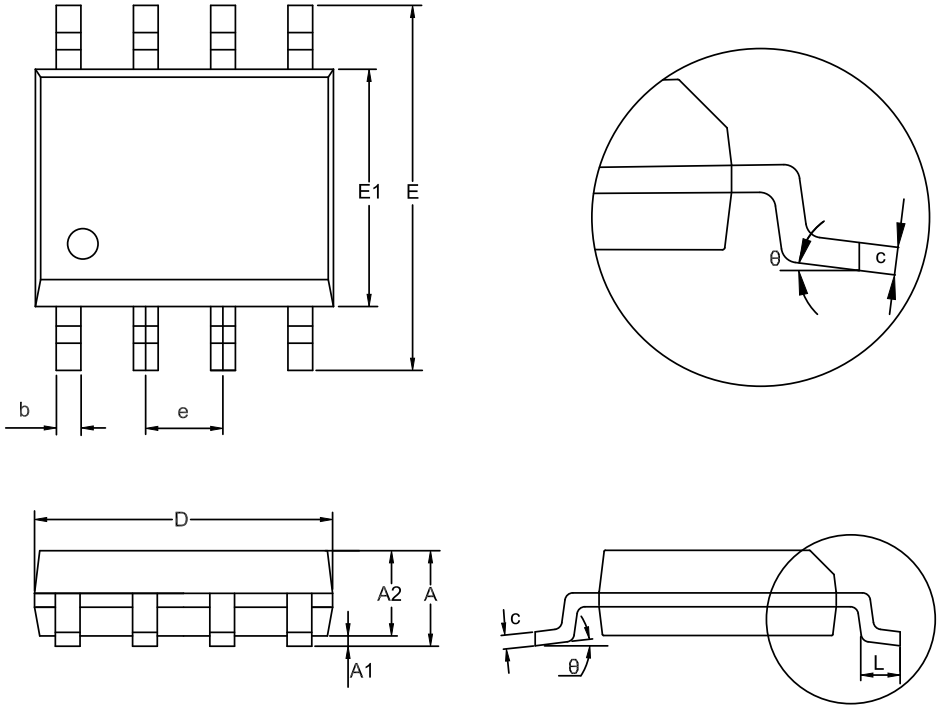


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM1525-SO1R-S	SOP8	330	17.6	6.4	5.4	2.1	8	12	Q1

Package Outline Dimensions

SOP8

Package Outline Dimensions SO1(SOP-8-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.550	0.049	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.000	0.016	0.039
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Ambient Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPM1525-SO1R-S	−40ºC to 125ºC	SOP8	M1525	3	Tape & Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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