Automotive Single-Channel Ultra-High-Speed GaN Predriver

Features

- AEC-Q100 Grade-1 Qualified (TPM1025Q Only)
- 5-V Single Supply with Optimized Output Damping for GaN Reliability
- 7-A Peak Source and 5-A Sink-Drive Current
- 1-ns Minimum Input Pulse Width (Typical)
- Support 60-MHz Operating Frequency
- Low Propagation Delay
- Optimized Pinout for Nanosecond-pulse-width
- Fast Rise-and-Fall Times
- ESD Protection Exceeds JESD 22 – 2-kV HBM, 1-kV CDM
- Available in DFN2×2-6 and WLCSP Packages

Applications

- Laser Distance Measuring System
- Automotive Lidar
- Driver Monitoring System
- GaN DC/DC Conversion System

Description

The TPM1020/TPM1025/TPM1025Q is a family of low-side single-channel and ultra-high-speed gate drivers for GaN and logic-level MOSFETs. It is optimized for high-speed applications such as Lidar and high-density power converters with enhanced low propagation delay design. The 0.85-mm × 1.25-mm WLCSP package of the TPM1020 and the 2-mm × 2-mm DFN package of the TPM1025 minimize parasitic inductance in the gate driver power loop.

Typical Application Circuit

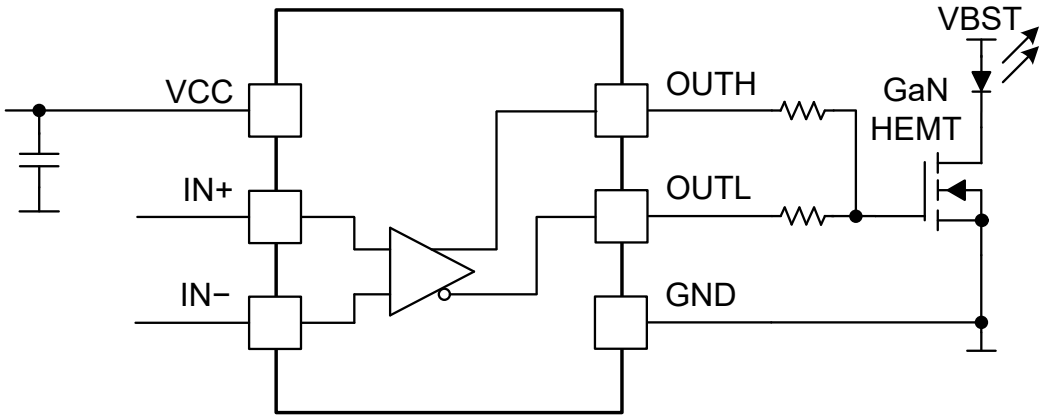


Table of Contents

Product Family Table

Order Number	Quality Grade	Package
TPM1020-WLPR	Industrial	WLCSP 0.85*1.25
TPM1025-DFOR	Industrial	DFN2X2-6
TPM1025Q-DFOR-S	Automotive	DFN2X2-6

Revision History

Date	Revision	Notes
2025-07-20	Rev.A.0	Initial release

Pin Configuration and Functions

DFN2X2-6
Top View

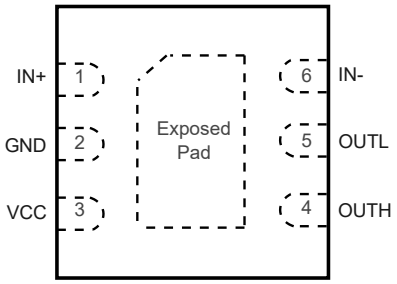


Table 1. Pin Functions: TPM1025

Pin No.	Pin Name	I/O	Description
1	IN+	I	Channel Positive Logic Input, Active High
2	GND	Ground	Device Ground
3	VCC	Supply	Device Supply
4	OUTH	O	Channel Pull-up Output
5	OUTL	O	Channel Pull-down Output
6	IN−	I	Channel Negative Logic Input, Active High
Exposed Pad	EP	G	Exposed Pad. Recommend to connect to GND.

WLCSP
Top View

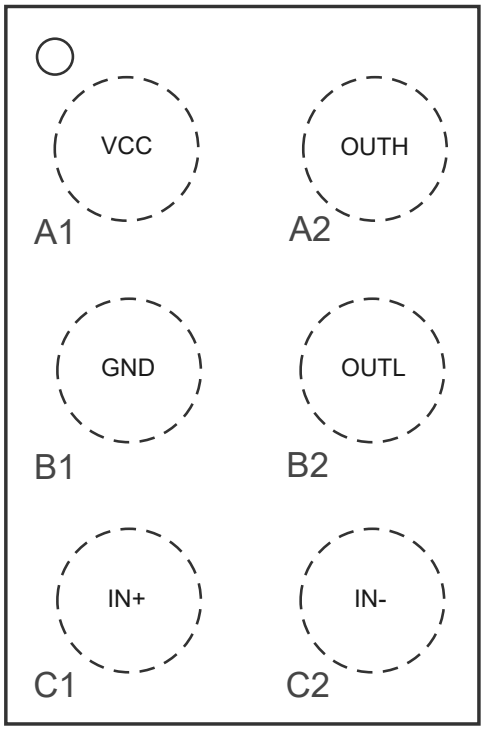


Table 2. Pin Functions: TPM1020

Pin No	Pin Name	I/O	Description
C1	IN+	I	Channel Positive Logic Input, Active High
B1	GND	Ground	Device Ground
A1	VCC	Supply	Device Supply
A2	OUTH	O	Channel Pull-up Output
B2	OUTL	O	Channel Pull-down Output
C2	IN−	I	Channel Negative Logic Input, Active High

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
VCC	Power Supply Voltage, VCC	−0.3	+6	V
V_{OUTx}	Output Voltage Range OUTH, OUTL	−0.3	VCC + 0.3	V
	Output Voltage Range OUTH, OUTL, 5-ns Transient	−5	VCC + 5	V
	Output Voltage Range OUTH, OUTL, 10-ns Transient	−2	VCC + 2	V
V_{INx}	Input Voltage Range IN+, IN−	−0.3	6	V
I_{OUTx}	Continuous Output Channel Current OUTH	−500	+500	mA
	Pulsed Output Channel Sourcing Current OUTH (500 ns)		7	A
	Pulsed Output Channel Sinking Current OUTL (500 ns)		5	A
T_J	Operating Junction Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 300 mV beyond the power supply, the input current should be limited to less than 10 mA.
(3) Power dissipation and thermal limits must be observed.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001，per AEC Q100-002	±2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002, per AEC Q100-011	±1	kV

Recommended Operating Conditions

Parameter		Min	Max	Unit
VCC	Power Supply Voltage, VCC	4.75	5.25	V
V_{INx}	Input Voltage IN+, IN−	0	VCC	V
V_{OUTx}	Output Voltage VOUTH, VOUTL	0	VCC	V
T_A	Operating Ambient Temperature Range	−40	125	℃

Thermal Information

Package Type	θ_{JA}	θ_{Jb}	θ_{JC}	Unit
DFN2X2-6	51.37	10.7	85.9	°C/W
WLCSP	133	38	1.7	°C/W

Electrical Characteristics

All test conditions: V_{CC} = 5 V, T_J = −40 °C to 150 °C, 1-μF capacitor between V_{CC} and GND, unless otherwise noted.

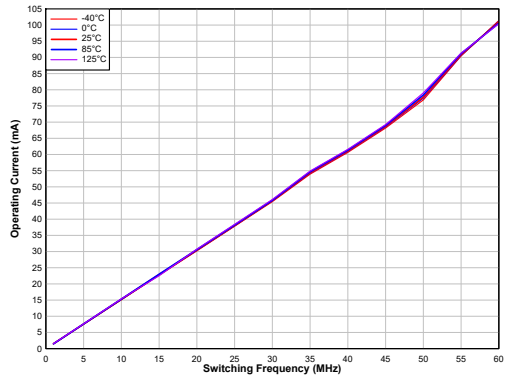
Parameter		Conditions	Min	Typ	Max	Unit
I_Q	VCC Quiescent Current	IN+ = H, IN− = L			100	μA
I_{OP}	VCC Operating Current	f_{SW} = 30 MHz, no load, R_{OUTH} = 2 Ω, R_{OUTL} = 2 Ω		40		mA
		f_{SW} = 30 MHz, 100-pF load, R_{OUTH} = 2 Ω, R_{OUTL} = 2 Ω		51		mA
V_{UVLO_rising}	Supply Under Voltage Lock Out Rising Threshold		3.92		4.35	V
V_{UVLO_hys}	Supply Under Voltage Lock Out Falling Hysteresis			85		mV
T_{OTP}	Over Temperature Shutdown, turn-off			170		°C
ΔT_{OTP}	Over Temperature Hysteresis			20		°C
V_{IN_H}	Input Signal High Threshold	Input high threshold	1.7		2.6	V
V_{IN_L}	Input Signal Low threshold	Input low threshold	1.1		1.8	V
V_{IN_HYS}	Input Hysteresis		0.38		1	V
$R_{IN+\_pulldown}$	IN+ Pull-down Resistance		100	150	250	kΩ
R_{IN-_pullup}	IN− Pull-up Resistance		100	150	250	kΩ
C_{IN}	Input Capacitance			1.45		pF
V_{OL}	Output Low Voltage. OUTxL	I_{OUTL} = 100 mA, IN+ = 0 V, IN− = 5 V			45	mV
V_{CCx} – V_{OHx}	Output High Voltage, OUTxH	I_{OUTH} = 100 mA, IN+ = 5 V, IN− = 0 V			52	mV
I_{OH}	Output Peak Sourcing Current	V_{OUTH} = 0 V, IN+ = 5 V, IN− = 0V		7		A
I_{OL}	Output Peak Sinking Current	V_{OUTL} = 5 V, IN+ = 0 V, IN− = 5V		5		A
T_{start}	Startup Time, VDD Rising above UVLO	IN+ = VDD, IN− = 0 V, VDD rising above UVLO to OUTH rising		40	78	μs
$T_{shut-off}$	ULVO Falling	IN+ = VDD, IN− = 0V, VDD falling below UVLO V to OUTH falling	0.7	2.5	3.5	μs
$T_{pd,\ r}$ (1)	Propagation Delay, Turn on	IN+ to OUTH, IN− = 0 V, 100-pF load	1.5	2.6	4.1	ns
$T_{pd,\ f}$ (1)	Propagation Delay, Turn off	IN+ to OUTL, IN− = 0 V, 100-pF load	1.8	2.9	4.4	ns
Δt_{pd}	Pulse Positive Distortion, ($t_{pd,\ f}$-$t_{pd,\ r}$)			300	610	ps
t_R	Output Rise-time	0-Ω series 220-pF load		650		ps

Parameter		Conditions	Min	Typ	Max	Unit
t_F	Output Fall-time	0-Ω series 220-pF load		850		ps
t_{PW}	Minimum Input Pulse Width That Changes Output State	0-Ω series 220-pF load		1.25		ns

(1) Guranteed by design.

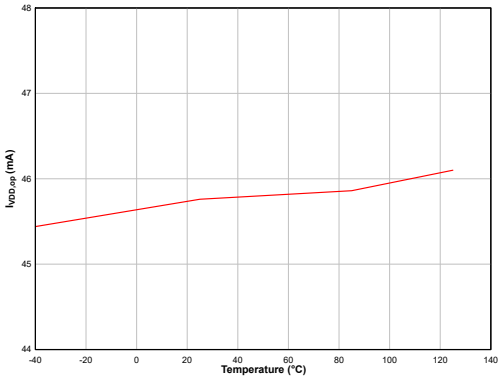
Typical Performance Characteristics

All test conditions: V_{OUT} = 5 V, T_A = +25°C, unless otherwise noted.



2 Ω in series with 100-pF Load

Figure 1. Operating Current vs. Temperature



2 Ω in series with 100-pF Load, frequency = 30 MHz

Figure 2. Operating Current vs. Temperature

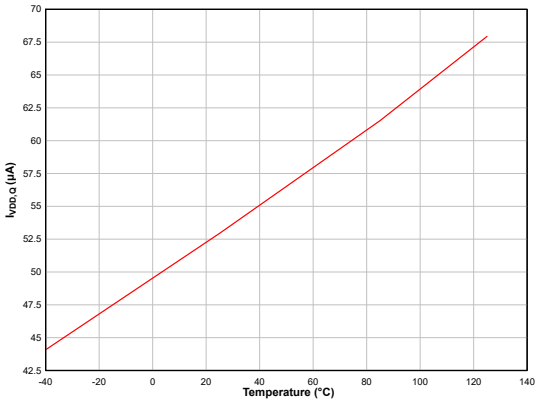
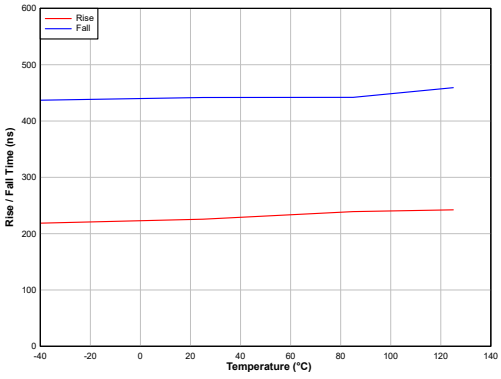
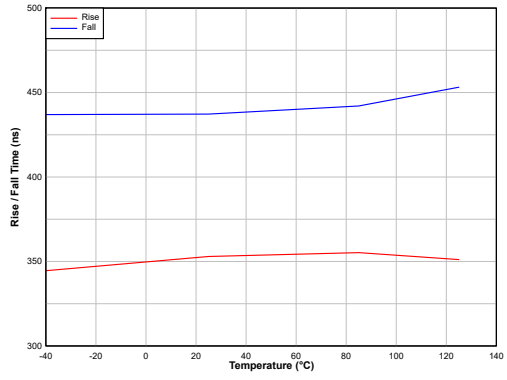


Figure 3. Quiescent current vs. Temperature



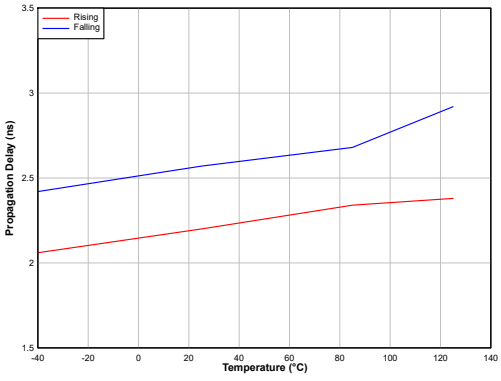
load = 220 pF

Figure 4. Rise & Fall time vs. Temperature



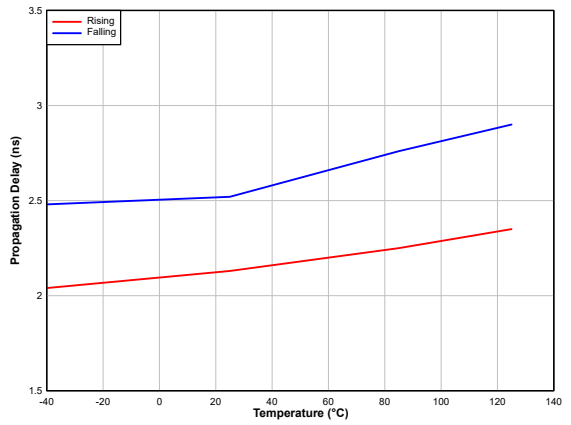
load = 1.8 nC

Figure 5. Rise & Fall time vs. Temperature



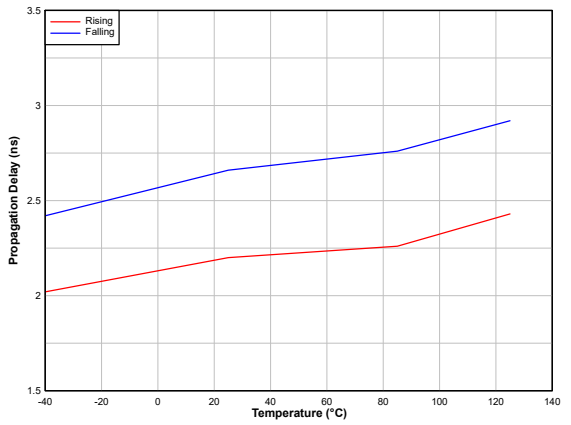
load = 100 nF

Figure 6. Propagation Delay vs. Temperature



load = 220 nF

Figure 7. Propagation Delay vs. Temperature



load = 1.8 pC

Figure 8. Propagation Delay vs. Temperature

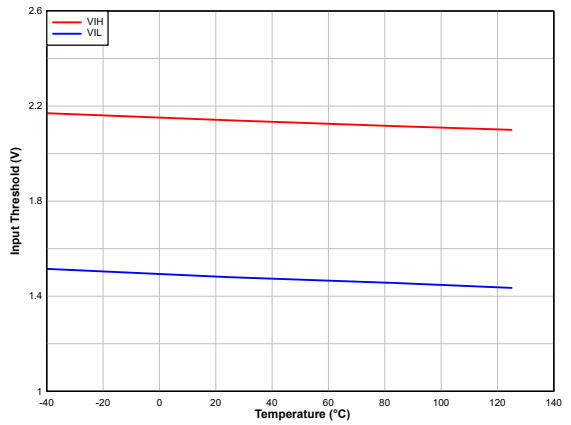


Figure 9. Input Threshold vs. Temperature

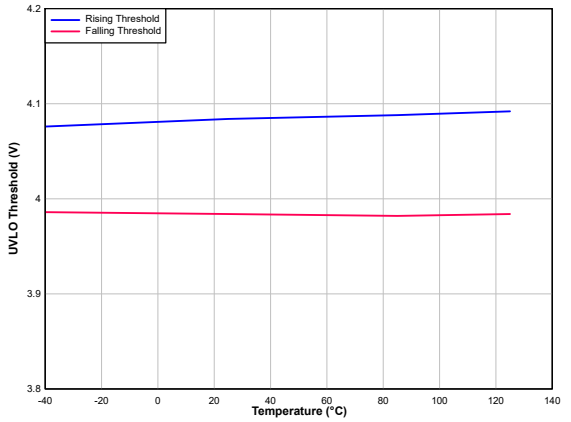
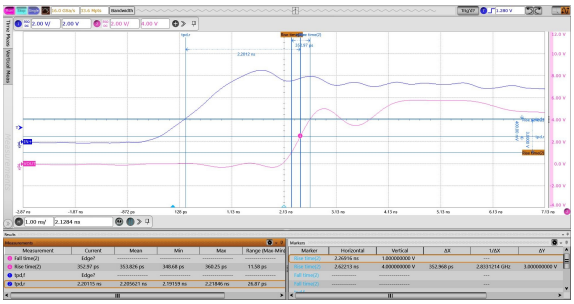
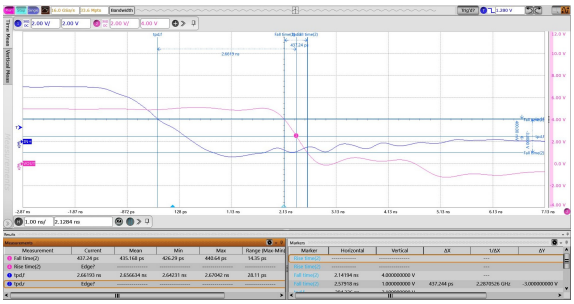


Figure 10. UVLO Threshold vs. Temperature



CH1: Input; CH2: GaN Transistor Gate

Figure 11. Rising Edge



CH1: Input; CH2: GaN Transistor Gate

Figure 12. Falling Edge

Detailed Description

Overview

The TPM1020/TPM1025/TPM1025Q is a family of low-side dual-channel and ultra-high-speed gate drivers for GaN and logic-level MOSFETs. It is optimized for high-speed applications such as Lidar and high-density power convertors with an enhanced low propagation delay design. The DFN2×2-6 package of the TPM1025 and the WLCSP package of the TPM1020 minimize parasitic inductance in the gate driver power loop and achieve state-of-the-art narrow pulse width.

Functional Block Diagram

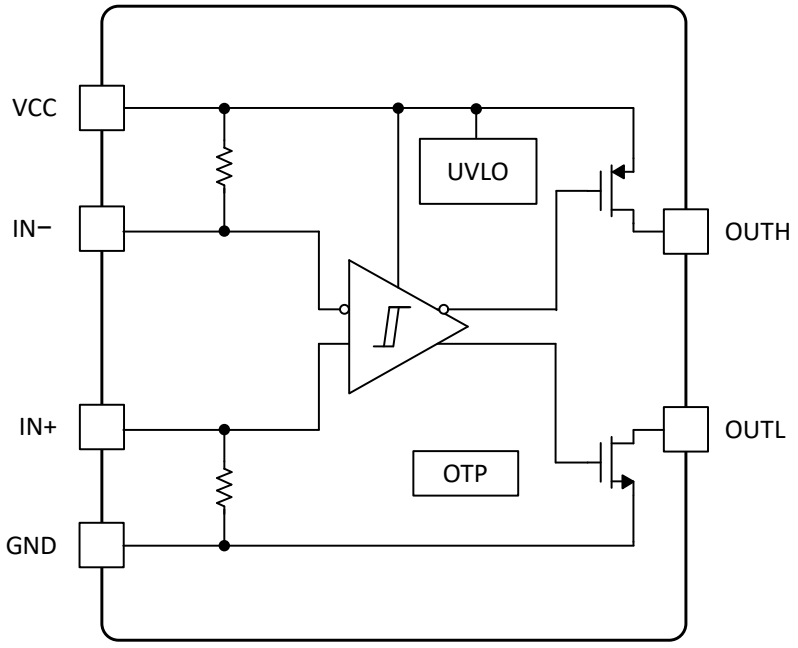


Figure 13. Functional Block Diagram

Feature Description

Supply and Under-Voltage-Lock-Out (UVLO)

The device has supply voltage under-voltage-lock-out (UVLO) monitors. When the supply voltage is above its rising threshold, the outputs are functional. When the supply voltage is below its falling threshold, the device pulls OUTL to GND. A short deglitch timer is inserted to avoid oscillations on the power supply.

Due to ultra-fast turn-on speed, channel output may drain high current on supply nodes within nanoseconds. 3PEAK recommends placing 3-terminal capacitors close to the device supply pins as low as possible. Parasitic inductance may prevent external capacitors from supplying current in such a short time.

Channel Input and Output

The channel inputs are connected to a low-latency Schmitt trigger. It can cut propagation delay without additional gates. The inputs are pulled low via internal resistors.

The TPM1025x provides split pull-up and pull-down paths. The split outputs allow users to independently configure pull-up and pull-down slew-rate via external resistors. The maximum output sink/source current is +7 A / −5 A. Configuring slew rates

may reduce ringing on GaN gate node due to parasitic inductance/capacitance, thus it can improve the reliability of GaN transistors.

Table 3. Output Truth Table

IN+	IN−	OUTH	OUTL
H	L	H	High-Impedance
L	H	High-Impedance	L
Floating (Internal Pull Down) or L	X	High-Impedance	L
X	Floating (Internal Pull Up) or H	High-Impedance	L

Over-Temperature Protection (OTP)

The TPM1025x provides an independent over-temperature protection function to independently disable each channel. When the junction temperature rises above the rising threshold, the channel outputs are disabled; when the junction temperature falls below the falling threshold, the channel outputs are enabled.

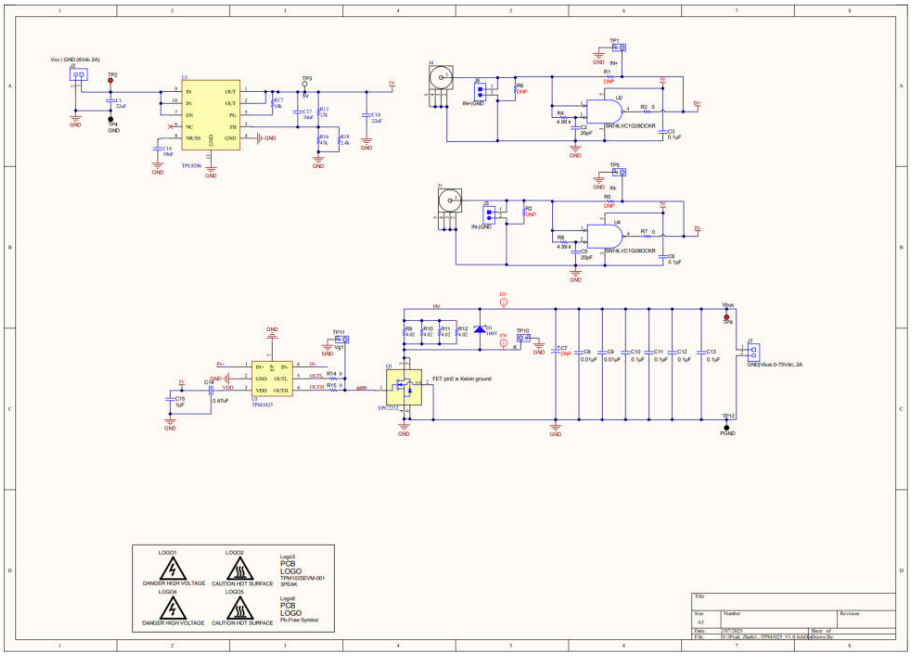
Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

In a modern Time-of-Flight (ToF) LiDAR system, it is necessary to ensure a narrow laser pulse. Gallium nitride (GaN) transistors are widely used in the industry due to their high switching frequency. As depicted in the schematic below, it is required to keep the gate driver output loop as small as possible to minimize parasitic inductance.

Typical Application



Designator	Value	Description	Package	MFR	Part No.	Quantity
U5	TPM1025	Low Side GaN and MOSFET Driver	WSON-6	3PEAK	TPM1025-DFOR	1
C1, C18	22uF	22uF/10V, 0805	0805	Murata	GRM21BR61A226ME51L	2
C2, C5	20 pF	CAP, CERM, 20 pF, 50 V, +/- 5%, C0G/NP0, 0402	0402	Murata	GRM1555C1H200JA01D	2

Designator	Value	Description	Package	MFR	Part No.	Quantity
C3, C6	0.1uF	CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0603	0603	Murata	GRM188R71E104KA01D	2
C7	4.7 µF	CAP, AL, 4.7 µF, 100 V, +/-20%, SMD	SMD,D8*L6.2mm	Nichicon	UUX2A4R7MCL1GS	0
C8, C9	0.01 µF	CAP, CERM, 0.01 µF, 100 V, +/- 1%, C0G/NP0, 0805	0805	KEMET	C0805C103F1GACTU	2
C10, C11, C12, C13	0.1 µF	CAP, CERM, 0.1 µF, 100 V, +/- 10%, X7R, 0603	0603	Murata	GRM188R72A104KA35D	4
C14	470nF	CAP, CERM, 0.1 µF, 100 V, +/- 10%, X7R, 0603	0603	Murata	NFM18PC474R0J3	1
C15	LWK107BJ225MV	CAP, CERM, 1 µF, 10 V, +/-20%, X5R, 0306	0306	TAIYO YUDEN	LWK107BJ105MV	1
C16, C17	10nF	CAP, CERM, 10nF, 25 V, +/-5%, X7R, 0603	0603	Murata	GRT1885C1E103JA02D	2
D1	Schottky Diode	Diode, Schottky, 100 V, 2 A, PowerDI123	SOD-123FL	DIODES	DFLS2100-7	1
Q1	GaN	GANFET N-CH, 100V, 18A DIE	SMD	EPC	EPC2212	1
R1, R5	DNP	RES, 10, 5%, 0.063 W, 0402	0402	VISHAY	CRCW040210R0JNED	0
R2, R6	DNP	RES, 50, 1%, 0.1 W, 0603	0603	VISHAY	CRCW060350R0FKEA	0
R3, R7	0	RES, 0, 5%, 0.063 W, 0402	0402	VISHAY	CRCW04020000Z0ED	2
R4, R8	4.99 k	RES, 4.99 k, 1%, 0.1 W, 0603	0603	VISHAY	CRCW06034K99FKEA	2
R9, R10, R11, R12	4.02	RES, 4.02, 1%, 0.1 W, 0603	0603	VISHAY	CRCW06034R02FKEA	4

Designator	Value	Description	Package	MFR	Part No.	Quantity
R13	12k	RES, 12K, 1%, 0.1 W, 0603	0603	VISHAY	CRCW060312K0FKAEC	1
R14, R15	0	RES, 0, 5%, 0.05 W, 0201	0201	PANASONIC	ERJ-1GE0R00C	2
R16	47k	RES, 47K, 1%, 0.33 W, 0603	0603	VISHAY	CRCW060347K0FKEAHP	1
R17	10k	RES, 10K, 1%, 0.1 W, 0603	0603	VISHAY	CRCW060310K0FKEA	1
R18	2.4k	RES, 2.4K, 1%, 0.1 W, 0603	0603	VISHAY	CRCW06032K40FKEA	1
U1	TPL9208	2A Output, High-PSRR, Low-Noise LDO Regulator	DFNWB2P5*2P5-10	3PEAK	TPL9208AD-DF5R-S	1
U2, U4	SN74LVC1G08DCKR	Single 2-Input Positive-AND Gate	SOT23-5	TI	SN74LVC1G08DCKR	2

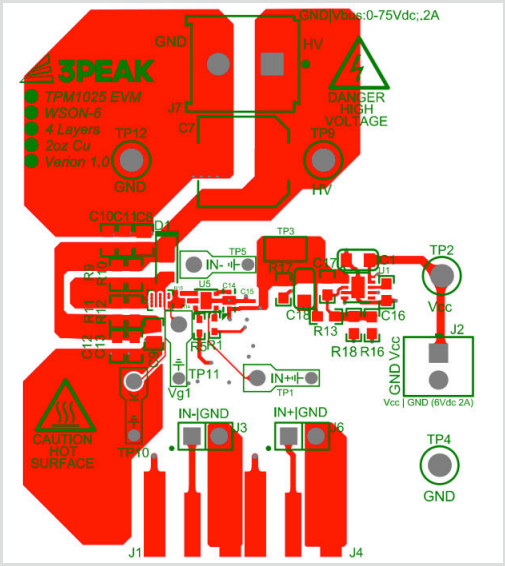
Figure 14.

Layout

Layout Guideline

- Both input capacitors and output capacitors must be placed to the device pins as close as possible.
- It is recommended to bypass the input pin to ground with a 0.1-μF bypass capacitor.
- It is recommended to use wide trace lengths or thick copper weight to minimize I×R drop and heat dissipation.
- Exposed pad must be connected to the PCB ground plane directly, the copper area must be as large as possible.

Layout Example



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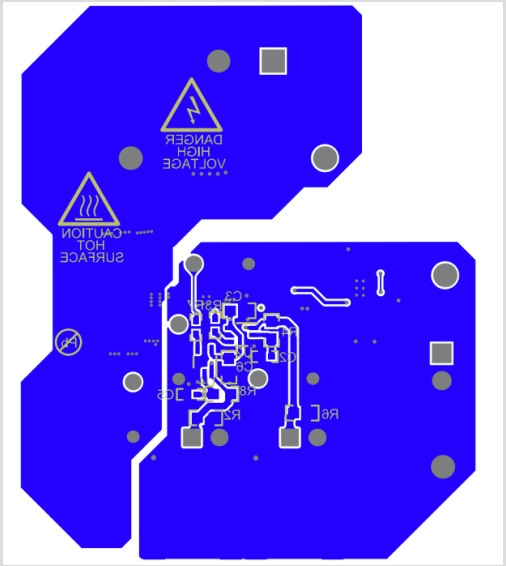
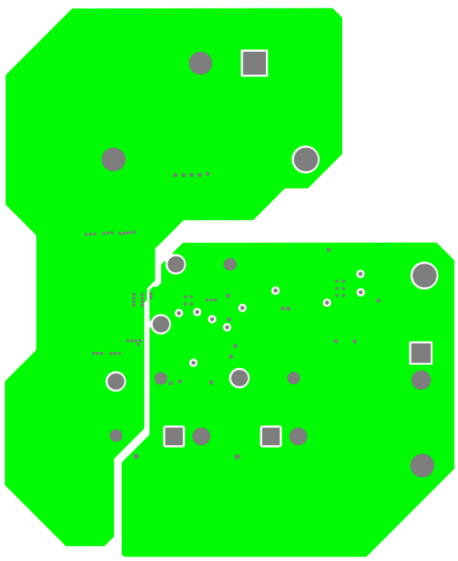
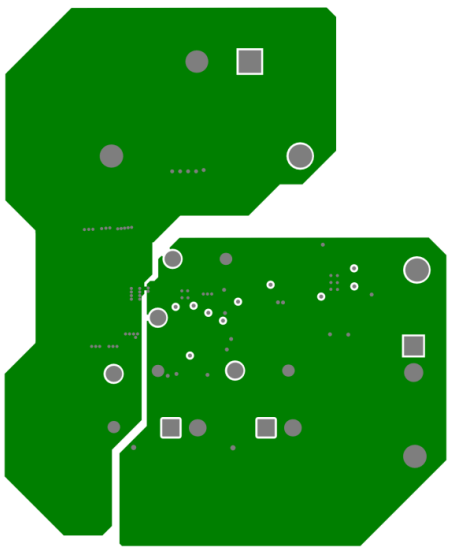


Bottom

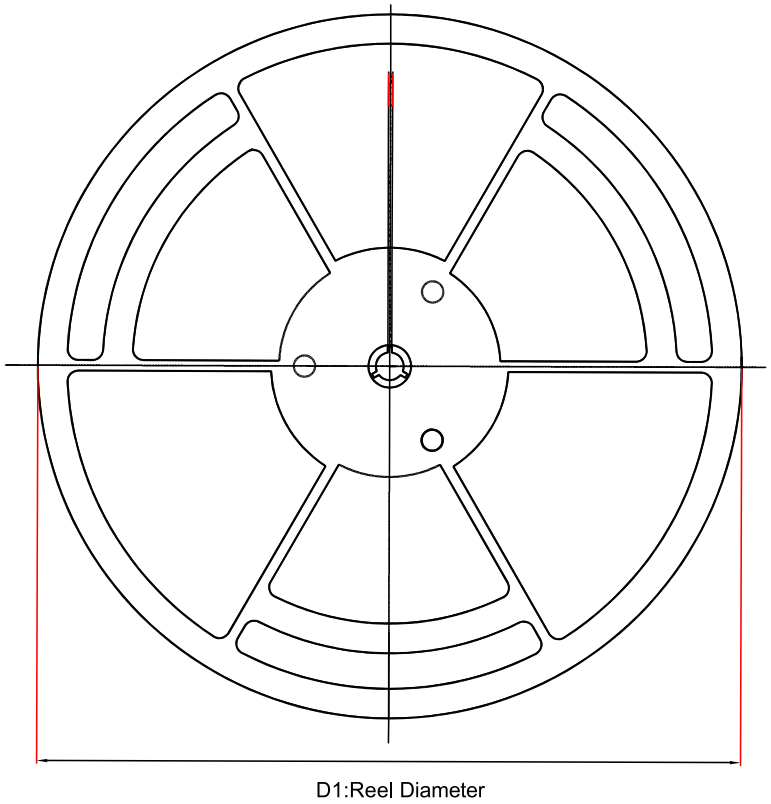


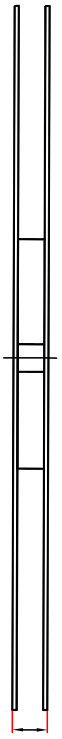
M1

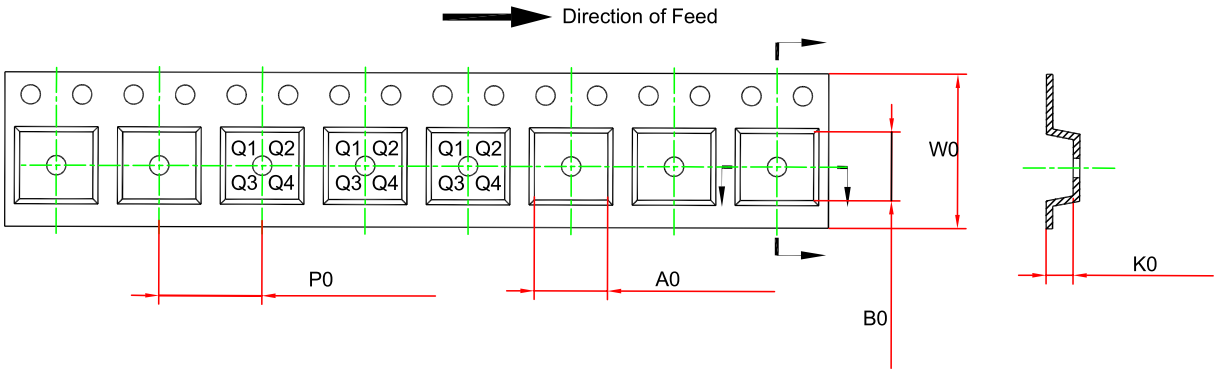


M2

Tape and Reel Information





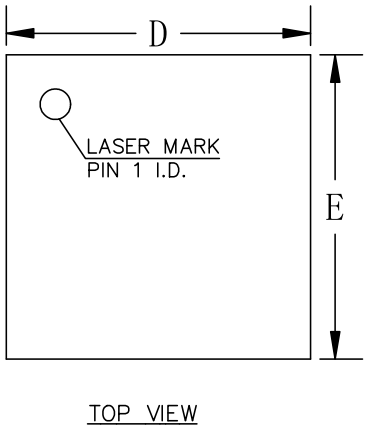


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM1025Q-DFOR-S	DFN2X2-6	180	12.5	2.3	2.3	1.0	4	8	Q1
TPM1025-DFOR	DFN2X2-6	180	12.5	2.3	2.3	1.0	4	8	Q1
TPM1020-WLPR	WLCSP	178	12.5	0.99	3.5	0.69	4	8	Q1

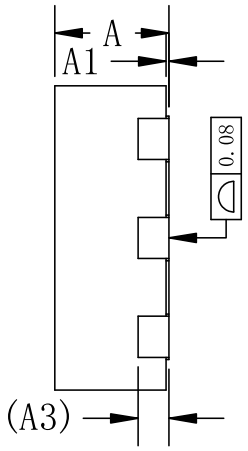
Package Outline Dimensions

DFN2X2-6

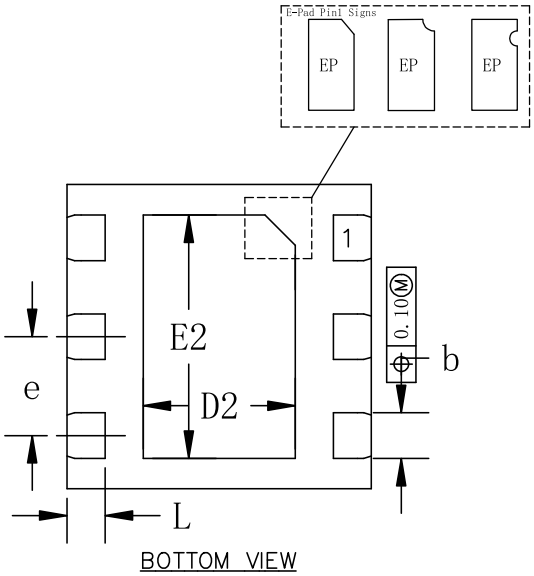
Package Outline Dimensions DFO(DFN2X2-6-A)



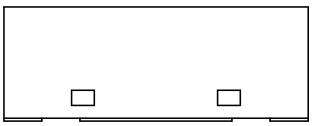
TOP VIEW



SIDE VIEW



BOTTOM VIEW



SIDE VIEW

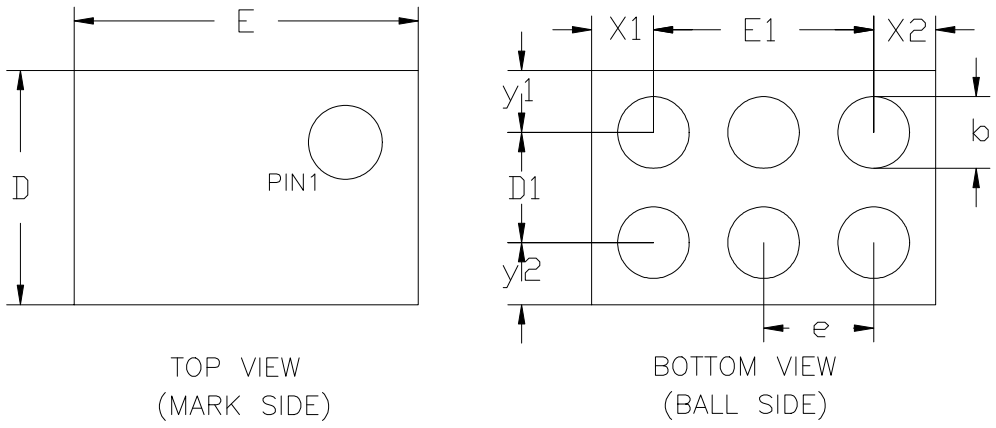
NOTES

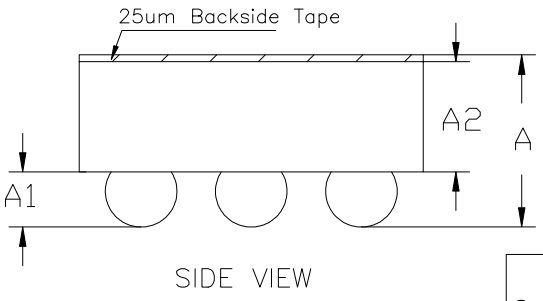
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.250	0.350	0.010	0.014
A3	0.150	0.250	0.006	0.010
D	1.900	2.100	0.075	0.083
E	1.900	2.100	0.075	0.083
D2	0.900	1.100	0.035	0.043
E2	1.500	1.700	0.059	0.067
e	0.650 BSC		0.026 BSC	
L	0.200	0.300	0.008	0.012

WLP 0.85mm×1.25mm

Package Outline Dimensions WLP(WLCSP-A)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.535	0.625	0.021	0.025
A1	0.180	0.220	0.007	0.009
A2	0.330	0.380	0.013	0.015
D	0.820	0.880	0.032	0.035
D1	0.400BSC		0.016	
E	1.220	1.280	0.048	0.050
E1	0.800BSC		0.031	
b	0.240	0.280	0.009	0.011
e	0.400BSC		0.016	
x1	0.225REF		0.009	
x2	0.225REF		0.009	
y1	0.225REF		0.009	
y2	0.225REF		0.009	

NOTES:
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Ambient Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPM1025Q-DFOR-S (1)	–40 °C to 125 °C	DFN2X2-6	Q15	MSL3	3000	Green
TPM1025-DFOR	–40 °C to 125 °C	DFN2X2-6	M15	MSL3	3000	Green
TPM1020-WLPR	–40 °C to 125 °C	WLCSP	2	MSL1	3000	Green

(1) Contact 3PEAK representatives for more information.
(2) The ambient temperature indicates the device operation condition range. Application thermal behavior needs to be taken care of when operating in high temperature scenarios.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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