3-A Output, High-PSRR, Low-Noise LDO Regulator

Features

- Input Voltage Range
  - without BIAS: 1.4 V to 6.5 V
  - with BIAS: 1.1 V to 6.5 V
- Output Voltage Options:
  - Adjustable Output Voltage: 0.5 V to 5.2 V
- ±1% Output Accuracy over Line Regulation, Load Regulation, and Operating Temperature Range with BIAS
- 3-A Maximum Output Current
- Low Dropout Voltage: 300 mV Maximum at 3 A
- High PSRR:
  - 65 dB at 1 kHz
  - 60 dB at 1 MHz
- 4-μV_{RMS} Output Voltage Noise
- Excellent Transient Response
- Enable and Adjustable Soft-Start Control
- Open-Drain Power-Good (PG) Output
- Stable with 10-µF or Greater Ceramic Output Capacitor
- Over-Current Protection
- Over-Temperature Protection
- Package Option:
  - QFN2.2X2.5-12

Applications

- Wireless Communication: CPU, ASIC, FPGA, CPLD, DSP
- High-Performance Analog: ADC, DAC, LVDS, VCO
- Noise-Sensitive Imaging: CMOS Sensors, Video ASICs

Description

The TPL9305FC is a 3-A high-current, 4-μV_{RMS} low-noise, high-PSRR, high-accuracy linear regulator with a typical 120-mV ultra-low dropout voltage at 3-A load condition. The TPL9305FC supports adjustable output voltage ranging from 0.5 V to 5.2 V with an external resistor divider.

Ultra-low noise, high PSRR, and high-output current capabilities make the TPL9305FC an ideal power supply for noise-sensitive applications, such as high-speed communication facilities, test and measurement devices, or high-definition imaging equipment. Accurate output voltage tolerance, output voltage remote sensing, excellent transient response, and adjustable soft-start control ensure the TPL9305FC an optimal power supply for the large-scale processors or digital loads, such as ASIC, FPGA, CPLD, and DSP.

The TPL9305FC provides a small QFN2.2X2.5-12 package with guaranteed operating junction temperature ranging (T_J) from −40°C to +125°C.

Typical Application Circuit

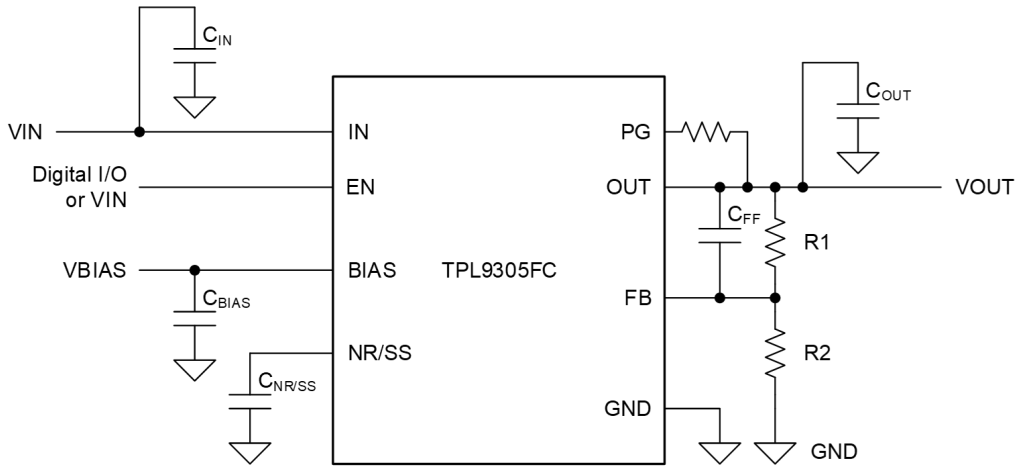


Table of Contents

Product Family Table

Order Number	Output Voltage (V)	Package
TPL9305AD-FC2R-S	Adjustable (0.5 V to 5.2 V)	QFN2.2X2.5-12

Revision History

Revision	Notes
Rev.A.0	Initial release.

Pin Configuration and Functions

TPL9305FC
12-Pin Flip-Chip QFN2.2X2.5 Package
Top View

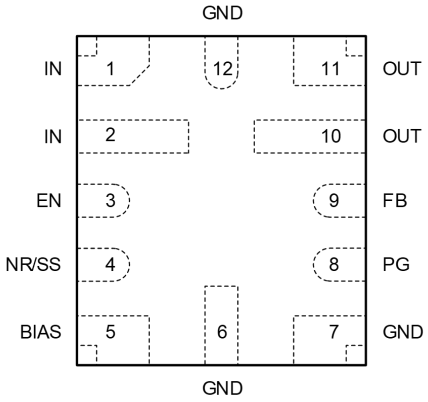


Table 1. Pin Functions: TPL9305FC

Pin No.	Pin Name	I/O	Description
5	BIAS	I	BIAS input pin. A 10-μF capacitor or larger must be connected between this pin and ground. Leave BIAS pin open or tied to ground when not used.
3	EN	I	Regulator enable pin. Drive EN high to turn on the regulator; drive EN low to turn off the regulator.
9	FB	I	Output voltage feedback pin. Connect to an external resistor divider to adjust the output voltage. A 10-nF feed-forward capacitor from FB to OUT (as close as possible to FB pin) is recommended to maximize regulator ac performance.
6, 7, 12	GND	–	Ground reference pin. Connect the GND pin to PCB ground plane directly.
1, 2	IN	I	Input voltage pin. Suggest connecting a 10-μF or larger ceramic capacitor from IN to ground (as close as possible to IN pin) to reduce the jitter from previous-stage power supply.
4	NR/SS	I	Noise-reduction and soft-start pin. A 10-nF or larger capacitor from NR/SS to GND (as close as possible to NR/SS pin) is recommended to maximize ac performance.
10, 11	OUT	O	Regulated output voltage pin. A 10-μF or larger ceramic capacitor from OUT to ground (as close as possible to OUT pin) is required to ensure regulator stability.
8	PG	O	Open-drain power-good output pin. Leave the PG pin open when not used.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
IN, BIAS, EN, PG		−0.3	7	V
OUT		−0.3	V_{IN} + 0.3	V
NR/SS, FB		−0.3	3.6	V
T_J	Maximum Junction Temperature	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
(2) All voltage values are with respect to GND.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
IN	Input Voltage	1.1		6.5	V
BIAS	BIAS Voltage	3		6.5	V
EN	Enable Voltage	0		6.5	V
OUT	Output Voltage	0.5		5.2	V
C_{IN}	Input Capacitor	10			μF
C_{OUT}	Output Capacitor	10	22		μF
C_{FF}	Feed-forward Capacitor		10	1000	nF
$C_{NR/SS}$	NR/SS Capacitor		10		nF
R_{PG}	Power-good Pull-up Resistor	10		100	kΩ
R_1	High-Side Resistor of the Resistor Divider		12.1		kΩ
R_2	Low-Side Resistor of the Resistor Divider			160	kΩ
T_J	Junction Temperature Range	−40		125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
FCQFN2.2X2.5-12	63.9	16.5	29.2	°C/W

Electrical Characteristics

All test conditions: T_J = −40°C to +125°C (typical value at T_J = +25°C), V_{IN} = $V_{OUT\ (NOM)}$ + 0.4 V or 1.4 V, whichever is greater; V_{BIAS} = open, $V_{OUT\ (NOM)}$ = 0.5 V, V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT} = 10 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, OUT connect to 50 Ω to ground, PG connected to 100 kΩ to OUT, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Supply Input Voltage and Current						
V_{IN} (1)	Input Voltage Range		1.1		6.5	V
V_{BIAS}	Bias Voltage Range	V_{IN} = 1.1 V	3		6.5	V
$UVLO_{IN1}$	V_{IN} UVLO with BIAS	V_{IN} rising with V_{BIAS} = 3 V			1.09	V
	Hysteresis	V_{BIAS} = 3 V		200		mV
$UVLO_{IN2}$	V_{IN} UVLO without BIAS	VIN rising			1.39	V
	Hysteresis			200		mV
$UVLO_{BIAS}$	V_{BIAS} UVLO	V_{BIAS} rising, V_{IN} = 1.1 V			2.9	V
	Hysteresis	V_{IN} = 1.1 V		200		mV
I_{GND}	Ground Current	V_{IN} = 6.5 V, I_{OUT} = 5 mA		5	15	mA
		V_{IN} = 1.4 V, I_{OUT} = 3 A		5	15	mA
		V_{IN} = 1.1 V, V_{BIAS} = 3 V, I_{OUT} = 3 A		5	15	mA
I_{SD}	Shutdown Current	V_{IN} = 6.5 V, V_{EN} = 0.4 V, PG = open			68	µA
I_{BIAS}	BIAS Pin Current	V_{IN} = 1.1 V, V_{BIAS} = 6.5 V, I_{OUT} = 3 A		2.5	5	mA
Enable and Power Good						
$V_{IH\ (EN)}$	EN High-Level Input	Device enable	1.1		6.5	V
$V_{IL\ (EN)}$	EN Low-Level Input	Device disable	0		0.4	V
I_{EN}	EN Leakage Current	V_{IN} = 6.5 V, V_{EN} = 0 V to 6.5 V	−0.2		0.2	µA
V_{PG}	PG Threshold	V_{OUT} falling		81%		× V_{OUT}
	Hysteresis			2%		× V_{OUT}
$V_{OL(PG)}$	PG Low-Level Output	V_{OUT} < V_{PG}, source 1 mA to PG pin			0.4	V
I_{PG}	PG Leakage Current	V_{OUT} > V_{PG}, apply 6.5 V at PG pin			1	µA

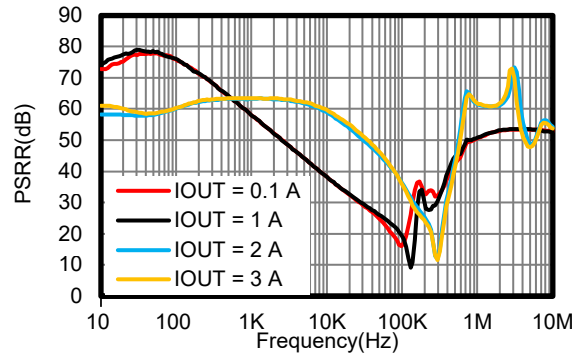
Parameter		Conditions		Min	Typ	Max	Unit
Regulated Output Voltage and Current							
V_{FB}	Feedback Voltage			0.495	0.5	0.505	V
I_{FB}	FB Leakage Current	V_{IN} = 6.5 V, stress V_{FB} = 0.5 V		−100		100	nA
$V_{NR/SS}$	NR/SS Voltage				0.5		V
$I_{NR/SS}$	NR/SS Charging Current	V_{IN} = 6.5 V, $V_{NR/SS}$ = GND		6	7.8	9	μA
	Accuracy (2)(3)	VIN = 1.4 V to 6.5 V, VOUT = 0.5 V to 5.2 V, IOUT = 5 mA to 3 A		0.5		5.2	V
		V_{IN} = 1.1 V, V_{BIAS} = 3 V to 6.5 V, V_{OUT} = 0.5 V to 5.2 V, I_{OUT} = 5 mA to 3 A		−1%		1%	
ΔV_{OUT}	Line Regulation	V_{IN} = 1.4 V to 6.5 V, I_{OUT} = 5 mA			0.03		mV/V
	Load Regulation	V_{IN} = 1.1 V, V_{BIAS} = 3 V to 6.5 V, I_{OUT} = 5 mA to 3 A			0.7		mV/A
		I_{OUT} = 5 mA to 3 A			0.8		mV/A
V_{DO}	Dropout Voltage without BIAS	V_{IN} = 1.4 V, I_{OUT} = 1 A, V_{FB} = 0.5 V – 3%			40	100	mV
		V_{IN} = 1.4 V, I_{OUT} = 2 A, V_{FB} = 0.5 V – 3%			80	200	mV
		V_{IN} = 1.4 V, I_{OUT} = 3 A, V_{FB} = 0.5 V – 3%			120	300	mV
		V_{IN} = 5.6 V, I_{OUT} = 3 A, V_{FB} = 0.5 V – 3%			120	300	mV
	Dropout Voltage with BIAS	V_{IN} = 1.1 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, V_{FB} = 0.5 V – 3%			40	100	mV
		V_{IN} = 1.1 V, V_{BIAS} = 5 V, I_{OUT} = 2 A, V_{FB} = 0.5 V – 3%			80	200	mV
		V_{IN} = 1.1 V, V_{BIAS} = 5 V, I_{OUT} = 3 A, V_{FB} = 0.5 V – 3%			120	300	mV
I_{LIM}	Output Current Limit	V_{OUT} forced at 0.9 × $V_{OUT(NOM)}$		3.7	4.7		A
PSRR and Noise							
PSRR	Power Supply Ripple Rejection	I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 100 nF, C_{OUT} = 47 μF || 10μF || 10μF	f = 1 kHz, V_{BIAS} = 3 V		65		dB
			f = 1 MHz, V_{BIAS} = 3 V		60		dB
			f = 1 kHz		65		dB
			f = 1 MHz		60		dB

Parameter		Conditions	Min	Typ	Max	Unit
PSRR and Noise						
V_N	Output Noise Voltage	BW = 10 Hz to 100 kHz, V_{IN} = 1.1 V, V_{OUT} = 0.5 V, V_{BIAS} = 5 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 10 nF, C_{OUT} = 47 µF || 10µF || 10µF		4		μV_{RMS}
		BW = 10 Hz to 100 kHz, V_{OUT} = 5 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 100 nF, C_{OUT} = 47 µF || 10µF || 10µF		8		μV_{RMS}
		BW = 10 Hz to 100 kHz, V_{OUT} = 5 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 10 nF, C_{OUT} = 47 µF || 10µF || 10µF		10		μV_{RMS}
Temperature Range						
T_{SD}	Thermal Shutdown	Temperature increasing		160		°C
	Hysteresis			20		°C

(1) Minimum V_{IN} = $V_{OUT\ (NOM)}$ + V_{DO} or 1.4 V or 1.1 V with V_{BIAS} = 3 V, whichever is greater.
(2) External resistor tolerances are not included.
(3) Output accuracy is not tested under this condition: V_{IN} > 4.5 V, V_{OUT} = 0.5 V, and I_{OUT} > 750 mA, because the power dissipation is higher than the maximum rating of the package.

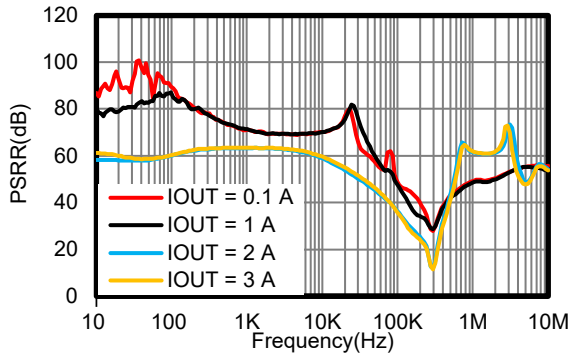
Typical Performance Characteristics

All test conditions: T_J = 25°C, V_{IN} = $V_{OUT\ (NOM)}$ + 0.4 V or 1.4 V, whichever is greater; $V_{OUT\ (NOM)}$ = 0.5 V, V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT} = 10 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, OUT connect to 50 Ω to ground, PG connected to 100 kΩ to OUT, unless otherwise noted.



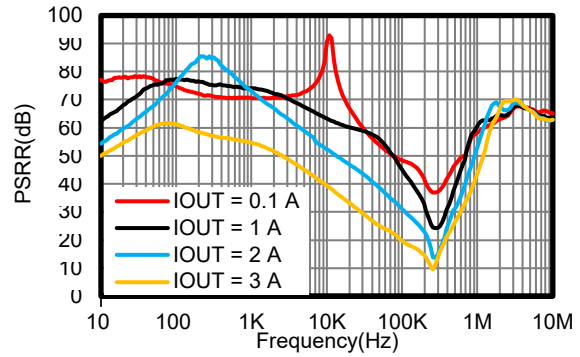
V_{IN} = 1.4 V, V_{OUT} = 0.5 V = 10 nF

Figure 1. PSRR



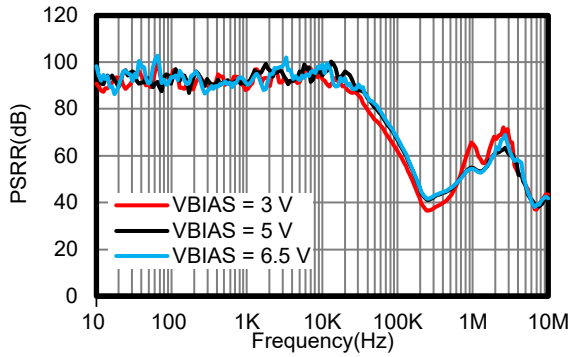
V_{IN} = 1.1 V, V_{BIAS} = 3 V, V_{OUT} = 0.5 V

Figure 2. PSRR



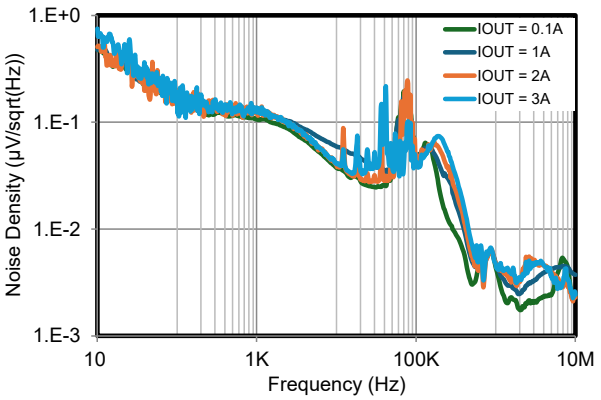
V_{IN} = 5.5 V, V_{OUT} = 5.2 V, without V_{BIAS}

Figure 3. PSRR



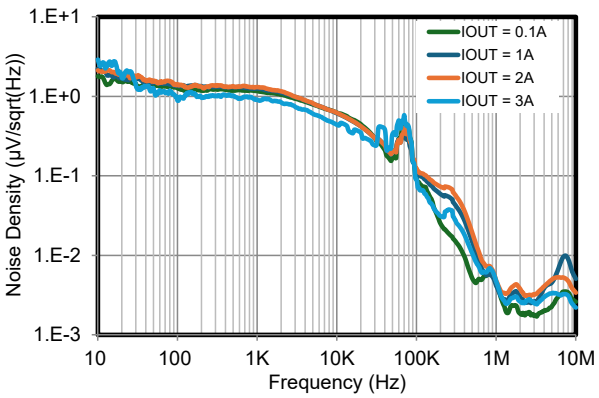
V_{IN} = 1.1 V, V_{OUT} = 0.5 V

Figure 4. V_{BIAS} PSRR



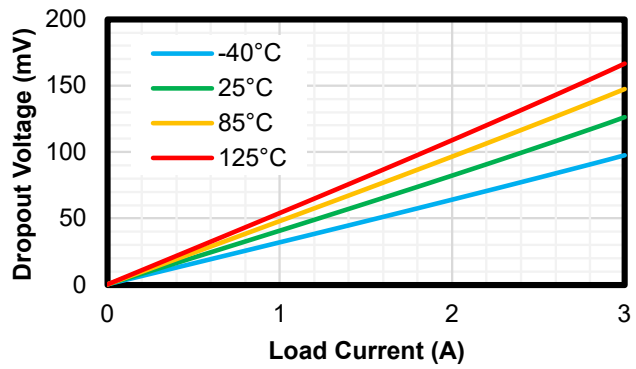
V_{IN} = 1.4 V, V_{OUT} = 0.5 V

Figure 5. Noise



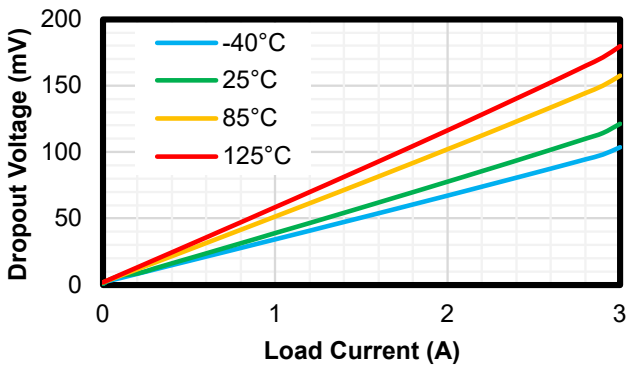
V_{IN} = 5.5 V, V_{OUT} = 5.2 V

Figure 6. Noise



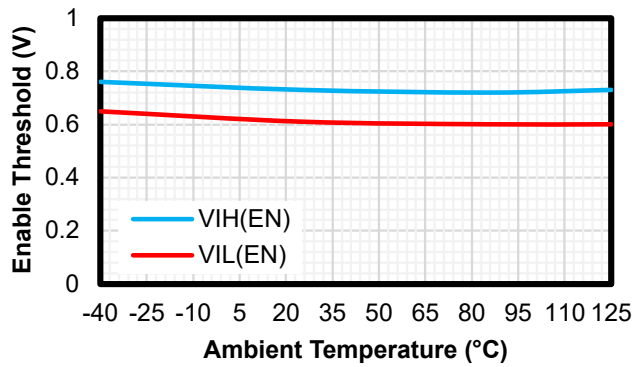
V_{IN} = 1.4 V

Figure 7. Dropout Voltage vs. Output Current



V_{IN} = 5.5 V

Figure 8. Dropout Voltage vs. Output Current



V_{IN} = 1.4 V

Figure 9. EN Threshold vs. Temperature

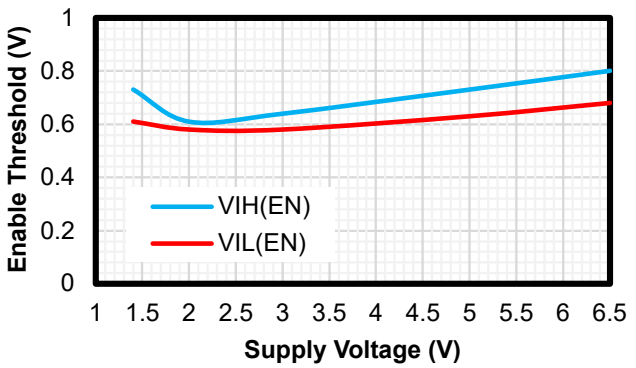
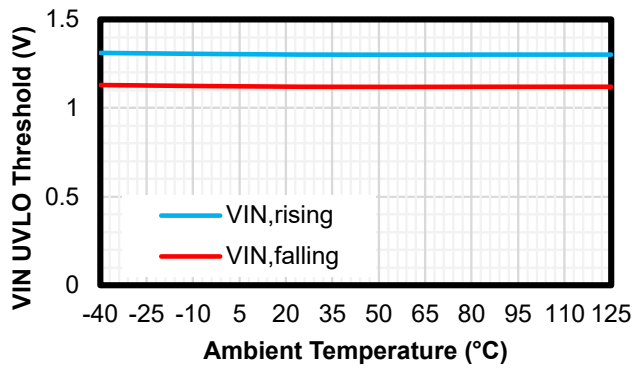
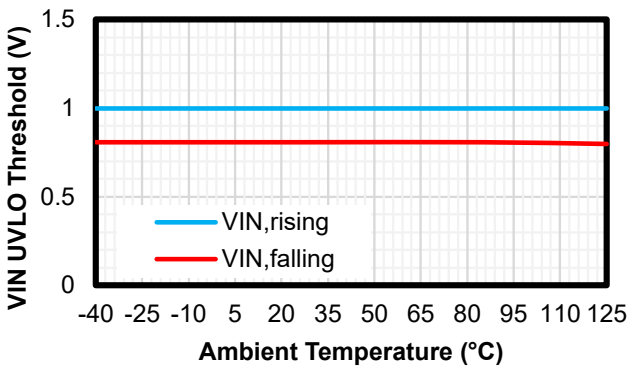


Figure 10. Enable Threshold vs. Input Voltage



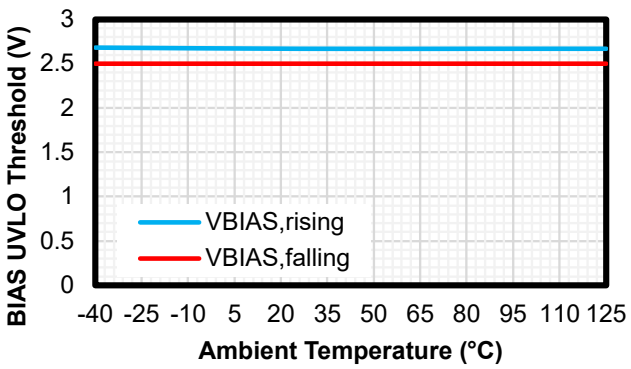
without V_{BIAS}

Figure 11. UVLOIN1 vs. Temperature



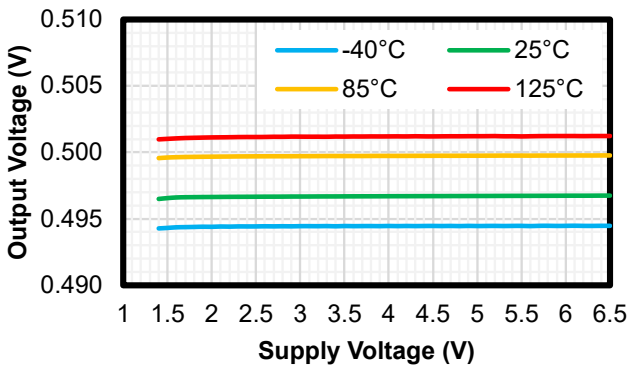
with V_{BIAS} = 3 V

Figure 12. UVLOIN2 vs. Temperature



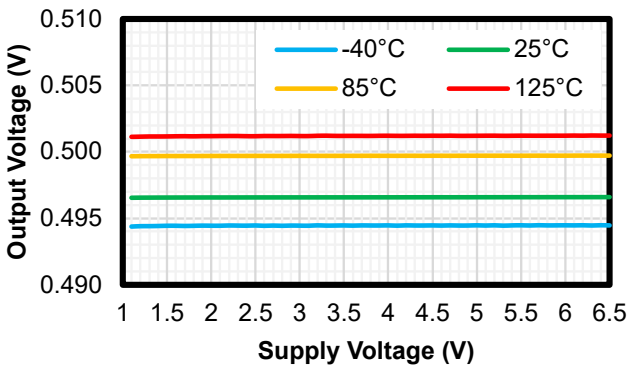
with V_{IN} = 1.1 V

Figure 13. BIAS UVLO vs. Temperature



without V_{BIAS}

Figure 14. Line Regulation



with V_{BIAS} = 3 V

Figure 15. Line Regulation

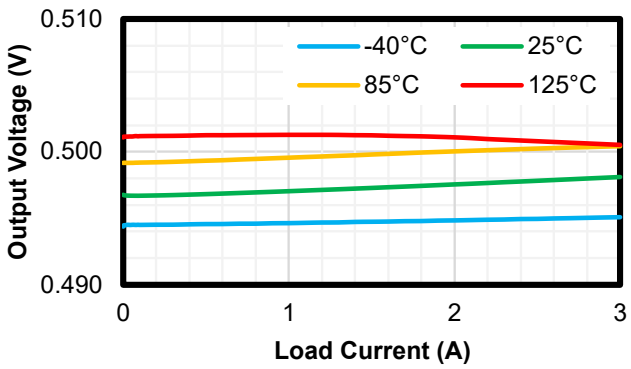
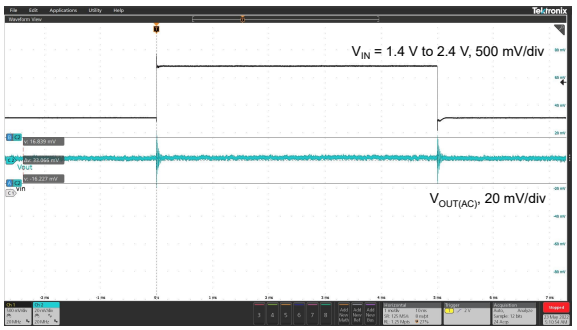
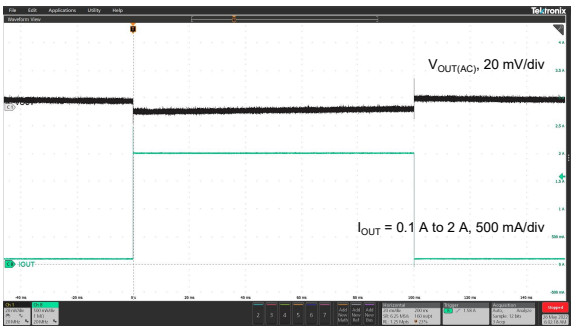


Figure 16. Load Regulation



V_{IN} = 1.4 V to 2.4 V, V_{OUT} = 0.5 V, I_{OUT} = 1 A

Figure 17. Line Transient



V_{IN} = 1.4 V, V_{OUT} = 0.5 V, I_{OUT} = 0.1 A to 2 A

Figure 18. Load Transient

Detailed Description

Overview

The TPL9305FC is a 3-A high-current, 4-μVRMS low-noise, high-PSRR, high-accuracy linear regulator with typically 120-mV ultra-low dropout voltage. The TPL9305FC supports adjustable output voltage ranging from 0.5 V to 5.2 V with an external resistor divider.

Ultra-low noise, high PSRR, and high output current capabilities make the TPL9305FC an ideal power supply for noise-sensitive applications, such as high-speed communication facilities, test and measurement devices, or high-definition imaging equipment. Accurate output voltage tolerance, output voltage remote sensing, excellent transient response, and adjustable soft-start control ensure the TPL9305FC series products optimal power supply for large-scale processors or digital loads, such as ASIC, FPGA, CPLD, and DSP.

Functional Block Diagram

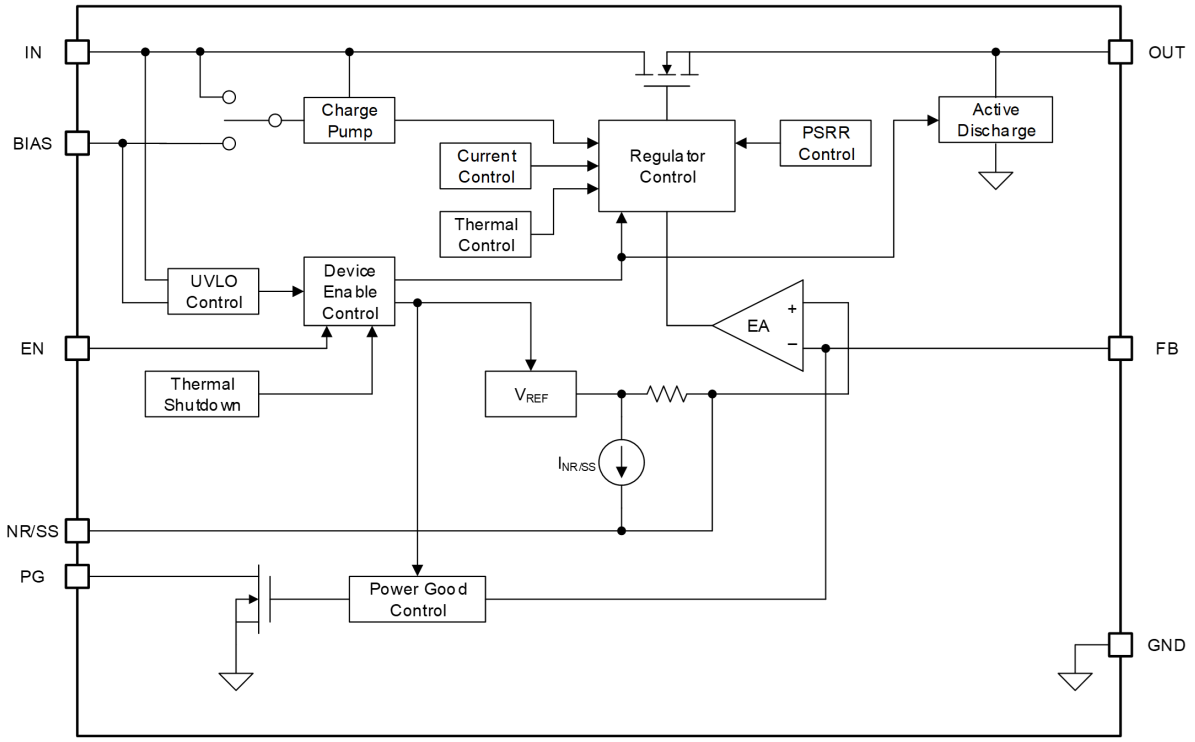


Figure 19. Functional Block Diagram

Feature Description

Enable (EN)

The TPL9305FC provides a device enable pin (EN) to enable or disable the device. Connect this pin to the GPIO of an external digital logic control circuit to control the device. When the VEN voltage falls below $V_{IL\ (EN)}$, the LDO device turns off, and when the VEN ramps above $V_{IH\ (EN)}$, the LDO device turns on.

Under-Voltage Lockout (UVLO)

The TPL9305FC uses an under-voltage lockout circuit to keep the output shut-off until the internal circuitry operates properly.

Adjustable Output Voltage

Using an external resistor divider, the output voltage of TPL9305FC is determined by the value of the resistor R1 and R2 in Figure 20. Use the Equation 1 to calculate the output voltage.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Where,

- the feedback voltage V_{FB} is 0.5 V
- R1 is the high-side feedback resistor
- R2 is the low-side feedback resistor

Output Soft-Start Control (NR/SS)

The TPL9305FC integrates a programmable soft-start function to control the output voltage ramp-up slew rate and start-up time. By selecting the external capacitor at the NR/SS pin ($C_{NR/SS}$), the output start-up time can be calculated with Equation 2.

$$t_{STRATUP} = 1.25 \times \frac{V_{NR/SS} \times C_{NR/SS}}{I_{NR/SS}} \quad (2)$$

Where,

- the typical value of $V_{NR/SS}$ is 0.5 V
- the typical value of $I_{NR/SS}$ is 7.8 μA
- $C_{NR/SS}$ is the external capacitor at the NR/SS pin

Charge Pump Noise

The TPL9305FC integrates a charge pump to improve the PSRR and transient response under low input voltage conditions. The charge pump circuit generates a minimal amount of noise at the frequency of around 15 MHz. It is recommended to use 10-nF to 100-nF bypass capacitors close to the load a ferrite bead between the LDO output and the load input capacitors, forming a pi-filter to reduce the high-frequency noise level.

Power Good (PG)

The TPL9305FC integrates an open-drain output power good indicator. Connect the PG pin to a pull-up voltage through a resistor from 10 kΩ to 100 kΩ if the power good function is used. Leave the PG pin open if it is not used.

After regulator startup, the PG pin keeps low impendence until the output voltage reaches the power good threshold $V_{PG, TH}$. When the output voltage is higher than $V_{PG, TH}$, the PG pin turns to high output impedance, and PG is pulled up to a high voltage level to indicate the output voltage is ready.

Output Active Discharge

The TPL9305FC integrates an output discharge path from OUT to GND. When the device is disabled, the output actively discharges the output voltage through an internal resistor of several hundred ohms.

Do not rely on this active discharge circuit for discharging large output capacitors when the input voltage falls below the output voltage. Reverse current flow through internal power MOSFET can permanently damage the device, and external current protection is essential at this condition.

Over-Current Protection and Short-to-Ground Protection

The TPL9305FC series integrates an internal current limit that helps to protect the device during fault conditions. When the output is pulled down below the target output voltage, over-current protection starts to work and limits the output current to a typical value of 4.7 A.

Under over-current conditions, the internal junction temperature ramps up quickly. When the junction temperature is high enough, it will cause over-temperature protection.

Over-Temperature Protection

The recommended operating junction temperature range is from −40°C to 125°C. When the junction temperature is between 125°C and the thermal shutdown (T_{SD}) threshold, the regulator can still work well, but reduces the lifetime of the device for long-term use.

The over-temperature protection works when the junction temperature exceeds the thermal shutdown (T_{SD}) threshold, which turns off the regulator immediately. When the device cools down and the junction temperature falls below the value, which equals to thermal shutdown threshold minus thermal shutdown hysteresis, the regulator turns on again.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPL9305FC is a 3-A high-current, low-noise, high-PSRR, high-accuracy linear regulator with a typical 120-mV ultra-low dropout voltage at 3-A load condition. The following application schematic shows the typical usage of the TPL9305FC.

Typical Application

Figure 20 shows a typical application schematic of the TPL9305FC.

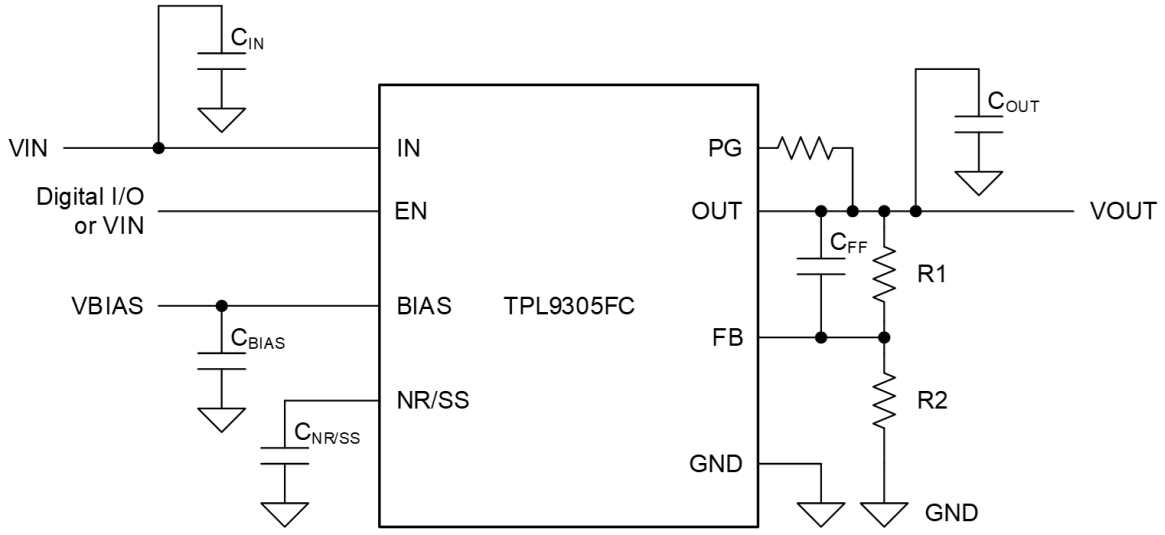


Figure 20. Typical Application Circuit

Input Capacitor and Output Capacitor

The TPL9305FC is designed to be stable with low equivalent series resistance (ESR) ceramic capacitors at the input, output, and noise-reduction pin (NR/SS). It is recommended to use ceramic capacitors with X7R-, X5R-, and COG-rated dielectric materials to get good capacitive stability across temperature ranges.

3PEAK recommends adding a 10-µF or greater capacitor with a 0.1-µF bypass capacitor in parallel at the IN pin to keep the input voltage stable. The voltage rating of the capacitors must be greater than the maximum input voltage.

To ensure loop stability, the TPL9305FC requires an output capacitor with a minimum effective capacitance value of 10 µF. 3PEAK recommends selecting an X7R-type 22-µF ceramic capacitor with low ESR over temperature.

Both input capacitors and output capacitors must be placed as close to the device pins as possible.

Power Dissipation

During normal operation, the LDO junction temperature should not exceed 125°C. Use below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using Equation 3.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (3)$$

The junction temperature can be estimated using Equation 4. θ_{JA} is the junction-to-ambient thermal resistance.

$$T_J = T_A + P_D \times \theta_{JA} \quad (4)$$

Layout

Layout Guideline

- Both input capacitors and output capacitors must be placed to the device pins as close as possible, and the vias between capacitors and device power pins must be avoided.
- It is recommended to bypass the input pin to ground with a 0.1-μF bypass capacitor. The loop area formed by the bypass capacitor connection, the IN pin, and the GND pin of the system must be as small as possible.
- It is recommended to use wide trace lengths or thick copper weight to minimize I×R drop and heat dissipation.

Layout Example

The following figure shows a layout example of TPL9305AD-FC2R-S.

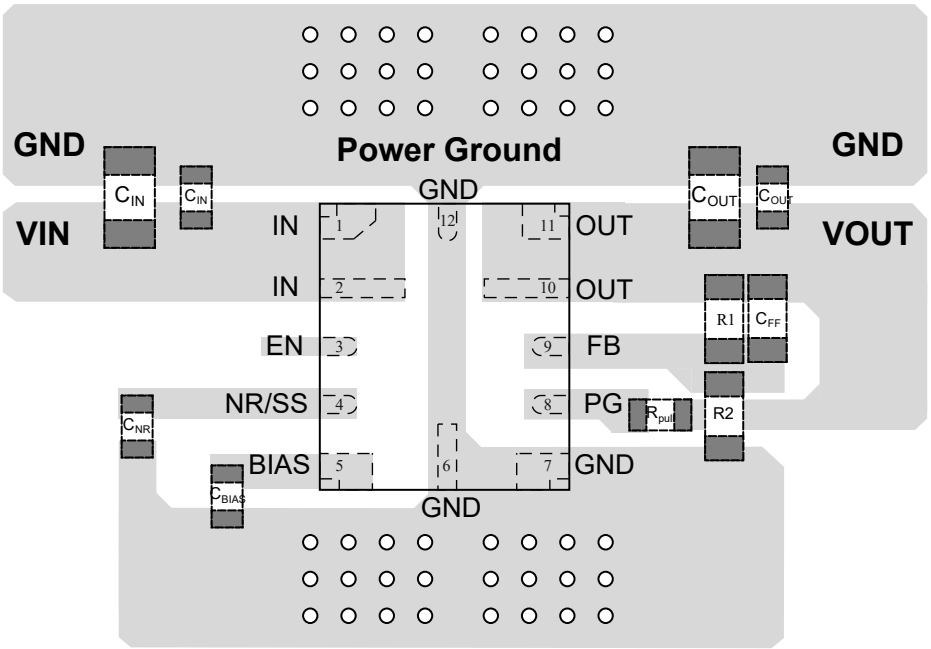
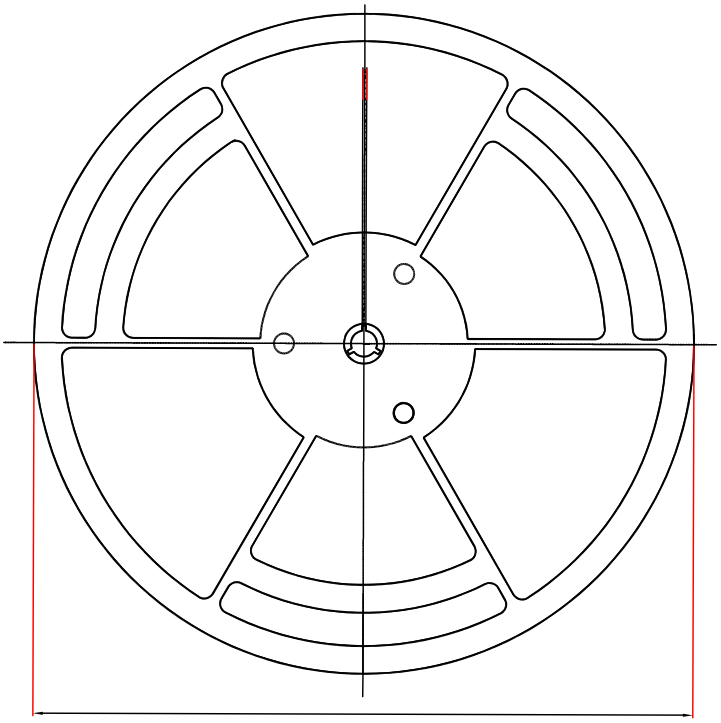
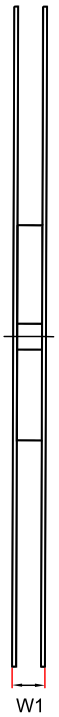
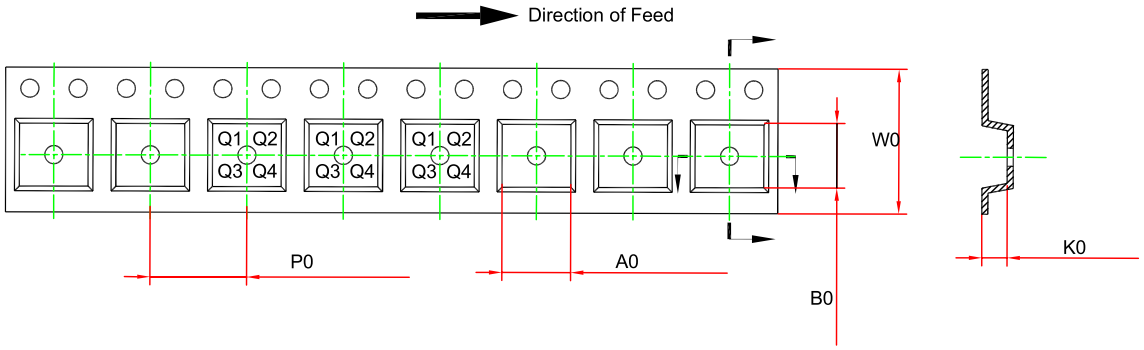


Figure 21. TPL9305AD-FC2R-S Layout Example

Tape and Reel Information





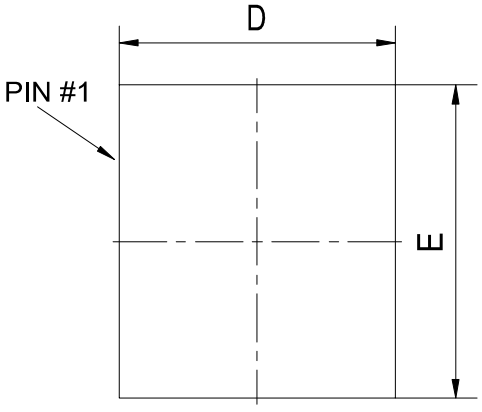


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPL9305AD-FC2R-S	QFN2.2X2.5-12	178	11.4	2.4	2.7	0.95	4	8	Q1

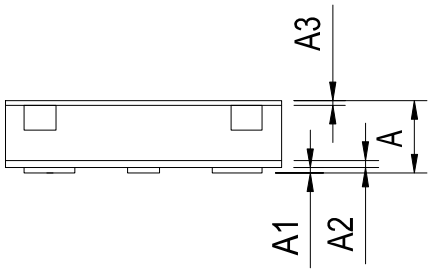
Package Outline Dimensions

QFN2.2X2.5-12

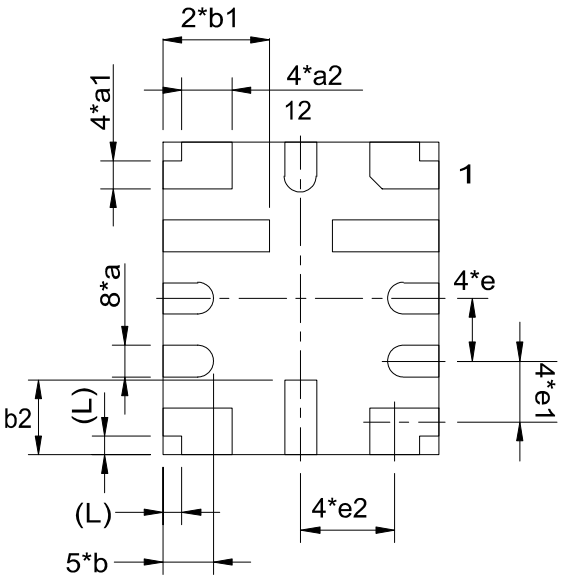
Package Outline Dimensions FC2(QFN2.2X2.5-12-B)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.040		0.002	
A2	0.100		0.004	
A3	0.035		0.001	
D	2.100	2.300	0.083	0.091
E	2.400	2.600	0.094	0.102
e	0.500		0.020	
e1	0.488		0.019	
e2	0.750		0.030	
a	0.200	0.300	0.008	0.012
a1	0.175	0.275	0.007	0.011
a2	0.350	0.450	0.014	0.018
b	0.300	0.500	0.014	0.018
b1	0.750	0.950	0.030	0.037
b2	0.500	0.700	0.018	0.028
L	0.150		0.006	

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPL9305AD-FC2R-S	–40°C to +125°C	QFN2.2X2.5-12	935	MSL3	Tape and Reel, 3,000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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