42-V 300-mA 2-Channel Low-Dropout Linear Regulator with Accurate Current Sense and Protection

Features

- Qualified for Automotive Applications
  - AEC-Q100 Grade 1, T_A: −40°C to +125°C
  - Junction Temperature, T_J: −40°C to +150°C
- Input Voltage: 4.5 V to 42 V, with 45-V Transient
- Output Voltage: 2 Output Channels, Adjustable from 1.5 V to 20 V
- ±2% Output Accuracy over Line Regulation, Load Regulation, and Operating Temperature Range
- 300-mA Maximum Output Current for Each Channel
- Low Dropout Voltage: 500-mV Maximum at 100-mA Load Current
- 5-µA Shutdown Current when EN is Low
- Accurate Current Sense and Diagnosis:
  - Open Load, Overcurrent and Short-circuit Detection
  - High Accuracy: ±3% @ I_{OUT} > 100mA
  - Multiplexing Current Sense to Save ADC Resource
- Input and Output Protections:
  - Reverse Battery Polarity Protection
  - Output Short-Circuit to Ground and Over Current Protection
  - Reverse Current and Short-to-Battery Protection
  - Output Inductive Load Clamp
  - Over Temperature Protection
- Stable with Wide Output Capacitor Range
  - Capacitance from 2.2 µF to 100 µF
  - ESR from 0.001 Ω to 5 Ω
- Package Options: ETSSOP16

Applications

- Automotive Infotainment Active Antenna Power Supply
- Automotive Telematics Active Antenna Power Supply
- Automotive Surround View Camera Power Supply

Description

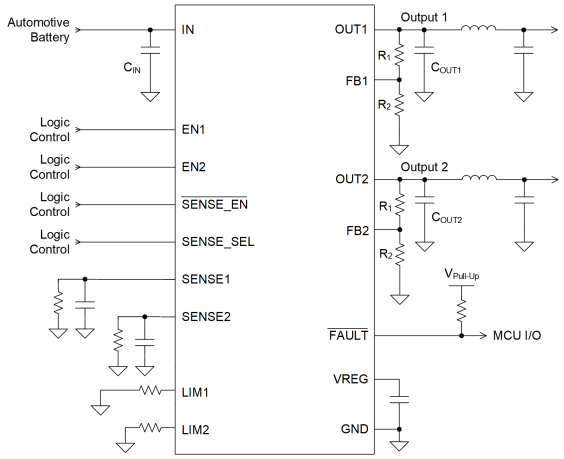
The TPL8772Q is a 2-channel wide-input-voltage low-dropout linear regulator integrated with output current sense and diagnosis function. This device supports operating voltage range from 4.5 V to 42 V, with a maximum transient voltage of 45 V.

The TPL8772Q has two individual adjustable outputs. Connecting an external resistor divider, the output voltage can be set from 1.5 V to 20 V for each channel separately. The output current of each channel is 300 mA, which is suitable for the phantom power or low-noise active antenna power in automotive.

The TPL8772Q offers SENSE1 pin and SENSE2 pin for each-channel current sensing. During normal operation, the output current of each channel can be obtained by measuring the voltage at the SENSE1/2 pin, for which the sense pin current is proportional to the current flow through the internal power MOS. Besides, by monitoring the sense pin voltage, it is easy to distinguish different faults, such as, open load, overload, output short-circuit to ground, over temperature, reverse current or output short-circuit to battery, and reverse input polarity.

The TPL8772Q provides an ETSSOP16 package with a thermal pad and is guaranteed to operate with the ambient temperature range from –40°C to +125°C.

Typical Application Circuit



42-V 300-mA 2-Channel Low-Dropout Linear Regulator with Accurate Current Sense and Protection

Table of Contents

Product Family Table

Order Number	Output Voltage (V)	Package
TPL8772Q-TSBR-S	1.5 V to 20 V	ETSSOP16

Revision History

Date	Revision	Notes
2023-10-15	Rev.Pre.0	Preliminary datasheet
2023-11-05	Rev.Pre.1	Updated Electrical Characteristics
2023-12-25	Rev.Pre.2	Updated Typical Performance Characteristics
2024-04-22	Rev.Pre.3	Updated Electrical Characteristics
2024-06-06	Rev.A.0	Initial released

Pin Configuration and Functions

TPL8772Q
ETSSOP16 Package
Top View

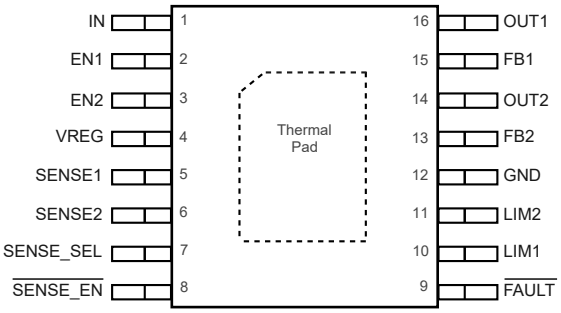


Table 1. Pin Functions: TPL8772Q

Pin No.	Name	I/O	Description
EN1, EN2	2, 3	I	Regulator output enable pins. Drive EN1 high to turn on the channel 1, and drive EN2 high to turn on channel 2; drive EN1 low to turn off channel 1, and drive EN2 low to turn off the channel 2.
$\overline{\text{FAULT}}$	9	O	Open-drain fault indication pin. Suggest pull-up this pin with an external 10-kΩ resistor.
FB1, FB2	13, 15	I	Output feedback pins. Connect an external resistor divider from OUT to GND to set the output voltage, or connect FB to GND directly for the current-limited switch operation.
GND	12	-	Ground reference pin. Connect GND pin to PCB ground plane directly.
IN	1	I	Input power supply pin. Bypass IN to GND with a 1 μF or greater capacitor.
LIM1, LIM2	10, 11	O	Current limit adjustment pins. Connect a resistor to ground to set the current limitation level of each channel. Or short this pin to ground directly to use the internal current limit.
OUT1, OUT2	14, 16	O	Regulated output voltage pins. Connect a 2.2 μF or greater capacitor to ground to ensure the regulator stability.
SENSE1, SENSE2	5, 6	O	Output current sense pins. The sense pin current is proportional to the current flow through the internal power MOS. Connect a resistor in parallel with a 1-μF capacitor to ground to set the sense pin output voltage level. Short this pin to ground directly if current sense is not used.
$\overline{\text{SENSE\_EN}}$	8	I	Current sense function enable pin. Drive this pin high to disable the current sense function and drive this pin low to enable the current sense function.
SENSE_SEL	7	I	Current sense channel select pin. When current sense function is enabled, drive this pin low to select channel 1 output current at SENSE 1 and drive this pin high to select channel 2 output current at SENSE 1.
VREG	4	O	Internal voltage regulator output pin. Connect a 1-μF capacitor to ground for the internal regulator stability.

(1) Thermal Pad **MUST** be connected to PCB ground plane directly.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
IN		−40	45	V
EN1, EN2		−0.3	45	V
OUT1, OUT2		−0.3	45	V
FB1, FB2, LIM1, LIM2, $\overline{\text{FAULT}}$, $\overline{\text{SENSE\_EN}}$, SENSE_SEL		−0.3	7	V
VREG		−0.3	7	V
SENSE1, SENSE2		−0.3	VREG + 0.3	V
T_J	Junction Temperature Range	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) All voltage values are with respect to GND.
(3) Not subject to production test, specified by design.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	AEC Q100-002	±2	kV
CDM	Charged Device Model ESD	AEC Q100-011	±1	kV

Recommended Operating Conditions

Parameter		Min	Max	Unit
IN		4.5	42	V
EN1, EN2		0	42	V
OUT1, OUT2	Regulation mode	1.5	20	V
	Switching mode	1.5	35	V
FB1, FB2, LIM1, LIM2, $\overline{\text{FAULT}}$, $\overline{\text{SENSE\_EN}}$, SENSE_SEL		0	5.5	V
C_{OUT}	Output Capacitor Requirements	2.2	100	μF
ESR	Output Capacitor ESR Requirements	0.001	5	Ω
T_A	Ambient Temperature Range	−40	125	°C
T_J	Junction Temperature Range	−40	150	°C

Thermal Information

Package Type	θ_{JA}	θ_{JB}	$\theta_{JC,top}$	Unit
ETSSOP16	33	12	30	°C/W

Electrical Characteristics

All test conditions: V_{IN} = 14 V, V_{EN} = 2 V, C_{IN} = C_{OUT} = 10 µF, I_{OUT} = 0.1 mA. T_A = −40°C to +125°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply Input Voltage and Current						
V_{IN}	Input Supply Voltage Range (1)		$V_{IN,MIN}$		42	V
UVLO	V_{IN} Under-Voltage Lockout Threshold	VIN rising, V_{EN} = 2 V, I_{OUT} = 0.1 mA		3.65	4	V
	Hysteresis			485		mV
I_{SD}	Shutdown Current	V_{EN} = 0 V		1.5	5	µA
I_Q	Quiescent Current	I_{OUT} = 0 mA		0.43	1.05	mA
		I_{OUT} = 1 mA		0.43	1.05	mA
		I_{OUT} = 300 mA (I_{OUT} of two channels are both 300 mA)		3.2	6	mA
$I_{LKG\_IN\_REV}$	Leakage Current of Input Voltage Reverse Polarity	–40 V < V_{IN} < 0 V, reverse current to IN		0.04		mA
Enable Control (EN1 and EN2)						
V_{IH_EN}	EN Logic Input High (Enable)		2		42	V
V_{IL_EN}	EN Logic Input Low (Disable)		0		0.7	V
I_{EN}	EN Pin Leakage Current	V_{EN} = 2 V to 42 V	0		4	µA
Current Sense Control ($\overline{SENSE\_EN}$, SENSE_SEL)						
V_{IH}	Logic-Input High Level		2		5.5	V
V_{IL}	Logic-Input Low Level		0		0.7	V
$I_{\overline{SENSE\_EN}}$	$\overline{SENSE\_EN}$ pin leakage current	$V_{\overline{SENSE\_EN}}$ = 5 V			10	µA
I_{SENSE_SEL}	SENSE_SEL Pin Leakage Current	V_{SENSE_SEL} = 5 V			10	µA
Output Voltage and Current						
V_{FB}	Feedback Voltage		−2%	1.233	2%	V
I_{FB}	FB Pin Leakage Current	Force V_{FB} = 1.3V	−1		1	µA
V_{OUT}	Output Accuracy (2)	V_{IN} = V_{IN_MIN} to 42 V, I_{OUT} = 10 mA , voltage variation on FB pin	−2%		2%	
ΔV_{LINE}	Line Regulation on FB pin (2)	I_{OUT} = 1 mA to 300 mA, voltage variation on FB pin			10	mV
ΔV_{LOAD}	Load Regulation on FB pin (2)	V_{IN} = 14 V, I_{OUT} = 1 mA to 300 mA, voltage variation on FB pin			20	mV
V_{DO}	Dropout Voltage (3)	Force V_{FB} = 1.2 V, I_{OUT} = 100 mA		300	500	mV
		Force V_{FB} = 1.2 V, I_{OUT} = 300 mA		900	1500	mV
I_{OUT}	Output Current Range	V_{OUT} in regulation	0		300	mA

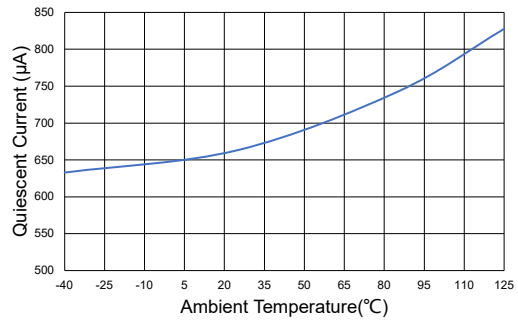
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{DIS}	Output Active Discharge Resistor	EN = GND		50		kΩ
V_{REG}	Internal Regulator Output Voltage	V_{IN} = V_{IN_MIN} to 42 V, I_{REG} = 0 mA	4	4.25	4.5	V
I_{REG_LIM}	Internal Regulator Output Current Limit		15		75	mA
Current Sense and Fault Detection						
I_{CL}	Internal Current Limit	Short LIM1 or LIM2 to GND	340		550	mA
K_{CL}	OUT1/2 to LIM1/2 Current Ratio (I_{OUTx}/I_{LIMx})	V_{IN} = V_{IN_MIN} to 42 V, I_{OUT} = 50 mA to 300 mA		198		
I_{LIM}	Adjustable Current-Limit Accuracy	V_{IN} = V_{IN_MIN} to 42 V, I_{OUT} = 50 mA to 300 mA	−8%		8%	
K_{SENSE}	OUT1/2 to SENSE1/2 Current Ratio (I_{OUTx}/I_{SENSEx})	V_{IN} = V_{IN_MIN} to 42 V, I_{OUT} = 5 mA to 300 mA		198		
I_{SENSE}	Current Sense Accuracy	I_{OUT} = 100 mA to 300 mA	−3%		3%	
		I_{OUT} = 50 mA to 100 mA	−5%		5%	
		I_{OUT} = 10 mA to 50 mA	−10%		10%	
		I_{OUT} = 5 mA to 10 mA	−20%		20%	
I_{LKG}	Leakage Current of SENSE1, SENSE2, LIM1 and LIM2	EN = GND			2	μA
V_{SENSE_STB}	SENSE Pin Voltage of Short-to-Battery Fault	When short-to-battery fault or reverse-current fault occurs	3.05	3.1	3.3	V
V_{SENSE_OT}	SENSE Pin Voltage of Over-Temperature Fault	When over-temperature fault occurs	2.7	2.75	3	V
V_{SENSE_OC}	SENSE Pin Voltage of Over-Current Fault	When over-current fault occurs	2.4	2.5	2.65	V
I_{SENSE_H}	SENSE Pin Current of Fault Conditions	When short-to-battery fault, reverse-current fault, over-temperature fault or over-current fault occurs	3.3			mA
V_{TH_STB}	Short-to-Battery Threshold	V_{OUT} − V_{IN}, checked during startup	−500	−300	110	mV
I_{REV}	Reverse-Current Threshold	Power MOS is on	−100	−40	−1	mA
V_{TH_ILIM}	Current Limit Threshold	When output current is limited		1.233		V
$V_{OL\_\overline{FAULT}}$	Output Low Level of $\overline{FAULT}$	Sink 5 mA to $\overline{FAULT}$ pin			0.4	V
$I_{LKG\_\overline{FAULT}}$	Leakage current of $\overline{FAULT}$	Force 5 V at $\overline{FAULT}$ pin			1	μA
$t_{d\_SENSE\_SEL\_R}$	Current Sense Delay Time from the Rising Edge of SENSE_SEL (4)	$\overline{SENSE\_EN}$ = GND, SENSE_SEL rising from 0 to 5 V in 1 us		10		μs
$t_{d\_SENSE\_SEL\_F}$	Current Sense Delay Time from the Falling Edge of SENSE_SEL (4)	$\overline{SENSE\_EN}$= GND, SENSE_SEL falling from 0 to 5 V in 1us		10		μs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d\_\overline{SENSE\_EN}\_R}$	Current Sense Delay Time From the Rising Edge of $\overline{SENSE\_EN}$ (4)	$\overline{SENSE\_EN}$ rising from 0 to 5 V in 1us		10		μs
$t_{d\_\overline{SENSE\_EN}\_F}$	Current Sense Delay Time From the Falling Edge of $\overline{SENSE\_EN}$ (4)	$\overline{SENSE\_EN}$ falling from 0 to 5 V in 1us		10		μs
t_{d_RC}	Reverse-Current Fault or Short-to-Battery Fault Shutdown Deglitch Time (4)	The delay time from reverse current is detected to the power FET is switched off. I_{OUT} = −200 mA, T_A = 25°C		5	20	μs
t_{BLK_RC}	Reverse-Current Fault Detection Blanking Time (4)	Reverse-current fault detection after power up, the rising edge of EN1/2, current limitation event is over, or recovery from over temperature condition		16		ms
PSRR and Output Noise						
PSRR	Power Supply Rejection Ratio (4)	I_{OUT} = 10 mA, f = 100 Hz		90		dB
		I_{OUT} = 10 mA, f = 1 kHz		80		dB
		I_{OUT} = 10 mA, f = 100 kHz		80		dB
		I_{OUT} = 10 mA, f = 1 MHz		33		dB
V_N	Output RMS noise (4)	I_{OUT} = 10 mA, 10 Hz to 100 kHz		350		μV_{RMS}
Temperature Range						
T_{SD}	Thermal Shutdown Threshold (4)			175		°C
	Thermal Shutdown Hysteresis (4)			15		°C

(1) V_{IN_MIN} = 4.5 V or V_{OUT_NOM} + 1.5 V, whichever is greater.
(2) Tolerance of external resistor divider is not included.
(3) Dropout voltage is the minimum input-to-output voltage differential needed to maintain regulation at a specified output current. Dropout voltage is measured when forcing the FB voltage to 1.2 V. In dropout, the output voltage will be equal to (V_{IN} – V_{DO}).
(4) Not tested during production, guaranteed by design.

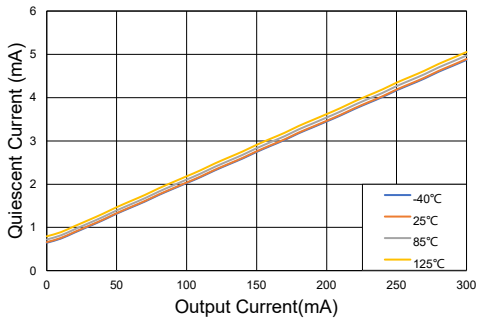
Typical Performance Characteristics

All test conditions: V_{IN} = 14 V, V_{EN} = 2 V, V_{OUT} = 5 V; C_{IN} = C_{OUT} = 10 µF, I_{OUT} = 0.1 mA. T_A = 25°C, unless otherwise noted.



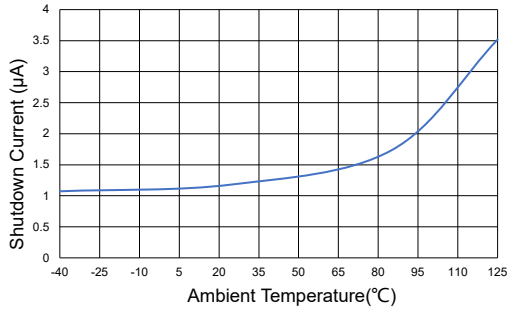
Both Channel 1 and Channel 2 are enabled

Figure 1. Quiescent Current vs Ambient Temperature



Both Channel 1 and Channel 2 are enabled

Figure 2. Quiescent Current vs Load Current



Both Channel 1 and Channel 2 are disabled

Figure 3. Shutdown Current vs Ambient Temperature

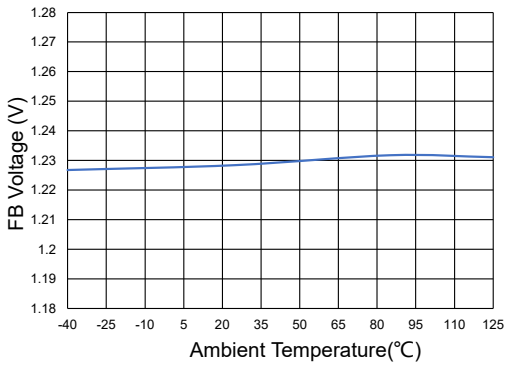
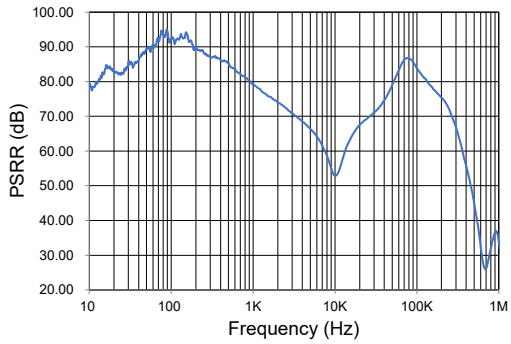
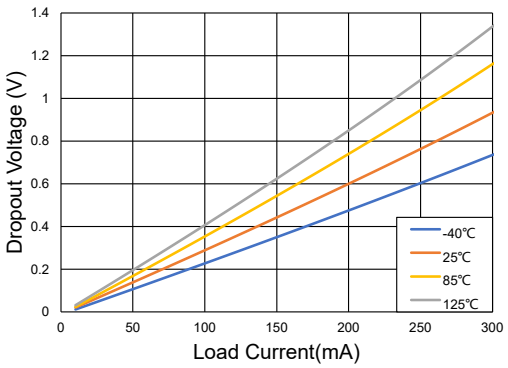


Figure 4. FB Voltage vs Ambient temperature



Load current = 10 mA

Figure 5. PSRR



V_{OUT} = 5 V

Figure 6. Dropout Voltage vs Load Current

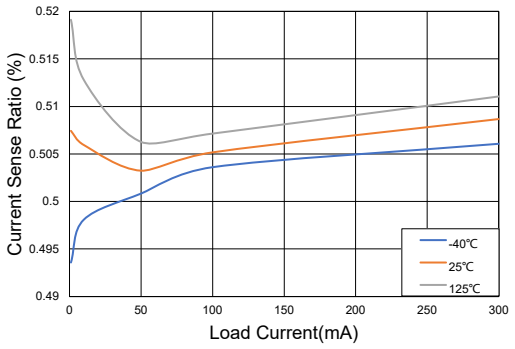


Figure 7. Current-Sense Ratio vs Load Current, Channel 1

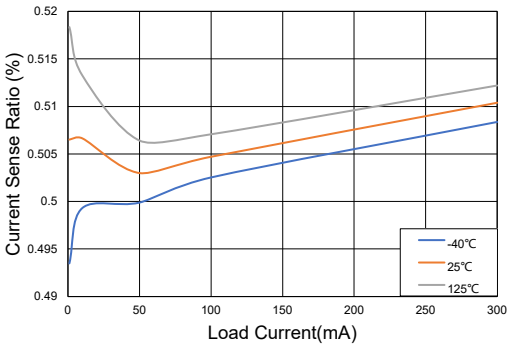


Figure 8. Current-Sense Ratio vs Load Current, Channel 2

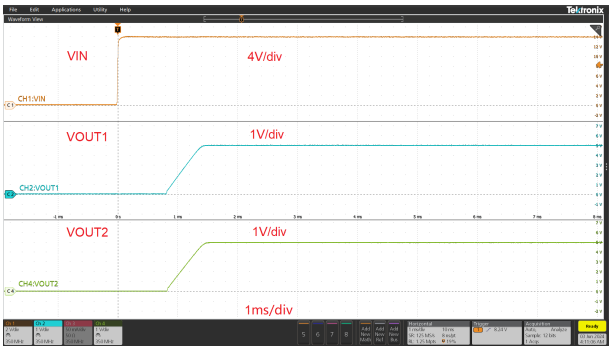


Figure 9. Startup Waveform

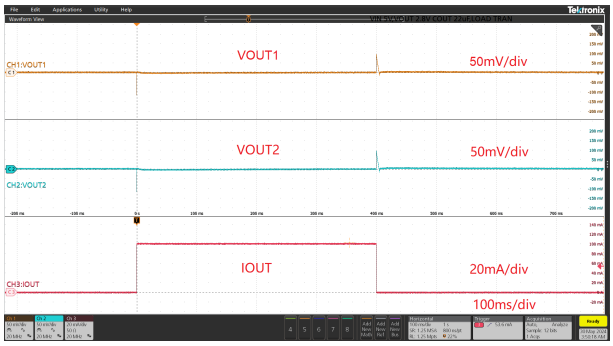


Figure 10. 0-mA to 100-mA Load Transient

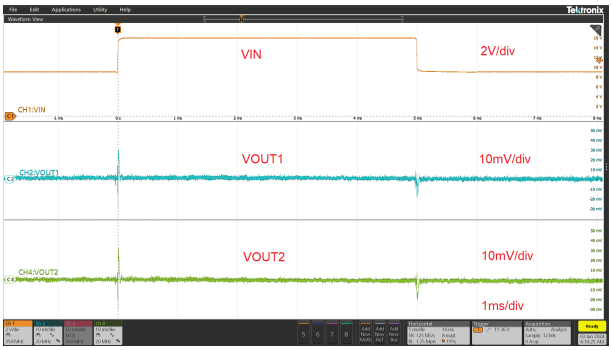


Figure 11. 9-V to 16-V Line Transient

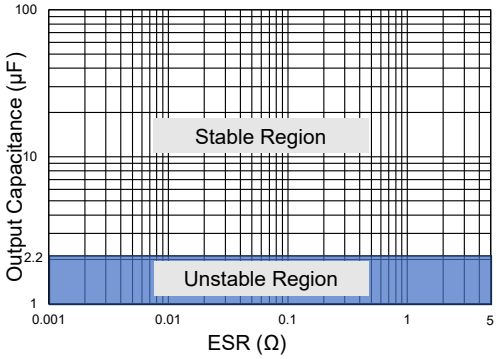


Figure 12. Output Capacitance Stability Range

Detailed Description

Overview

The TPL8772Q is a 2-channel wide-input-voltage low-dropout linear regulator integrated with output current sense and diagnosis function. This device supports operating voltage range from 4.5 V to 42 V, with a maximum transient voltage of 45 V.

The TPL8772Q has two individual adjustable outputs. Connect an external resistor divider, the output voltage can be set from 1.5 V to 20 V for each channel separately. The output current of each channel is 300 mA, which is suitable for the phantom power or low-noise active antenna power in automotive.

The TPL8772Q offers the SENSE1 pin and the SENSE2 pin for each-channel current sensing. During normal operation, the output current of each channel can be obtained by measuring the voltage at the SENSE1/2 pin, for which the sense pin current is proportional to the current flow through the internal power MOS. Besides, by monitoring the sense pin voltage, it is easy to distinguish different faults, such as open load, over load, output short-circuit to ground, over temperature, reverse current or output short-circuit to the battery, and reverse input polarity.

Functional Block Diagram

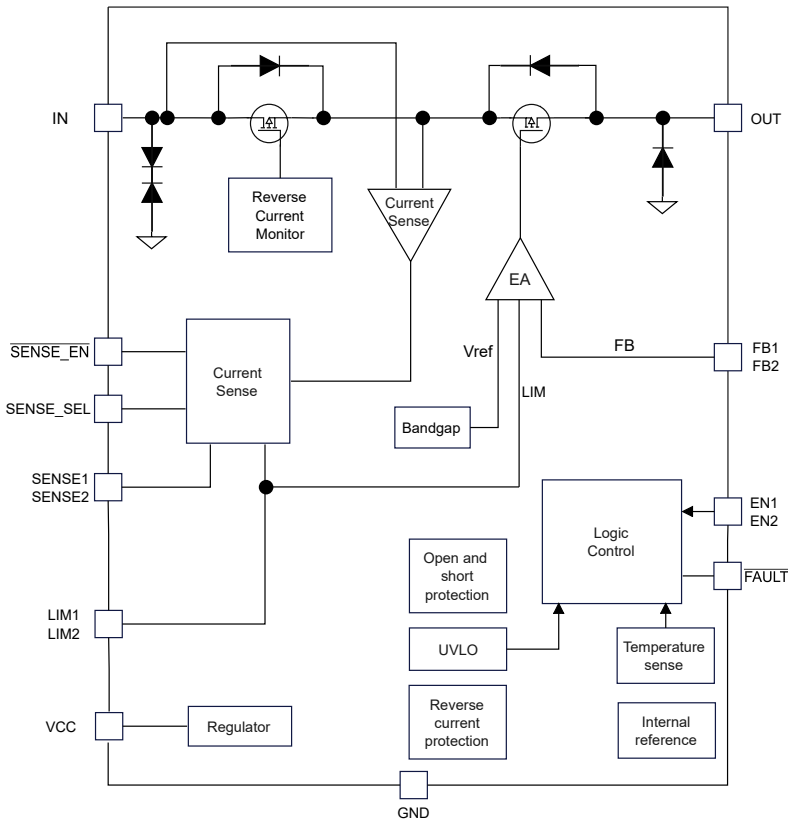


Figure 13. Functional Block Diagram

Feature Description

Enable (EN1, EN2)

The enable pins are active high. Connect this pin to the GPIO of an external processor or digital logic control circuit to enable and disable the device. Or connect this pin to the IN pin for self-bias applications.

Under-Voltage Lockout (UVLO)

TPL8772Q uses an under-voltage lockout circuit to keep the output shut off until the internal circuitry operates properly. Refer to the Electrical Characteristics table for UVLO threshold and hysteresis.

Regulated Output Voltage (OUT)

The output voltage of TPL8772Q can be set from 1.5 V to 20 V for each channel separately. When the input voltage is higher than V_{OUT_NOM} + V_{DO}, the output pin is the regulated output based on the selected voltage version. When the input voltage falls below V_{OUT_NOM} + V_{DO}, the output pin tracks the input voltage minus the dropout voltage based on the load current.

Adjustable Output Voltage

Use an external resistor divider to select an output voltage between 1.5 V and 20 V. Use the following formula to calculate the output voltage. The recommended value for both R1 and R2 is less than 100 kΩ.

$$V_{OUT} = V_{FB} \times \frac{R_1 + R_2}{R_2} \quad (1)$$

Fault Detection

Before the device goes into current-limit mode the output current-sense voltage is linearly proportional to the actual load current. During the short-circuit condition the output current-sense voltage is between 2.4 V and 2.65 V (2.5 V typical). During the thermal-shutdown condition, the output current-sense voltage is between 2.7 V and 3 V (2.75 V typical). During the reverse-current and short-to-battery condition the output current-sense voltage is between 3.05 V and 3.3 V (3.1 V typical).

FAILURE MODE	V_{SENSEx}	$\overline{FAULT}$	LDO SWITCH OUTPUT	LATCHED
Open load	$I_{OUT} \times R_{SENSEx}/198$	High	Enabled	No
Normal		High	Enabled	No
Overcurrent		High	Enabled	No
Short-circuit or current limit	2.4 to 2.65 V	Low	Enabled	No
Thermal shutdown	2.7 to 3 V	Low	Disabled	No
Output short-to-battery	3.05 to 3.3 V	Low	Disabled	Yes
Reverse current	3.05 to 3.3 V	Low	Disabled	Yes

Current Sense Multiplexing

When dealing with limited ADC resources, the device offers a multiplexing solution for current sensing. By utilizing just one current sense pin and one ADC, it enables monitoring of all antenna outputs. The SENSE_SEL pin plays a crucial role in selecting the specific channels for current monitoring. Additionally, the $\overline{SENSE\_EN}$ pin allows for enabling and disabling the SENSE pin, enabling multiplexing between different chips. This approach significantly reduces the hardware requirements, as only a single ADC and one resistor are needed for diagnosing the current-sense of multiple outputs.

The following table shows the selection logic for the current sense.

$\overline{\text{SENSE\_EN}}$	SENSE_SEL	SENSE1 STATUS	SENSE2 STATUS
Low	Low	CH1 current	CH2 current
Low	High	CH2 current	High impedance
High	-	High impedance	High impedance

The following figure shows the application of Current Multiplexing.

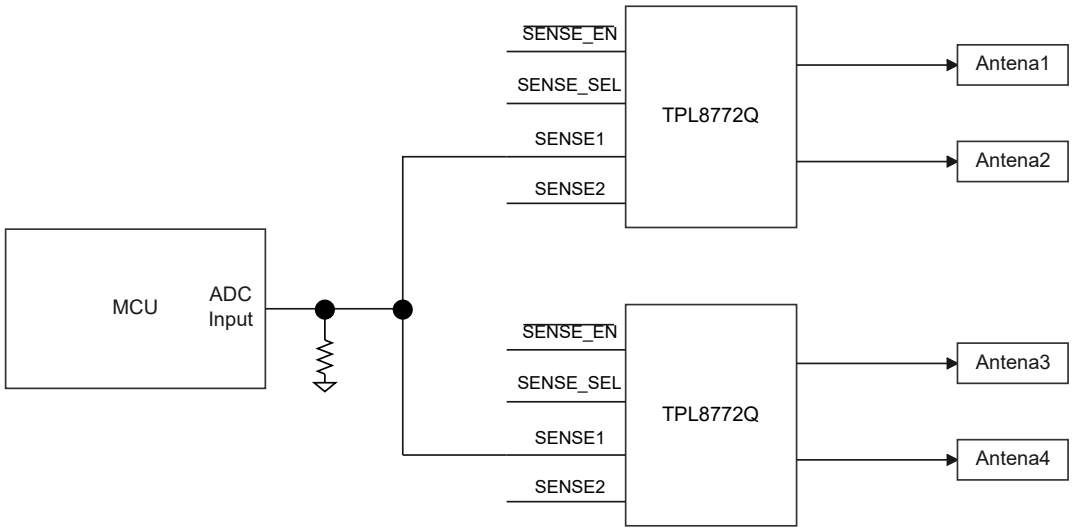


Figure 14. Current Multiplexing Application

Over-Current Protection

The TPL8772Q series integrates an internal current limit that helps to protect the regulator during fault conditions, e.g., the output is shorted to ground, or the output is forced below V_{OUT_NOM}. The output voltage is not regulated when the device is in current limit, and $V_{OUT} = I_{CL} \times R_{LOAD}$.

Short-to-Battery and Reverse Current Detection

To detect an Out-Short-to-Battery fault, each channel compares the voltage levels between the OUT and IN pins prior to activating the switch. The short-to-battery detection occurs every time the LDO switch is enabled, either on the rising edge of the EN pin or during the recovery phase from thermal shutdown. If the device identifies the short-to-battery fault during this process, it will immediately latch off the LDO switch, assert the ERR pin to a low state, and internally pull up the SENSE voltage of the faulty channel to a voltage rail ranging from 3.05 V to 3.3 V. Once the short-to-battery condition is resolved and the EN pin is toggled, the device will resume normal operation.

If a short-to-battery fault leads to a reverse current flow lasting for more than 5 μs, the LDO switch will be latched off automatically, and the ERR pin will be asserted to a low state to indicate the fault. To clear this latched condition after a short-to-battery (reverse current) fault, the cause of the fault must first be removed, and subsequently, the EN pin must be toggled to enable normal operation of the device.

Over-Temperature Protection

The over-temperature protection starts to work when the junction temperature exceeds the thermal shutdown (TSD) threshold, which turns off the regulator immediately. When the device cools down and the junction temperature falls below the thermal shutdown threshold minus thermal shutdown hysteresis, the regulator turns on again.

The junction temperature range should be limited according to the Recommended Operating Conditions table, continuously operating above the junction temperature range will reduce the device lifetime.

Integrated Reverse-Polarity Protection

The device integrates a reverse-connected PMOS to block the reverse current during reverse polarity at the input and output short-to-battery conditions. A special ESD structure at the input is specified to withstand –40 V.

Integrated Inductive Clamp

During output turnoff, the cable inductance continues to source the current from the output of the device. To facilitate the dissipation of inductive energy accumulated in the cable, the device incorporates an inductive clamp. Additionally, an internal diode is interconnected between the OUT and GND pins, boasting a DC-current capability of 300 mA for the purpose of inductive clamp protection.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPL8772Q is a 2-channel wide-input-voltage low-dropout linear regulator integrated with output current sense and diagnosis function. The following application schematic shows a typical usage of the TPL8772Q.

Typical Application

Figure 15 shows the typical application schematic of the TPL8772Q series.

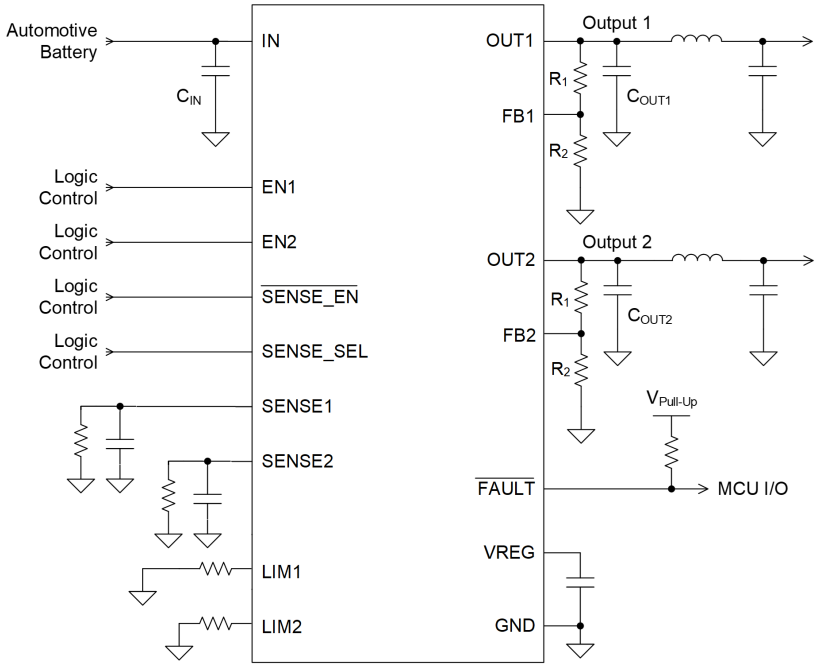


Figure 15. Typical Application Circuit

Current Sense Resistor Selection

The current-sense outputs, SENSE1 and SENSE2, are designed to provide a current that is proportional to the output current flowing through the OUT1 and OUT2 pins of the device. Specifically, the sense current is related to the output current by a factor of 1/198.

The current-sense resistor recommendation is shown in the following table.

Maxiumum Output Current	Recommended Current Sense Resistor
300 mA	1 kΩ
200 mA	1.5 kΩ

100 mA	3 kΩ

Current-Limit Resistor Selection

The device allows for programmable current limiting through the use of external resistors connected to the LIMx pins (LIM1 and LIM2). The current flowing through these LIMx pins is designed to be proportional to the load current at the corresponding OUTx pins (OUT1 and OUT2). Internally, these LIMx pins are connected to a current-limit comparator that references a voltage of 1.233 V.

The programmable current limit accuracy is 8% maximum across all conditions. The following Equation shows how to calculate the maximum current limit value. And this result does not include resistor tolerance in the calculation.

$$R_{LIMx} = \frac{1.08 \times 198 \times 1.233\ V}{I_{LIMx(MAX)}} \quad (2)$$

If internal fixed current limit of the device is needed, short the LIM pin to ground.

Input Capacitor and Output Capacitor

3PEAK recommends adding a 10 μF or greater capacitor with a 0.1 μF bypass capacitor in parallel at the IN pin to keep the input voltage stable. The voltage rating of the capacitors must be greater than the maximum input voltage.

To ensure loop stability, the TPL8772Q series requires an output capacitor of 2.2 μF to 100 μF with an ESR range from 0.001 Ω to 5 Ω. 3PEAK recommends selecting an X7R type 10-μF ceramic capacitor with low ESR over temperature.

Both input capacitors and output capacitors must be placed as close to the device pins as possible.

Power Dissipation and Thermal Consideration

During normal operation, the LDO junction temperature should meet the requirement in the Recommended Operating Conditions table. Use the below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using Equation 3.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (3)$$

The junction temperature can be estimated using Equation 4. θ_{JA} is the junction-to-ambient thermal resistance.

$$T_J = T_A + P_D \times \theta_{JA} \quad (4)$$

Layout

Layout Guideline

- Both input capacitors and output capacitors must be placed to the device pins as close as possible, and the vias between capacitors and device power pins must be avoided.
- It is recommended to bypass the input pin to ground with a 0.1-μF bypass capacitor. The loop area formed by the bypass capacitor connection, the IN pin and the GND pin of the system must be as small as possible.
- It is recommended to use wide and thick copper to minimize I×R drop and heat dissipation.

Layout Example

The following figure shows a layout example of TPL8772Q-TSBR-S.

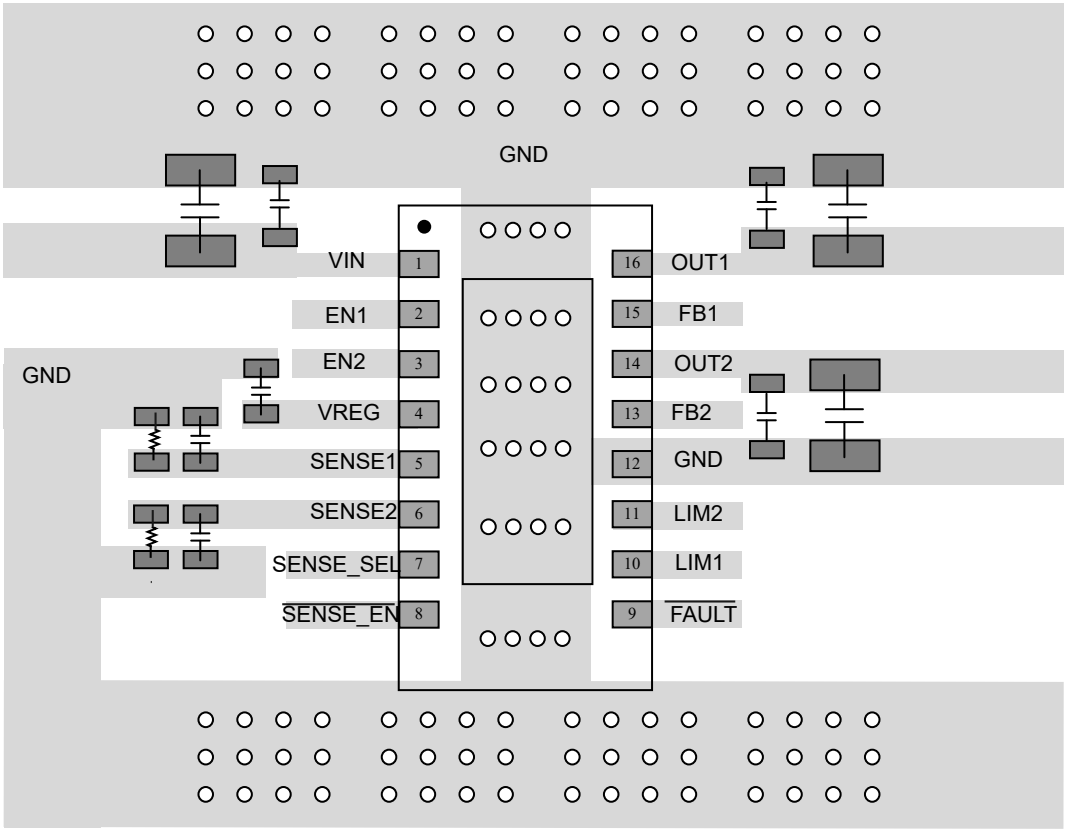
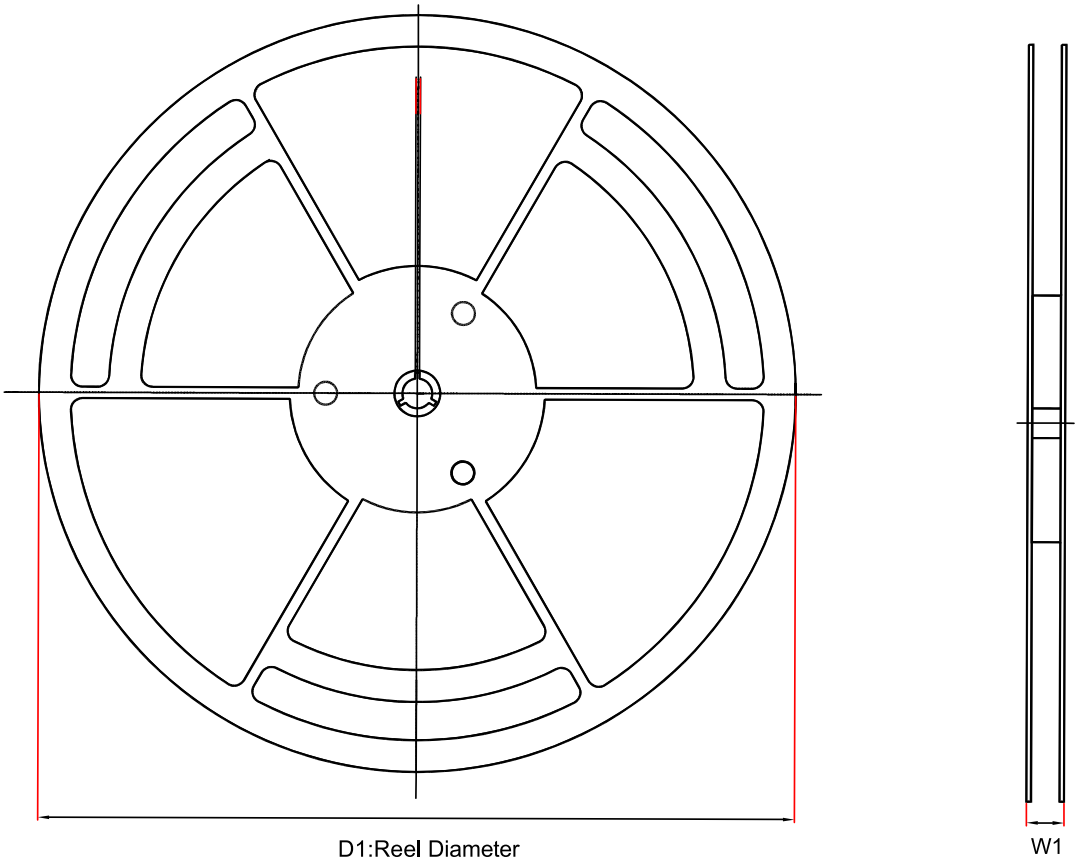
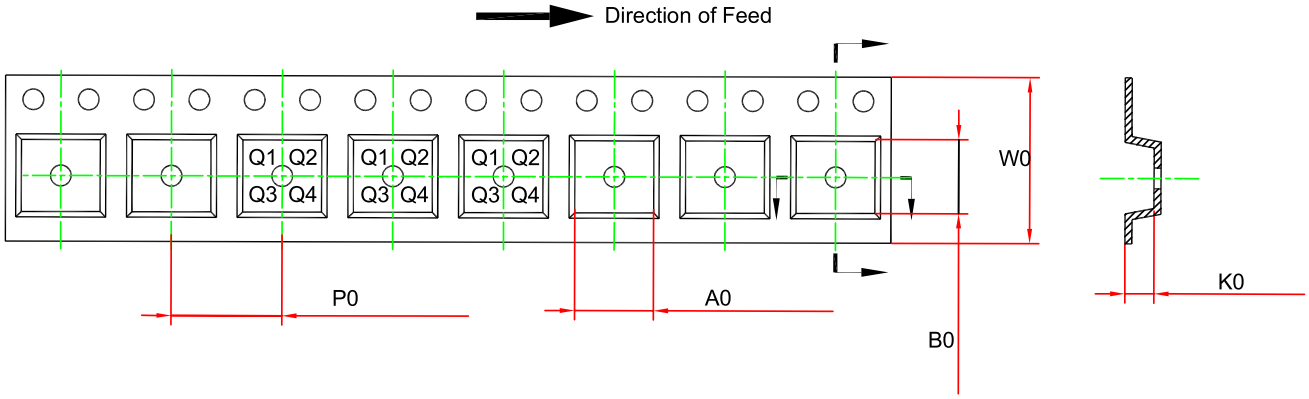


Figure 16. TPL8772Q-TSBR-S Layout Example

Tape and Reel Information



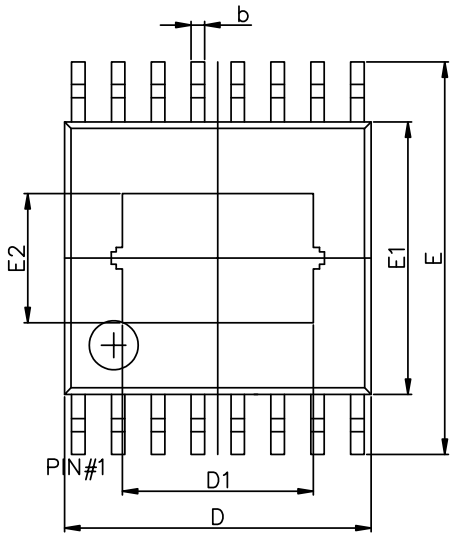


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPL8772Q-TSBR-S	ETSSOP16	330	17.6	6.8	5.4	1.3	8	12	Q1

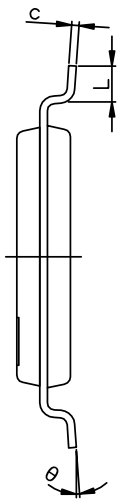
Package Outline Dimensions

ETSSOP-16

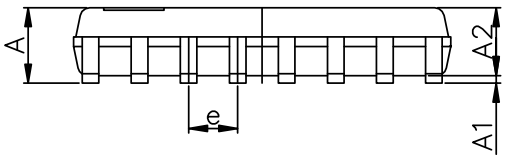
Package Outline Dimensions TSB(ETSSOP-16-D)



Top View



Side View



Bottom View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	---	1.100	---	0.043
A1	0.050	0.150	0.002	0.006
A2	0.850	0.950	0.033	0.037
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
D1	3.015	3.215	0.119	0.127
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
E2	2.005	2.205	0.079	0.087
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.020	0.028
θ	1°	7°	1°	7°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPL8772Q-TSBR-S	−40 to 150°C	ETSSOP16	L8772	MSL3	3,000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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