42-V/450-mA Wide-Input Ultra-low Quiescent Current Low-Dropout Linear Regulator

Features

- Qualified for Automotive Applications:
  - AEC-Q100 Grade 1, T_A: −40°C to +125°C
  - Junction Temperature, T_J: −40°C to +150°C
- Input Voltage: 3 V to 42 V
- Output Voltage:
  - Adjustable from 1.215 V to 21 V
- ±2% Output Accuracy Over Line Regulation, Load Regulation, and Operating Temperature Range
- Low Current Consumption:
  - 1-μA Shutdown Current
  - 5-μA Typical Quiescent Current
- 450-mA Maximum Output Current
- Low Dropout Voltage: 700 mV typical at 400 mA Load Current
- Stable with 2.2-μF to 200-μF Output Capacitor with ESR Range from 0.001 Ω to 5 Ω
- Integrated Protection:
  - Over-Current Protection
  - Over-Temperature Protection
- Package Option:
  - DFN3X3-8

Applications

- Automotive Clusters and Infotainment
- Automotive Headlights and Interior Lighting
- Automotive Domain Control
- Automotive BCM and Door Handler

Description

The TPL8051Q is a series of products supporting operating with 3 V to 42 V (45-V maximum transient voltage). Operating with as low as 3 V allows the TPL8051Q to continue to work well during cold-crank and start-stop conditions.

The TPL8051Q is a series of 5-μA ultra-low quiescent low-dropout voltage linear regulators with 450-mA maximum output current capability.

With the above features, the TPL8051Q series of products are the optimal solutions for powering the MCU, CAN/LIN transceivers in the always-on applications, and the battery-connected applications in the automotive systems.

The TPL8051Q series provides adjustable output voltage options, and the TPL8051Q supports a wide range of output capacitors from 2.2 μF to 200 μF with an ESR range from 0.001 Ω to 5 Ω. Also, the TPL8051Q series integrates over-current protection and over-temperature protection.

The TPL8051Q series operates in the ambient temperature range from –40°C to +125°C.

Typical Application Circuit

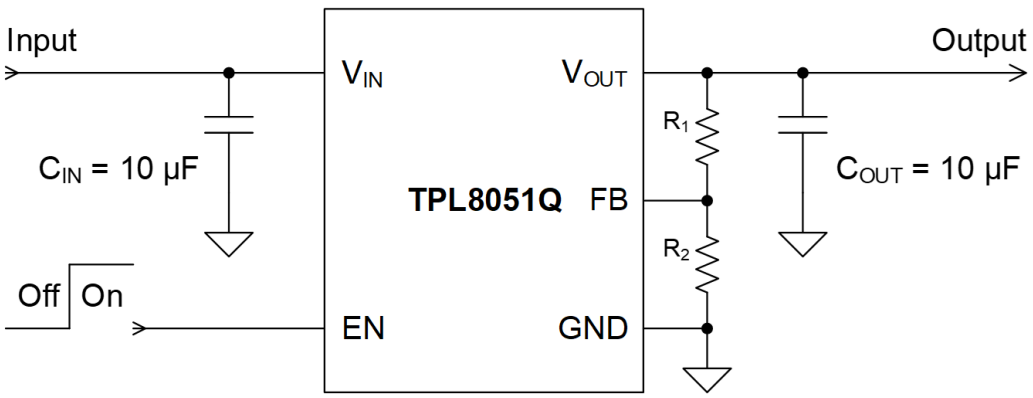


Table of Contents

Product Family Table

Order Number	Output Voltage (V)	Package
TPL8051ADQ-DFCR-S	Adjustable (1.215 V to 21 V)	DFN3X3-8

Revision History

Revision	Notes
Rev.A.0	Initial release

Pin Configuration and Functions

TPL8051Q
DFN3X3-8 Package
Top View

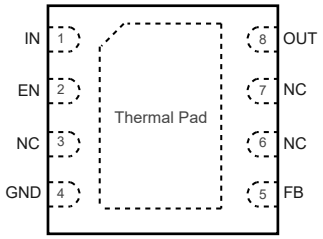


Table 1. Pin Functions: TPL8051Q

Pin No.	Name	I/O	Description
2	EN	I	Regulator enable pin. Drive EN high to turn on the regulator and drive EN low to turn off the regulator.
5	FB	I	Output feedback pin. Connect a resistor divider from OUT to FB and FB to GND to set the output voltage.
4	GND	-	Ground reference pin. Connect the GND pin to the PCB ground plane directly.
1	IN	I	Input voltage pin.
3, 6, 7	NC	–	No connection.
8	OUT	O	Regulated output voltage pin.
–	Thermal Pad	–	Thermal Pad **MUST** be connected to PCB ground plane directly.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
EN, IN		−0.3	45	V
OUT		−0.3	45	V
FB		−0.3	20	V
T_J	Junction Temperature Range	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) All voltage values are with respect to GND.
(3) Not subject to production test, specified by design.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	AEC Q100-002	±2	kV
CDM	Charged Device Model ESD	AEC Q100-011, all pins	±1	kV

Recommended Operating Conditions

Parameter		Min	Max	Unit
IN		3	42	V
EN		0	V_{IN}	V
OUT		0	21	V
C_{OUT} (1)(2)	Output Capacitor Requirements	2.2	200	μF
ESR (2)	Output Capacitor ESR Requirements	0.001	5	Ω
T_A	Ambient Temperature Range	−40	125	°C

(1) The minimum output capacitance requirement is applicable for a worst-case capacitance tolerance of 30%.
(2) Not subject to production test, specified by design.

Thermal Information

Package Type	θ_{JA}	$\theta_{JC, TOP}$	Unit
DFN3X3-8	45.0	88.8	°C/W

Electrical Characteristics

All test conditions: V_{IN} = 13.5 V, V_{EN} = 2 V, C_{IN} = C_{OUT} = 10 µF, I_{OUT} = 0.1 mA. T_A = −40°C to +125°C, unless otherwise noted.

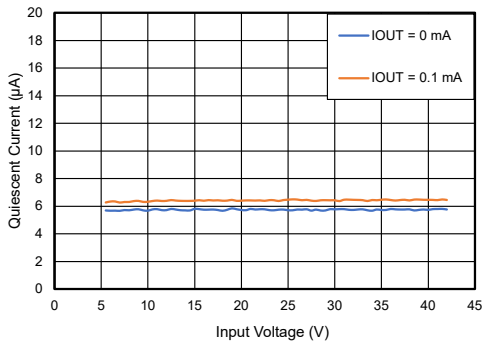
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply Input Voltage and Current						
V_{IN}	Input Supply Voltage Range (1)		$V_{IN, MIN}$		42	V
UVLO	V_{IN} Under-Voltage Lockout Threshold	V_{IN} rising, V_{EN} = 2 V, I_{OUT} = 0.1 mA		2.7	2.9	V
	Hysteresis			270		mV
I_{SD}	Shutdown Current	V_{EN} = 0 V, V_{IN} = 13.5 V		1	4	µA
I_Q	Quiescent Current	I_{OUT} = 0 mA, V_{IN} = 13.5 V		5	10	µA
		I_{OUT} = 0.1 mA, V_{IN} = 13.5 V		6	12	µA
		I_{OUT} = 100 mA, V_{IN} = 13.5 V		400		µA
Enable Input Voltage and Current						
$V_{IH, EN}$	EN Logic Input High (Enable)		2		V_{IN}	V
$V_{IL, EN}$	EN Logic Input Low (Disable)		0		0.7	V
I_{EN}	EN Pin Leakage Current	V_{EN} = 2 V to 42 V			200	nA
Regulated Output Voltage and Current						
V_{FB}	Feedback Voltage	V_{IN} = 6.5 V to 42 V, V_{OUT} = V_{FB}	1.191	1.215	1.239	V
I_{FB}	FB Pin Leakage Current	V_{IN} = 6.5 V to 42 V, V_{FB} = 1.3 V			100	nA
V_{OUT}	Output Accuracy (2)	V_{IN} = 6.5 V to 42 V, I_{OUT} = 1 mA to 450 mA	−2%		2%	
ΔV_{OUT}	Line Regulation	V_{IN} = 6.5 V to 42 V, I_{OUT} = 1 mA		0.004		%/V
	Load Regulation	V_{IN} = 6.5 V, I_{OUT} = 1 mA to 450 mA		0.0005		%/mA
V_{DO}	Dropout Voltage (3)	I_{OUT} = 200 mA, V_{OUT} = 3.3 V		375	600	mV
		I_{OUT} = 400 mA, V_{OUT} = 3.3 V		750	1200	mV
		I_{OUT} = 200 mA, V_{OUT} = 5 V		350	600	mV
		I_{OUT} = 400 mA, V_{OUT} = 5 V		700	1000	mV
I_{OUT}	Output Current Range	V_{OUT} in regulation	0		450	mA
I_{CL}	Output Current Limit	V_{OUT} is forced to 0.9*$V_{OUT\ (NOM)}$	451	600	700	mA
t_{SU}	Start-Up Time (4)	From EN ≥ VIH, EN to OUT ≥ 95% of $V_{OUT\ (NOM)}$		4		ms
PSRR	Power Supply Rejection Ratio (4)	I_{OUT} = 10 mA, f = 1 kHz		50		dB
		I_{OUT} = 10 mA, f = 1MHz		50		dB
Temperature Range						
T_{SD}	Thermal Shutdown Threshold (4)			175		°C
	Thermal Shutdown Hysteresis (4)			20		°C

(1) $V_{IN, MIN}$ = 3 V or $V_{OUT\ (NOM)}$ + 1 V, whichever is greater.

(2) Resistor tolerance is not included.
(3) Dropout voltage is the minimum input-to-output voltage differential needed to maintain regulation at a specified output current. Dropout voltage is measured when the output voltage has dropped 100 mV from the nominal value. In dropout, the output voltage will be equal to (V_{IN} – V_{DO}).
(4) Not test during production.

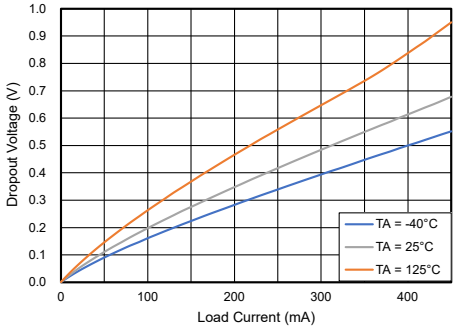
Typical Performance Characteristics

All test conditions: V_{IN} =13.5 V, V_{EN} = 2 V, C_{IN} = C_{OUT} = 10 µF, I_{OUT} = 0.1 mA. T_A = −40°C to +125°C, unless otherwise noted.



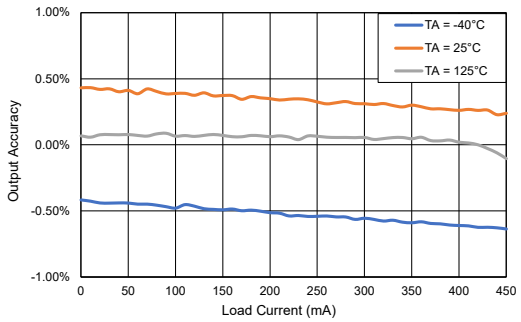
V_{OUT} = 5 V

Figure 1. Quiescent Current vs. Input Voltage



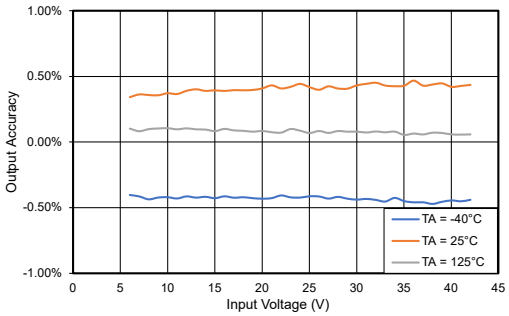
V_{OUT} = 5 V

Figure 2. Dropout Voltage vs. Load Current



V_{OUT} = 5 V

Figure 3. Load Regulation



V_{OUT} = 5 V

Figure 4. Line Regulation

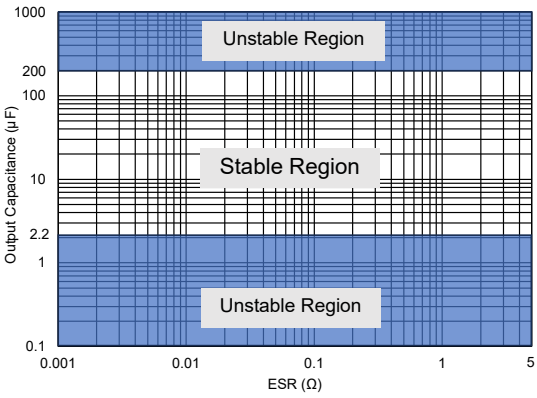
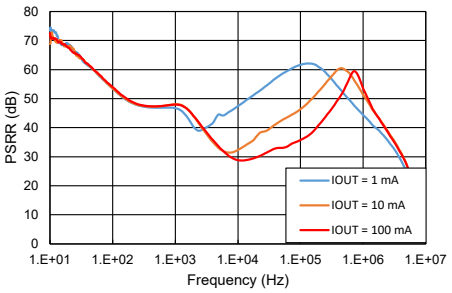
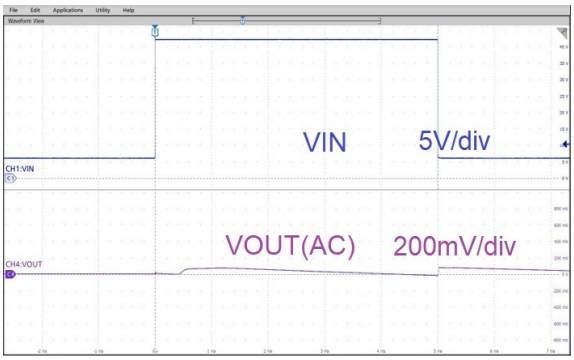


Figure 5. Output Capacitance vs. ESR stability



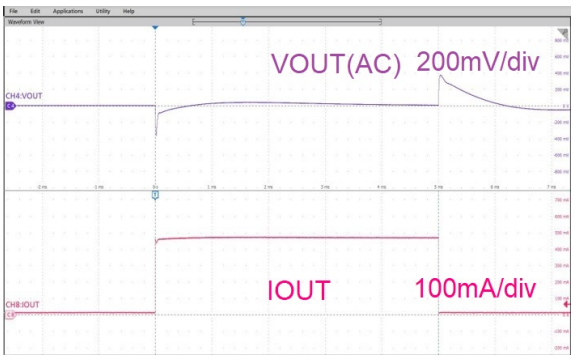
V_{OUT} = 5 V

Figure 6. PSRR



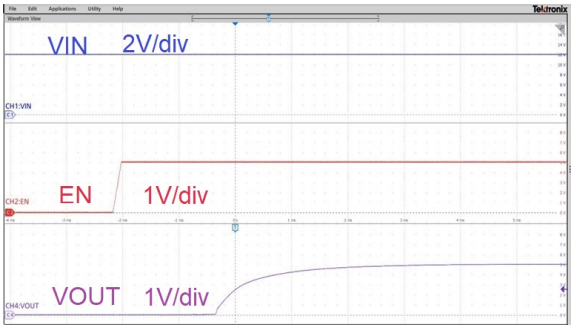
C_{OUT} = 10 µF, V_{IN} = 6 V to 42 V

Figure 7. Line Transient



C_{OUT} = 10 µF, I_{OUT} = 10 mA to 450 mA

Figure 8. Load Transient



C_{OUT} = 10 µF, V_{OUT} = 0 V to 5 V

Figure 9. Startup Waveform

Detailed Description

Overview

The TPL8051Q series supports operating with 3 V to 42 V (45-V maximum transient voltage). Operating with as low as 3 V allows the TPL8051Q to continue to work well during cold-crank and start-stop conditions.

The TPL8051Q is a series of 5-μA ultra-low quiescent low-dropout voltage linear regulators with 450-mA maximum output current capability.

With the above features, the TPL8051Q series of products are the optimal solutions for powering the MCU, CAN/LIN transceivers in the always-on applications, and the battery-connected applications in the automotive systems.

The TPL8051Q series provides an adjustable output voltage option, and the TPL8051Q supports a wide range of output capacitors from 2.2 μF to 200 μF with an ESR range from 0.001 Ω to 5 Ω. Also, the TPL8051Q series integrates over-current protection and over-temperature protection.

Functional Block Diagram

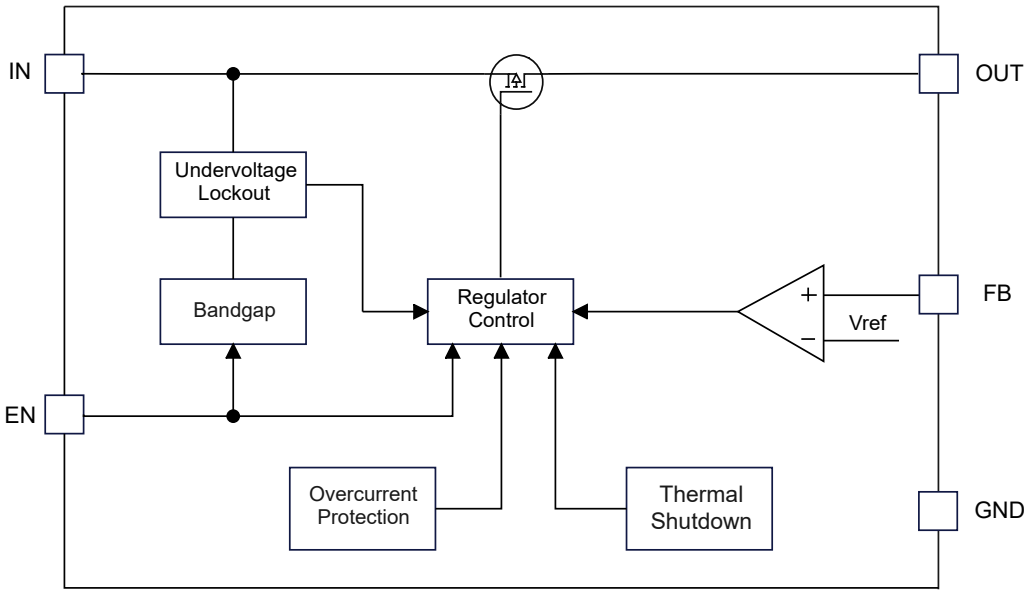


Figure 10. Functional Block Diagram

Feature Description

Enable (EN)

The enable pin (EN) is active high. Connect this pin to the GPIO of an external processor or digital logic control circuit to enable and disable the device. Or connect this pin to the IN pin for self-bias applications.

Under-Voltage Lockout (UVLO)

The TPL8051Q series uses an under-voltage lockout circuit to keep the output shut off until the internal circuitry operates properly. Refer to the Electrical Characteristics table for the UVLO threshold and hysteresis.

Regulated Output Voltage (OUT)

When the input voltage is higher than $V_{OUT\ (NOM)}$ + VDO, the output pin is the regulated output based on the selected voltage version. When the input voltage falls below $V_{OUT\ (NOM)}$ + V_{DO}, the output pin tracks the input voltage minus the dropout voltage based on the load current.

Adjustable Output Voltage

Use the external resistor divider to select an output voltage between 1.215 V and 21 V. Use the following Equation to calculate the output voltage.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Over-Current Protection

The TPL8051Q series integrates an internal current limit that helps to protect the regulator during fault conditions, e.g., the output is shorted to ground, or the output is forced below $V_{OUT\ (NOM)}$. The output voltage is not regulated when the device is in current limit, and $V_{OUT} = I_{CL} \times R_{LOAD}$.

Over-Temperature Protection

The over-temperature protection starts to work when the junction temperature exceeds the thermal shutdown (T_{SD}) threshold, which turns off the regulator immediately. When the device cools down and the junction temperature falls below the thermal shutdown threshold minus thermal shutdown hysteresis, the regulator turns on again. The junction temperature range should be limited according to the Recommended Operating Conditions table; continuously operating above the junction temperature range will reduce the lifetime of the device.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPL8051Q is a series of 42-V 5-μA ultra-low quiescent low-dropout voltage linear regulators with 450-mA maximum output current capability. The following application schematic shows a typical usage of the TPL8051Q series.

Typical Application

Figure 11 shows the typical application schematic of the TPL8051Q series.

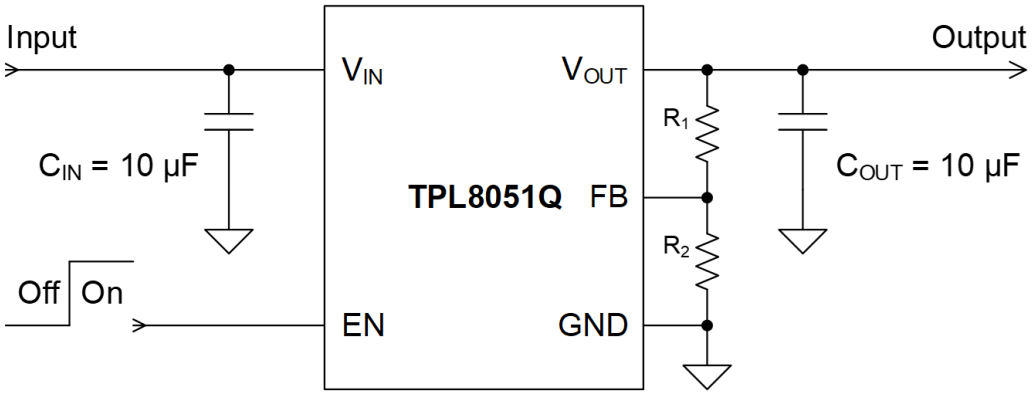


Figure 11. Typical Application Circuit

Input Capacitor and Output Capacitor

The device requires an input decoupling capacitor, the value of which depends on the application. 3PEAK recommends adding a 10-μF or greater capacitor with a 0.1-μF bypass capacitor in parallel at the IN pin to keep the input voltage stable. The voltage rating of the capacitors must be greater than the maximum input voltage.

To ensure loop stability, the TPL8051Q series requires an output capacitor of 2.2 μF to 200 μF with an ESR range from 0.001 Ω to 5 Ω. 3PEAK recommends selecting an X7R type 10-μF ceramic capacitor with low ESR over temperature.

Both input and output capacitors must be placed as close to the device pins as possible.

Power Dissipation and Thermal Consideration

During normal operation, the LDO junction temperature should meet the requirement in the Recommended Operating Conditions table. Use the equations below to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using Equation 2.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (2)$$

The junction temperature can be estimated using Equation 3. θ_{JA} is the junction-to-ambient thermal resistance.

$$T_J = T_A + P_D \times \theta_{JA} \quad (3)$$

Layout

Layout Guideline

- Both input and output capacitors must be placed to the device pins as close as possible, and the vias between capacitors and device power pins must be avoided.
- It is recommended to bypass the input pin to ground with a 0.1-μF bypass capacitor. The loop area formed by the bypass capacitor connection, the IN pin, and the GND pin of the system must be as small as possible.
- It is recommended to use wide and thick copper to minimize I×R drop and heat dissipation.

Layout Example

The following figure shows a layout example of TPL8051ADQ-DFCR-S.

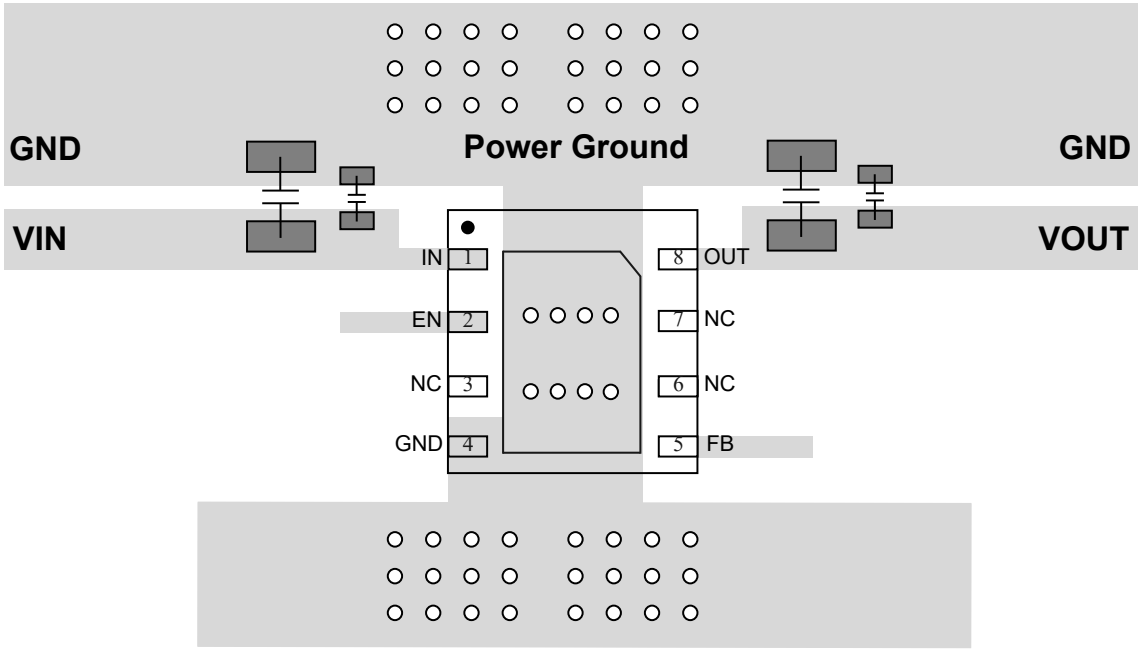
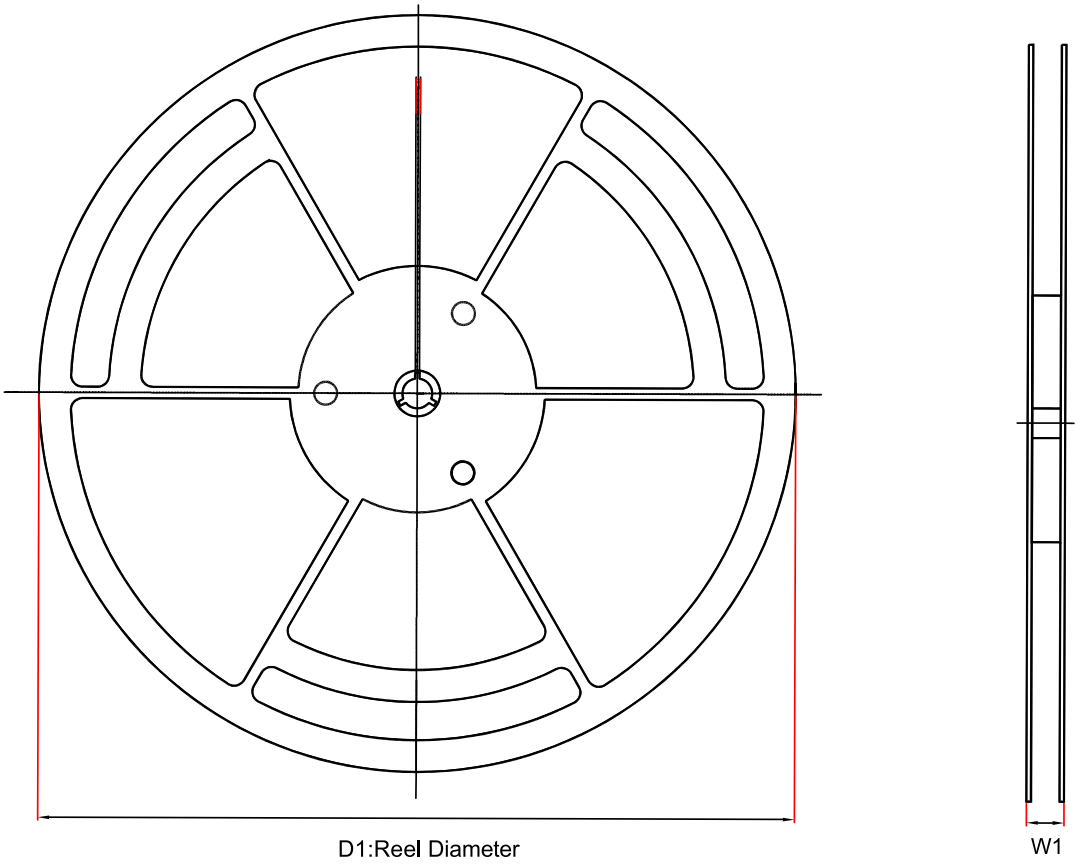
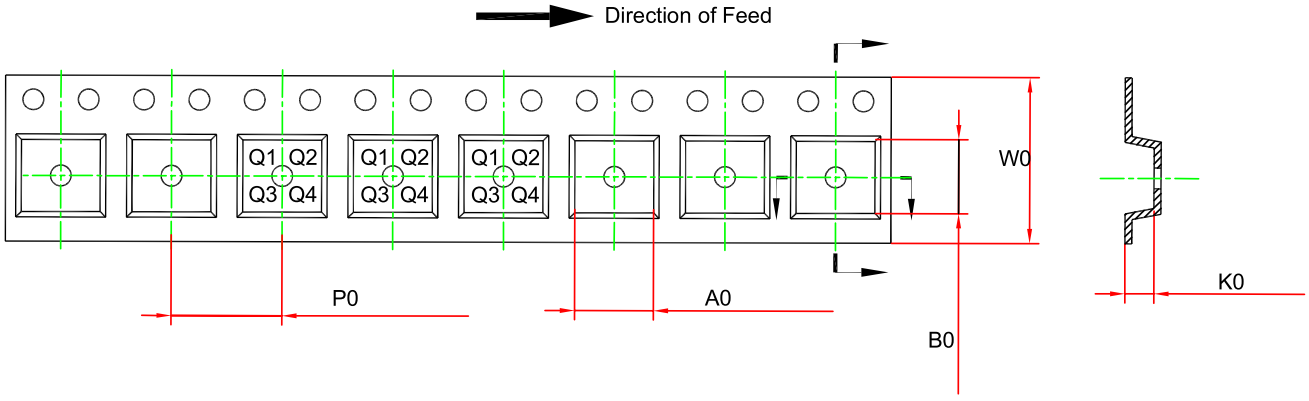


Figure 12. TPL8051ADQ-DFCR-S Layout Example

Tape and Reel Information



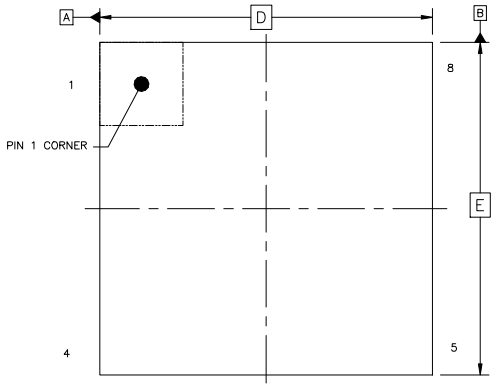


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPL8051ADQ-DFCR-S	DFN3X3-8	330	17.6	3.3	3.3	1.1	8	12	Q1

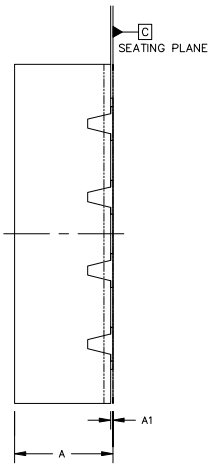
Package Outline Dimensions

DFN3X3-8

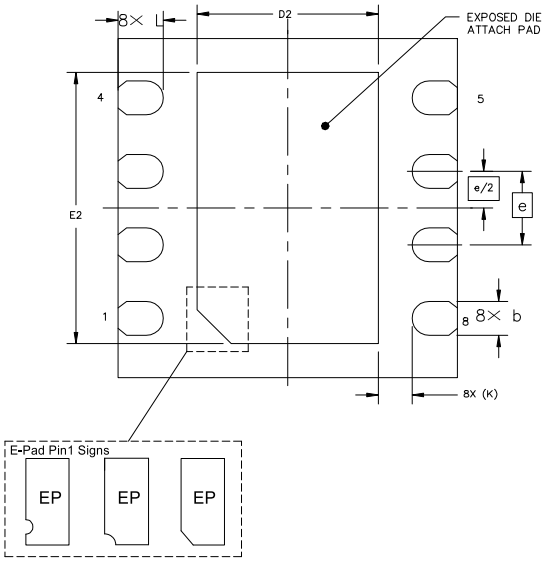
Package Outline Dimensions DFC(DFN3X3-8-J)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.031	0.035
A1	0.000	0.050	0.000	0.002
D	2.900	3.100	0.114	0.122
D2	1.500	1.700	0.059	0.067
E	2.900	3.100	0.114	0.122
b	0.250	0.350	0.010	0.014
E2	2.300	2.500	0.091	0.098
e	0.650 BSC		0.026 BSC	
L	0.350	0.450	0.014	0.018
K	0.300 REF		0.012 REF	

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPL8051ADQ-DFCR-S	−40 to 125°C	DFN3X3-8	L51AD	MSL3	4,000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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Performance Information. Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

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