20-V 200-mA Ultra-Low Noise Ultra-High PSRR Low Dropout Linear Regulator

Features

- Wide Input Voltage Range: 2.5 V to 20 V
- Adjustable Output Voltage Range: 1.2 V to 15 V
- ±2% Accuracy over Line Regulation, Load Regulation, and Operating Temperature Range
- 200-mA Maximum Output Current
- Low Dropout Voltage: 400 mV Max at 200 mA
- Ultra-High PSRR:
  - 110 dB at 1 kHz
  - 80 dB at 1 MHz
- Ultra-Low Output Noise:
  - 1 μV_{RMS} from 10 Hz to 100 kHz
  - 2 nV/sqrt (Hz) at 10 kHz
- Excellent Transient Response
- Precision Enable Threshold
- Adjustable Current Limit with External Resistor
- Open-Drain Power Good Indication
- Adjustable Power-Good Threshold
- Stable with a minimum 4.7-µF Output Capacitor
- Integrated Protection
  - Over-Current Protection
  - Over-Temperature Protection
- Package Options:
  - DFN3X3-10

Applications

- Low-Noise Power Supplies
- Analog Supply: PLL, VCO, Mixer, LNA, ADC
- Low-Noise Instrumentation
- ATE Test Equipment

Description

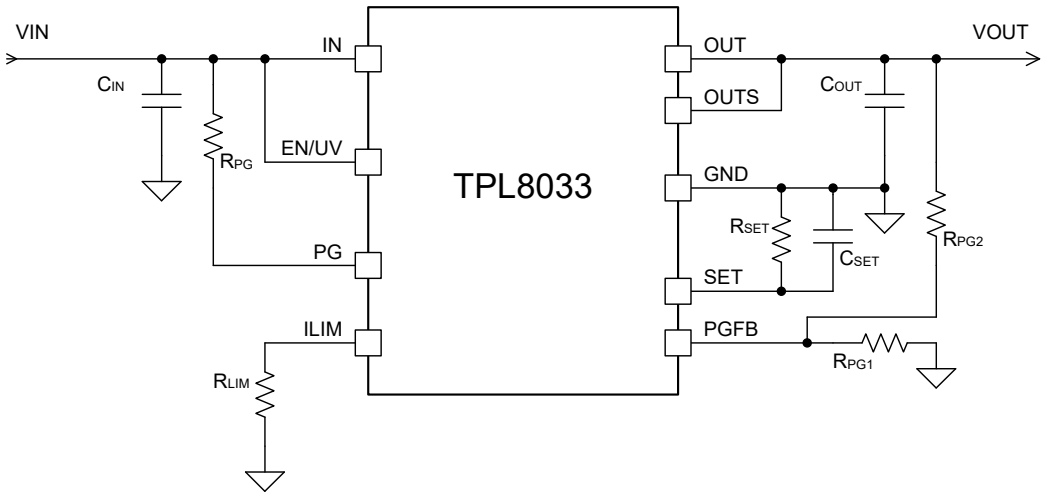
The TPL8033 is a 20-V 200-mA high-performance low-dropout linear regulator with 1-μV_{RMS} ultra-low noise and 110-dB ultra-high PSRR. The TPL8033 supports adjustable output from 1.2 V to 15 V with a single resistor and is stable with 4.7 µF to 100 µF.

The TPL8033 implements a precision current reference and a high-performance voltage buffer. With an external capacitor connecting to the current reference, the output voltage noise can be further reduced.

The TPL8033 features adjustable output current limit with a single external resistor and adjustable power-good threshold with an external resistors divider. The TPL8033 also integrates over-current protection and over-temperature protection to enhance system reliability.

The TPL8033 provides thermal-enhanced 10-pin DFN3X3 and EMSOP packages with guaranteed operating temperature ranging from –40°C to +125°C.

Typical Application Circuit



20-V 200-mA Ultra-Low Noise Ultra-High PSRR Low Dropout Linear Regulator

Table of Contents

Product Family Table

Order Number	Output Voltage (V)	Output Current	Package
TPL8033AD-DF8R	Adjustable	200 mA	DFN3X3-10

Revision History

Date	Revision	Notes
2022-09-10	Rev.Pre.0	Preliminary Revision.
2023-02-28	Rev.A.0	Initial Released.

Pin Configuration and Functions

TPL8033
DFN3X3-10 Package
Top View

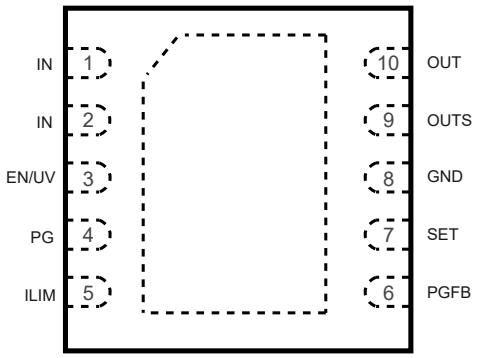


Table 1. Pin Functions: TPL8033

Pin DFN3X3	Name	I/O	Description
3	EN/UV	I	Enable/UVLO pin. Drive EN/UV high to turn on the regulator; drive EN/UV low to turn off the regulator. Connecting an external resistor divider from IN, EN/UV to GND to set the UVLO threshold. For automatic startup, connect EN to IN directly.
8	GND	-	Ground reference pin. Connect GND to PCB ground plane directly.
5	ILIM	O	Current limit adjustment pin. Connect a resistor from ILIM to GND to set an accurate output current limit value.
1, 2	IN	I	Input voltage pin. A 10-μF or larger ceramic capacitor from IN to GND (as close as possible to IN pin) is required to reduce the jitter from the previous-stage power supply.
10	OUT	O	Regulated output voltage pin. A 4.7-μF or larger ceramic capacitor from OUT to GND (as close as possible to OUT pin) is required to ensure the regulator stability.
9	OUTS	I	Output voltage sense input pin. Kelvin connect OUTS to the output capacitor and the load.
4	PG	O	Open-drain power-good output pin. Leave PG open if not used.
6	PGFB	I	Power-good threshold-setup pin. Connecting an external resistor divider from OUT, PGFB to GND to set the programmable power good threshold. Tie PGFB to IN directly if power good and fast start-up functionalities are not used.
7	SET	O	Output voltage setup pin. Connect a resistor from SET to GND to set the output voltage. A capacitor from SET to GND is recommended to improve output noise, PSRR and transient response performance.

(1) The exposed Pad MUST be connected to a large-area ground plane directly to maximize the thermal performance.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
IN, EN/UV		−0.3	22	V
OUT, OUTS, SET		−0.3	16	V
PG, PGFB		−0.3	22	V
OUT − OUTS		−1.2	1.2	V
ILIM		−0.3	1	V
T_J	Maximum Junction Temperature	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) All voltage values are with respect to ground.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±3000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
V_{IN}		2.5	20	V
$V_{EN/UV}$		0	20	V
V_{OUT}, V_{OUTS}		1.2	15	V
V_{SET}		0	15	V
V_{PG}, V_{PGFB}		0	20	V
V_{ILIM}		0	0.3	V
I_{OUT}		0	200	mA
C_{OUT}		4.7	100	µF
T_J	Junction Temperature Range	−40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JB}	$\theta_{JC,BOTTOM}$	Unit
DFN3X3-10	58	15	32	°C/W

Electrical Characteristics

All test conditions: V_{IN} = $V_{OUT(NOM)}$ + 1 V or 2.5 V, whichever is greater; OUTS ties directly to OUT, C_{IN} = C_{OUT} = 4.7 µF, C_{SET} = 4.7 µF, $V_{EN/UV}$ = 5 V, I_{OUT} = 1 mA, −40°C ≤ T_J ≤ +125°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Supply Voltage and Current						
V_{IN} (1)	Input Supply Voltage		$V_{IN, MIN}$		20	V
$V_{IN,UVLO}$	Input Voltage Under-Voltage Lockout Threshold	V_{IN} rising		1.9	2.4	V
		Hysteresis		100		mV
I_Q (2)	Quiescent Current	I_{OUT} = 10 µA, T_J = 25°C		2.2		mA
		I_{OUT} = 1 mA		2.8		mA
		I_{OUT} = 50 mA		3.6		mA
		I_{OUT} = 100 mA		5.1		mA
I_{SD}	Shutdown Current	$V_{EN/UV}$ = 0 V		4		µA
Enable and Power Good						
$V_{EN/UV}$	EN/UV Pin Voltage Threshold	$V_{EN/UV}$ rising		1.23		V
		Hysteresis		120		mV
$I_{EN/UV}$	EN/UV Pin Current	V_{IN} = 20 V, $V_{EN/UV}$ = 0 V	−1		1	µA
		V_{IN} = 20 V, $V_{EN/UV}$ = 1.24 V, T_J = 25°C		0.15		µA
		V_{IN} = 0 V, $V_{EN/UV}$ = 20 V		0.5		µA
V_{PGFB}	PGFB Pin Voltage Threshold	V_{PGFB} rising		300		mV
		Hysteresis		8		mV
I_{PGFB}	PGFB Pin Current	V_{IN} = 2 V, V_{PGFB} = 300 mV		1.5		nA
$V_{OL(PG)}$	PG Pin Low-Level Output Voltage	V_{OUT} < V_{PG}, source 0.1 mA to PG pin		57	100	mV
I_{PG}	PG Pin Leakage Current	V_{OUT} > V_{PG}, apply 20 V at PG pin			1	µA
Output Voltage and Current						
I_{SET}	SET Pin Current	V_{IN} = 2.5 V, V_{OUT} = 1.2 V, I_{OUT} = 1 mA, T_J = 25°C		100		µA
		V_{IN} = 2.5 V to 20 V, V_{OUT} = 1.2 V to 15 V, I_{OUT} = 1 mA to 200 mA		100		µA
	Fast Startup SET Pin Current	V_{IN} = 2.8 V, V_{OUT} = 1.3 V, V_{PGFB} = 289 mV, T_J = 25°C		2		mA
ΔI_{SET}	Change in I_{SET} with V_{SET}	V_{IN} = 20 V, I_{OUT} = 1 mA, V_{SET} = 1.3 V to 15 V		30		nA
		V_{IN} = 20 V, I_{OUT} = 1 mA, V_{SET} = 1.2 V to 15 V		30		nA

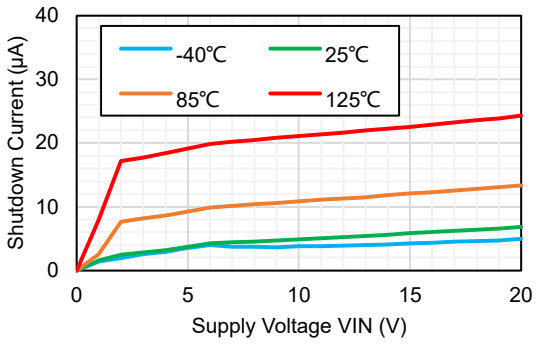
Parameter		Conditions	Min	Type	Max	Unit
Output Voltage and Current						
ΔI_{SET}	SET Pin Current Line Regulation	V_{IN} = 2.5 V to 20 V, V_{OUT} = 1.2 V, I_{OUT} = 1 mA		2		nA/V
	SET Pin Current Load Regulation	V_{IN} = 2.5 V, V_{OUT} = 1.2 V, I_{OUT} = 1 mA to 200 mA		3		nA
V_{OS}	Output Voltage Offset, V_{OUT} − V_{SET}	V_{IN} = 2.5 V, V_{OUT} = 1.2 V, I_{OUT} = 1 mA, T_J = 25°C		1		mV
		V_{IN} = 2.5 V to 20 V, V_{OUT} = 1.2 V to 15 V, I_{OUT} = 1 mA to 200mA		2		mV
ΔV_{OS}	Change in V_{OS} with V_{SET}	V_{IN} = 20 V, I_{OUT} = 1 mA, V_{SET} = 1.2 V to 15 V		30		μV/V
	V_{OS} Voltage Line Regulation	V_{IN} = 2.5 V to 20 V, V_{OUT} = 1.2 V, I_{OUT} = 1 mA		0.03		mV
	V_{OS} Voltage Load Regulation	V_{IN} = 2.5 V, V_{OUT} = 1.2 V, I_{OUT} = 1 mA to 200 mA		0.3		mV
V_{DO} (3)	Dropout Voltage	I_{OUT} = 1 mA, T_J = 25°C		250		mV
		I_{OUT} = 50 mA		250		mV
		I_{OUT} = 150 mA		250		mV
		I_{OUT} = 200 mA		250		mV
I_{CL}	Internal Current Limit	V_{IN} = 2.5 V, V_{OUT} = 0 V		320		mA
		V_{IN} = 12 V, V_{OUT} = 0 V, T_J = 25°C		320		mA
		V_{IN} = 20 V, V_{OUT} = 0 V		320		mA
	Adjustable Current Limit	Current limit ratio		125		mA×kΩ
		V_{IN} = 2.5 V, V_{OUT} = 0 V, R_{LIM} = 625 Ω		200		mA
		V_{IN} = 2.5 V, V_{OUT} = 0 V, R_{LIM} = 2.5 kΩ		50		mA
t_{STR}	Start-Up Time	V_{IN} = 6 V, V_{OUT} = 5 V, I_{LOAD} = 200 mA, C_{SET} = 0.47 μF, V_{PGFB} = 6 V		55		ms
		V_{IN} = 6 V, V_{OUT} = 5 V, I_{LOAD} = 200 mA, C_{SET} = 4.7 μF, V_{PGFB} = 6 V		550		ms
		V_{IN} = 6 V, V_{OUT} = 5 V, I_{LOAD} = 200 mA, C_{SET} = 4.7 μF, R_{PG1} = 50 kΩ, R_{PG2} = 700 kΩ (with Fast Start-Up to 90% of V_{OUT})		10		ms

Parameter		Conditions	Min	Type	Max	Unit
PRSS and Output Noise						
PSRR	Power Supply Rejection Ratio	I_{OUT} = 200 mA, V_{Ripple} = 500 mV_{PP}, f = 120 Hz, C_{OUT} = 4.7 µF, C_{SET} = 4.7 µF		110		dB
		I_{OUT} = 200 mA, V_{Ripple} = 150 mV_{PP}, f = 10 kHz, C_{OUT} = 4.7 µF, C_{SET} = 0.47 µF		90		dB
		I_{OUT} = 200 mA, V_{Ripple} = 150 mV_{PP}, f = 100 kHz, C_{OUT} = 4.7 µF, C_{SET} = 0.47 µF		80		dB
		I_{OUT} = 200 mA, V_{Ripple} = 150 mV_{PP}, f = 1 MHz, C_{OUT} = 4.7 µF, C_{SET} = 0.47 µF		80		dB
		I_{OUT} = 200 mA, V_{Ripple} = 80 mV_{PP}, f = 10 MHz, C_{OUT} = 4.7 µF, C_{SET} = 0.47 µF		50		dB
V_N	Output Noise Spectral Density	V_{OUT} = 3.3 V, I_{OUT} = 200 mA, f = 10 Hz, C_{OUT} = 4.7 µF, C_{SET} = 0.47 µF		525		nV/√Hz
		V_{OUT} = 1.2 V to 15 V, I_{OUT} = 200 mA, f = 10 Hz, C_{OUT} = 4.7 µF, C_{SET} = 4.7 µF		68		nV/√Hz
		V_{OUT} = 1.2 V to 15 V, I_{OUT} = 200 mA, f = 10 kHz, C_{OUT} = 4.7 µF, C_{SET} = 4.7 µF		2.3		nV/√Hz
		V_{OUT} = 3.3 V, I_{OUT} = 200 mA, f = 10 Hz to 100 kHz, C_{OUT} = 4.7 µF, C_{SET} = 0.47 µF		2.5		$µV_{RMS}$
		V_{OUT} = 1.2 V to 15 V, I_{OUT} = 200 mA, f = 10 Hz to 100 kHz, C_{OUT} = 4.7 µF, C_{SET} = 4.7 µF		1		$µV_{RMS}$
	I_{SET} Current RMS Output Noise	BW = 10 Hz to 100 kHz		6		nA_{RMS}
Temperature Range						
T_{SD}	Thermal Shutdown Threshold			170		°C
		Hysteresis		20		°C

(1) $V_{IN,MIN}$ = $V_{OUT(NOM)}$ + 1 V or 2.5 V, whichever is greater.
(2) I_{SET} and I_{LIM} are not included.
(3) Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. Dropout voltage is measured for output ≥ 2 V. In dropout, the output voltage is equal to: V_{IN} – $V_{DROPOUT}$.

Typical Performance Characteristics

All test conditions: V_{IN} = $V_{OUT(NOM)}$ + 1 V or 2.5 V, whichever is greater; OUTS ties directly to OUT, C_{IN} = C_{OUT} = 4.7 µF, C_{SET} = 4.7 µF, $V_{EN/UV}$ = 5 V, I_{OUT} = 1 mA, −40°C ≤ T_J ≤ +125°C, unless otherwise noted.



$V_{EN/UV}$ = 0 V

Figure 1. Shutdown Current

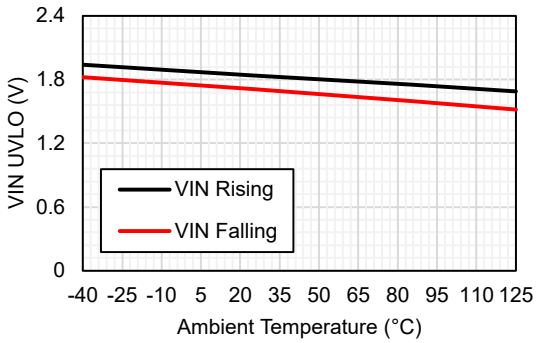


Figure 2. Supply Voltage UVLO

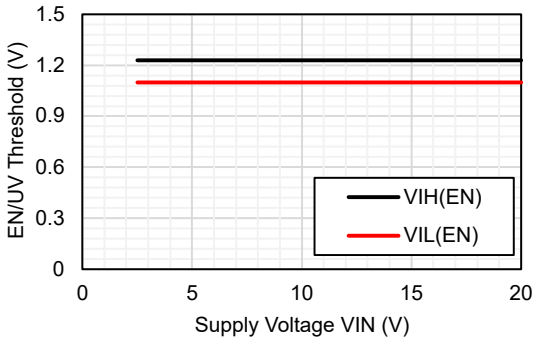
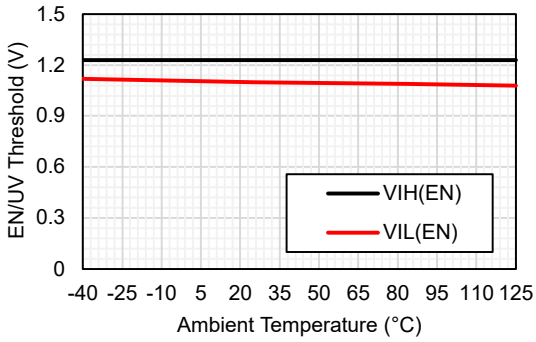
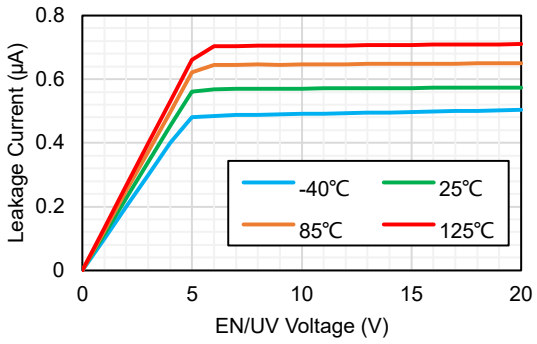


Figure 3. EN/UV Threshold



V_{IN} = 2.5 V

Figure 4. EN/UV Threshold vs Temperature



$V_{EN/UV}$ = V_{IN}

Figure 5. EN/UV Leakage Current

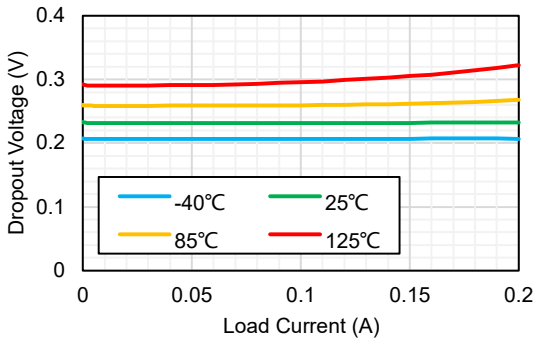
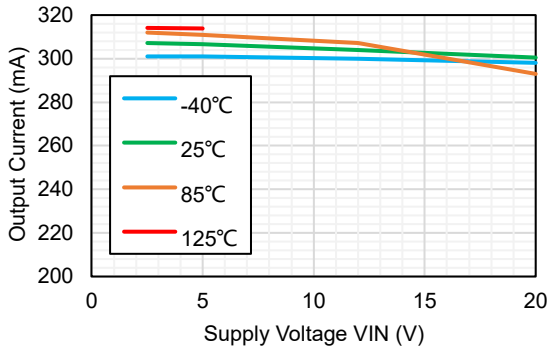
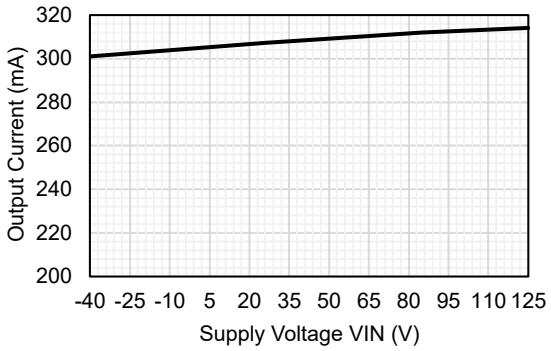


Figure 6. Dropout Voltage



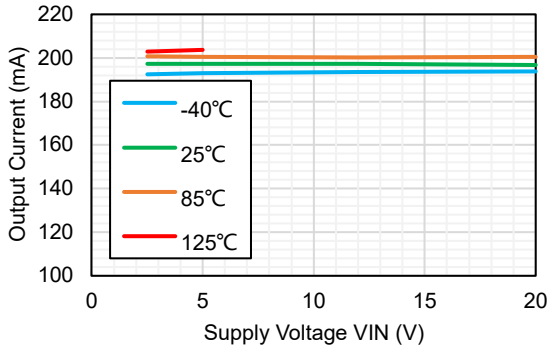
R_{ILIM} = 0

Figure 7. Current Limit



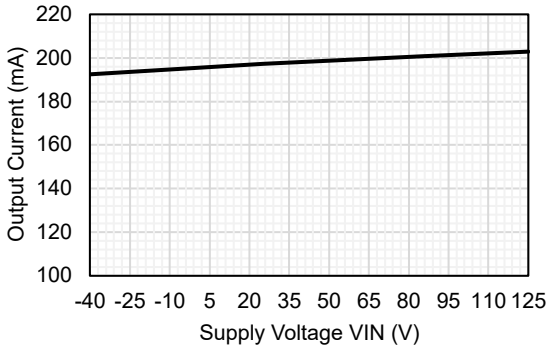
R_{ILIM} = 0

Figure 8. Current Limit vs Temperature



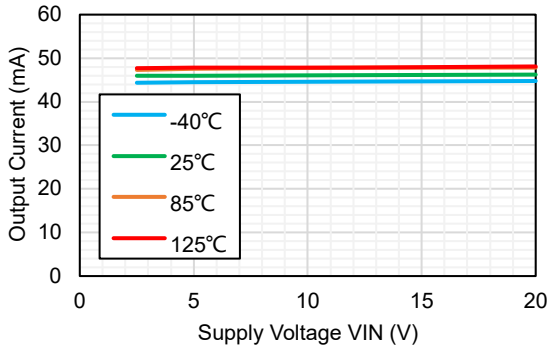
R_{ILIM} = 620 Ω

Figure 9. Current Limit



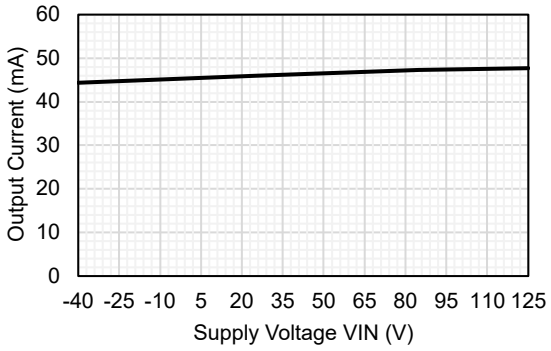
R_{ILIM} = 620 Ω

Figure 10. Current Limit vs Temperature



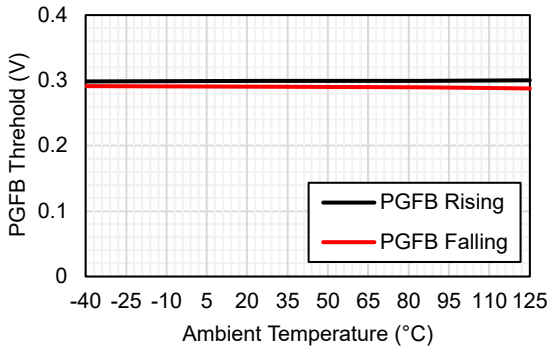
R_{ILIM} = 2.5 kΩ

Figure 11. Current Limit



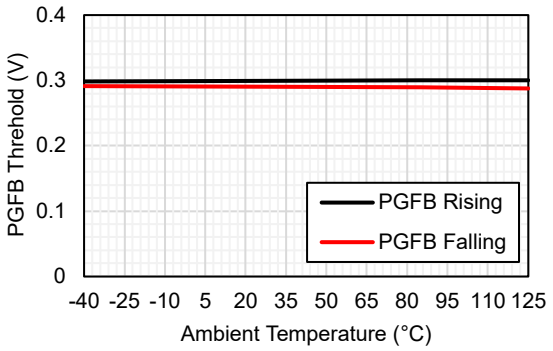
R_{ILIM} = 2.5 kΩ

Figure 12. Current Limit vs Temperature



V_{IN} = 2.5 V

Figure 13. PGFB Threshold



V_{IN} = 20 V

Figure 14. PGFB Threshold

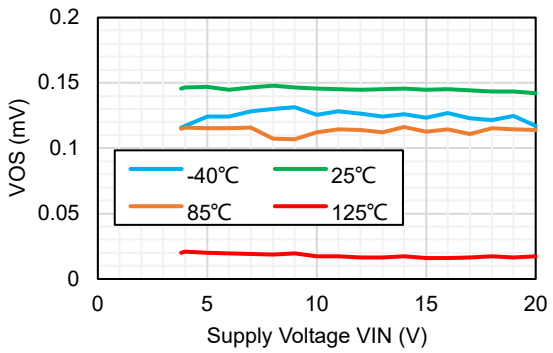
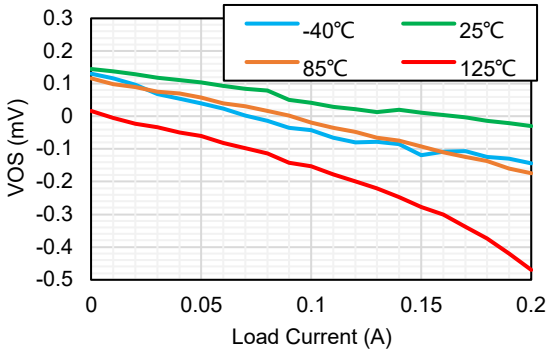


Figure 15. VOS Line Regulation



V_{IN} = 4.3 V

Figure 16. VOS Load Regulation

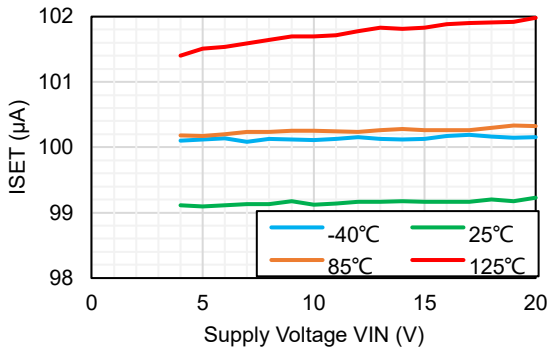


Figure 17. ISET Line Regulation

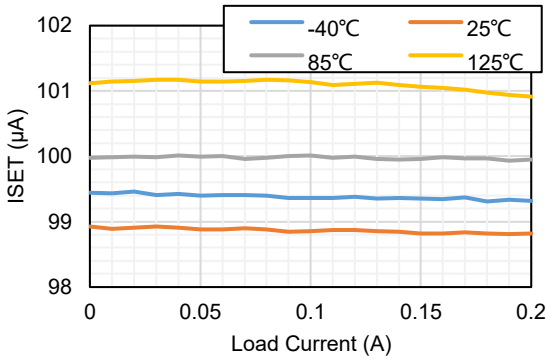
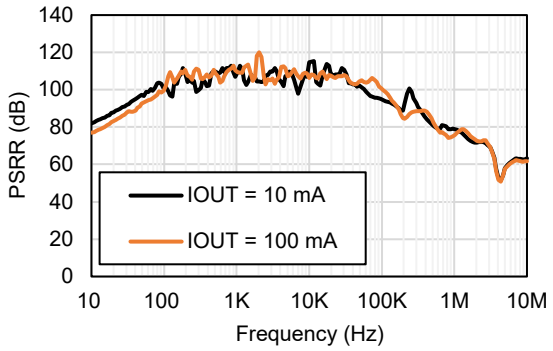
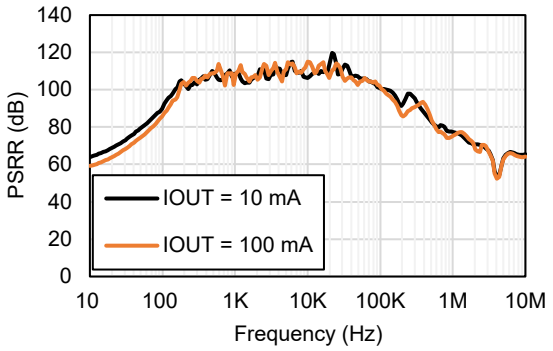


Figure 18. ISET Load Regulation



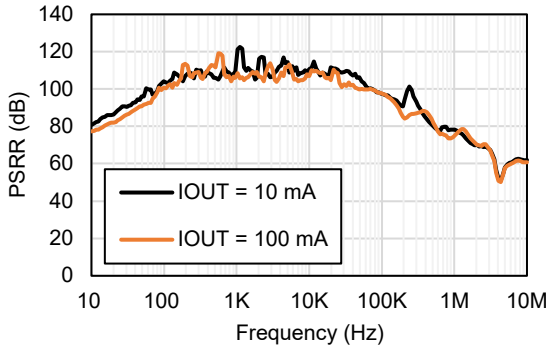
V_{IN} = 5.3 V, V_{OUT} = 3.3 V, C_{SET} = 4.7 µF

Figure 19. PSRR



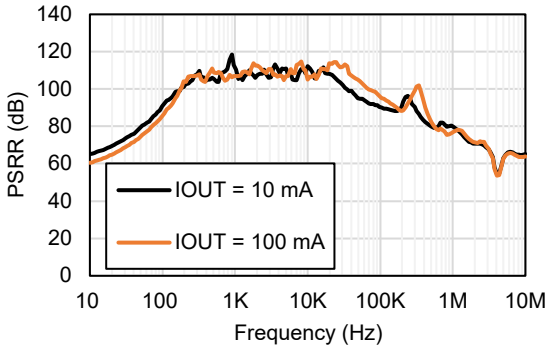
V_{IN} = 5.3 V, V_{OUT} = 3.3 V, C_{SET} = 0.47 µF

Figure 20. PSRR



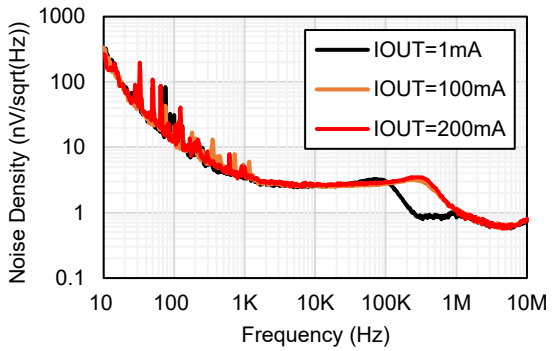
V_{IN} = 5 V, V_{OUT} = 3.3 V, C_{SET} = 4.7 µF

Figure 21. PSRR



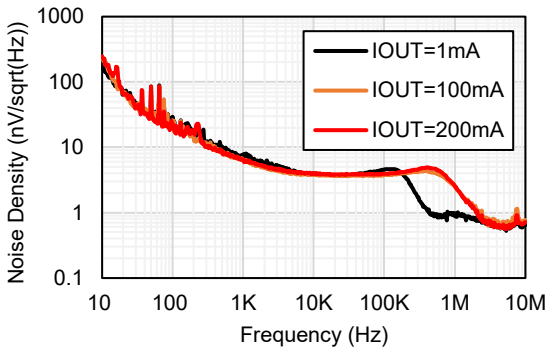
V_{IN} = 5 V, V_{OUT} = 3.3 V, C_{SET} = 0.47 µF

Figure 22. PSRR



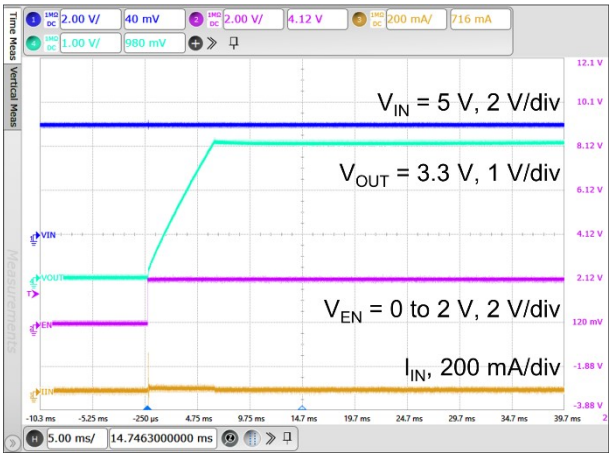
V_{IN} = 5 V, V_{OUT} = 3.3 V, C_{SET} = 4.7 µF

Figure 23. Noise



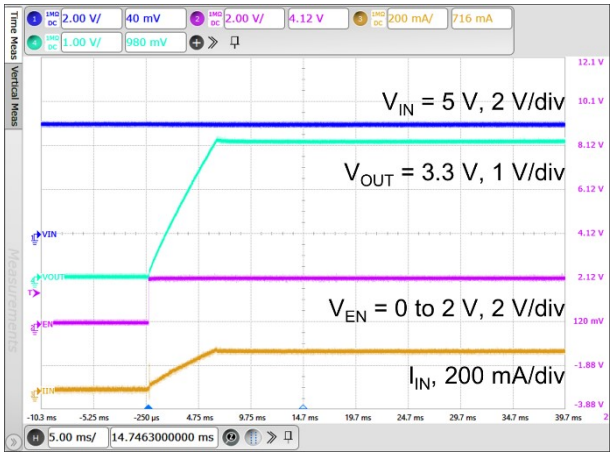
V_{IN} = 2.5 V, V_{OUT} = 1.2 V, C_{SET} = 4.7 µF

Figure 24. Noise



I_{OUT} = 0

Figure 25. EN/UV Startup

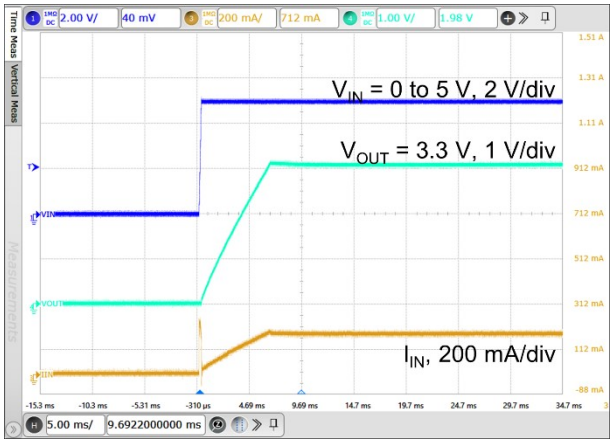


I_{OUT} = 200 mA

Figure 26. EN/UV Startup

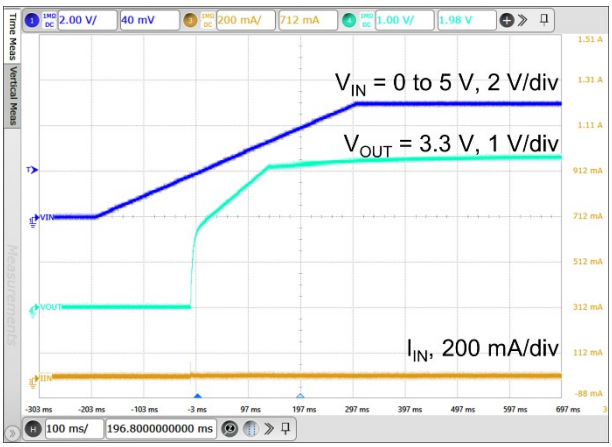
V_{IN} starts in 100 µs,I_{OUT} = 0

Figure 27. VIN Startup



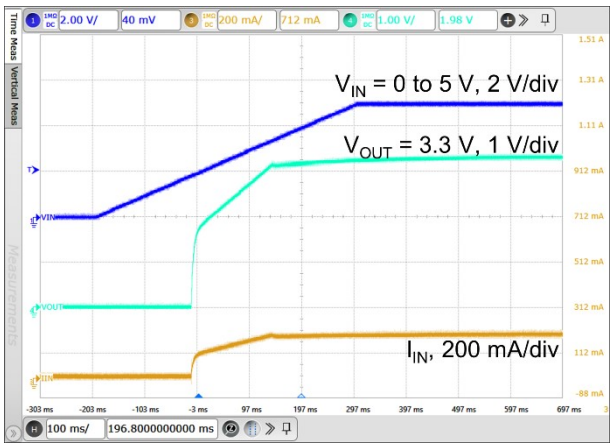
V_{IN} starts in 100 µs, I_{OUT} = 200 mA

Figure 28. VIN Startup



V_{IN} starts in 500 ms, I_{OUT} = 0

Figure 29. VIN Startup



V_{IN} starts in 500 ms, I_{OUT} = 200mA

Figure 30. VIN Startup

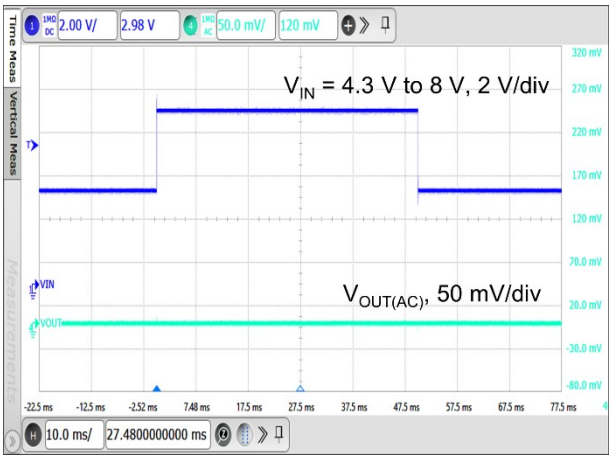


Figure 31. Line Transient

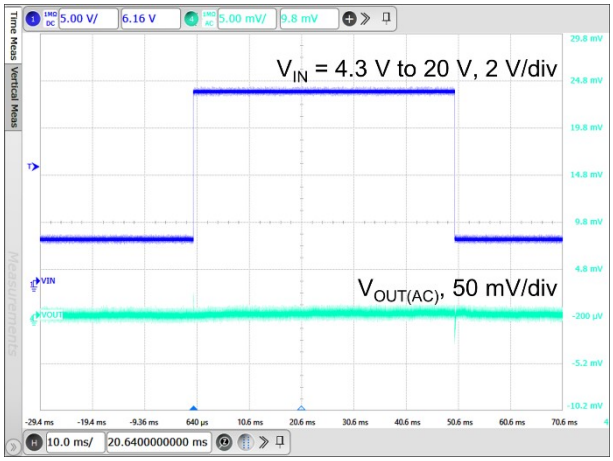


Figure 32. Line Transient

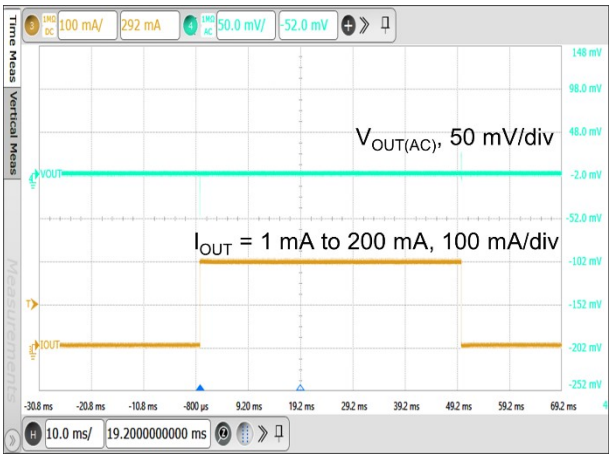


Figure 33. Load Transient

Detailed Description

Overview

The TPL8033 is a 20-V 200-mA high-performance low-dropout linear regulator with 1-μV_{RMS} ultra-low noise and 110-dB ultra-high PSRR. The TPL8033 support adjustable output from 1.2 V to 15 V with a single resistor and is stable with 4.7 µF to 100 µF.

The TPL8033 implements a precision current reference and a high-performance voltage buffer. With an external capacitor connecting to the current reference, the output voltage noise can be further reduced.

The TPL8033 features adjustable output current limit with a single external resistor and adjustable power-good threshold with an external resistors divider. The TPL8033 also integrates over-current protection and over-temperature protection to enhance system reliability.

Functional Block Diagram

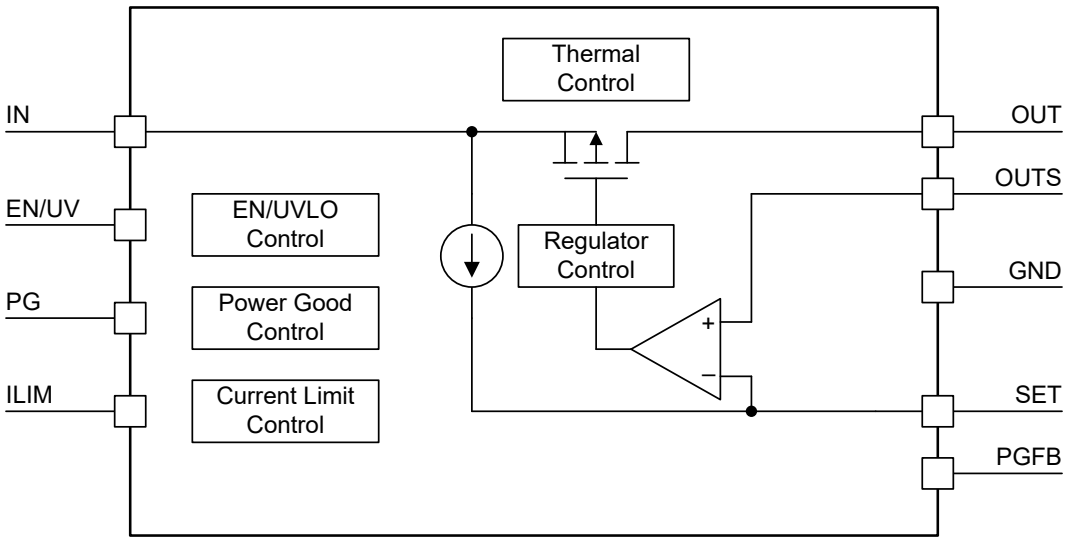


Figure 34. Functional Block Diagram

Feature Description

Enable/UVLO (EN/UV)

The TPL8033 integrates an EN/UV pin to turn on or turn off the device. This pin has an accurate 1.23-V turn-on threshold with 120-mV hysteresis. This EN/UV threshold can be used to set an accurate under-voltage lockout (UVLO) threshold of the input voltage with a resisitor divider connected from V_{IN} to GND. The UVLO threshold can be calculated according to Equation 1.

$$V_{IN,\,UVLO} = 1.23V \times \left(1 + \frac{R_{EN2}}{R_{EN1}}\right) + I_{EN} \times R_{EN2} \quad (1)$$

where,

- R_{EN1} is the low-side resistor connected from the EN/UV pin to the GND pin.
- R_{EN2} is the high-side resistor connected from the IN pin to the EN/UV pin.
- I_{EN} is the EN/UV pin current. This current can be neglected if the R_{EN1} is less than 100 kΩ.

If accurate UVLO is not used, connect EN/UV pin to VIN directly or a digital logic control circuit.

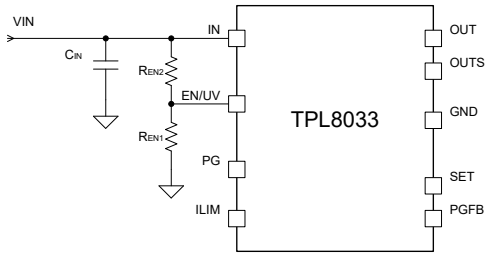


Figure 35. UVLO Threshold

Adjustable Output Voltage (SET, OUT, OUTS)

The TPL8033 integrates a precision 100-μA current source flowing out of the SET pin. The output voltage can be set by connecting an external resistor (R_{SET}) and capacitor (C_{SET}) at this SET pin. Below table provides different output voltage options with corresponding external resistors.

The OUTS pin of the TPL8033 provides a Kelvin sense connction to the output. The ground side of the resistor at the SET pin provides a Kelvin sense connection to the ground side of the load.

Table 2. Output Voltage and R_{SET} Resistors

V_{OUT} (V)	RSET (kΩ)
2.5	24.9
3.3	33.2
5	49.9
12	121
15	150

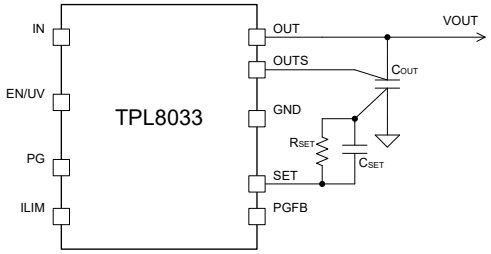


Figure 36. OUTS Pin Kelvin Sense Connction

Power Good (PG)

The TPL8033 integrates an open-drain output power good indicator. Connect the PG pin to a pull-up voltage through a resistor from 10 kΩ to 100 kΩ if the power good function is used. Left the PG pin open if it is not used.

After regulator startup, the PG pin keeps low impendence until the output voltage reaches the power good threshold, $V_{PG,TH}$. When the output voltage is higher than $V_{PG,TH}$, the PG pin turns to high output impedance, and PG is pulled up to a high voltage level to indicate the output voltage is ready.

Please note, the power good function is disabled in shutdown mode.

Adjustable Power Good Threshold (PGFB)

The TPL8033 integrates an adjustable power-good threshold, of which the value can be set by a external resistor divider. Use Equation 2 to calculate the power good threshold.

$$V_{PG,TH} = 0.3V \times \left(1 + \frac{R_{PG2}}{R_{PG1}}\right) + I_{PGFB} \times R_{PG2} \quad (2)$$

where,

- R_{PG1} is the low-side resistor connected from the PGFB pin to the GND pin.
- R_{PG2} is the high-side resistor connected from the OUT pin to the PGFB pin.
- I_{PGFB} is the PGFB pin curret. This current can be neglected if the R_{PG1} is less than 30 kΩ.

Please note, the adjustable power good function is disabled in shutdown mode.

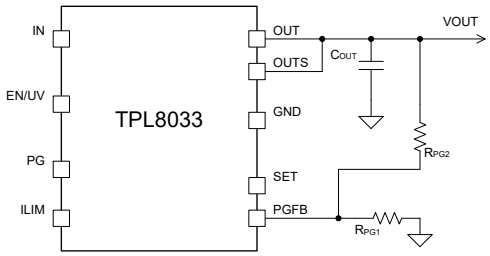


Figure 37. Power Good Threshold

Over-Current Protection(ILIM)

The TPL8033 integrates a current limit circuit that helps to protect the device during fault conditions. The default current limit value is typically 320 mA, and the TPL8033 also provides an adjustable option set by an external resistor R_{ILIM}. Use Equation 3 to calculate the adjustable current limit value.

Current (3)

For example:

- when R_{LIM} = 2.5 kΩ, the output current limit is set to 50 mA.
- when R_{LIM} = 625 Ω, the output current limit is set to 200 mA.

Over-Temperature Protection

The over-temperature protection starts to work when the junction temperature exceeds the thermal shutdown threshold, which turns off the regulator immediately. Until when the device cools down and the junction temperature falls below a value which equals to the thermal shutdown threshold minus thermal shutdown hysteresis, the regulator turns on again.

The junction temperature range should be limited according to the Recommended Operating Conditions table, continuously operating above the junction temperature range reduces the device lifetime.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPL8033 is a 20-V 200-mA high-performance low-dropout linear regulator with 1-μV_{RMS} ultra-low noise and 110-dB ultra-high PSRR.

Typical Application

The Figure 38 shows the typical application schematic.

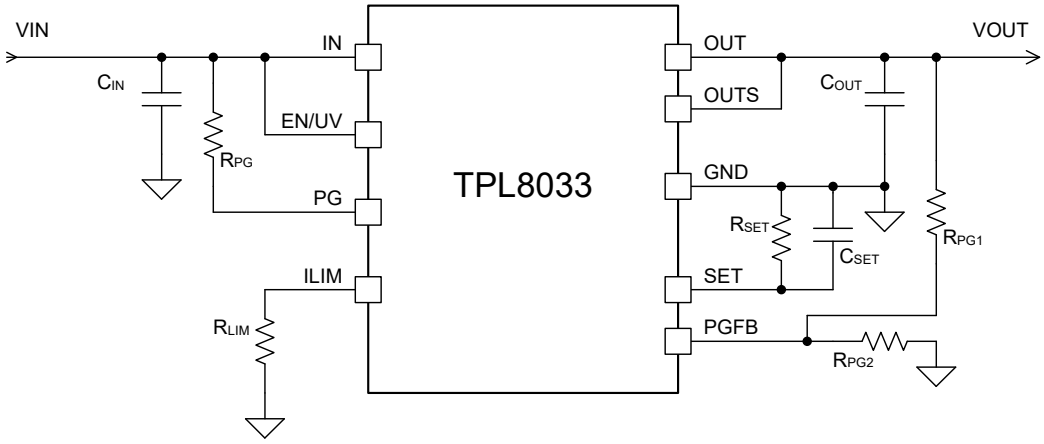


Figure 38. Typical Application Circuit

Input Capacitor and Output Capacitor

3PEAK recommends adding a 10-µF or greater capacitor at the IN pin to keep the input voltage stable. The voltage rating of the capacitors must be higher than the maximum input voltage.

To ensure the loop stability, the TPL8033 requires a ceramic capacitor from 4.7 µF to 100 µF at the regulator output. 3PEAK recommends selecting a 10-µF or greater X7R ceramic capacitor with low ESR range at the OUT pin.

Both input capacitors and output capacitors must be placed as close to the device pins as possible.

Power Dissipation and Thermal Consideration

During the normal operation, the LDO junction temperature should meet the requirement in the Recommended Operating Conditions table. Use the equations below to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using below equation.

$$P_D = (V_{IN} - V_{BAT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (4)$$

The junction temperature can be estimated using below equation. θ_{JA} is the junction-to-ambient thermal resistance.

$$T_J = T_A + P_D \times \theta_{JA} \quad (5)$$

Layout

Layout Guideline

- Both input capacitors and output capacitors must be placed as close to the device pins as possible.
- It is recommended to bypass the IN pin to ground with a 10-μF capacitor in parallel with a 0.1-μF small ceramic capacitor. The loop area formed by the bypass capacitor connection, the IN pin, and the GND pin of the system must be as small as possible.
- It is required to place a decoupling 4.7-μF or greater capacitor at the output. A small 0.1-μF ceramic capacitor in parallel is recommended to filter the noise and improve the output transient performance.
- It is recommended to use wide and thick trace to minimize I×R drop and heat dissipation.

Layout Example

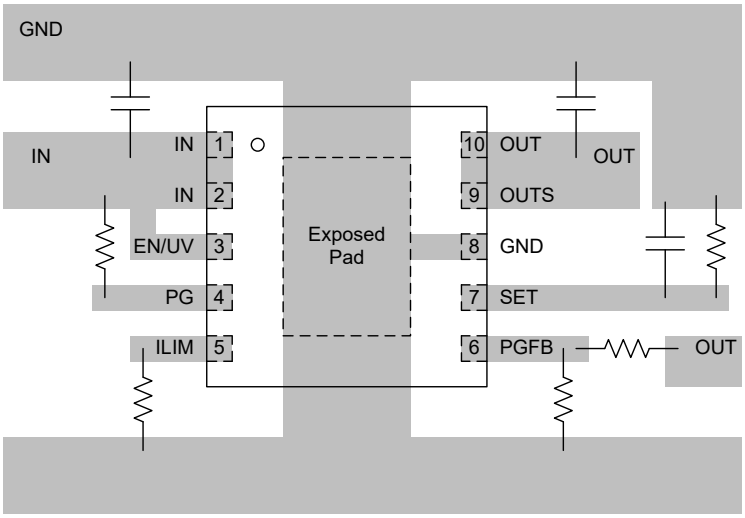
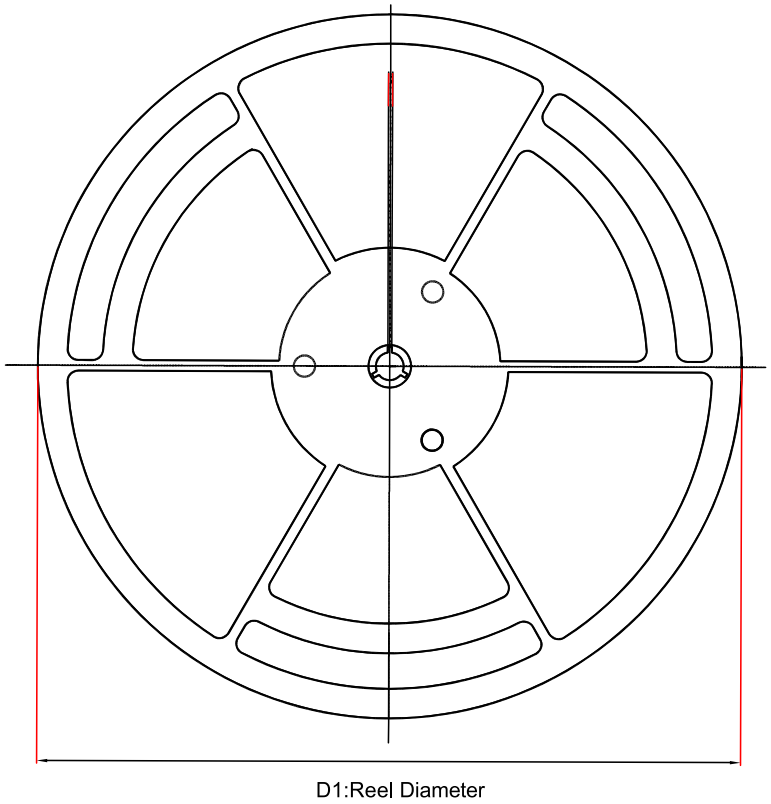
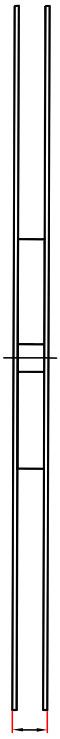
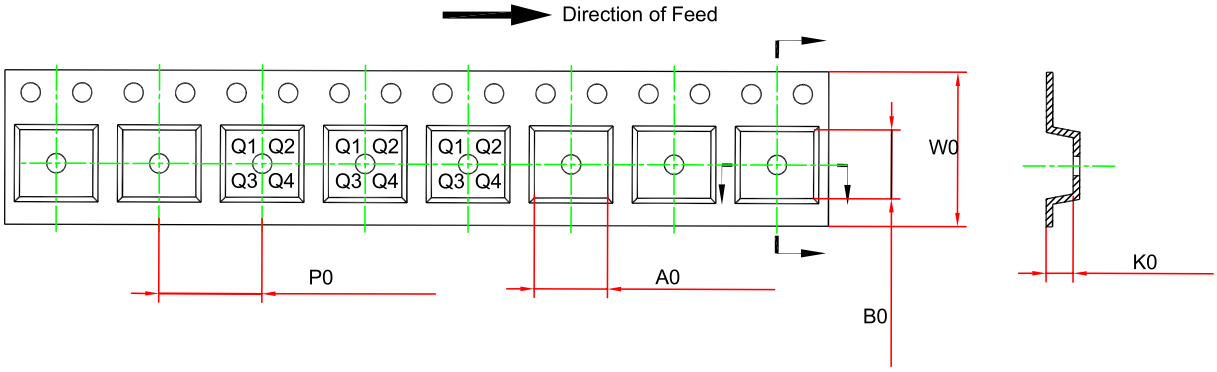


Figure 39. Layout Example

Tape and Reel Information





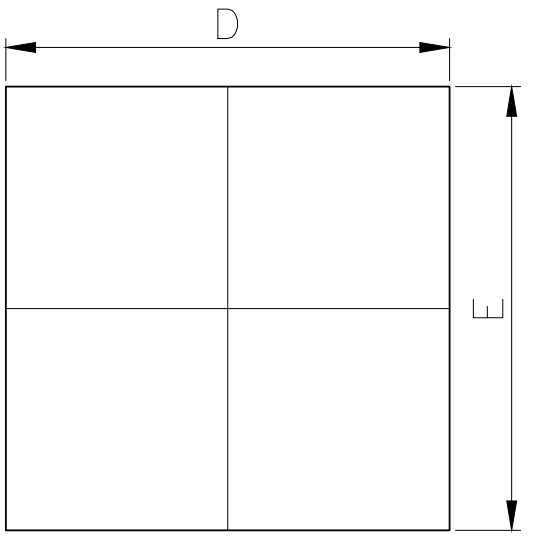


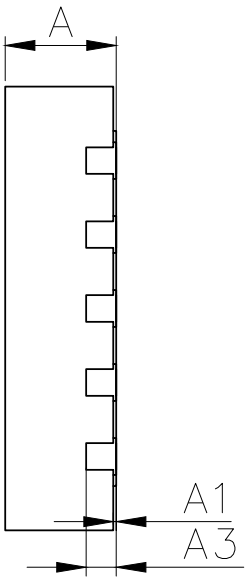
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPL8033AD-DF8R	DFN3X3-10	330	17.6	3.3	3.3	1.1	8	12	Q1

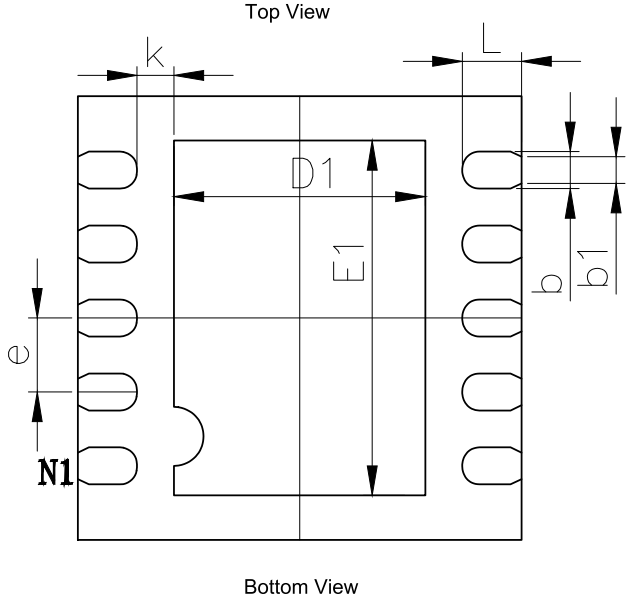
Package Outline Dimensions

DFN3X3-10

Package Outline Dimensions DF8(DFN3X3-10-A)







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.200	0.300	0.008	0.012
b1	0.180 REF		0.007 REF	
A3	0.150	0.250	0.006	0.010
D	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E	2.900	3.100	0.114	0.122
E1	2.300	2.500	0.091	0.098
e	0.500 BSC		0.020 BSC	
L	0.325	0.475	0.013	0.019

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPL8033AD-DF8R	−40°C to +125°C	DFN3X3-10	L83A	MSL3	4,000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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