350-nA Ultra Low Quiescent Current, 300-mA Linear Regulator

Features

- Typical 350-nA Ultra-low Quiescent Current
- Input Voltage Range: 2.05 V to 5.5 V
- Output Voltage Options:
  - Fixed: 3.3 V
- ±1.5% Output Accuracy through Operating Conditions
- Maximum Output Current: 300 mA
- Low Shutdown Current
- Low Dropout Voltage: 400 mV typ @ 200mA
- Current Limit and Thermal Protection
- Stable with 1 µF to 22 µF Ceramic Capacitor
- Active Output Discharge while Disable
- Soft-start Limits Input Current Surge During Enable
- Junction Temperature Range: −40°C to +125°C
- Packages: SOT23-5 and DFN1x1-4

Applications

- Handheld Devices with Battery Power Supply
- Portable Devices with Battery Power Supply
- Wearable Applications, Bluetooth Headsets
- Wireless and IoT Modules
- Personal Electronics, Personal Healthcare

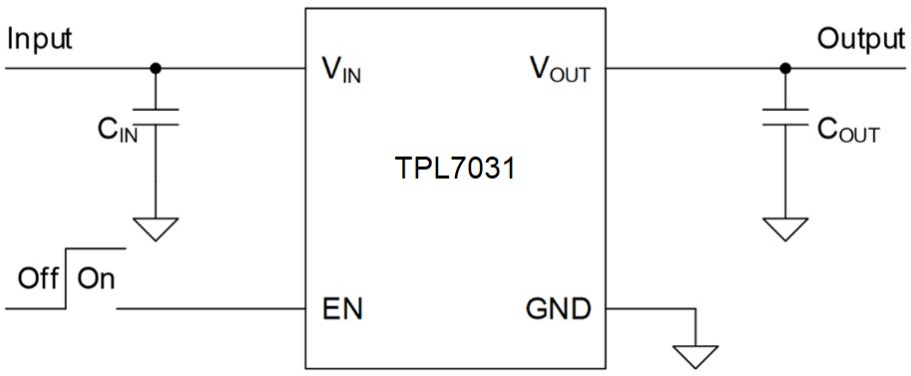
Description

The TPL703133 is an ultra-low quiescent current low-dropout linear regulator (LDO) that can source 300 mA with excellent transient performance.

The TPL703133, with an ultra-low typical IQ of 350 nA, is designed specifically for applications where very-low quiescent current is a critical parameter. When in shutdown or disabled mode, the device consumes ultra-low Current that helps increase the shelf life of the battery.

The TPL703133 has Current-limit and thermal overload protection which improves the reliability under heavy load conditions. The TPL703133 series is fully specified for T_J = –40°C to +125°C operation.

Typical Application Schematic



TPL703133 Series

Table of Contents

Product Family Table

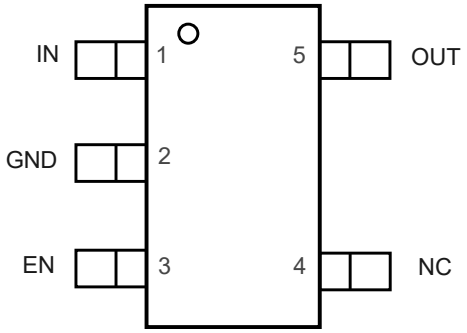
Order Number	Output Voltage (V)	Package
TPL703133-S5TR	Fixed 3.3 V	SOT23-5
TPL703133-DF1R	Fixed 3.3 V	DFN1x1-4

Revision History

Date	Revision	Notes
2025-08-15	Rev.A.0	Released Version

Pin Configuration and Functions

TPL703133
SOT23-5 Package
Top View



TPL703133
DFN1X1-4 Package
Top View

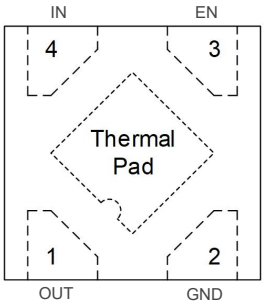


Table 1. Pin Functions: TPL703133

Pin Number		Name	I/O	Description
SOT23-5	DFN1X1-4			
3	3	EN	I	Regulator enable pin. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to IN directly.
2	2	GND	–	Ground reference pin. Connect the GND pin to the PCB ground plane directly.
1	4	IN	I	Input voltage pin. Bypass IN to GND with a 1 μF or greater capacitor.
4	–	NC	–	No connection.
5	1	OUT	O	Regulated output voltage pin. Bypass OUT to GND with a 1 μF or greater capacitor.

(1) Thermal pad must be connected to the PCB ground plane to maximize the thermal performance.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
V_{IN}, V_{EN}	Input Voltage	−0.3	6	V
V_{OUT}	Output Voltage	−0.3	6	V
T_J	Junction Temperature Range	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime
(2) All voltage values are with respect to GND.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
V_{IN}	Input Voltage	2.05	5.5	V
V_{EN}	Enable Voltage	0	V_{IN}	V
V_{OUT}	Output Voltage	0	5	V
I_{OUT}	Output Current	0	300	mA
T_J	Operating Junction Temperature Range	−40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOT23-5	280	62	°C/W
DFN1x1-4	210	110	°C/W

Electrical Characteristics

All test conditions: V_{IN} = $V_{OUT\ (NOM)}$ + 0.5 V, C_{OUT} = 1 µF, T_J = –40°C to 125°C, all typical values are at T_J = 25°C, unless otherwise noted.

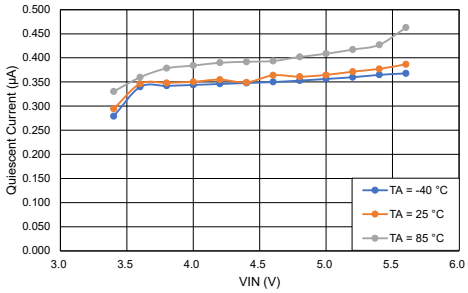
Parameter		Conditions	Min	Typ	Max	Unit
Supply Voltage and Current						
V_{IN}	Input Voltage Range		2.05		5.5	V
I_{GND}	Ground Pin Current	I_{OUT} = 0 mA, –40°C ≤ T_J ≤ +85°C		350	550	nA
		I_{OUT} = 1 mA, –40°C ≤ T_J ≤ +85°C		0.6	2	µA
		I_{OUT} = 100 mA –40°C ≤ T_J ≤ +85°C		40	100	µA
I_{SHDN}	Shutdown Current	EN = GND, T_A = +25°C		2		nA
UVLO	V_{IN} Under-Voltage Lock-out	V_{IN} Rising		1.95	2.05	V
		Hysteresis		70		mV
Enable Input Voltage and Current						
$V_{IH\ (EN)}$	EN Logic-input High Level		1.1		V_{IN}	V
$V_{IL\ (EN)}$	EN Logic-input Low Level		0		0.3	V
I_{EN}	EN Pin Leakage Current	EN = 5 V		0.5	50	nA
Regulated Output Voltage and Current						
V_{OUT}	Output Voltage Accuracy	I_{OUT} = 1 mA	–1.5%		1.5%	
ΔVOUT	Line Regulation	V_{IN} = $V_{OUT\ (NOM)}$ + 0.5 V to 5.5 V, I_{OUT} = 60 mA			5	mV
	Load Regulation	I_{OUT} = 1 mA to 300 mA		40	50	mV
V_{DO}[1]	Dropout Voltage	V_{IN} = 0.98 × $V_{OUT\ (NOM)}$, I_{OUT} = 200 mA			310	mV
I_{OUT}	Output Current	V_{OUT} in Regulation	0		300	mA
I_{CL}	Output Current Limit	V_{OUT} = 0.9 × $V_{OUT\ (NOM)}$	301		900	mA
R_{DIS}	Output Discharge Resistance	V_{IN} = $V_{OUT\ (NOM)}$ + 1 V, EN = GND		280		Ω
PSRR	Power Supply Rejection Ratio	I_{OUT} = 30 mA, f = 1k Hz, C_{OUT} = 1 µF		55		dB
V_N	Output Noise Voltage	I_{OUT} = 1 mA, V_{OUT} = 3.3 V, BW = 10Hz to 100 kHz		150		μV_{RMS}

Parameter		Conditions	Min	Typ	Max	Unit
T_{STR}	Start-up Time from EN Assertion to 0.98 × $V_{OUT\ (NOM)}$	I_{OUT}= 1 mA, C_{OUT} = 1 µF		1		ms
Temperature Range						
T_{SD}	Thermal Shutdown Temperature			155		ºC
	Thermal Shutdown Hysteresis			15		ºC

(1) Dropout voltage is the minimum input-to-output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage will be equal to $V_{IN} – V_{DROPOUT}$.

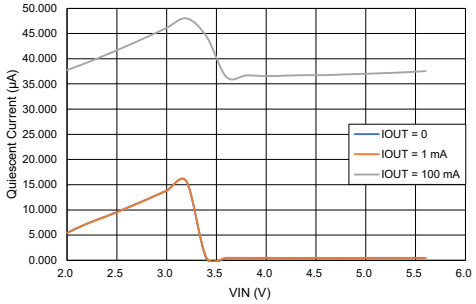
Typical Performance Characteristics

All test conditions: V_{IN} = $V_{OUT\ (NOM)}$ + 1 V or 2.4 V, whichever is greater; C_{OUT} = 2.2 µF, T_A = +25°C, unless otherwise noted.



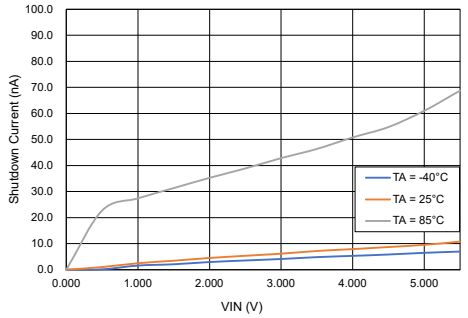
V_{OUT} = 3.3 V, I_{OUT} = 0

Figure 1. Ground Current vs. Input Voltage



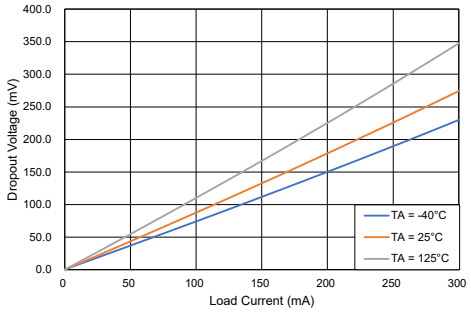
V_{OUT} = 3.3 V, T_A = 25°C

Figure 2. Ground Current vs. Input Voltage



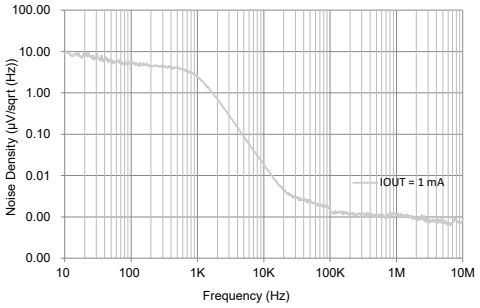
V_{OUT} = 3.3 V

Figure 3. Shutdown Current vs. Input Voltage



V_{OUT} = 3.3 V

Figure 4. Dropout Voltage vs. Output Current



V_{OUT} = 3.3 V

Figure 5. Noise

Detailed Description

Overview

The TPL703133 is an ultra-low quiescent current low-dropout linear regulator (LDO) that can source 300 mA with excellent transient performance.

The TPL703133, with an ultra-low typical IQ of 350 nA, is designed specifically for applications where very-low quiescent current is a critical parameter. When in shutdown or disabled mode, the device consumes ultra-low Current that helps increase the shelf life of the battery.

The TPL703133 has Current-limit and thermal overload protection which improves the reliability under heavy load conditions. The TPL703133 series is fully specified for T_J = –40°C to +125°C operation.

Functional Block Diagram

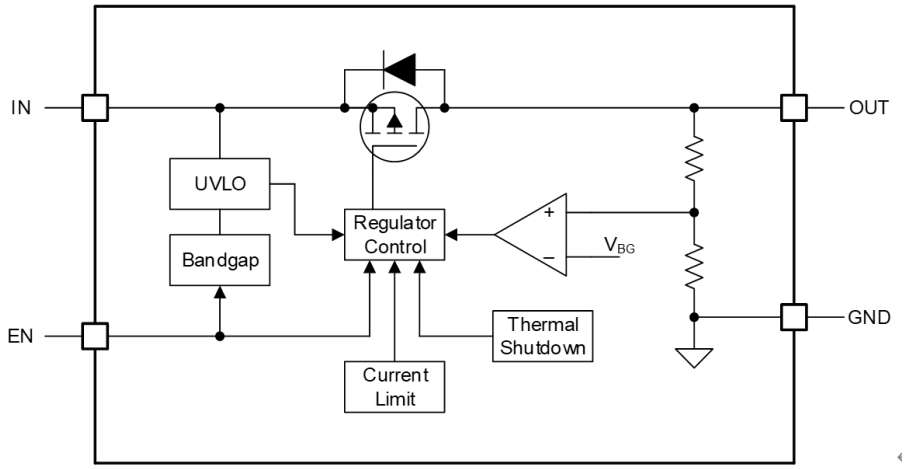


Figure 6. TPL703133 Series

Feature Description

Enable

The enable pin (EN) is active high. Connect this pin to the GPIO of an external processor or digital logic control circuit to enable and disable the device, or connect this pin to the IN pin for self-bias applications.

Under-voltage Lockout (UVLO)

The TPL703133 series uses an under-voltage lockout circuit (UVLO = 1.95 V) to keep the output shut off until the internal circuitry operates properly.

Regulated Output Voltage

The TPL703133 series is available in fixed voltage versions. When the input voltage is higher than $V_{OUT\ (NOM)}$ + V_{DO}, the output pin is the regulated output based on the selected voltage version. When the input voltage falls below $V_{OUT\ (NOM)}$ + V_{DO}, the output pin tracks the input voltage minus the dropout voltage based on the load current. When the input voltage drops below the UVLO threshold, the output keeps shut off.

Current Limit

The TPL703133 series integrates an internal current limit that helps to protect the regulator during fault conditions. Output voltage is not regulated when the device is in current limit mode, and VOUT equals $I_{CL} \times R_{LOAD}$.

Short-Circuit Protection

The TPL703133 series integrates a short-circuit protection. When the output pin is shorted to ground or forced to a voltage below 0.2 V, the output current of the TPL703133 series is limited to a typical value of 200 mA.

Thermal Shutdown

During normal operation, the LDO junction temperature should not exceed 125°C. When the junction temperature exceeds the thermal shutdown threshold, the LDO shuts down the output immediately. Until the junction temperature falls below the thermal shutdown threshold minus thermal shutdown hysteresis, the output turns on again.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPL703133 is a series of 300 mA low-dropout linear regulators with ultra-low quiescent current. The following application schematic shows a typical usage of the TPL703133 series.

Typical Application

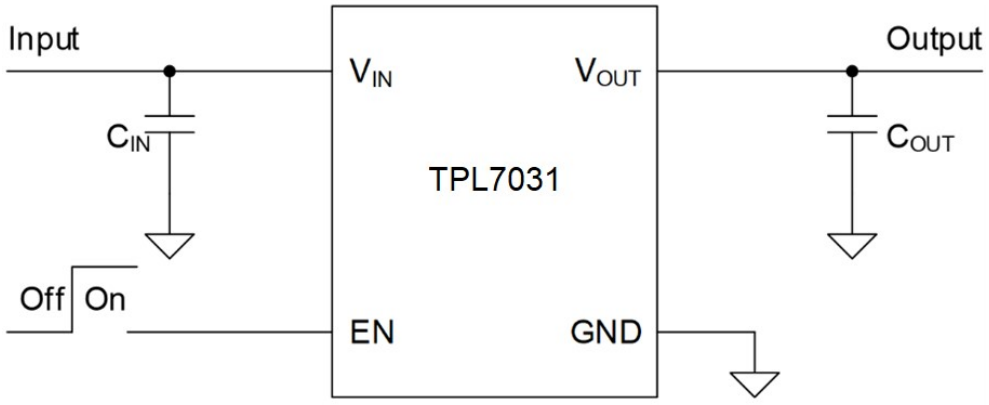


Figure 7. TPL703133 Series Application Schematic

Input Capacitor and Output Capacitor

3PEAK recommends adding a 1 μF or greater capacitor with a 0.1-μF bypass capacitor in parallel at the IN pin to keep the input voltage stable. The voltage rating of the capacitors must be greater than the maximum input voltage.

To ensure loop stability, the TPL703133 series requires an output capacitor with a capacitance value of from 1 μF to 22 μF. 3PEAK recommends selecting an X5R- or X7R-type ceramic capacitor with low ESR over temperature. A larger output capacitor is recommended to get better transient response.

Both input capacitors and output capacitors must be placed as close to the device pins as possible.

Power Dissipation

During normal operation, the LDO junction temperature should not exceed 125°C. Use the equations below to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using Equation 1.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (1)$$

The junction temperature can be estimated using Equation 2. θ_{JA} is the junction-to-ambient thermal resistance (See Section *Thermal Information*).

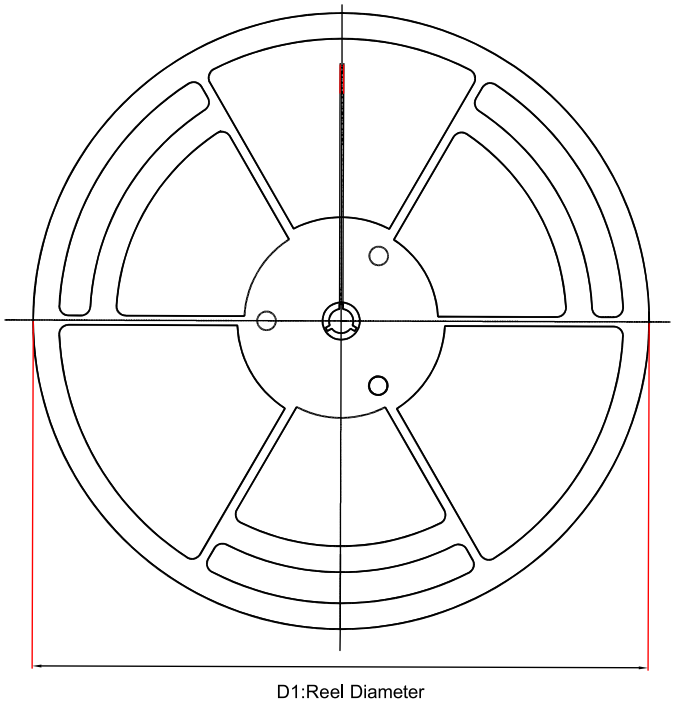
$$I_J = I_A + P_D \times \theta_{JA} \quad (2)$$

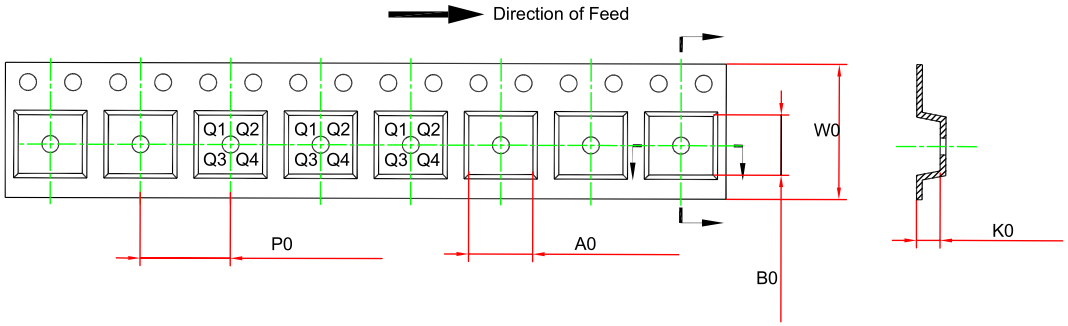
Layout

Layout Guideline

- Both input and output capacitors must be placed as close to the device pins as possible.
- It is recommended to bypass the input pin to the ground with a 0.1-μF bypass capacitor. The loop area formed by the bypass capacitor connection, the IN pin, and the GND pin of the system must be as small as possible.
- It is recommended to use wide and thick copper to minimize I×R drop and heat dissipation.

Tape and Reel Information



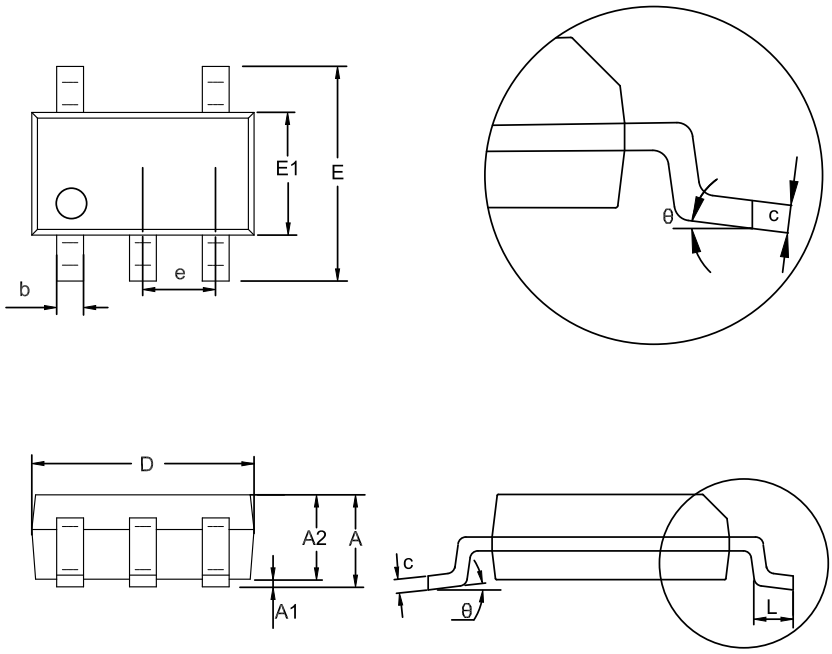


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPL703133-S5TR	SOT23-5	180	12	3.3	3.25	1.4	4	8	Q3
TPL703133-DF1R	DFN1x1-4	180	12.5	1.16	1.16	0.5	2	8	Q1

Package Outline Dimensions

SOT23-5

Package Outline Dimensions S5T(SOT23-5-A)



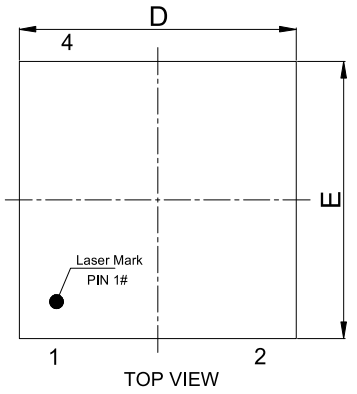
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.280	0.500	0.011	0.020
c	0.100	0.230	0.004	0.009
D	2.820	3.020	0.111	0.119
E	2.600	3.000	0.102	0.118
E1	1.500	1.720	0.059	0.068
e	0.950 BSC		0.037 BSC	
L	0.300	0.600	0.012	0.024
θ	0	8°	0	8°

NOTES

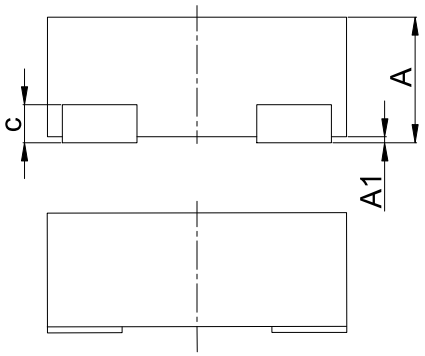
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

DFN1X1-4

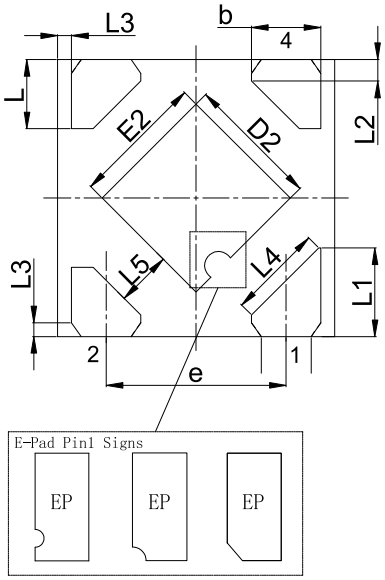
Package Outline Dimensions DF1(DFN1X1-4-A)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.350	0.400	0.014	0.016
A1	0.000	0.050	0.000	0.002
b	0.200	0.300	0.008	0.012
c	0.070	0.170	0.003	0.007
D	0.950	1.050	0.037	0.041
D2	0.430	0.530	0.017	0.021
E	0.950	1.050	0.037	0.041
E2	0.430	0.530	0.017	0.021
e	0.650 BSC		0.026 BSC	
L	0.200	0.300	0.008	0.012
L1	0.270	0.370	0.011	0.015
L2	0.077 BSC		0.003 BSC	
L3	0.050 BSC		0.002 BSC	
L4	0.340 BSC		0.013 BSC	
L5	0.200 BSC		0.008 BSC	

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Junction Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPL703133-S5TR	−40 to 125°C	SOT23-5	LQH	MSL3	Tape and Reel, 3,000	Green
TPL703133-DF1R	−40 to 125°C	DFN1x1-4	LQH	MSL3	Tape and Reel, 12,000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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