2-A Sink and Source DDR Termination Regulator

Features

- V_{IN} Voltage Range: 3 V to 5.5 V
- V_{LDOIN} Voltage Range: 1 V to 3.5 V
- V_{OUT} Minimum Output Voltage: 0.5 V
- Input Voltage Tracking from ½ × REFIN
- 2-A Sink and Source Current Capability for DDR Termination
- Integrated Power MOSFETs
- Output Remote Sensing
- Fast Load-Transient Response
- Built-in Soft-Start and UVLO, Current Limit, and Thermal Shutdown Protection
- Support DDR, DDR2, DDR3, DDR3L, Low Power DDR3, and DDR4 VTT Power Supply Applications
- Operating Temperature Range: –40°C to +125°C
- Small Package with DFN2×2-10
- Pb−Free and RoHS Compliant

Applications

- Memory VTT Regulator for DDR, DDR2, DDR3, DDR3L, Low Power DDR3, and DDR4
- Notebooks, Desktops, and Workstations
- Servers, Networking Equipment, and Datacenters
- Telecom and Base Station

Description

With the development of main processors in PCs and servers, more and more source double-data-rate (DDR) memories are required in the mainboard, where the input voltage becomes lower and lower, and the space limitation becomes higher and higher.

The TPL51206 is a series of 2-A sink and source DDR termination regulators specifically designed for DDR applications with heavy space limitations. The TPL51206 series of devices implements a fast load-transient response and only requires a minimum output capacitance of 10 µF.

The TPL51206 series supports a remote-sensing function and all power requirements for DDR VTT bus termination. In addition, the TPL51206 series provides S3 and S5 control pins which can be used to control the power state in DDR applications, setting OUT to high-impedance in the S3 state (suspend to RAM) and discharging OUT and REFOUT in S4 or S5 state (suspend to disk).

The TPL51206 series is available in the thermally efficient DFN2×2-10 package with the thermal pad and supports the operating temperature range from −40°C to +125°C.

Typical Application Circuit

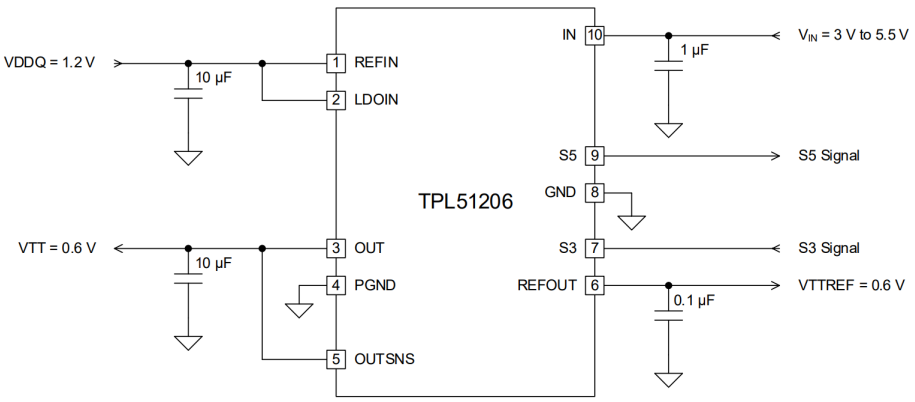


Table of Contents

Product Family Table

Part Number	Output Current	Orderable Number	Package	Transport Media, Quantity	MSL	Marking information
TPL51206	2 A	TPL51206-DFFR	DFN2×2-10	3,000	3	206

Revision History

Date	Revision	Notes
2020-08-31	Rev.Pre.0	Preliminary version
2020-12-31	Rev.A.0	Initial release
2024-11-20	Rev.A.1	1.Updated to a new datasheet format 2.Corrected the vertical coordinate scale of I_{OUT} in Figure 20 3.Corrected "V_{IN}" to "V_{LDOIN}" in the power dissipation calculation equation
2024-12-05	Rev.A.2	Corrected the Figure number from "Figure 19" to "Figure 20" in above notes of the Rev.A.1

Pin Configuration and Functions

TPL51206 Series
DFN2×2-10
Top View

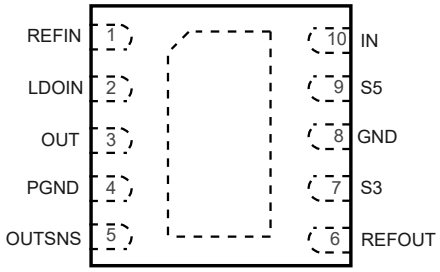


Table 1. Pin Functions: TPL51206 Series

Pin No.	Name	I/O	Description
8	GND	-	The ground reference pin. Connect the GND pin to the PCB ground plane directly.
10	IN	I	The regulator power supply input pin. A 1-μF or larger ceramic capacitor from IN to ground (as close as possible to the IN pin) is required to reduce the jitter from the previous-stage power supply.
2	LDOIN	I	The LDO power supply input pin.
3	OUT	O	The LDO output voltage pin. A total capacitance of 10 μF or larger from OUT to ground (as close as possible to OUT pin) is required to ensure regulator stability.
5	OUTSNS	I	The LDO output voltage sense pin. Connect SNS to the remote DDR termination bypass capacitors to get accurate remote feedback sensing of the voltage of OUT.
4	PGND	-	The power ground pin. Connect the PGND pin to the PCB ground plane directly.
1	REFIN	I	The reference input for the REFOUT pin. A 1/2 resistor divider is integrated internally.
6	REFOUT	O	The reference output pin. Connect to the ground through a 0.1-μF to 1-μF ceramic capacitor.
7	S3	I	The S3 signal input pin.
9	S5	I	The S5 signal input pin.

(1) The exposed PAD must be connected to a large-area ground plane to maximize the thermal performance.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
IN, LDOIN, REFIN, S3, S5		−0.3	6	V
PGND to GND		−0.3	0.3	V
OUT, OUTSNS, REFOUT		−0.3	3.6	V
T_J	Maximum Junction Temperature	−40	150	°C
T_{STG}	Storage Temperature Range	−55	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond the Absolute Maximum Ratings may cause permanent damage to the device.
(2) All voltage values are with respect to GND.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	±2000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	±1500	V

Recommended Operating Conditions

Parameter		Min	Max	Unit
IN	Regulator Input Voltage	3	5.5	V
LDOIN	LDO Input Voltage	–0.1	3.5	V
REFIN	LDO Input Sense Voltage	−0.1	3.5	V
S3, S5	S3, S5 Signal Input Voltage	–0.1	5.5	V
OUT	LDO Output Voltage	–0.1	3.5	V
OUTSNS	LDO Output Sense Voltage	–0.1	3.5	V
REFOUT	Reference Output Voltage	–0.1	3.5	V
PGND	Power Ground Voltage to GND	–0.1	0.1	V
T_J	Junction Temperature Range	–40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
DFN2×2-10	67.8	13.2	°C/W

Electrical Characteristics

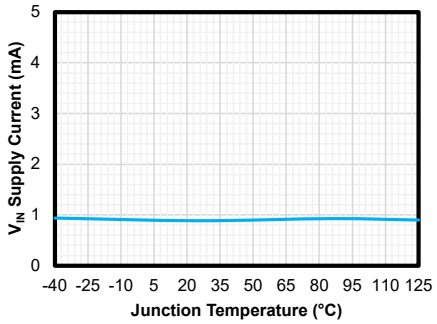
All test conditions: T_J = −40°C to +125°C (typical value at T_J = 25°C), V_{IN} = 5 V, V_{LDOIN} = V_{REFIN}, V_{S3} = V_{S5} = 5 V, C_{IN} = 10 µF, and C_{OUT} = 10 µF, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Supply Input Voltage and Current						
V_{IN}	Input Supply Voltage Range		3		5.5	V
V_{LDOIN}	LDO Input Voltage Range				3.5	V
V_{IN_UVLO}	Undervoltage Lockout of IN	T_A = 25°C, V_{IN} Rising		2.9	3	V
	Hysteresis			180		mV
I_{IN_S0}	Input Supply Current of IN, S0	T_A = 25°C, V_{S3} = V_{S5} = 5 V, V_{LDOIN} = V_{REFIN} = 1.8 V, I_{OUT} = 0 mA		0.89		mA
I_{IN_S3}	Input Supply Current of IN, S3	T_A = 25°C, V_{S3} = 0 V, V_{S5} = 5 V, V_{LDOIN} = V_{REFIN} = 1.8 V, I_{OUT} = 0 mA		0.34		mA
I_{IN_SD}	Shutdown Current of IN, S4 or S5	T_A = 25°C, V_{S3} = V_{S5} = 0 V, V_{LDOIN} = V_{REFIN} = 1.8 V, I_{OUT} = 0 mA		0.1	5	µA
I_{LDOIN_S0}	Input Current of LDOIN, S0	T_A = 25°C, V_{S3} = V_{S5} = 5 V, V_{LDOIN} = V_{REFIN} = 1.8 V, I_{OUT} = 0 mA		2	10	µA
I_{LDOIN_S3}	Input Current of LDOIN, S3	T_A = 25°C, V_{S3} = 0 V, V_{S5} = 5 V, V_{LDOIN} = V_{REFIN} = 1.8 V, I_{OUT} = 0 mA		2	10	µA
I_{LDOIN_SD}	Shutdown Current of LDOIN, S4 or S5	T_A = 25°C, V_{S3} = V_{S5} = 0 V, V_{LDOIN} = V_{REFIN} = 1.8 V, I_{OUT} = 0 mA		0.2	5	µA
Reference Input and Output						
I_{REFIN}	Input Current of REFIN	V_{REFIN} = 1.8 V		30		µA
V_{REFOUT}	Reference Output Voltage			$\frac{V_{REFIN}}{2}$		V
V_{REFOUT_TOL}	Tolerance of REFOUT to REFIN	$\lvert I_{REFOUT}\rvert \le 10$ mA, 1.2 V ≤ V_{REFIN} ≤ 1.8 V	49%		51%	
		$\lvert I_{REFOUT}\rvert \le 100$ µA, 1.2 V ≤ V_{REFIN} ≤ 1.8 V	49%		51%	
I_{REFOUT_SRC}	Source Current Limit of REFOUT	V_{REFIN} = 1.8 V, V_{REFOUT} = 0 V	10			mA
I_{REFOUT_SNK}	Sink Current Limit of REFOUT	V_{REFIN} = 0 V, V_{REFOUT} = 1.8 V	10			mA
I_{REFOUT_DIS}	Discharge Current of REFOUT	T_A = 25°C, V_{S3} = V_{S5} = 0 V, V_{REFOUT} = 0.5 V		8		mA

Parameter		Conditions	Min	Typ	Max	Unit
Regulated Output Voltage and Current						
V_{OUT}	Output Voltage, $V_{OUT} = \frac{V_{REFIN}}{2}$	$\lvert I_{OUT}\rvert \le 10$ mA, 1.2 V ≤ V_{REFIN} ≤ 1.8 V	−20		20	mV
		$\lvert I_{OUT}\rvert \le 1$ A, 1.2 V ≤ V_{REFIN} ≤ 1.8 V	−30		30	mV
		$\lvert I_{OUT}\rvert \le 2$ A, 1.2 V ≤ V_{REFIN} ≤ 1.8 V	−40		40	mV
I_{OUT_SRC}	Source Current Limit of OUT	V_{REFIN} = 1.8 V, V_{OUT} = V_{OUTSNS} = 0.7 V	2			A
I_{OUT_SNK}	Sink Current Limit of OUT	V_{REFIN} = 1.8 V, V_{OUT} = V_{OUTSNS} = 1.1 V	2			A
I_{OUT_LKG}	Leakage Current of OUT	T_A = 25°C, V_{S3} = 0 V, V_{S5} = 5 V, V_{OUT} = V_{REFOUT}		1	10	μA
I_{OUT_DIS}	Discharge Current of OUT	T_A = 25°C, V_{S3} = V_{S5} = V_{REFIN} = 0 V, V_{OUT} = 0.5V		50		mA
I_{OUTSNS_BIAS}	Input Bias Current of OUTSNS	V_{S3} = V_{S5} = 5 V, V_{OUTSNS} = V_{REFOUT}	−0.1		0.1	μA
I_{OUTSNS_LKG}	Leakage Current of OUTSNS	V_{S3} = 0 V, V_{S5} = 5 V, V_{OUTSNS} = V_{REFOUT}	−0.1		0.1	μA
S3 and S5						
V_{IH}	High-Level Input of S3 and S5		1.7			V
V_{IL}	Low-Level Input of S3 and S5				0.5	V
V_{HL_SYS}	Hysteresis of S3 and S5			0.3		V
I_{HL_LKG}	Leakage Current of S3 and S5		−1		1	μA
Temperature Range						
T_{SD}	Thermal shutdown threshold	Temperature Increasing		160		°C
	Hysteresis			20		°C

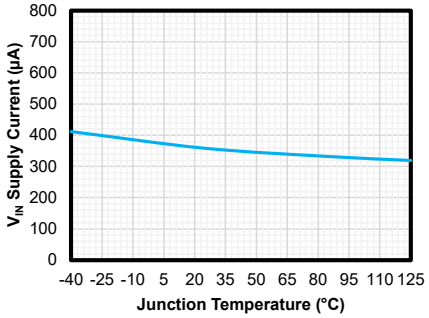
Typical Performance Characteristics

All test conditions: T_J = −40°C to +125°C (typical value at T_J = 25°C), V_{IN} = 5 V, V_{LDOIN} = V_{REFIN}, V_{S3} = V_{S5} = 5 V, C_{IN} = 10 µF, and C_{OUT} = 10 µF, unless otherwise noted.



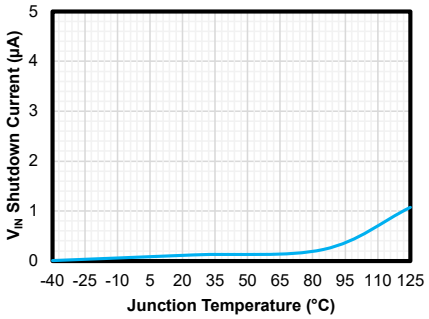
V_{LDOIN} = 1.8 V, S3 = S5 = 5 V, S0

Figure 1. V_{IN} Supply Current vs. Junction Temperature



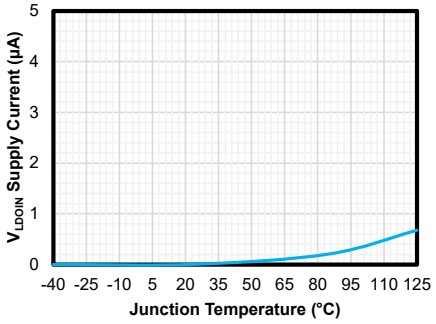
V_{LDOIN} = 1.8 V, S3 = 0 V, S5 = 5 V, S3

Figure 2. V_{IN} Supply Current vs. Junction Temperature



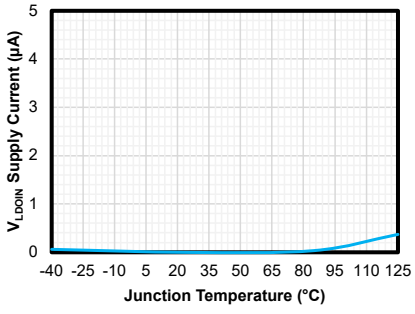
V_{LDOIN} = 1.8 V, S3 = S5 = 5 V, S4 or S5

Figure 3. V_{IN} Shutdown Current vs. Junction Temperature



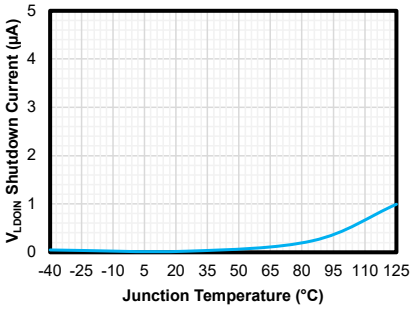
V_{LDOIN} = 1.8 V, S3 = S5 = 5 V, S0

Figure 4. V_{LDOIN} Supply Current vs. Junction Temperature



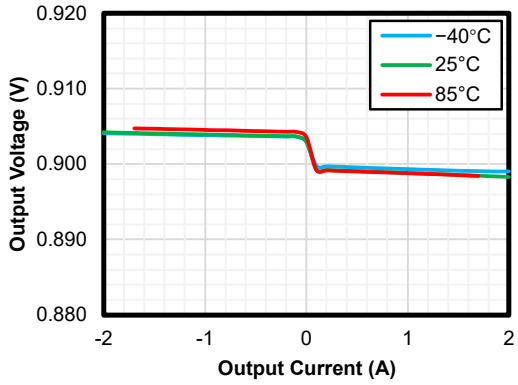
V_{LDOIN} = 1.8 V, S3 = 0 V, S5 = 5 V, S0

Figure 5. V_{LDOIN} Supply Current vs. Junction Temperature



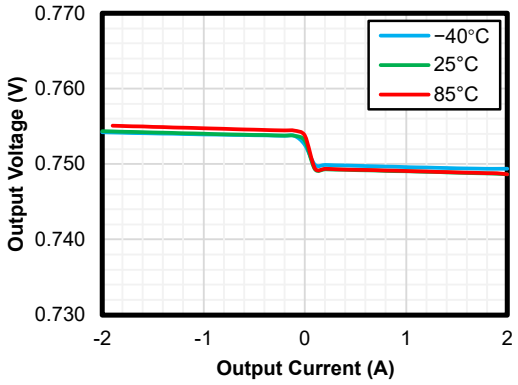
V_{LDOIN} = 1.8 V, S3 = S5 = 0 V, S4 or S5

Figure 6. V_{LDOIN} Shutdown Current vs. Junction Temperature



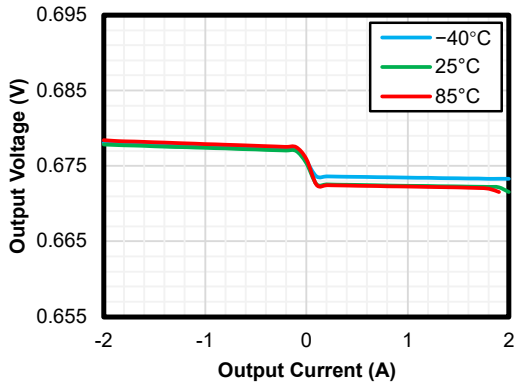
V_{LDOIN} = 1.8 V, DDR2

Figure 7. OUT Load Regulation



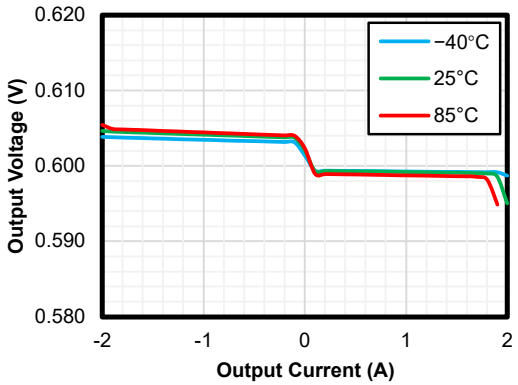
V_{LDOIN} = 1.5 V, DDR3

Figure 8. OUT Load Regulation



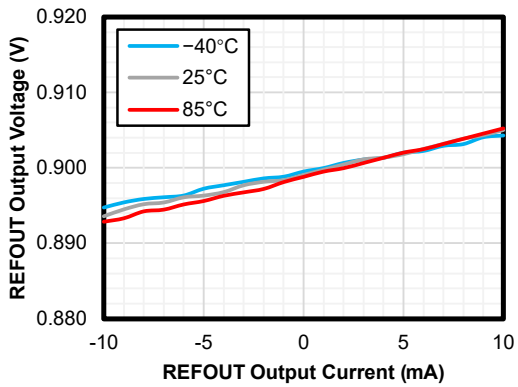
V_{LDOIN} = 1.35 V, DDR3L

Figure 9. OUT Load Regulation



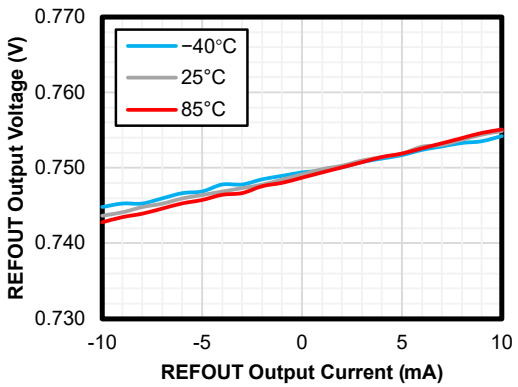
V_{LDOIN} = 1.2 V, LP DDR3 or DDR4

Figure 10. OUT Load Regulation



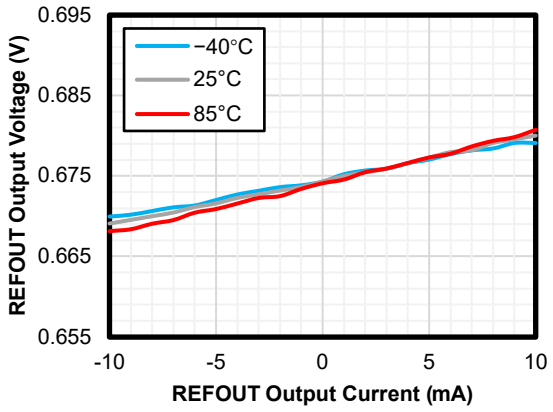
V_{LDOIN} = 1.8 V, DDR2

Figure 11. REFOUT Load Regulation



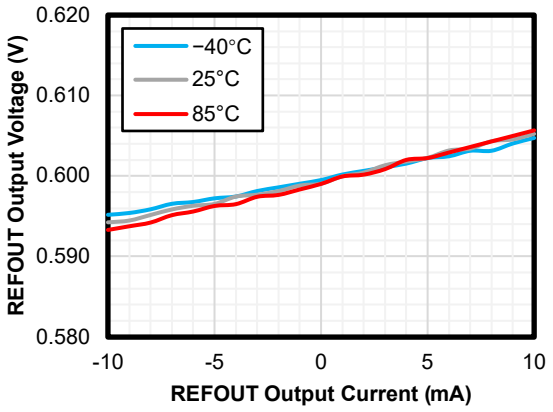
V_{LDOIN} = 1.5 V, DDR3

Figure 12. REFOUT Load Regulation



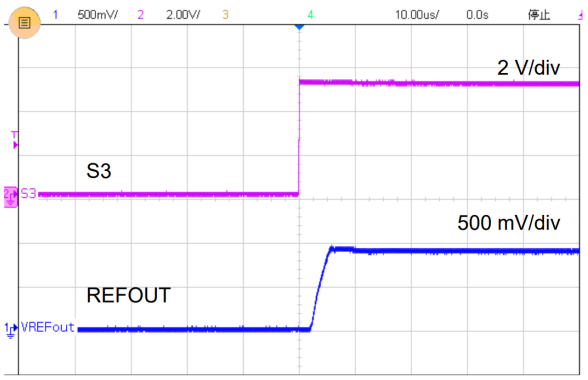
V_{LDOIN} = 1.35 V, DDR3L

Figure 13. REFOUT Load Regulation



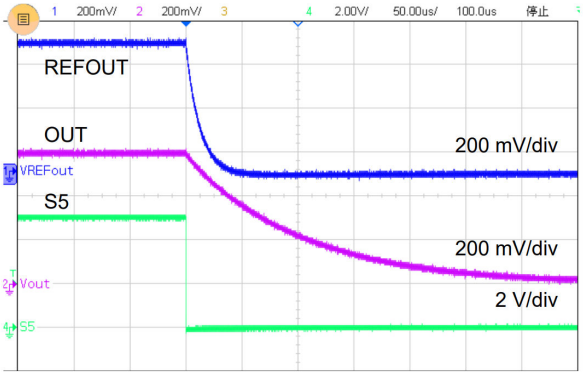
V_{LDOIN} = 1.2 V, LP DDR3 or DDR4

Figure 14. REFOUT Load Regulation



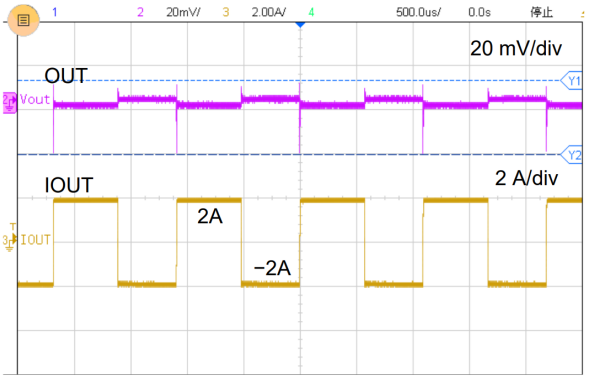
V_{LDOIN} = 1.8 V, S3 Enable, 10 µs/div

Figure 15. Power Up



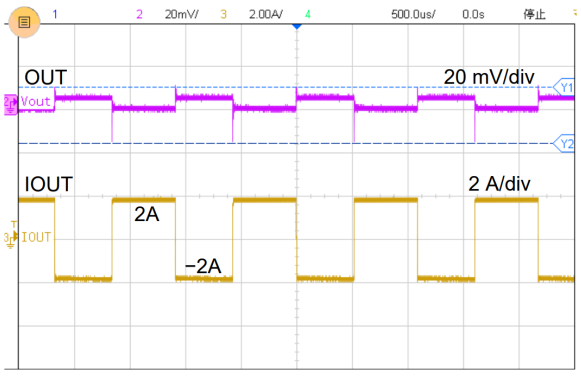
V_{LDOIN} = 1.8 V, S5 Enable, 50 µs/div

Figure 16. Power Down



V_{LDOIN} = 1.8 V, OUT = 0.9 V, 500 µs/div

Figure 17. Load Transient

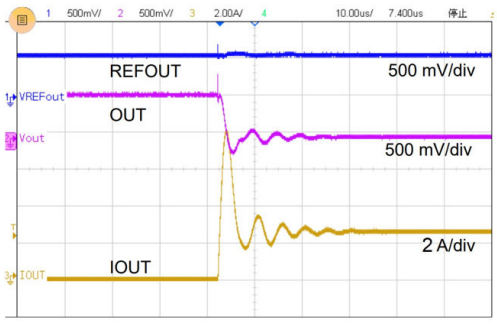


V_{LDOIN} = 1.2 V, OUT = 0.6 V, 500 µs/div

Figure 18. Load Transient

V_{LDOIN} = 1.8 V, OUT = 0.9 V, 20 µs/div

Figure 19. Output Short-to-GND Protection



V_{LDOIN} = 1.2 V, OUT = 0.6 V, 20 µs/div

Figure 20. Output Short-to-GND Protection

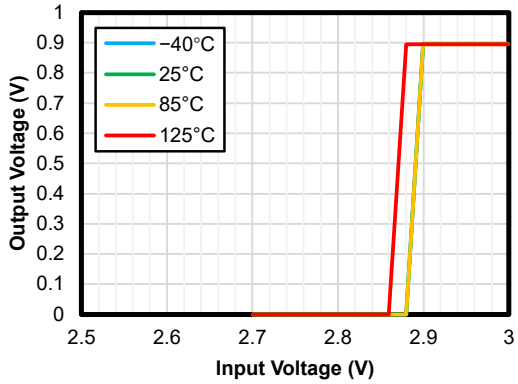


Figure 21. V_{IN} UVLO Rising

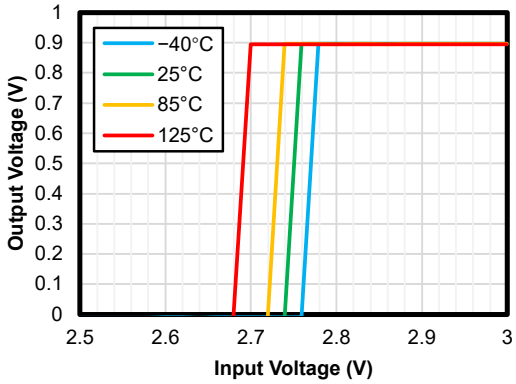


Figure 22. V_{IN} UVLO Falling

Detailed Description

Overview

The TPL51206 is a series of 2-A sink and source DDR termination regulators specifically designed for DDR applications with heavy space limitations. The TPL51206 series implements a fast load-transient response and only requires a minimum output capacitance of 10 µF.

The TPL51206 series supports a remote-sensing function and all power requirements for DDR VTT bus termination. In addition, the TPL51206 series provides S3 and S5 control pins which can be used to control the power state in DDR applications, setting OUT to high impedance in the S3 state (suspend to RAM) and discharging OUT and REFOUT in S4 or S5 state (suspend to disk).

Functional Block Diagram

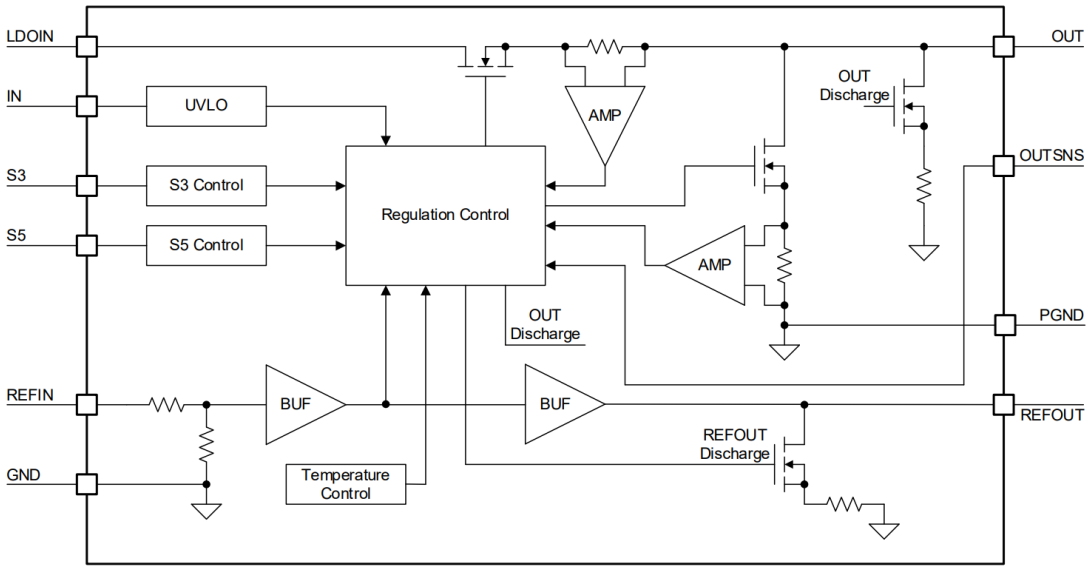


Figure 23. Functional Block Diagram

Feature Description

Sink and Source Regulator (OUT and OUTSNS)

The TPL51206 is a series of 2-A sink and source DDR termination regulators specifically designed for DDR applications with heavy space limitations. The TPL51206 series integrates a high-performance and low-dropout linear regulator with a fast-feedback loop that can support fast-load transient response with small ceramic capacitors. To get tight regulation tolerance, the remote sensing pin, the OUTSNS pin, must be connected to the OUT pin through a separate trace from a high-current path.

Voltage Reference (LDOIN, REFIN and REFOUT)

The TPL51206 series uses the voltage at the REFIN pin as the reference input, and the reference output at the REFOUT pin exactly follows the $1/2 \times V_{REFIN}$ within the tolerance of V_{REFOUT_TOL}. When the TPL51206 series is configured for standard

DDR applications, the LDOIN pin, and the REFIN pin are directly connected with the input voltage range from 1 V to 3.5 V, and the voltage at the REFIN pin is divided by half through an internal resistor divider.

The REFOUT pin of the TPL51206 series implements a minimum of 10 mA of sink or source current capability. During normal operation, the REFOUT pin cannot be open, and a 0.1-μF to 1-μF X5R or better ceramic capacitor is required for stable operation.

IN Under-voltage Lockout

The TPL51206 series uses an under-voltage lockout circuit to keep the regulator shut off until the IN voltage exceeds the rising UVLO threshold of IN.

S3 and S5 Control

The TPL51206 series integrates the S3 and S5 pins to control the device state. Table 1 shows the state of the device with different S3 and S5 logic level combinations, and the corresponding status of REFOUT and OUT.

Table 2. S3 and S5 Control Table

STATE	S3	S5	REFOUT	OUT
S0	HIGH	HIGH	ON	ON
S3	LOW	HIGH	ON	OFF (High-Z)
S4, S5	LOW	LOW	OFF (Discharge)	OFF (Discharge)

(1) In the S4 or S5 state, S3 = S5 = LOW, all the outputs are turned off and discharge to power ground.
(2) In the S3 state, S3 = LOW and S5 = HIGH, the OUT pin is turn-off in the high-impedance state.
(3) In the S0 state, S3 = S5 = HIGH, the device is in normal operation mode.

Power Sequence Control

It is recommended to power up and power down the TPL51206 series with the power sequence shown in Figure 24.

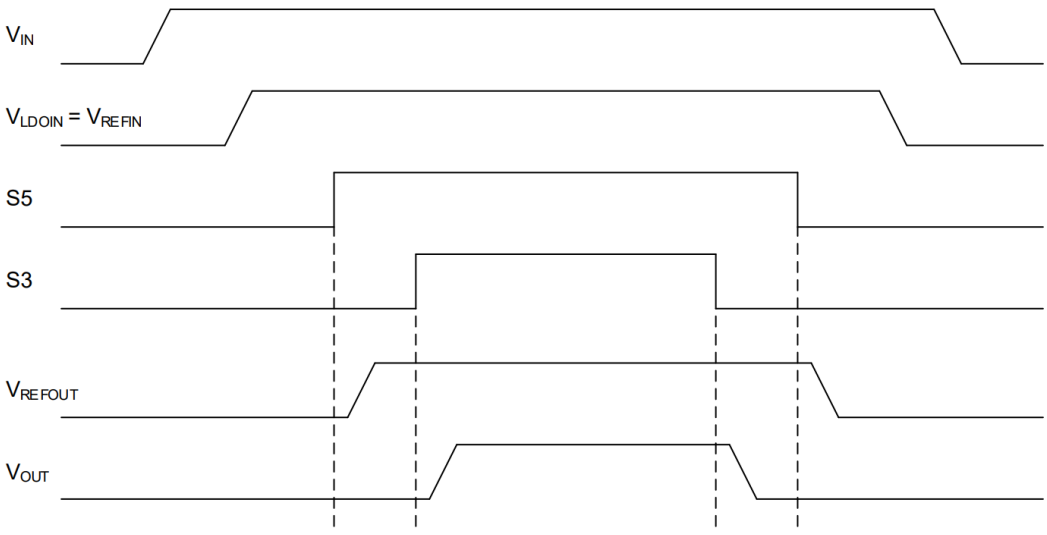


Figure 24. Power Up and Down Sequence Control

OUT Over-Current Protection

The TPL51206 series integrates constant over-current protection. When the absolute value of the output sink or source current is greater than 2 A, the current is limited to I_{OUT_SNK} or I_{OUT_SRC}, and the output voltage is out of regulation.

Over-Temperature Protection

The recommended operating junction temperature range is −40°C to 125°C. When the junction temperature is between 125°C and the thermal shutdown (TSD) threshold, the regulator can still work well, but it reduces the device lifetime for long-term uses. The over-temperature protection works when the junction temperature exceeds the thermal shutdown (TSD) threshold, which turns off the regulator immediately. Until the device cools down and the junction temperature falls below the thermal shutdown threshold minus thermal shutdown hysteresis, the regulator turns on again.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPL51206 is a series of 2-A sink and source DDR termination regulators specifically designed for DDR applications. The following application schematic shows a typical usage of the TPL51206 series.

Typical Application

Adjustable Output Operation

Figure 25 shows the typical application schematic of the TPL51206 series in DDR4 applications.

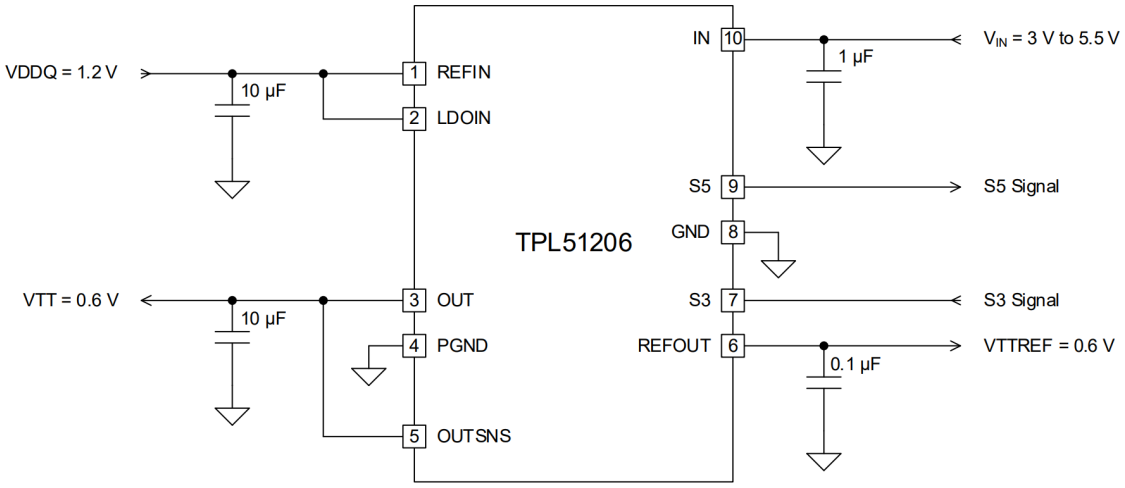


Figure 25. Typical Application Schematic

IN Input Capacitor

3PEAK recommends placing a 1-µF or greater capacitor with a 0.1-µF bypass capacitor in parallel close to the IN pin to keep the input voltage stable. The voltage rating of the capacitors must be greater than the maximum input voltage.

LDOIN Input Capacitor

3PEAK recommends placing a 10-µF or greater capacitor with a 0.1-µF bypass capacitor in parallel close to the LDOIN pin to keep the voltage stable during transient. More input capacitors are required if there are large output capacitors used at the OUT pin. It is suggested to place input capacitors with half of the output capacitance value at the LDOIN pin.

Power Dissipation

During normal operation, the LDO junction temperature should not exceed 125°C. Use the below equations to calculate the power dissipation and estimate the junction temperature. The power dissipation can be calculated using Equation 1.

$$P_D = (V_{LDOIN} - V_{OUT}) \times I_{OUT} + V_{LDOIN} \times I_{GND} \quad (1)$$

The junction temperature can be estimated using Equation 2. θ_{JA} is the junction-to-ambient thermal resistance.

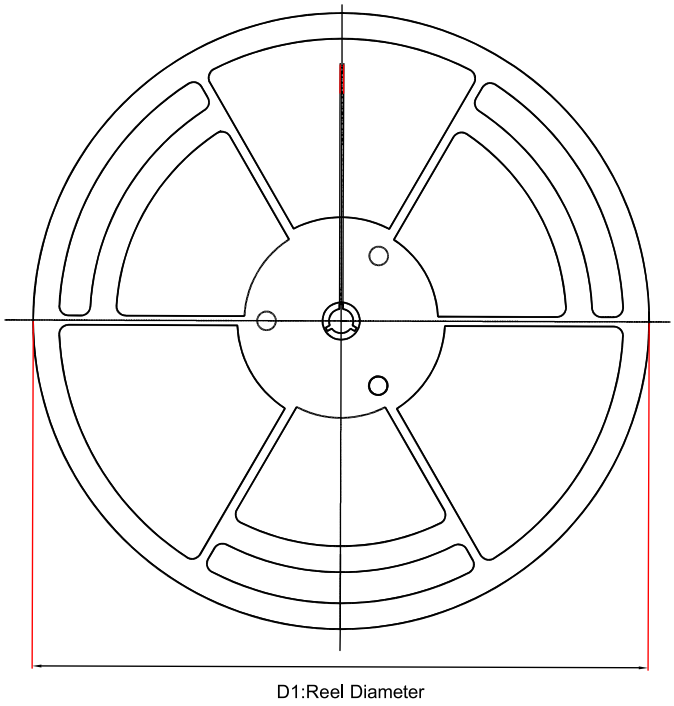
$$T_J = T_A + P_D \times \theta_{JA} \quad (2)$$

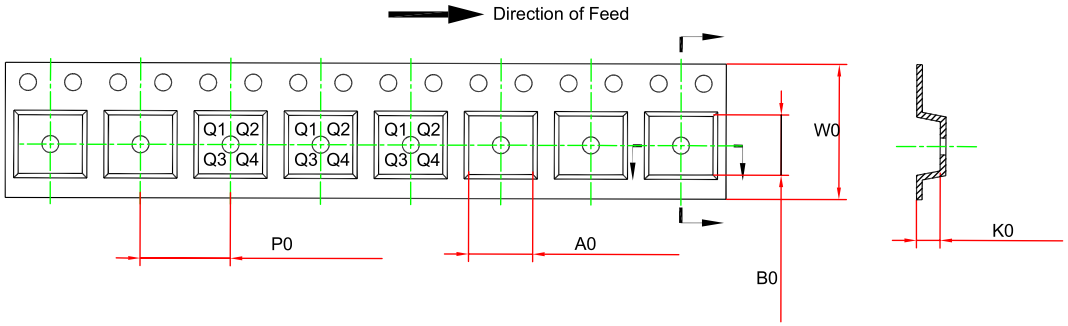
Layout

Layout Requirements

- Both input capacitors and output capacitors must be placed as close to the device pins as possible.
- Suggest bypassing the input pin to ground with a 0.1-μF bypass capacitor. The loop area formed by the bypass capacitor connection, the voltage input pin, and the ground pin of the system must be as small as possible.
- Suggest using wide trace lengths or thick copper weight to minimize the I×R drop and heat dissipation.
- The GND pin and the PGND pin must be connected to the thermal pad with multiple thermal vias as many as possible connected to the internal ground planes.

Tape and Reel Information



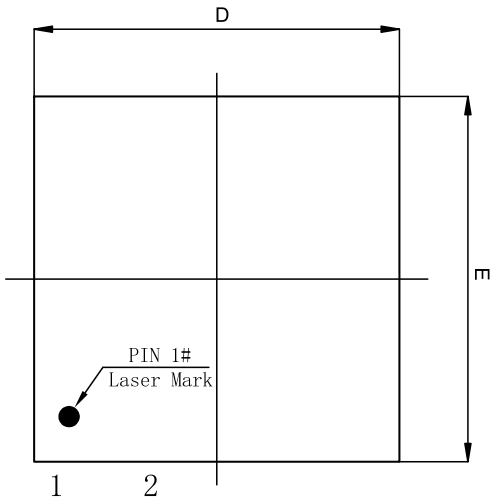


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPL51206-DFFR	DFN2×2-10	180	13.1	2.3	2.3	1.1	4	8	Q2

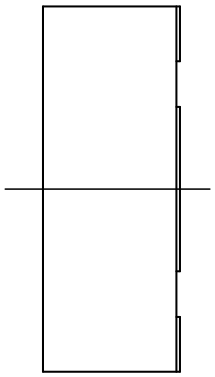
Package Outline Dimensions

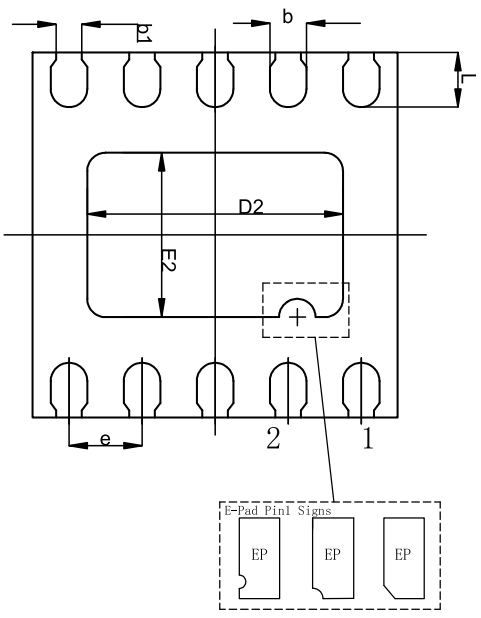
DFN2X2-10

Package Outline Dimensions DFF(DFN2X2-10-A)

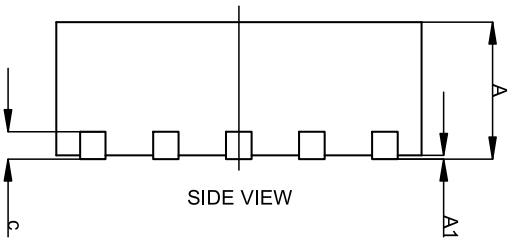


TOP VIEW





BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.150	0.250	0.006	0.010
c	0.150	0.250	0.006	0.010
D	1.900	2.100	0.075	0.083
D2	1.300	1.500	0.051	0.059
E	1.900	2.100	0.075	0.083
E2	0.800	1.000	0.031	0.039
e	0.400 BSC		0.016 BSC	
L	0.250	0.350	0.010	0.014

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPL51206-DFFR	−40 to 125°C	DFN2×2-10	206	MSL3	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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