Features

- V_{IN} Voltage: Support 2.5-V, 3.3-V and 5-V Power Rails
- V_{LDOIN} Voltage Range: 1.1 V to 3.5 V
- Flexible Input Voltage Tracking Directly from REFIN or Through External Resistor Divider
- 3-A Sink and Source Current Capability for DDR Termination
- Integrated Power MOSFETs
- Output Remote Sensing
- Fast Load-Transient Response
- Output Ramps Up in 35 μs
- Open-Drain Power Good to Monitor OUT Regulation
- Built in Soft-Start and UVLO, Current Limit and Thermal Shutdown Protection
- Support DDR, DDR2, DDR3, DDR3L, Low Power DDR3 and DDR4 VTT Applications
- Operating Temperature Range: –40°C to +125°C
- Small Package with 3×3 DFN-10
- Pb−Free and are RoHS Compliant

Applications

- Memory VTT Regulator for DDR, DDR2, DDR3, DDR3L, Low Power DDR3 and DDR4
- Notebooks, Desktops, and Workstations
- Servers, Networking Equipments and Datacenters
- Telecom and Base Station

Description

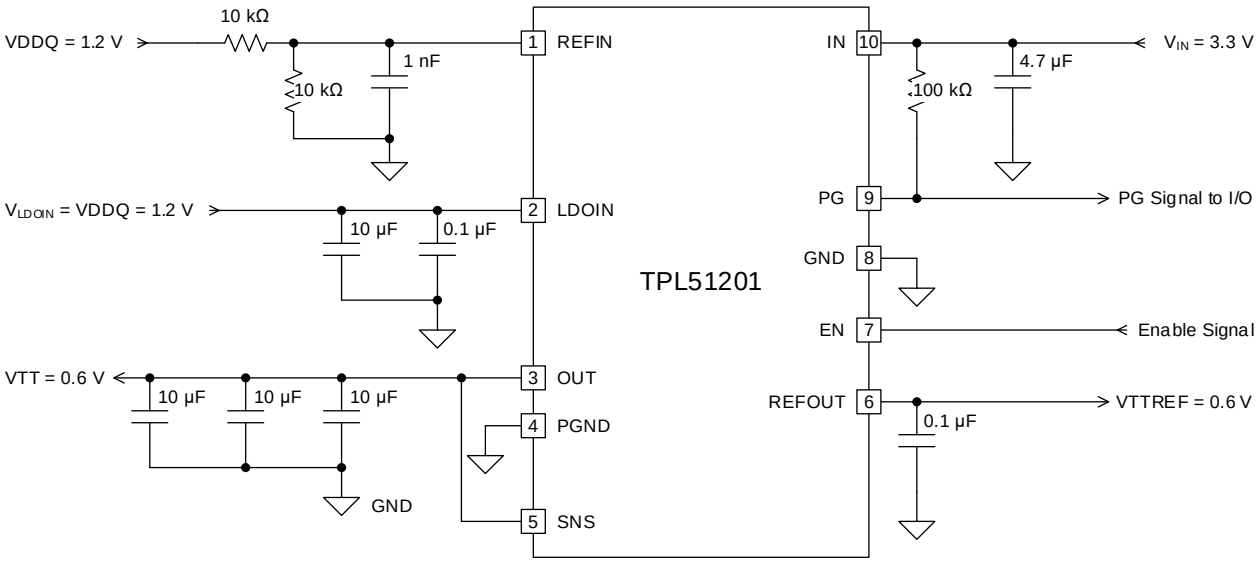
With the development of main processors in PCs and servers, more and more source double-data-rate (DDR) memories are required in the mainboard, where the input voltage becomes lower and lower, and space limitation becomes higher and higher.

The TPL51201 series devices are 3-A sink and source DDR termination regulators specifically designed for the DDR applications with heavy space limitation. The TPL51201 series devices implement a fast load-transient response and only requires a minimum output capacitance of 20 μF.

The TPL51201 series devices support a remote-sensing function and all power requirements for DDR VTT bus termination. In addition, the TPL51201 series devices provide an open-drain PG signal for VTT regulation indication and an EN signal that can be used to discharge VTT for DDR applications.

The TPL51201 series devices are available in the thermally efficient 10-pin 3×3 DFN package with thermal pad, and support the operating temperature range from –40°C to +125°C.

Typical Application Schematic



Product Family Table

Part Number	Output Current	Orderable Number	Package	Transport Media, Quantity	MSL	Marking information
TPL51201G-S	3 A	TPL51201G-DF8R-S	3×3 DFN-10	4,000	MSL3	L200

Table of Contents

Revision History

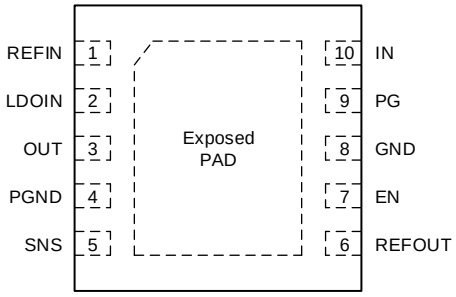
Date	Revision	Notes
2020/11/23	Rev.Pre	Preliminary Version
2021/05/31	Rev.A.0	Initial Released
2021/09/30	Rev.A.1	Add more details of OUT and SNS Output Capacitor in Page 14

Pin Configuration and Functions

TPL51201 Series

DFN-10 Package

Top View



Pin Functions

NAME	PIN NUMBER	TYPE	DESCRIPTION
EN	7	I	Regulator enable pin. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to VDDQ directly.
GND	8	–	Ground reference pin. Connect GND pin to PCB ground plane directly.
IN	10	I	Regulator power supply input pin. A 1-μF or larger ceramic capacitor from IN to ground (as close as possible to IN pin) is required to reduce the jitter from previous-stage power supply.
LDOIN	2	I	LDO power supply input pin.
OUT	3	O	LDO output voltage pin. Total capacitance of 20-μF or larger from OUT to ground (as close as possible to OUT pin) is required to ensure regulator stability.
PG	9	O	Open-drain power-good output pin.
PGND	4	–	Power ground pin. Connect PGND pin to PCB ground plane directly.
REFIN	1	I	Reference input pin. For DDR application, set to VDDQ/2 through resistor divider.
REFOUT	6	O	Reference output pin. Connect to ground through a 0.1-μF to 1-μF ceramic capacitor.
SNS	5	I	LDO output voltage sense pin. Connect SNS to the remote DDR termination bypass capacitors to get accurate remote feedback sensing of OUT voltage.

(1) Exposed PAD must be connected to a large-area ground plane to maximum the thermal performance.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
EN, IN, LDOIN, PG, REFIN, SNS		–0.3	6	V
PGND to GND		–0.3	0.3	V
OUT, REFOUT		–0.3	3.6	V
T_J	Junction Temperature Range	–40	150	°C
T_{STG}	Storage Temperature Range	–55	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond the Absolute Maximum Ratings may permanently damage the device.

(2) All voltage values are with respect to GND.

ESD Ratings

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	±2000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	±1500	V

Recommended Operating Conditions

Parameter		Min	Max	Unit
IN	Regulator input voltage	2.375	5.5	V
LDOIN	LDO input voltage	–0.1	3.5	V
EN	Regulator enable voltage	–0.1	3.5	V
OUT	LDO output voltage	–0.1	3.5	V
SNS	LDO output sense voltage	–0.1	3.5	V
REFIN	Reference input voltage	0.5	1.8	V
REFOUT	Reference output voltage	–0.1	1.8	V
PG	Power-good pull-up voltage	–0.1	3.5	V
PGND	Power ground voltage to GND	–0.1	0.1	V
T_J	Junction Temperature Range	–40	125	°C

Thermal Information

Package	θ_{JA}	$\theta_{JC,bottom}$	Unit
3×3 DFN-10	77.66	16.33	°C/W

Electrical Characteristics

T_J = –40°C to +125°C (typical value at T_J = +25°C), V_{IN} = V_{EN} = 3.3 V; V_{LDOIN} = 1.8 V, V_{REFIN} = 0.9 V, V_{SNS} = 0.9 V, C_{IN} = 10 µF, and C_{OUT} = 3 x 10 µF; unless otherwise noted unless otherwise noted.

Parameter		Test Conditions	Min	Typ	Max	Unit
Supply Input Voltage and Current						
V_{IN}	Input supply voltage range		2.375		5.5	V
V_{LDOIN}	LDO input voltage range				3.5	V
$UVLO_{IN}$	Input supply UVLO	T_A = +25°C, V_{IN} rising		2.3	2.375	V
	Hysteresis			50		mV
I_{IN}	Input supply current of IN	T_A = +25°C, V_{EN} = 3.3 V, I_{OUT} = 0 mA		0.8	1	mA
I_{IN_SD}	Shutdown current of IN	T_A = +25°C, V_{EN} = 0 V, V_{REFIN} = 0 V, I_{OUT} = 0 mA		65	80	µA
		T_A = +25°C, V_{EN} = 0 V, V_{REFIN} > 0.4 V, I_{OUT} = 0 mA		200	400	µA
I_{LDOIN}	Input current of LDOIN	T_A = +25°C, V_{EN} = 3.3 V, I_{OUT} = 0 mA		1	50	µA
I_{LDOIN_SD}	Shutdown current of LDOIN	T_A = +25°C, V_{EN} = 0 V, I_{OUT} = 0 mA		1	50	µA
Reference Input and Output						
V_{REFIN}	Reference input voltage		0.5		1.8	V
$UVLO_{REFIN}$	Reference input UVLO	T_A = +25°C, V_{REFIN} rising	360	390	420	mV
	Hysteresis			20		mV
I_{REFIN}	Input current of REFIN	V_{EN} = 3.3 V		1		µA
V_{REFOUT}	Reference output voltage			V_{REFIN}		V
V_{REFOUT_TOL}	Tolerance of REFOUT to REFIN	−1 mA ≤ I_{REFOUT} ≤ 1 mA, 0.5 V ≤ V_{REFIN} ≤ 1.8 V	−12		12	mV
		−10 mA ≤ I_{REFOUT} ≤ 10 mA, 0.5 V ≤ V_{REFIN} ≤ 1.8 V	−15		15	mV
I_{REFOUT_SRCL}	Source current limit of REFOUT	V_{REFOUT} = 0.5 V	10	60		mA
I_{REFOUT_SNKL}	Sink current limit of REFOUT	V_{REFOUT} = 1.5 V	10	60		mA
Regulated Output Voltage and Current						
V_{OUT}	Output voltage	V_{REFOUT} = 1.25 V (DDR1), I_{OUT} = 0 A		1.25		V
		Tolerance	−15		15	mV
		V_{REFOUT} = 0.9 V (DDR2), I_{OUT} = 0 A		0.9		V
		Tolerance	−15		15	mV
		V_{REFOUT} = 0.75 V (DDR3), I_{OUT} = 0 A		0.75		V
		Tolerance	−15		15	mV
		V_{REFOUT} = 0.675 V (DDR3L), I_{OUT} = 0 A		0.675		V
		Tolerance	−15		15	mV
		V_{REFOUT} = 0.6 V (DDR4), I_{OUT} = 0 A		0.6		V
		Tolerance	−15		15	mV
ΔV_{OUT}	Tolerance of OUT to REFOUT	–2 A < I_{OUT} < 2 A	−25		25	mV
I_{OUT_SRCL}	Source current limit of OUT	V_{SNS} = 90% × V_{REFOUT}	3		4.5	A
I_{OUT_SNKL}	Sink current limit of OUT	V_{SNS} = 110% × V_{REFOUT}	3.2		5.5	A
R_{DIS}	Discharge resistance	T_A = +25°C, V_{REFIN} = 0 V, V_{OUT} = 0.3 V, V_{EN} = 0 V		12		Ω

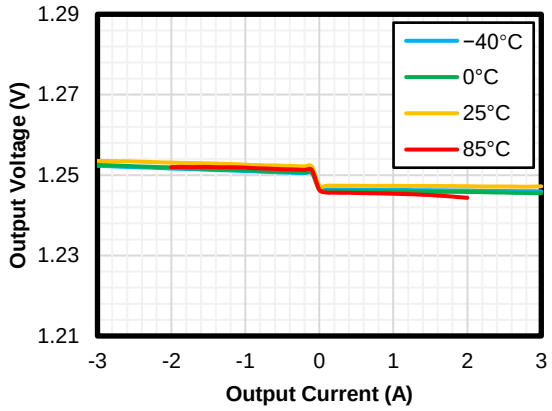
Electrical Characteristics (continued)

T_J = –40°C to +125°C (typical value at T_J = +25°C), V_{IN} = V_{EN} = 3.3 V; V_{LDOIN} = 1.8 V, V_{REFIN} = 0.9 V, V_{SNS} = 0.9 V, C_{IN} = 10 µF, and C_{OUT} = 3 x 10 µF; unless otherwise noted unless otherwise noted.

Parameter		Test Conditions	Min	Typ	Max	Unit
Enable Control						
V_{EN}	EN High-level input voltage	Device enable	1.7			V
	EN Low-level input voltage of	Device disable			0.5	V
	Hysteresis			0.25		V
I_{EN}	Leakage current of EN	T_A = +25°C, V_{EN} = 0 V to 6.5 V	–1		1	µA
Power Good						
V_{PG}	PG lower threshold	With respect to REFOUT	–23.5%	–20%	–17.5%	
	PG upper threshold	With respect to REFOUT	17.5	20%	23.5%	
	Hysteresis			5%		
I_{PG}	Leakage current of PG				1	µA
$V_{OL(PG)}$	PG low-level output voltage	Source 4 mA to PG pin			0.4	V
$t_{DLY(PG)}$	PG start-up delay	Startup rising edge, V_{SNS} within 15% of V_{REFOUT}		2		ms
$t_{DLY(PG\_B)}$	PG start-up bad delay	V_{SNS} is beyond the ±20% PG trip threshold		10		µs
Temperature Range						
T_{SD}	Thermal shutdown threshold	Temperature increasing		155		°C
	Hysteresis			25		°C
T_J	Operating junction temperature		–40		125	°C

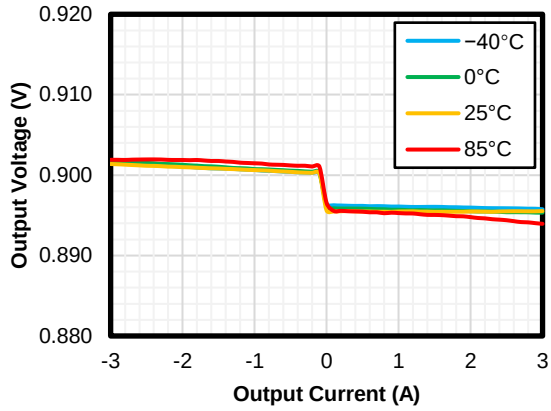
Typical Performance Characteristics

T_J = –40°C to +125°C (typical value at T_J = +25°C), V_{IN} = V_{EN} = 3.3 V; V_{LDOIN} = 1.8 V, V_{REFIN} = 0.9 V, V_{SNS} = 0.9 V, C_{IN} = 10 µF, and C_{OUT} = 3 x 10 µF; unless otherwise noted unless otherwise noted.



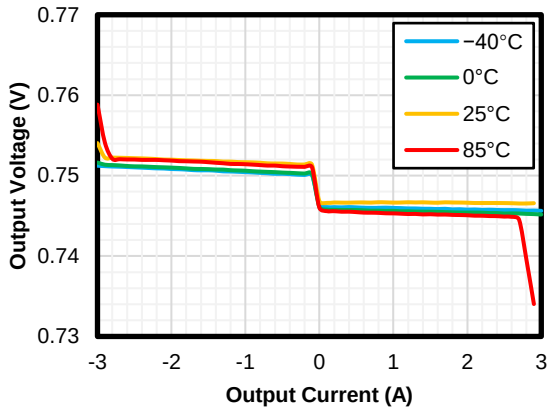
V_{IN} = 3.3 V DDR

Figure 1 OUT Load Regulation



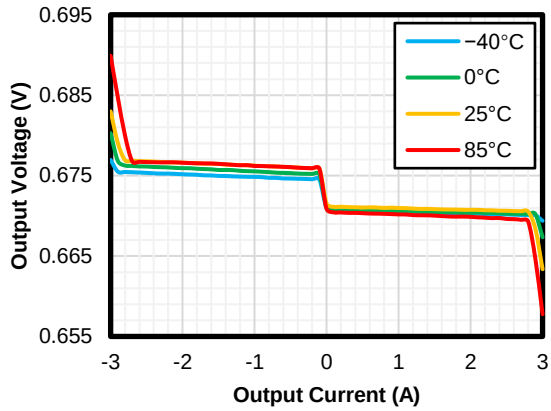
V_{IN} = 3.3 V DDR2

Figure 2 OUT Load Regulation



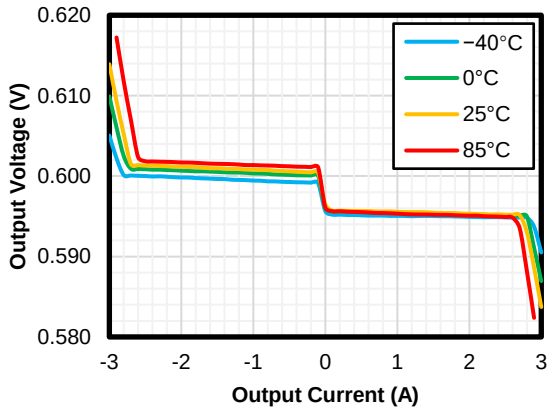
V_{IN} = 3.3 V DDR3

Figure 3 OUT Load Regulation



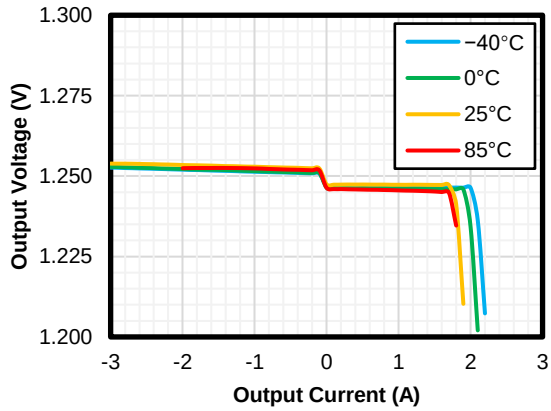
V_{IN} = 3.3 V DDR3L

Figure 4 OUT Load Regulation



V_{IN} = 3.3 V LP DDR3 or DDR4

Figure 5 OUT Load Regulation

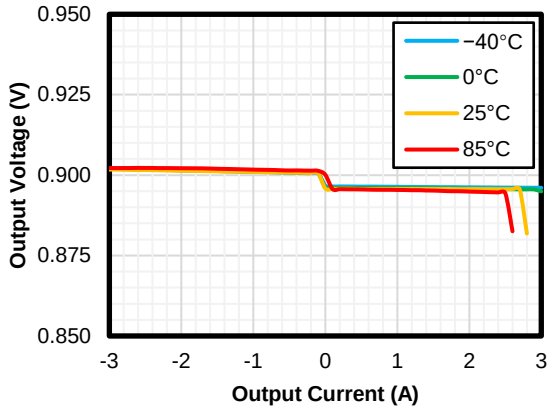


V_{IN} = 2.5 V DDR

Figure 6 OUT Load Regulation

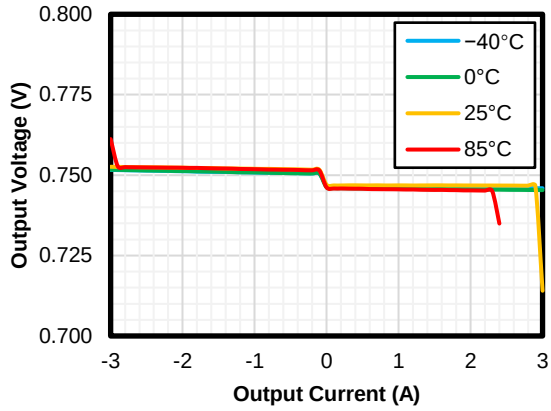
Typical Performance Characteristics (continued)

T_J = –40°C to +125°C (typical value at T_J = +25°C), V_{IN} = V_{EN} = 3.3 V; V_{LDOIN} = 1.8 V, V_{REFIN} = 0.9 V, V_{SNS} = 0.9 V, C_{IN} = 10 µF, and C_{OUT} = 3 x 10 µF; unless otherwise noted unless otherwise noted.



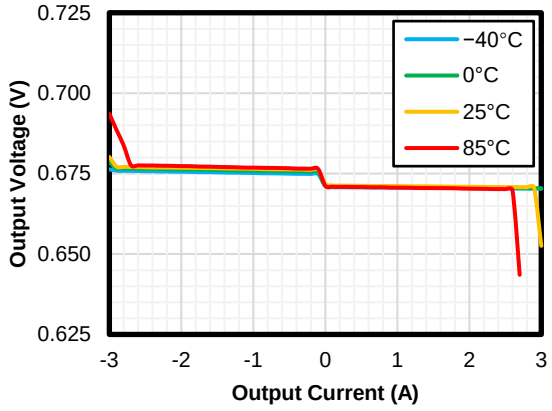
V_{IN} = 2.5 V DDR2

Figure 7 OUT Load Regulation



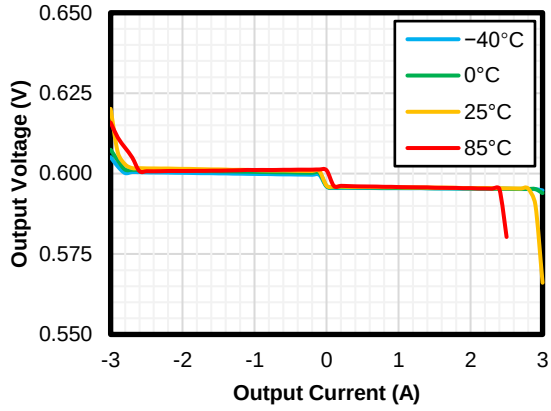
V_{IN} = 2.5 V DDR3

Figure 8 OUT Load Regulation



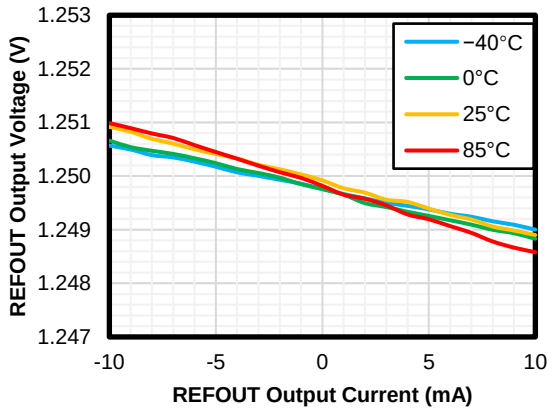
V_{IN} = 2.5 V DDR3L

Figure 9 OUT Load Regulation



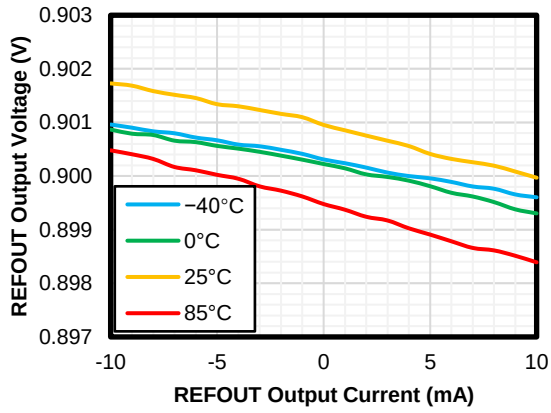
V_{IN} = 2.5 V LP DDR3 or DDR4

Figure 10 OUT Load Regulation



DDR

Figure 11 REFOUT Load Regulation

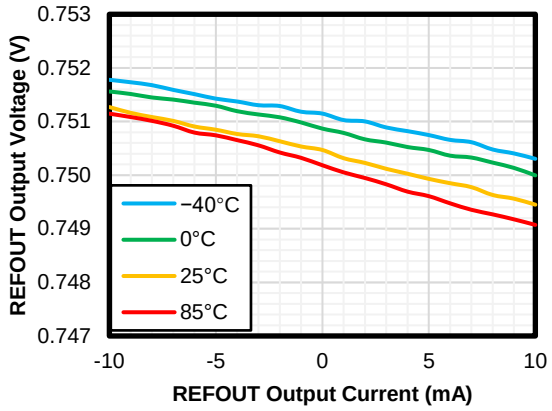


DDR2

Figure 12 REFOUT Load Regulation

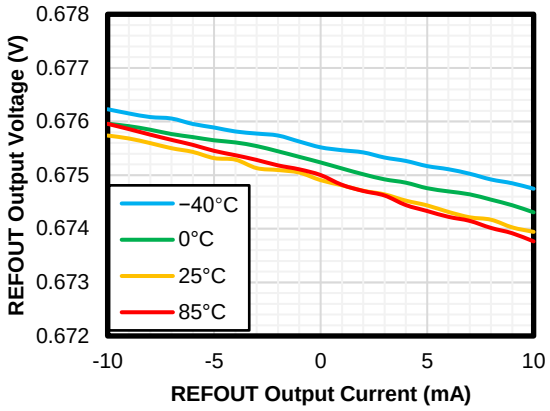
Typical Performance Characteristics (continued)

T_J = –40°C to +125°C (typical value at T_J = +25°C), V_{IN} = V_{EN} = 3.3 V; V_{LDOIN} = 1.8 V, V_{REFIN} = 0.9 V, V_{SNS} = 0.9 V, C_{IN} = 10 µF, and C_{OUT} = 3 x 10 µF; unless otherwise noted unless otherwise noted.



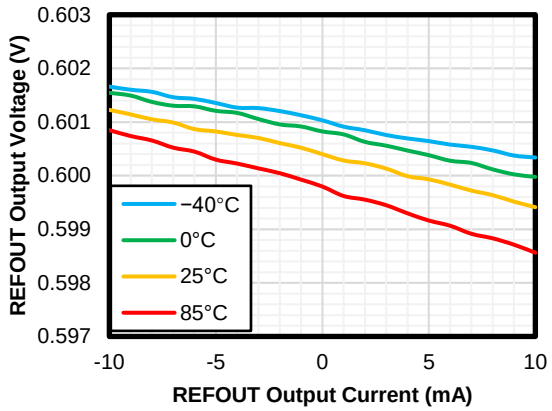
DDR3

Figure 13 REFOUT Load Regulation



DDR3L

Figure 14 REFOUT Load Regulation



DDR4

Figure 15 REFOUT Load Regulation

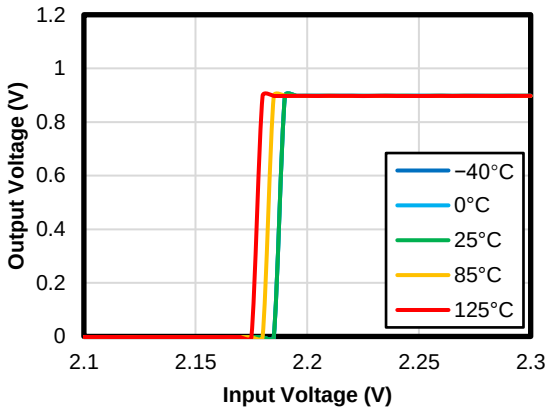
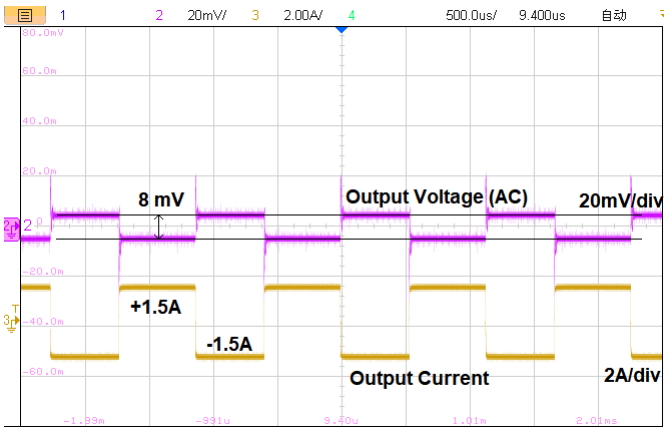
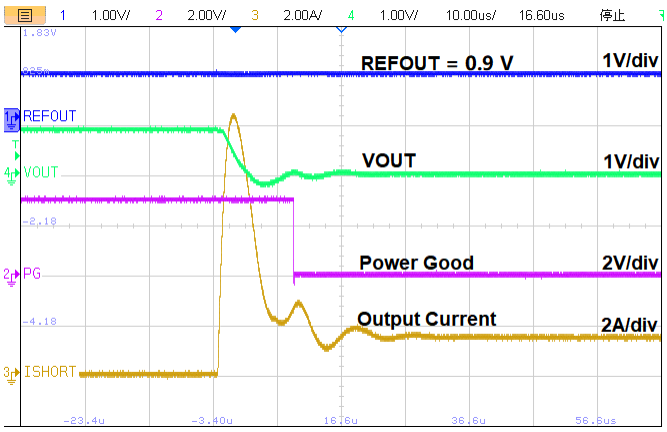


Figure 16 UVLO Rising



500 µs/div

Figure 17 Load Transient



10 µs/div

Figure 18 Output Short-to-GND Protection

Detailed Description

Overview

The TPL51201 series devices are 3-A sink and source DDR termination regulators specifically designed for the DDR applications with heavy space limitation. The TPL51201 series devices implement a fast load-transient response and only requires a minimum output capacitance of 20 µF.

The TPL51201 series devices support a remote-sensing function and all power requirements for DDR VTT bus termination. In addition, the TPL51201 series devices provide an open-drain PG signal for VTT regulation indication and an EN signal that can be used to discharge VTT for DDR1 to DDR4 applications.

Functional Block Diagram

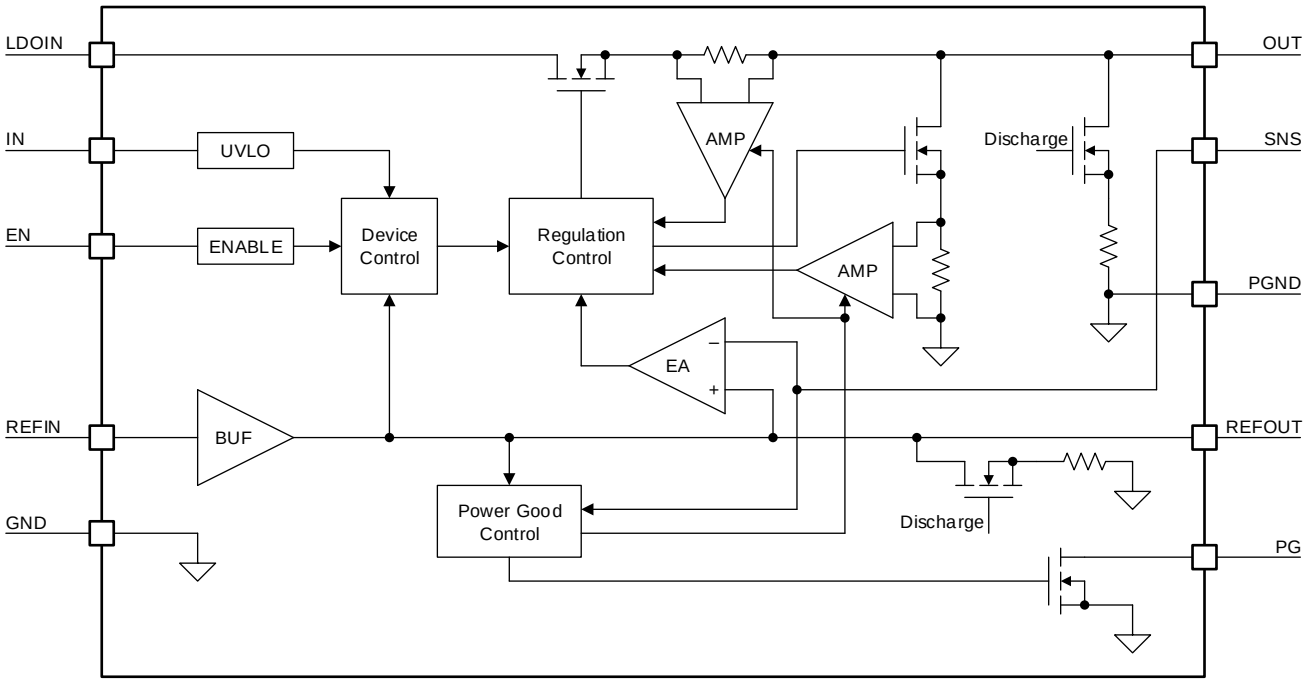


Figure 19 Functional Block Diagram

Feature Description

Sink and Source Regulator (OUT and SNS)

The TPL51201 series devices are 3-A sink and source DDR termination regulators specifically designed for the DDR applications with heavy space limitation. The TPL51201 series integrate a high-performance, low-dropout linear regulator with fast-feedback loop that can support fast load transient response with small ceramic capacitors. To get tight regulation tolerance, the remote sensing pin, SNS pin, must be connected to OUT pin through a separate trace from high current path.

Voltage Reference (REFIN and REFOUT)

The TPL51201 series uses the voltage at the REFIN pin as the reference voltage, and the output voltage at the REFOUT pin exactly follow the REFIN voltage within the tolerance of VREFOUT_TOL. When the TPL51201 series are configured for standard DDR applications, the voltage at the REFIN pin is divided through an external voltage divider from the DDR supply bus, VDDQ.

The TPL51201 series support the REFIN input voltage range from 0.5 V to 1.8 V. When the REFIN voltage is higher than rising UVLO threshold of REFIN and IN voltage is ready, there is voltage regulated at the REFOUT pin, which the REFOUT pin is independent with EN status.

Enable Control (EN)

The TPL51201 series integrate the high-active device enable control feature. Connect this pin to the GPIO of an external processor or digital logic control circuit to enable and disable the device.

Under-voltage Lockout (IN UVLO)

The TPL51201 series use an under-voltage lockout circuit to keep the regulator shut off until IN voltage exceeds the rising UVLO threshold of IN.

Power-Good Indicator (PG)

The TPL51201 series integrate an open-drain output power good indicator. After regulator startup, the PG pin keeps low impendence until the output voltage enters the power-good window, ±20% of REFOUT voltage. When output voltage enters the power-good window, the PG pin turns to high output impedance, and PG is pulled up to high-voltage level after 2-ms delay to indicate the output voltage is ready. It is recommended to connect a 100-kΩ pull-up resistor between PG pin and the pull-up voltage supply.

Over-Current Protection

The TPL51201 series integrate a constant over-current protection. When the output voltage exists the power-good window, ±20% of REFOUT voltage, the current-limit level reduces 50% of the full level. After the output voltage enters the power-good window, the current-limit level is released to the full level.

Over-Temperature Protection

The recommended operating junction temperature range is –40°C to 125°C. When the junction temperature is between 125°C and the thermal shutdown (TSD) threshold, the regulator can still work well, but it will reduce the device lifetime for long-term using.

The over-temperature protection works when the junction temperature exceeds the thermal shutdown (TSD) threshold, which turns off the regulator immediately. Until when the device cools down and the junction temperature falls below the thermal shutdown threshold minus thermal shutdown hysteresis, the regulator turns on again.

Application and Implementation

NOTE

Information in the following applications sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPL51201 series devices are 3-A sink and source DDR termination regulators specifically designed for the DDR applications. The following application schematic shows a typical usage of the TPL51201 series.

Typical Application

Adjustable Output Operation

Figure 20 shows the typical application schematic of the TPL51201 series in DDR4 applications.

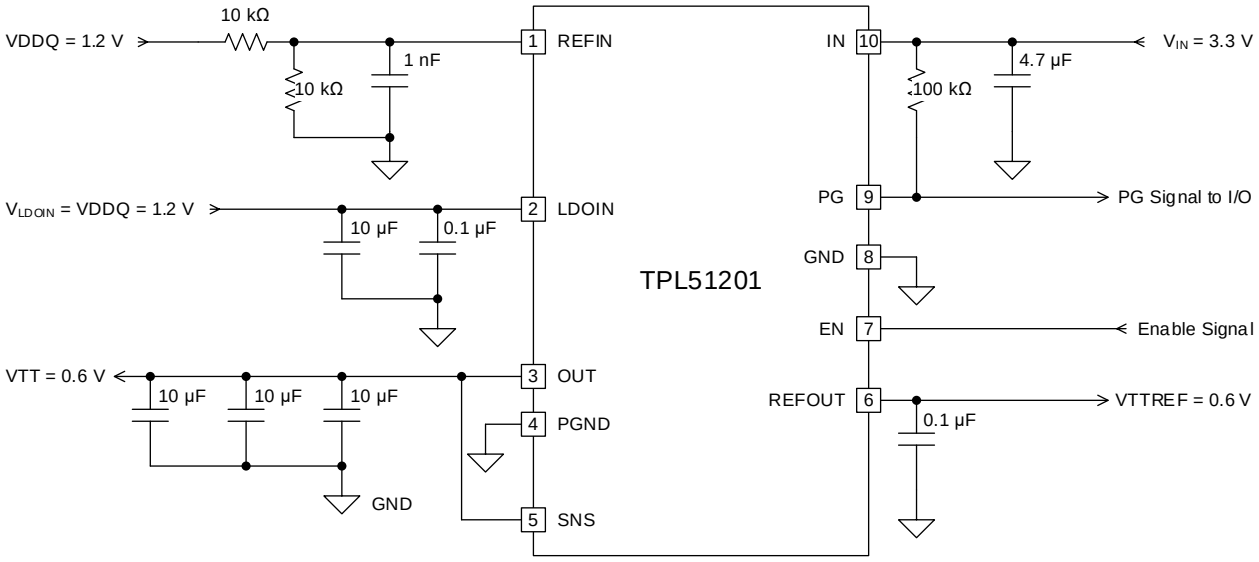


Figure 20 Typical Application Schematic

IN Input Capacitor

3PEAK recommends placing a 1-µF or greater capacitor with a 0.1-µF bypass capacitor in parallel close to IN pin to keep the input voltage stable. The voltage rating of the capacitors must be greater than the maximum input voltage.

LDOIN Input Capacitor

3PEAK recommends placing a 10-µF or greater capacitor with a 0.1-µF bypass capacitor in parallel close to LDOIN pin to keep the voltage stable during transient. More input capacitors are required if there are large output capacitors used at the OUT pin. It is suggested to place input capacitors with a half of the output capacitance value at the LDOIN pin.

OUT and SNS Output Capacitor

To ensure stable operation, the TPL51201 series requires output capacitors of 20 µF or greater. 3PEAK recommends selecting three 10-µF X5R-or X7R-type ceramic capacitor in parallel to minimize the equivalent series resistance (ESR) and equivalent series inductance (ESL). The output capacitors must be placed as close to the OUT pin as possible.

When using remote sense function, to prevent the instability issue caused by parasitic parameters of the long output power trace, it is recommended to keep total capacitance of C_{OUT} between 10 µF and 30 µF, and the total capacitance of the remote DDR termination bypass capacitors should be greater than that of $3\times C_{OUT}$.

Application Waveform

Test condition: VIN = VEN = 3.3 V; VLDOIN = 1.2 V, VREFIN = 0.6 V, IOUT = 1 A, CIN = 10 µF, and COUT = 3 x 10 µF.

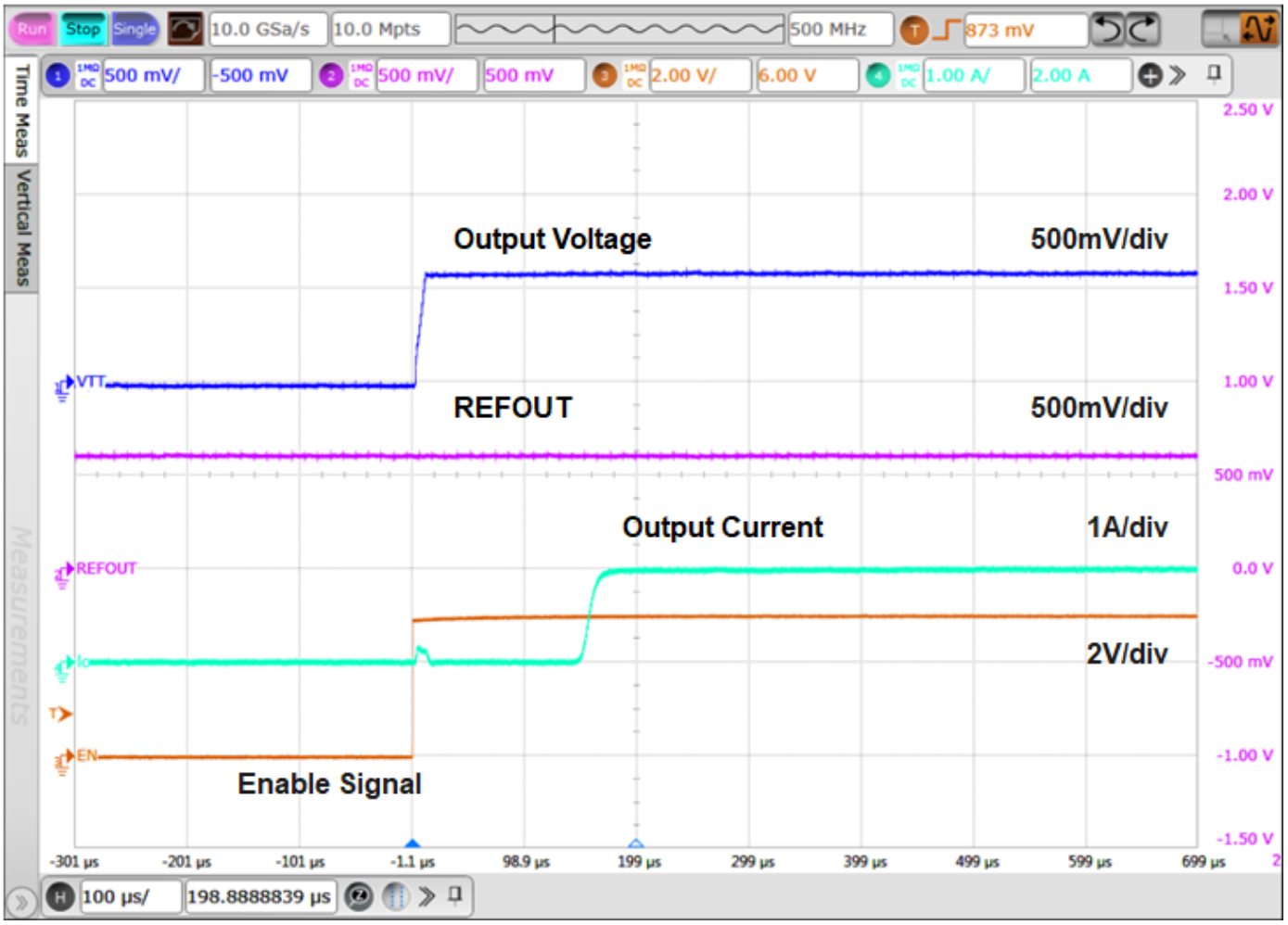


Figure 21 Output Voltage Startup Waveform

Power Dissipation

During normal operation, LDO junction temperature should not exceed 125°C. Using below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using Equation 1.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (1)$$

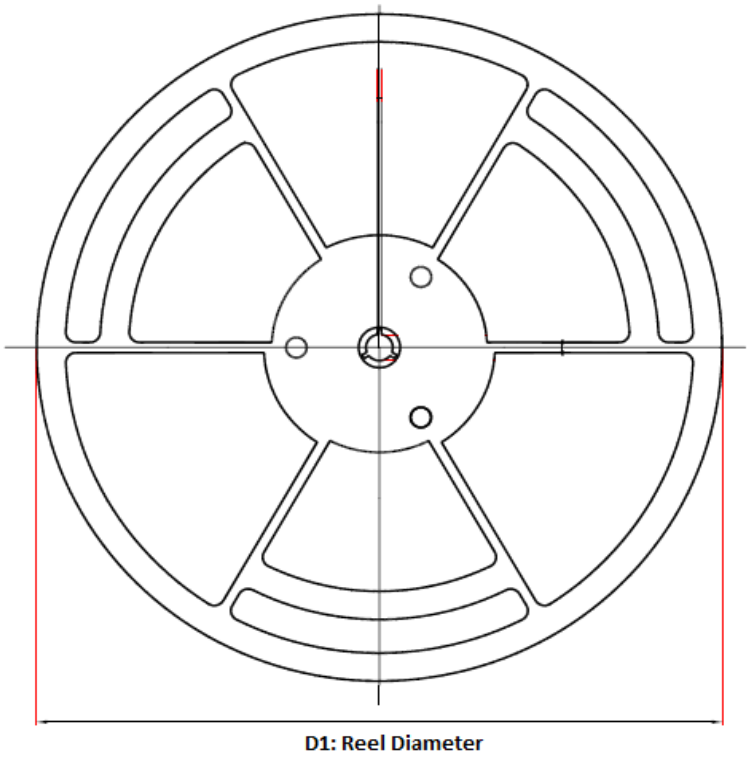
The junction temperature can be estimated using Equation 2. θ_{JA} is the junction-to-ambient thermal resistance.

$$T_J = T_A + P_D \times \theta_{JA} \quad (2)$$

Layout Requirements

- Both input capacitors and output capacitors must be placed as close to the device pins as possible.
- Suggest bypass the input pin to ground with a 0.1 μF bypass capacitor. The loop area formed by the bypass capacitor connection, voltage input pin and the ground pin of the system must be as small as possible.
- Suggest use wide trace lengths or thick copper weight to minimize I×R drop and heat dissipation.
- The GND pin and the PGND pin must be connected to the thermal pad with multiple thermal vias as many as possible connected to the internal ground planes.

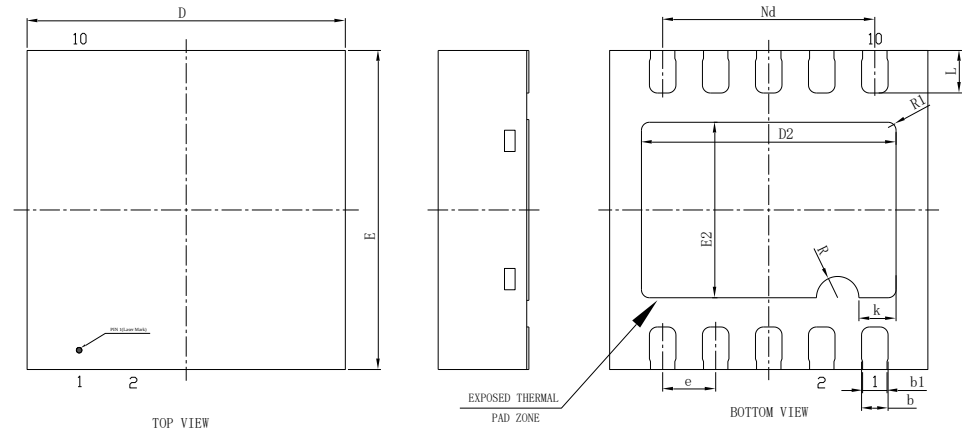
Tape and Reel Information



Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPL51201G-DF8R-S	3×3 DFN-10	330	17.6	3.3	3.3	1.1	8	12	Q2

Package Outline Dimensions

3×3 DFN-10



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1	0.23REF		
c	0.203REF		
D	2.90	3.00	3.10
D2	2.35	2.40	2.45
e	0.50BSC		
Nd	2.00BSC		
E	2.90	3.00	3.10
E2	1.60	1.65	1.70
L	0.35	0.40	0.45
R	0.20REF		
R1	0.075REF		
k	0.35REF		

** 特殊设计：D2和E2尺寸的公差是±0.05；
引脚根部缩小较少；

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