3-A Sink and Source DDR Termination Regulator

Features

- V_{IN} Voltage: Support 2.5-V, 3.3-V, and 5-V Power Rails
- V_{LDOIN} Voltage Range: 1.1 V to 3.5 V
- Flexible Input Voltage Tracking Directly from REFIN or through External Resistor Divider
- 3-A Sink and Source Current Capability for DDR Termination
- Integrated Power MOSFETs
- Output Remote Sensing
- Fast Load-Transient Response
- Open-Drain Power Good to Monitor OUT Regulation
- Built in Soft-Start and UVLO, Current Limit, and Thermal Shutdown Protection
- Support DDR, DDR2, DDR3, DDR3L, Low-Power DDR3 and DDR4 VTT Applications
- Operating Temperature Range: –40°C to +125°C
- Small Package DFN3×3-10
- Pb−Free and RoHS-Compliant

Applications

- Memory VTT Regulator for DDR, DDR2, DDR3, DDR3L, Low-Power DDR3 and DDR4
- Notebooks, Desktops, and Workstations
- Servers, Networking Equipment, and Datacenters
- Telecom and Base Station

Description

With the development of main processors in PCs and servers, more source double-data-rate (DDR) memories are required in the mainboard, where the input voltage becomes lower, and the space limitation becomes higher.

The TPL51200 is a series of the 3-A sink and source DDR termination regulators, specifically designed for DDR applications with heavy space limitations. The TPL51200 series implements a fast load-transient response and only requires a minimum output capacitance of 20 µF.

The TPL51200 series supports a remote-sensing function and meets all power requirements for DDR VTT bus termination. In addition, the TPL51200 series provides an open-drain PG signal for VTT regulation indication, and an EN signal that can be used to discharge VTT for DDR applications.

The TPL51200 series is available in the thermally efficient DFN3×3-10 package with a thermal pad. The operating temperature range is from –40°C to +125°C.

Typical Application Schematic

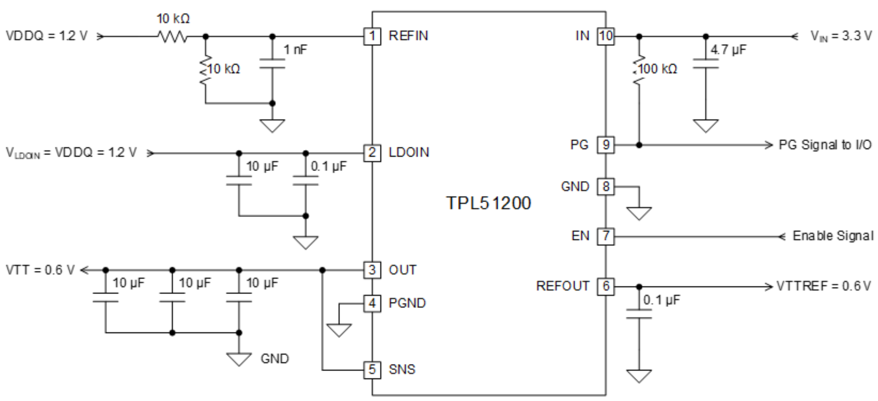


Table of Contents

Product Family Table

Part Number	Output Current	Orderable Number	Package	Transport Media, Quantity	MSL	Marking information
TPL51200	3 A	TPL51200-DF8R	DFN3×3-10	4000	3	L200

Revision History

Date	Revision	Notes
2019-11-30	Rev.Pre.0	Preliminary version.
2020-05-15	Rev.A.0	Initial released.
2020-12-22	Rev.A.1	1. Added Tape and Reel Information. 2. Updated Package Outline Dimensions.
2024-03-25	Rev.A.2	Updated Thermal Information.
2024-11-14	Rev.A.3	1. Updated to a new datasheet format. 2. Corrected "VIN" to "VLDOIN" in the power dissipation calculation equation.

Pin Configuration and Functions

TPL51200 Series
DFN3×3-10
Top View

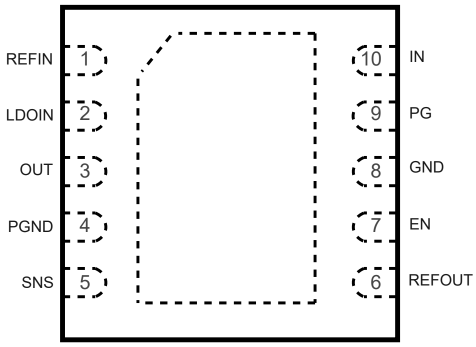


Table 1. Pin Functions

Pin No.	Name	I/O	Description
1	REFIN	I	Reference input pin. For DDR applications, set to V_{DDQ} / 2 through a resistor divider.
2	LDOIN	I	LDO power supply input pin.
3	OUT	O	LDO output voltage pin. A total capacitance of 20-μF or larger from OUT to GND (as close as possible to the OUT pin) is required to ensure regulator stability.
4	PGND	–	Power ground pin. Connect the PGND pin to the PCB ground plane directly.
5	SNS	I	LDO output voltage sense pin. Connect SNS to the remote DDR termination bypass capacitors to get accurate remote feedback sensing of OUT voltage.
6	REFOUT	O	Reference output pin. Connect to GND through a 0.1-μF to 1-μF ceramic capacitor.
7	EN	I	Regulators enable pin. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. For automatic startup, connect EN to V_{IN} directly.
8	GND	–	Ground reference pin. Connect the GND pin to the PCB ground plane directly.
9	PG	O	Open-drain power-good output pin.
10	IN	I	Regulator power supply input pin. A 1-μF or larger ceramic capacitor from IN to GND (as close as possible to the IN pin) is required to reduce the jitter from the previous-stage power supply.

(1) The exposed PAD must be connected to a large-area ground plane to maximize thermal performance.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
EN, IN, LDOIN, PG, REFIN, SNS		–0.3	6	V
PGND to GND		–0.3	0.3	V
OUT, REFOUT		–0.3	3.6	V
T_J	Junction Temperature Range	–40	150	°C
T_{STG}	Storage Temperature Range	–55	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
(2) All voltage values are with respect to GND.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	±2000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	±1500	V

Recommended Operating Conditions

Parameter		Min	Max	Unit
IN	Regulator Input Voltage	2.375	5.5	V
LDOIN	LDO Input Voltage	–0.1	3.5	V
EN	Regulator Enable Voltage	–0.1	3.5	V
OUT	LDO Output Voltage	–0.1	3.5	V
SNS	LDO Output Sense Voltage	–0.1	3.5	V
REFIN	Reference Input Voltage	0.5	1.8	V
REFOUT	Reference Output Voltage	–0.1	1.8	V
PG	Power-Good Pull-Up Voltage	–0.1	3.5	V
PGND	Power Ground Voltage to GND	–0.1	0.1	V
T_J	Junction Temperature Range	–40	125	°C

Thermal Information

Package	θ_{JA}	θ_{JB}	$\theta_{JC,TOP}$	Unit
DFN3x3-10	42.07	10.08	75.14	°C/W

Electrical Characteristics

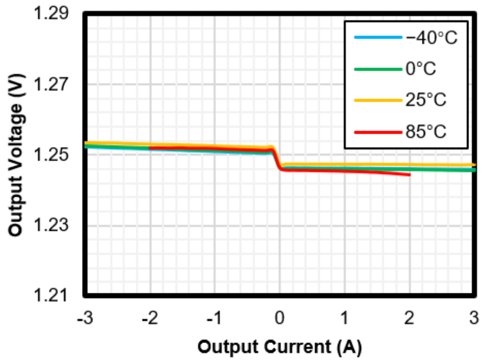
All test conditions: T_J = –40°C to +125°C (typical value at T_J = +25°C), V_{IN} = V_{EN} = 3.3 V, V_{LDOIN} = 1.8 V, V_{REFIN} = 0.9 V, V_{SNS} = 0.9 V, C_{IN} = 10 µF, and C_{OUT} = 3 x 10 µF, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply Input Voltage and Current						
V_{IN}	Input Supply Voltage Range		2.375		5.5	V
V_{LDOIN}	LDO Input Voltage Range				3.5	V
$UVLO_{IN}$	Input Supply UVLO	T_A = 25°C, V_{IN} rising		2.3	2.375	V
	Hysteresis			50		mV
I_{IN}	Input Supply Current of IN	T_A = 25°C, V_{EN} = 3.3 V, I_{OUT} = 0 mA		0.8	1	mA
I_{IN_SD}	Shutdown Current of IN	T_A = 25°C, V_{EN} = 0 V, V_{REFIN} = 0 V, I_{OUT} = 0 mA		65	80	µA
		T_A = 25°C, V_{EN} = 0 V, V_{REFIN} > 0.4 V, I_{OUT} = 0 mA		200	400	µA
I_{LDOIN}	Input Current of LDOIN	T_A = 25°C, V_{EN} = 3.3 V, I_{OUT} = 0 mA		1	50	µA
I_{LDOIN_SD}	Shutdown Current of LDOIN	T_A = 25°C, V_{EN} = 0 V, I_{OUT} = 0 mA		1	50	µA
Reference Input and Output						
V_{REFIN}	Reference Input Voltage		0.5		1.8	V
$UVLO_{REFIN}$	Reference Input UVLO	T_A = 25°C, V_{REFIN} rising	360	390	420	mV
	Hysteresis			20		mV
I_{REFIN}	Input Current of REFIN	V_{EN} = 3.3 V		1		µA
V_{REFOUT}	Reference Output Voltage			V_{REFIN}		V
V_{REFOUT_TOL}	Tolerance of REFOUT to REFIN	−1 mA ≤ I_{REFOUT} ≤ 1 mA, 0.5 V ≤ V_{REFIN} ≤ 1.8 V	−12		12	mV
		−10 mA ≤ I_{REFOUT} ≤ 10 mA, 0.5 V ≤ V_{REFIN} ≤ 1.8 V	−15		15	mV
I_{REFOUT_SRCL}	Source Current Limit of REFOUT	V_{REFOUT} = 0.5 V	10	60		mA
I_{REFOUT_SNKL}	Sink Current Limit of REFOUT	V_{REFOUT} = 1.5 V	10	60		mA
Regulated Output Voltage and Current						
V_{OUT}	Output Voltage	V_{REFOUT} = 1.25 V (DDR1), I_{OUT} = 0 A		1.25		V
		Tolerance	−15		15	mV
		V_{REFOUT} = 0.9 V (DDR2), I_{OUT} = 0 A		0.9		V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Tolerance	−15		15	mV
		V_{REFOUT} = 0.75 V (DDR3), I_{OUT} = 0 A		0.75		V
		Tolerance	−15		15	mV
		V_{REFOUT} = 0.675 V (DDR3L), I_{OUT} = 0 A		0.675		V
		Tolerance	−15		15	mV
		V_{REFOUT} = 0.6 V (DDR4), I_{OUT} = 0 A		0.6		V
		Tolerance	−15		15	mV
ΔV_{OUT}	Tolerance of OUT to REFOUT	–2 A < I_{OUT} < 2 A	−25		25	mV
I_{OUT_SRCL}	Source Current Limit of OUT	V_{SNS} = 90% × V_{REFOUT}	3		4.5	A
I_{OUT_SNKL}	Sink Current Limit of OUT	V_{SNS} = 110% × V_{REFOUT}	3.2		5.5	A
R_{DIS}	Discharge Resistance	T_A = +25°C, V_{REFIN} = 0 V V_{OUT} = 0.3 V, V_{EN} = 0 V		12		Ω
Enable Control						
V_{EN}	EN High-Level Input Voltage	Device enable	1.7			V
	EN Low-Level Input Voltage	Device disable			0.5	V
	Hysteresis			0.25		V
I_{EN}	Leakage Current of EN	T_A = 25°C V_{EN} = 0 V to 6.5 V	–1		1	μA
Power Good						
V_{PG}	PG Lower Threshold	With respect to REFOUT	–23.5	–20	–17.5	%
	PG Upper Threshold	With respect to REFOUT	17.5	20	23.5	%
	Hysteresis			5		%
I_{PG}	Current Leakage of PG				1	μA
$V_{OL(PG)}$	PG Low-Level Output Voltage	Source 4 mA to PG pin			0.4	V
$t_{DLY(PG)}$	PG Start-up Delay	Start-up rising edge, V_{SNS} within 15% of V_{REFOUT}		2		ms
$t_{DLY(PG\_B)}$	PG Start-up Bad Delay	V_{SNS} is beyond the ±20% PG trip threshold		10		μs
Temperature Range						
T_{SD}	Thermal Shutdown Threshold	Temperature increasing		155		°C
	Hysteresis			25		°C
T_J	Operating Junction Temperature		–40		125	°C

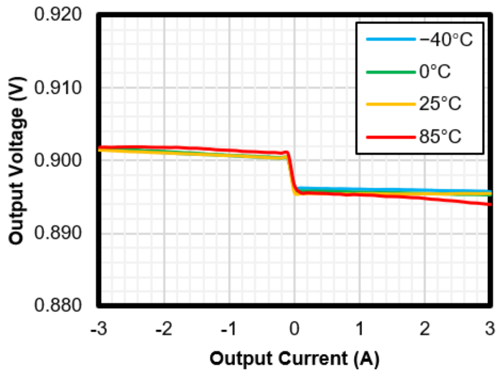
Typical Performance Characteristics

All test conditions: T_J = –40°C to +125°C (typical value at T_J = +25°C), V_{IN} = V_{EN} = 3.3 V, V_{LDOIN} = 1.8 V, V_{REFIN} = 0.9 V, V_{SNS} = 0.9 V, C_{IN} = 10 μF, and C_{OUT} = 3 x 10 μF, unless otherwise noted.



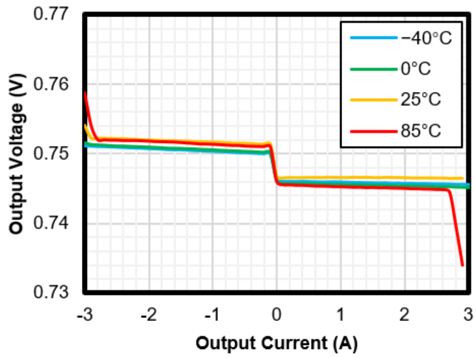
V_{IN} = 3.3 V DDR

Figure 1. OUT Load Regulation



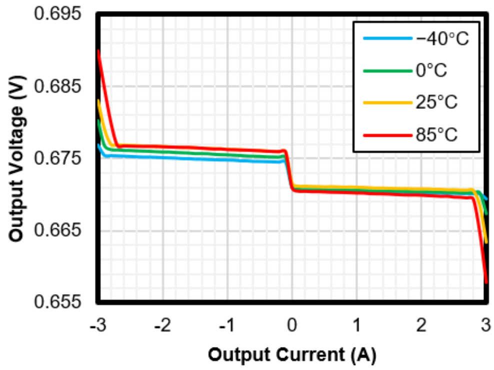
V_{IN} = 3.3 V DDR2

Figure 2. OUT Load Regulation



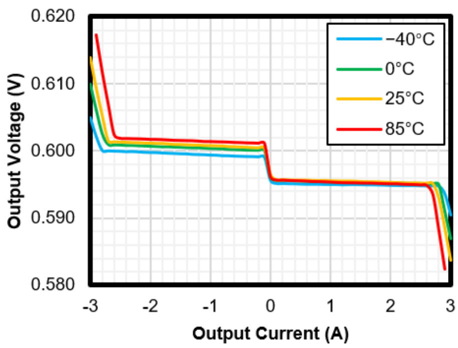
V_{IN} = 3.3 V DDR3

Figure 3. OUT Load Regulation



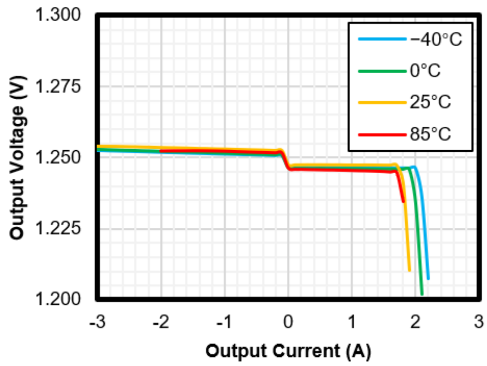
V_{IN} = 3.3 V DDR3L

Figure 4. OUT Load Regulation



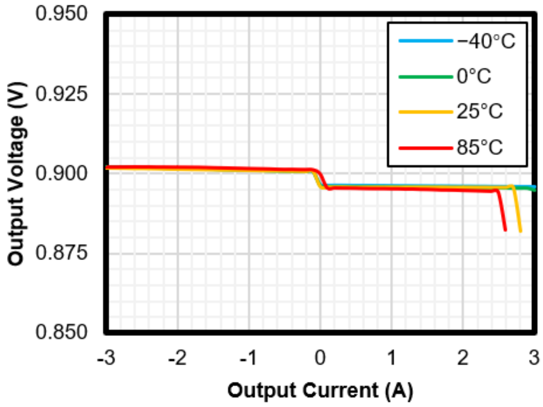
V_{IN} = 3.3 V LP DDR3 or DDR4

Figure 5. OUT Load Regulation



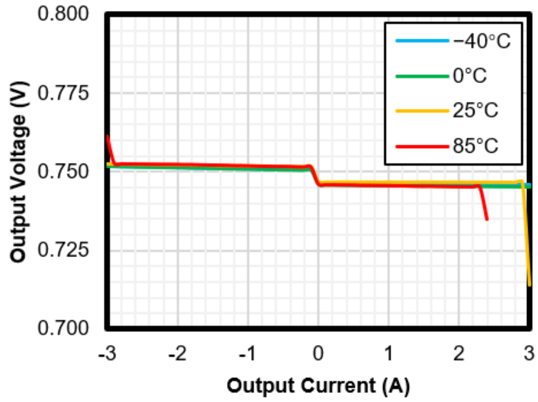
V_{IN} = 2.5 V DDR

Figure 6. OUT Load Regulation



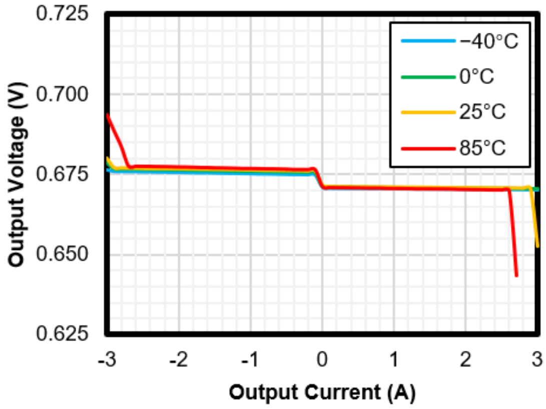
V_{IN} = 2.5 V DDR2

Figure 7. OUT Load Regulation



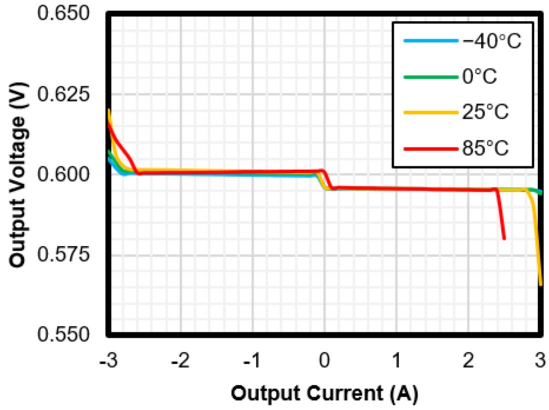
V_{IN} = 2.5 V DDR3

Figure 8. OUT Load Regulation



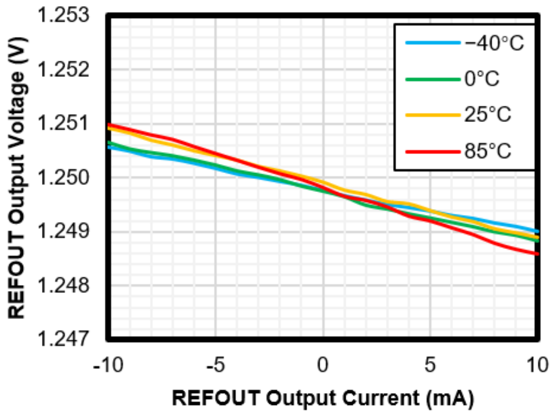
V_{IN} = 2.5 V DDR3L

Figure 9. OUT Load Regulation



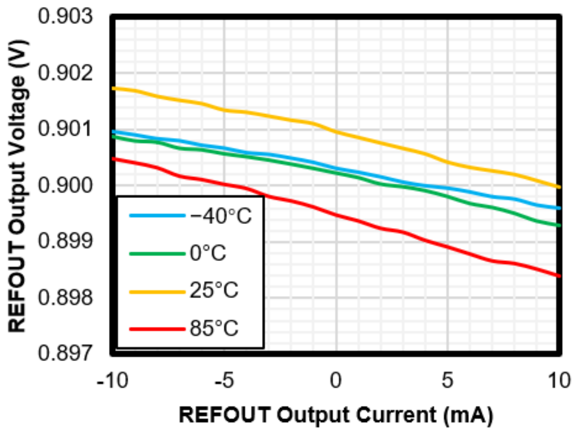
V_{IN} = 2.5 V LP DDR3 or DDR4

Figure 10. OUT Load Regulation



DDR

Figure 11. REFOUT Load Regulation



DDR2

Figure 12. REFOUT Load Regulation

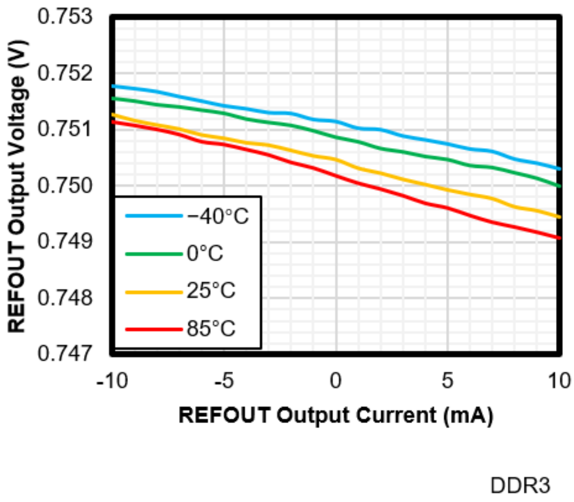


Figure 13. REFOUT Load Regulation

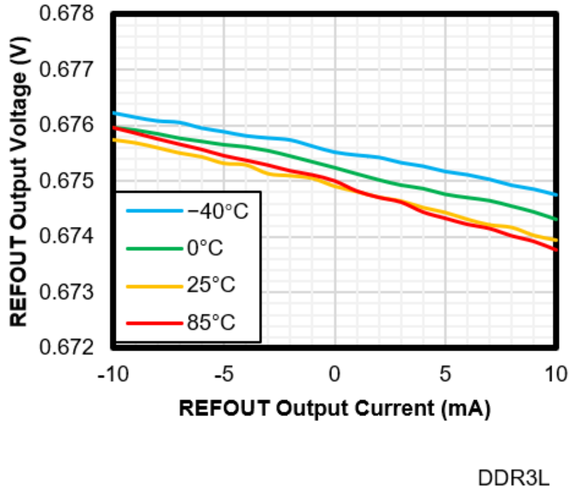


Figure 14. REFOUT Load Regulation

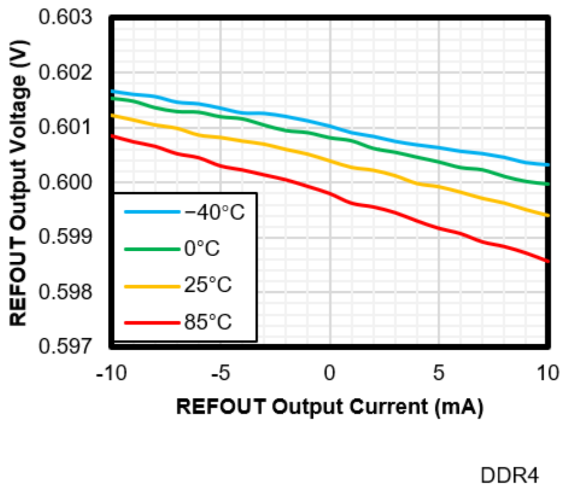


Figure 15. REFOUT Load Regulation

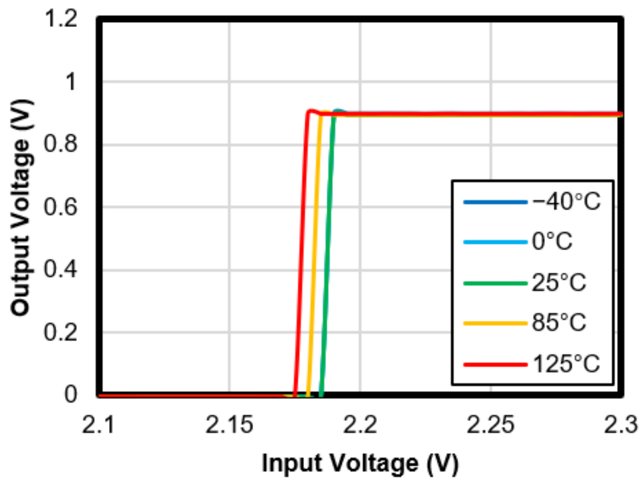


Figure 16. UVLO Rising

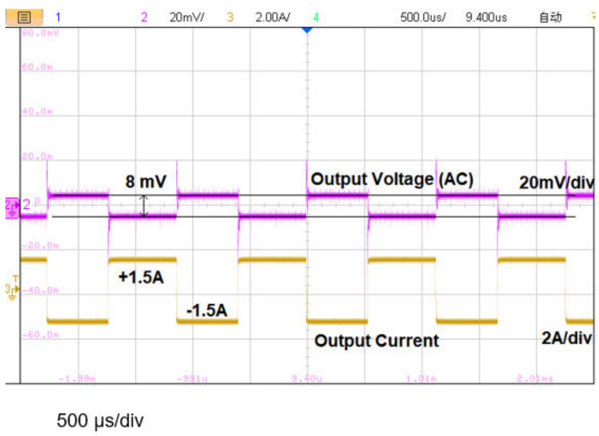


Figure 17. Load Transient

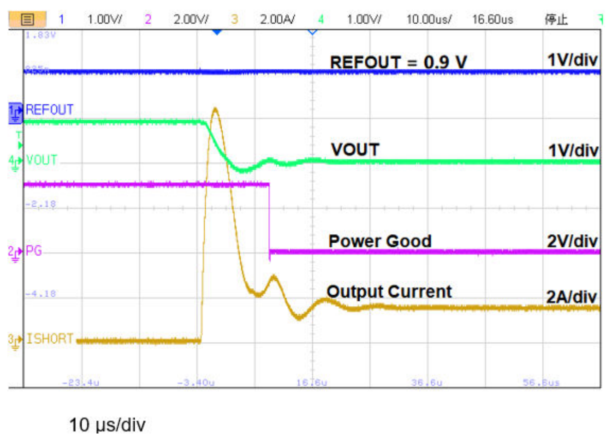


Figure 18. Output Short-to-GND Protection

Detailed Description

Overview

The TPL51200 is a series of 3-A sink and source DDR termination regulators specifically designed for DDR applications with heavy space limitations. The TPL51200 series implements a fast load-transient response and only requires a minimum output capacitance of 20 μF.

The TPL51200 series supports a remote-sensing function and meets all power requirements for DDR VTT bus termination. In addition, the TPL51200 series provides an open-drain PG signal for VTT regulation indication, and an EN signal that can be used to discharge VTT for DDR1 to DDR4 applications.

Functional Block Diagram

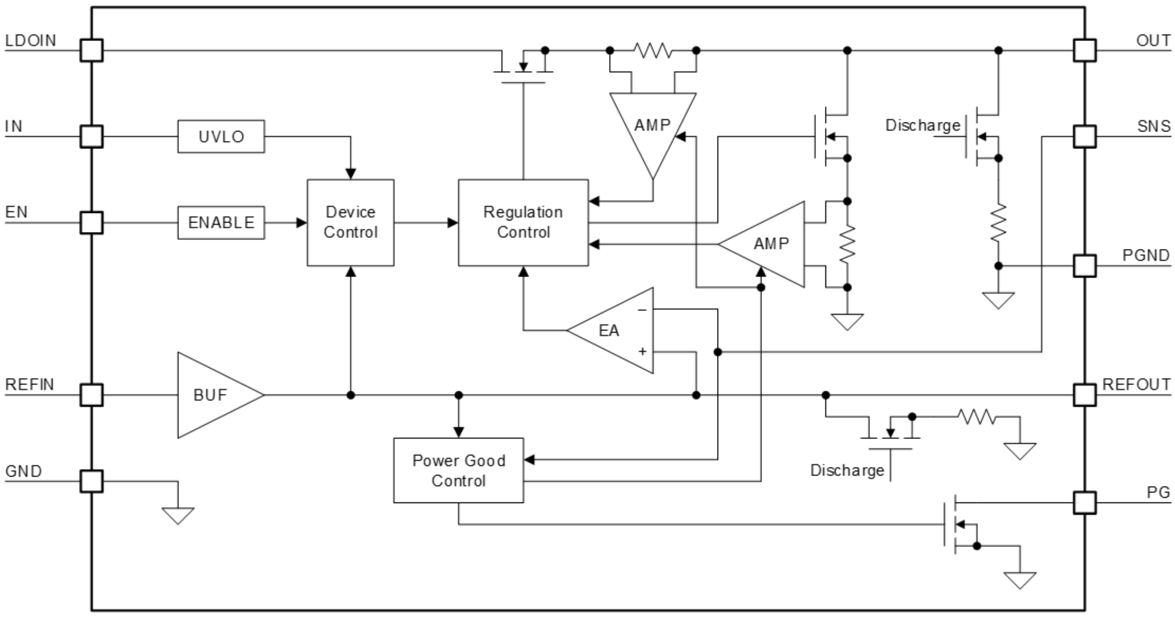


Figure 19. Functional Block Diagram

Feature Description

Sink and Source Regulator (OUT and SNS)

The TPL51200 is a series of 3-A sink and source DDR termination regulators specifically designed for DDR applications with heavy space limitations. The TPL51200 series integrates a high-performance and low-dropout linear regulator with a fast-feedback loop that supports fast load transient response with small ceramic capacitors. To get tight regulation tolerance, the remote sensing pin, the SNS pin, must be connected to the OUT pin through a separate trace from the high current path.

Voltage Reference (REFIN and REFOUT)

The TPL51200 series uses the voltage at the REFIN pin as the reference voltage, and the output voltage at the REFOUT pin exactly follows the REFIN voltage within the tolerance of V_{REFOUT_TOL}. When the TPL51200 series is configured for standard DDR applications, the voltage at the REFIN pin is divided through an external voltage divider from the DDR supply bus, V_{DDQ}.

The TPL51200 series supports the REFIN input voltage range from 0.5 V to 1.8 V. When the REFIN voltage is higher than the rising UVLO threshold of REFIN and IN voltage is ready, there is voltage regulated at the REFOUT pin, which the REFOUT pin is independent with EN status.

Enable Control (EN)

The TPL51200 series integrates a high-active device enable control feature. Connect this pin to the GPIO of an external processor or digital logic control circuit to enable and disable the device.

Under-Voltage Lockout (IN UVLO)

The TPL51200 series uses an under-voltage lockout circuit to keep the regulator shut off until the IN voltage exceeds the rising UVLO threshold of IN.

Power-Good Indicator (PG)

The TPL51200 series integrates an open-drain output power good indicator. After regulator startup, the PG pin keeps low impendence until the output voltage enters the power-good window, ±20% of REFOUT voltage. When output voltage enters the power-good window, the PG pin turns to high output impedance, and PG is pulled up to a high-voltage level after a 2-ms delay indicating the output voltage is ready. It is recommended to connect a 100-kΩ pull-up resistor between the PG pin and the pull-up voltage supply.

Over-Current Protection

The TPL51200 series integrates constant over-current protection. When the output voltage exists the power-good window, ±20% of REFOUT voltage, the current-limit level reduces 50% of the full level. After the output voltage enters the power-good window, the current-limit level is released to the full level.

Over-Temperature Protection

The recommended operating junction temperature range is from –40°C to 125°C. When the junction temperature is between 125°C and the thermal shutdown (TSD) threshold, the regulator can still work well, but the device lifetime for long-term use is reduced.

The over-temperature protection works when the junction temperature exceeds the thermal shutdown (TSD) threshold, which turns off the regulator immediately. When the device cools down and the junction temperature falls below the thermal shutdown threshold minus thermal shutdown hysteresis, the regulator turns on again.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPL51200 is a series of 3-A sink and source DDR termination regulators specifically designed for DDR applications. Figure 20 shows a typical usage of the TPL51200 series.

Typical Application

Adjustable Output Operation

Figure 20 shows the typical application schematic of the TPL51200 series in DDR4 applications.

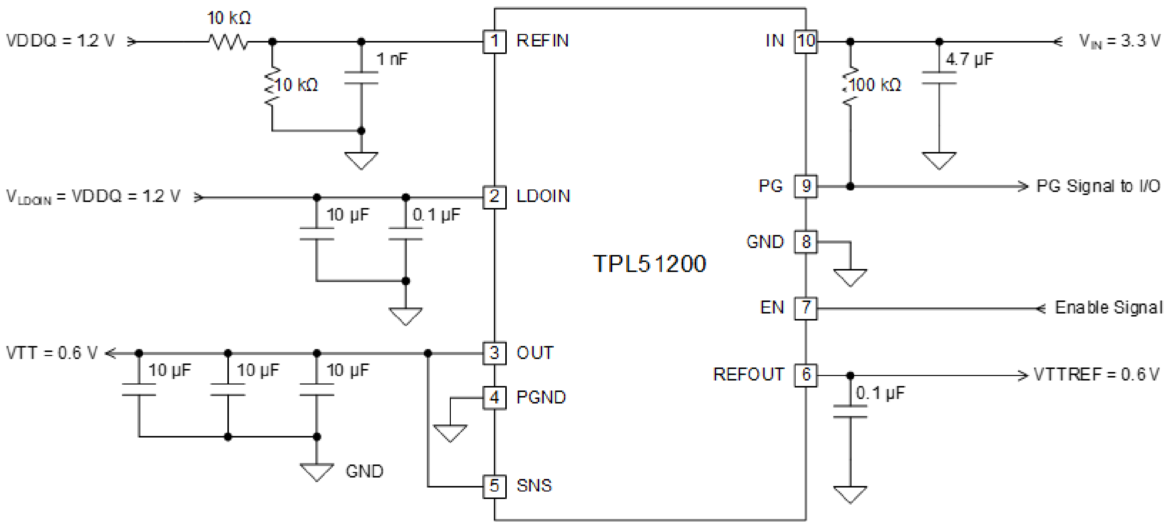


Figure 20. Typical Application Schematic

IN Input Capacitor

3PEAK recommends placing a 1-µF or greater capacitor with a 0.1-µF bypass capacitor in parallel close to the IN pin to keep the input voltage stable. The voltage rating of the capacitors must be greater than the maximum input voltage.

LDOIN Input Capacitor

3PEAK recommends placing a 10-µF or greater capacitor with a 0.1-µF bypass capacitor in parallel close to the LDOIN pin to keep the voltage stable during transient. More input capacitors are required if large output capacitors are used at the OUT pin. It is suggested to place input capacitors with half of the output capacitance value at the LDOIN pin.

Output Capacitor

To ensure stable operation, the TPL51200 series requires output capacitors of 20 µF or greater. 3PEAK recommends selecting three 10-µF X5R-or X7R-type ceramic capacitors in parallel to minimize the equivalent series resistance (ESR) and equivalent series inductance (ESL). The output capacitors must be placed as close to the OUT pin as possible.

Power Dissipation

During normal operation, the LDO junction temperature should not exceed 125°C. Use the equations below to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using Equation 1.

$$P_D = (V_{LDOIN} - V_{OUT}) \times I_{OUT} + V_{LDOIN} \times I_{GND} \quad (1)$$

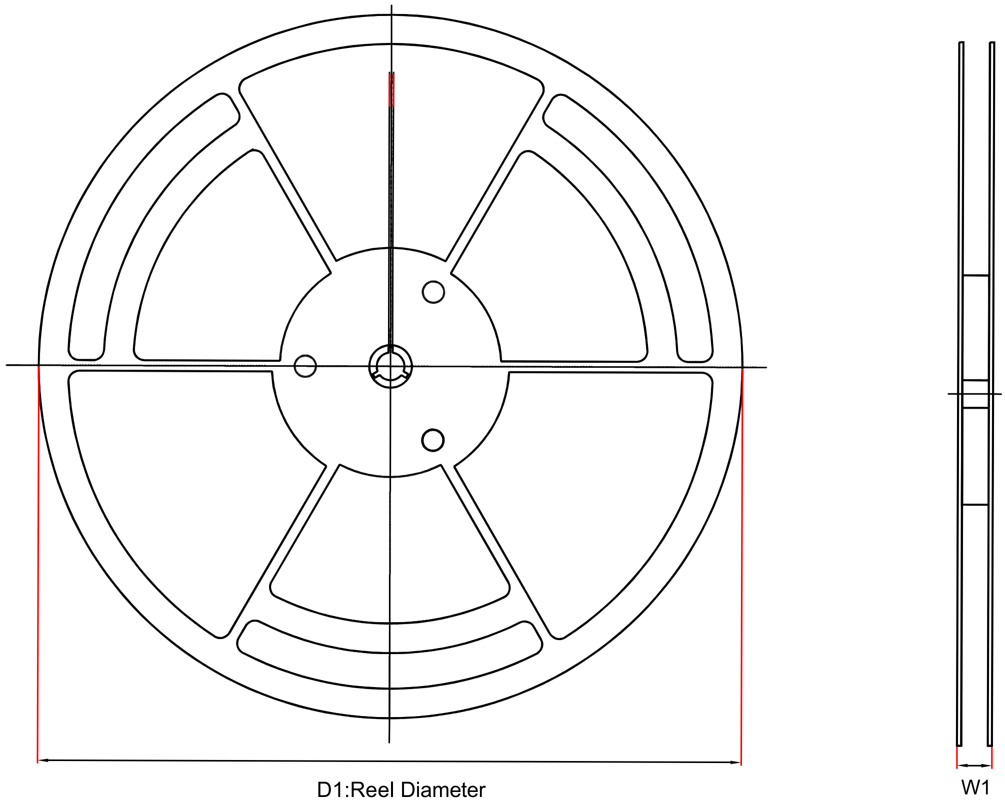
The junction temperature can be estimated using Equation 2. θ_{JA} is the junction-to-ambient thermal resistance.

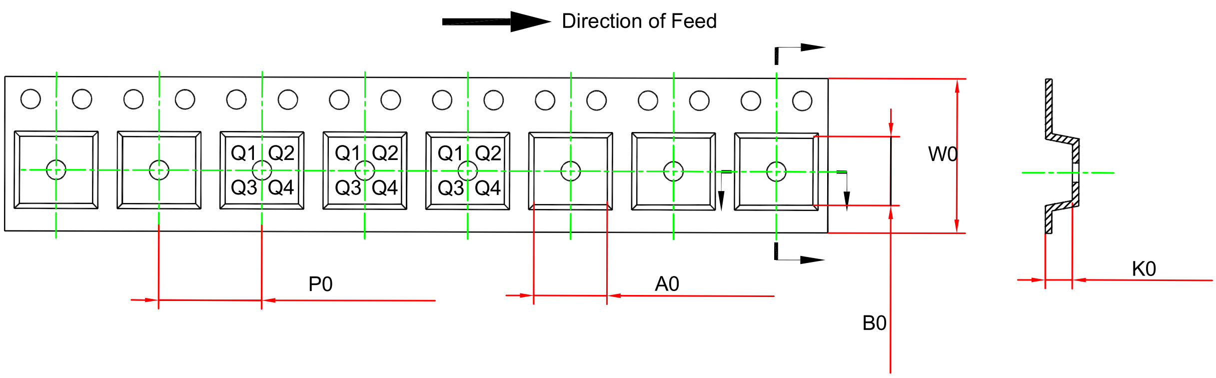
$$T_J = T_A + P_D \times \theta_{JA} \quad (2)$$

Layout Requirements

- Both input/output capacitors must be placed as close to the device pins as possible.
- Suggest bypassing the input pin to ground with a 0.1 µF bypass capacitor. The loop area formed by the bypass capacitor connection, voltage input pin and the ground pin of the system must be as small as possible.
- Suggest using wide trace lengths or thick copper weight to minimize I×R drop and heat dissipation.
- The GND pin and the PGND pin must be connected to the thermal pad with as many multiple thermal vias as possible connected to the internal ground planes.

Tape and Reel Information



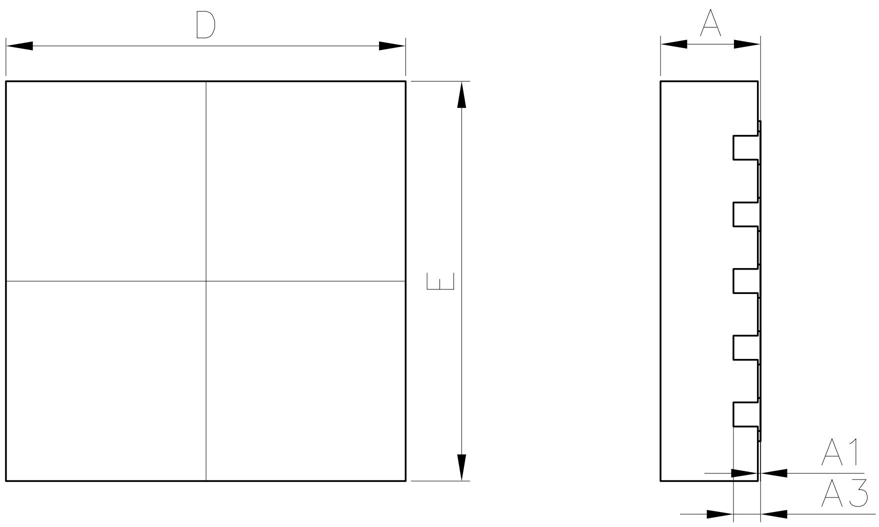


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPL51200-DF8R	DFN3×3-10	330	17.6	3.3	3.3	1.1	8	12	Q2

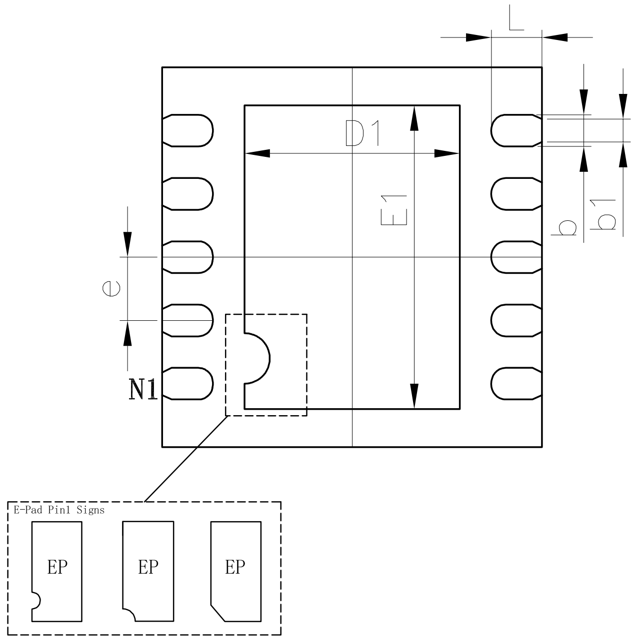
Package Outline Dimensions

DFN3X3-10

Package Outline Dimensions DF8(DFN3X3-10-A)



Top View Side View



Bottom View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.200	0.300	0.008	0.012
b1	0.180 REF		0.007 REF	
A3	0.150	0.250	0.006	0.010
D	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E	2.900	3.100	0.114	0.122
E1	2.300	2.500	0.091	0.098
e	0.500 BSC		0.020 BSC	
L	0.325	0.475	0.013	0.019

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

IMPORTANT NOTICE AND DISCLAIMER

Performance Information. Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

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