4-Channel Power Supply Sequencing and Supervisory Circuits

Features

- Input Voltage Range 2 V to 5.5 V
- Sustain up to 22 V Input with Shunt Reference Structure
- Shunt Reference Output Capability up to 15 mA
- Four-Channel Power Supply Monitor and Sequence Control
  - 3.5% Accurate Adjustable Threshold Monitors Voltages down to 0.98V for Each Channel
  - Independent Channel Enable/Disable Control
  - Independent Channel Adjustable Time by Capacitor
  - Open Drain Output
- Global Enable Control All Channels
- Power Good Indication for All Channels
- 5% High Accuracy of Sequence Timing
- QFN3.5x3.5-20 Package

Applications

- Communications
- Servers and Networking Elements
- Multiple Power Supply Sequencing
- Microcontroller Power Sequencing

Description

TPK1034 is a low voltage four-channel power monitor and sequencer. The power supply range is 2 V to 5.5 V, while if the shunt reference is enabled, the TPK1034 can sustain up to 22 V supply voltage. Each channel has an independent and adjustable threshold that can monitor voltage down to 0.98 V. If the monitored voltage falls below the threshold, the corresponding output is low. If the monitored voltage rises above the threshold, the output turns high after a capacitor-set delay time, the channel output is open-drain configuration.

With the power monitor function, the TPK1034 can achieve power sequencing control, and the capacitor of each channel can adjust the sequencing timing.

TPK1034 has an overall enable control for all channel outputs. When overall enable is active, each channel can be controlled by the corresponding enable. The overall enable control can disable all channel outputs by turning channel output low in a fixed sequence from channel 4 to channel 3, then channel 2 and channel 1. There is a delay time before each channel outputs low, which can be adjustable by another capacitor.

TPK1034 also includes a power good indication with open-drain active high to indicate all channels output high.

Typical Application Circuit

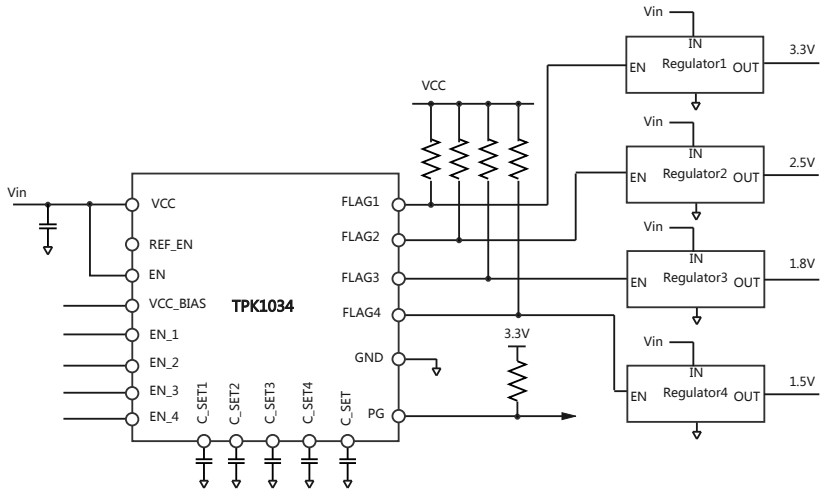


Table of Contents

Product Family Table

Order Number	MSL	MPQ	Marking	Package
TPK1034-QF6R-S	1	4000	K1034	QFN3.5x3.5-20

Revision History

Date	Revision	Notes
2024-9-30	Rev.A.0	Initial release

Pin Configuration and Functions

TPK1034
Top View

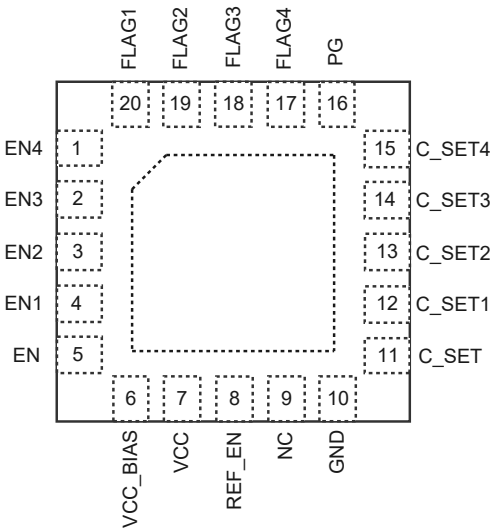


Table 1. Pin Functions: TPK1034

Pin No.	Name	I/O	Description
1	EN4	I	Channel 4 power monitor or channel enable control. If the voltage on this pin falls below the internal falling threshold, FLAG4 output is low. If the voltage on this pin rises above the rising threshold, FLGA4 output is high after delay time programmed by the capacitor on C_SET4.
2	EN3	I	Channel 3 power monitor or channel enable control. If the voltage on this pin falls below the internal falling threshold, FLAG3 output is low. If the voltage on this pin rises above the rising threshold, FLGA3 output is high after the delay time programmed by the capacitor on C_SET3.
3	EN2	I	Channel 2 power monitor or channel enable control. If the voltage on this pin falls below the internal falling threshold, FLAG2 output is low. If the voltage on this pin rises above the rising threshold, FLGA2 output is high after the delay time programmed by the capacitor on C_SET2.
4	EN1	I	Channel 1 power monitor or channel enable control. If the voltage on this pin falls below the internal falling threshold, FLAG1 output is low. If the voltage on this pin rises above the rising threshold, FLGA1 output is high after the delay time programmed by the capacitor on C_SET1.
5	EN	I	Overall EN Control. Drive EN high, then each channel can be used.

Pin No.	Name	I/O	Description
6	VCC_BIAS	I	Bias Voltage before VCC power on. Provide a bias voltage on this pin to pull the Flag low before VCC power on.
7	VCC	I	Input power supply.
8	REF_EN	I	Shunt reference enable input. Leave it not connected if used, connect to VCC if not used.
9	NC	-	Not Connected.
10	GND	GND	Ground.
11	C_SET	O	Overall delay time set pin. Connect a capacitor from C_SET to GND to set the all channels power down delay.
12	C_SET1	O	Delay time set pin 1. Connect a capacitor from C_SET1 to GND to set the FLAG1 high delay time.
13	C_SET2	O	Delay time set pin 2. Connect a capacitor from C_SET2 to GND to set the FLAG1 high delay time.
14	C_SET3	O	Delay time set pin 3. Connect a capacitor from C_SET3 to GND to set the FLAG1 high delay time.
15	C_SET4	O	Delay time set pin 4. Connect a capacitor from C_SET4 to GND to set the FLAG1 high delay time.
16	PG	O	Power Good
17	FLAG4	O	Channel 4 output.
18	FLAG3	O	Channel 3 output.
19	FLAG2	O	Channel 2 output.
20	FLAG1	O	Channel 1 output.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
Input	VCC, EN, EN1, EN2, EN3, EN4, VCC_BIAS, REF_EN to GND	−0.3	6	V
Output	C_SET, C_SET1, C_SET2, C_SET3, C_SET4, PG, FLAG1, FLAG2, FLAG3, FLAG4	−0.3	6	V
T_J	Maximum Junction Temperature	−40	150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.
(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	2000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Thermal Information

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
QFN3.5x3.5-20	34.1	8.1	20.8	°C/W

Electrical Characteristics

All test conditions: V_{CC}=2V~5.5V, T_A=40℃ to 125℃, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Power Supply						
V_{CC}	Input Supply Voltage		2		5.5	V
I_Q	Operation Quiescent Current	V_{CC} = 5 V, REF is disabled			250	μA
		V_{CC} = 3.3 V, REF is disabled			250	μA
V_{REF}	Shunt Reference Voltage	VCC as shunt reference output voltage when shunt reference is enabled	4.85	5	5.15	V
I_{REF}	Reference Output Capability				15	mA
UVLO	Under Voltage Lockout	Vcc rising		1.8		V
UVLO_HYS				0.2		V
REF_EN						
V_{REF_EN}	REF_EN High Threshold	REF_EN rising		3.85		V
	REF_EN Low Threshold	REF_EN falling		1.2		V
R_{REF_EN}	REF_EN Internal Pulldown			500		kΩ
Enable and Monitor Threshold						
V_{IH_EN}	EN High Threshold Voltage	EN rising	1.193	1.23	1.267	V
$V_{IH\_EN\_HYS}$	EN Hysteresis	EN falling	0.2	0.24		V
R_{EN}	EN Pull-down Resistor			550		kΩ
t_{GR_EN}	EN Glitch Rejection			500		ns
V_{IN_ENx}	ENx Fall Threshold Voltage	ENx falling, x = 1,2,3,4	0.943	0.983	1.022	V
$V_{IH\_ENx\_HYS}$	ENx Hysteresis	EN rising, x = 1,2,3,4		0.23		V
R_{ENx}	ENx Pull-down Resistor	x = 1,2,3,4		550		kΩ
t_{GR_ENx}	ENx Glitch Rejection	x = 1,2,3,4		500		ns
Flag/PG Output						
I_{LKG_FLAGx}	FLAGx Leakage Current	V_{FLAGx}=5 V, x = 1, 2, 3, 4			1	μA
V_{OL_FLAGx}	FLAGx Output Low	I_{FLAGx}= 3 mA, x=1, 2, 3, 4, VCC > 1.2 V			0.2	V
		I_{FLAGx}= 3 mA, x = 1, 2, 3 , 4 , VCC = 0 V, VCC_BIAS > 1.2 V			0.2	V
I_{PG}	PG Leakage Current	V_{PG} = 5 V			1	μA
V_{PG}	PG Output Low	I_{PG} = 3 mA, VCC > 1.2 V			0.2	V
		IPG = 3 mA, VCC = 0, VCC_Bias > 1.2 V			0.2	V

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Timing						
V_{HTH}	High Threshold Level			1.06		V
V_{LTH}	Low Threshold Level			0.47		V
I_{SRC}	Source Current			9.7		μA
I_{SNK}	Sink Current			9.7		μA
$t_{ENx\_FLAGx\_CLK}$	ENx High to Flagx High Delay	C_SETx open, x = 1, 2, 3, 4		75		μs
		C_SETx = 330 pF, x = 1, 2, 3, 4		4.9		ms
		C_SETx = 1 nF, x= 1, 2, 3, 4	14.145	14.89	15.634	ms
		C_SETx =100 nF, x = 1, 2, 3, 4	1414.5	1489	1563.4	ms
$t_{ENx\_FALGx\_L}$	ENx Low to Flagx Low Delay			1		μs
t_{EN_FLAG1}	EN Low to Flag1 Low Delay	C_SET = open		300		μs
		C_SET = 330 pF		19.6		ms
		C_SET = 1 nF	56.58	59.56	62.536	ms
		C_SET = 100 nF	5658	5956	6253.6	ms
t_{EN_FLAG2}	EN Low to Flag2 Low Delay	C_SET = open		225		μs
		C_SET = 330 pF		14.7		ms
		C_SET = 1 nF	42.435	44.67	46.902	ms
		C_SET = 100 nF	4243.5	4467	4690.2	ms
t_{EN_FLAG3}	EN Low to Flag3 Low Delay	C_SET = open		150		μs
		C_SET = 330 pF		9.8		ms
		C_SET = 1 nF	28.29	29.78	31.268	ms
		C_SET = 100 nF	2829	2978	3126.8	ms
t_{EN_FLAG4}	EN Low to Flag4 Low Delay	C_SET = open		75		μs
		C_SET = 330 pF		4.9		ms
		C_SET = 1 nF	14.145	14.89	15.634	ms
		C_SET = 100 nF	1414.5	1489	1563.4	ms

Typical Performance Characteristics

All test conditions: V_{CC}=5V, T_A=25°C, unless otherwise noted.

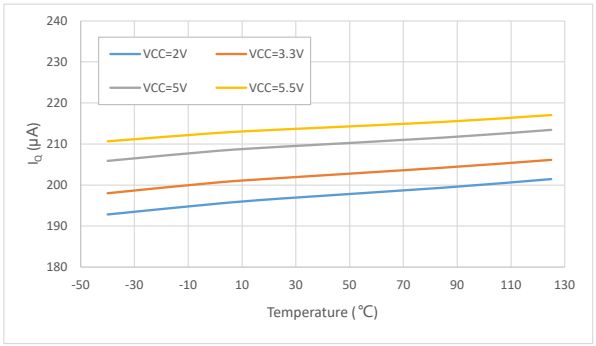


Figure 1. Quiescent Current (Shunt Reference Disabled) vs. Temperature

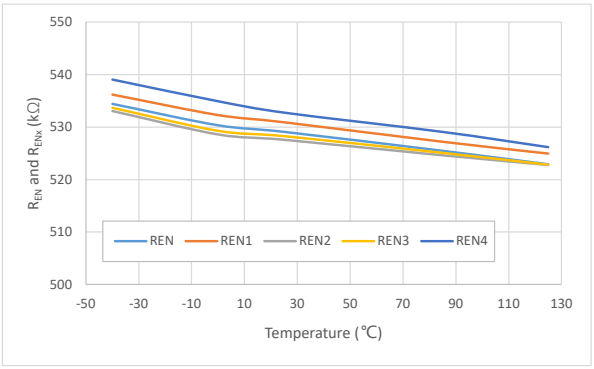


Figure 2. EN, EN1, EN2, EN3, EN4 Pull Down Resistor vs. Temperature

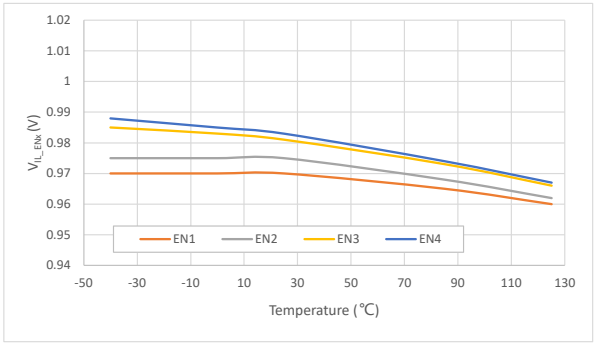


Figure 3. EN1, EN2, EN3 and EN4 Falling Threshold vs. Temperature

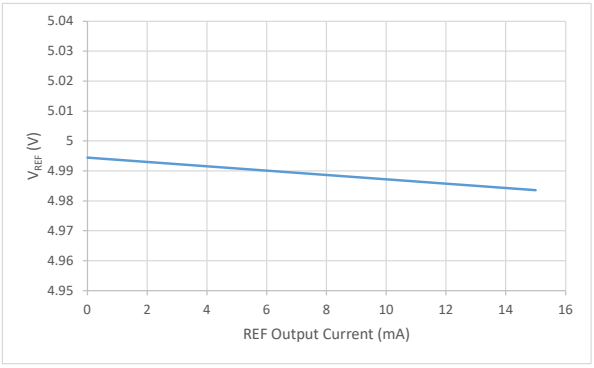


Figure 4. Shunt Ref Output Voltage vs. Output Current

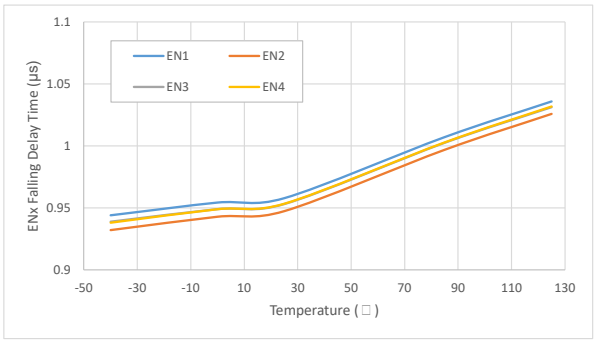


Figure 5. ENx Falling Delay Time vs. Temperature with VCC=5V

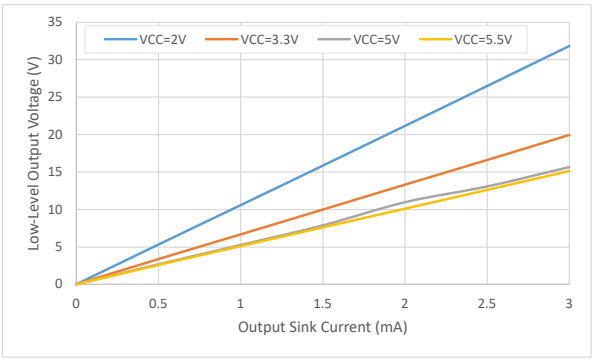


Figure 6. FLAGx (x=1,2,3,4) Output Low Voltage vs. Output Sink Current

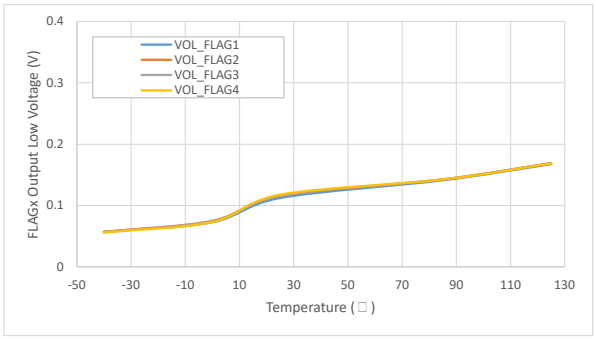


Figure 7. FLAGx (x=1,2,3,4) Output Low Voltage vs. Temperature with VCC=0V and Vbias=1.2V

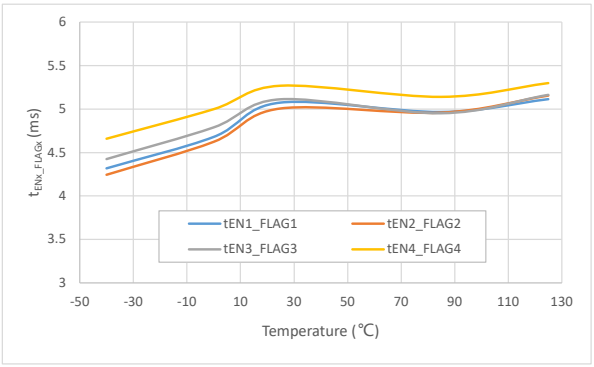


Figure 8. ENx to FLAGx High Delay vs. Temperature with C_SETx=330pF (x=1,2,3,4)

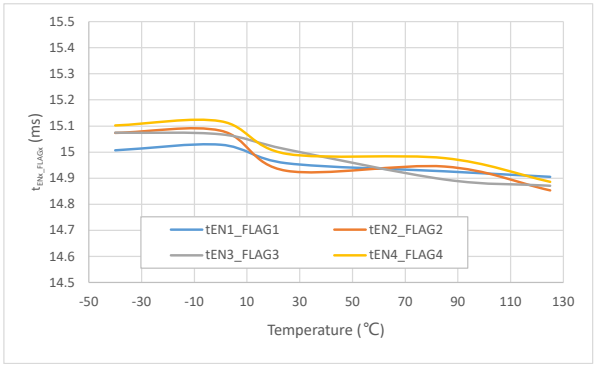


Figure 9. ENx to FLAGx High Delay vs. Temperature with C_SETx=1nF (x=1,2,3,4)

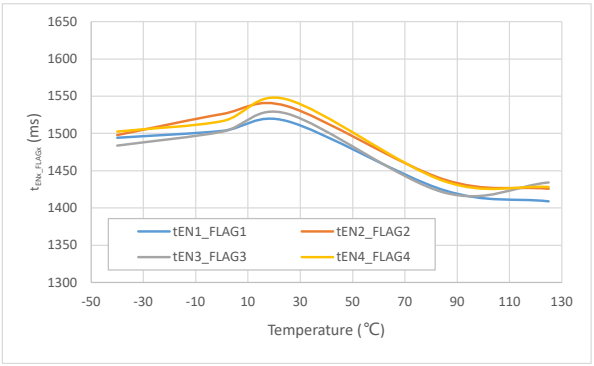


Figure 10. ENx to FLAGx High Delay vs. Temperature with C_SETx=100nF (x=1,2,3,4)

Detailed Description

Overview

TPK1034 is a low voltage four-channel power sequencer. The power supply range is 2 V to 5.5 V, if the shunt reference structure is enabled, the TPK1034 can sustain up to 22 V supply voltage. Each channel has an independent and adjustable threshold that can monitor voltage down to 0.98 V. If the monitored voltage falls below the threshold, the corresponding output is low. If the monitored voltage rises above the threshold, the output turns high after a capacitor-set delay time, the channel output is open-drain configuration.

With the power monitor function, the TPK1034 can achieve power sequencing control, and the capacitor of each channel can adjust the sequencing timing.

TPK1034 has an overall enable control for all channel outputs. When overall enable is active, each channel can be controlled by corresponding enable. The overall enable control can disable all channel outputs by turning channel output low in a fixed sequence from channel 4 to channel 3, then channel 2 and channel 1. There is a delay time before each channel output low, which can be adjustable by another capacitor.

TPK1034 also includes a power good indication with open-drain active high to indicate all channels output high.

Functional Block Diagram

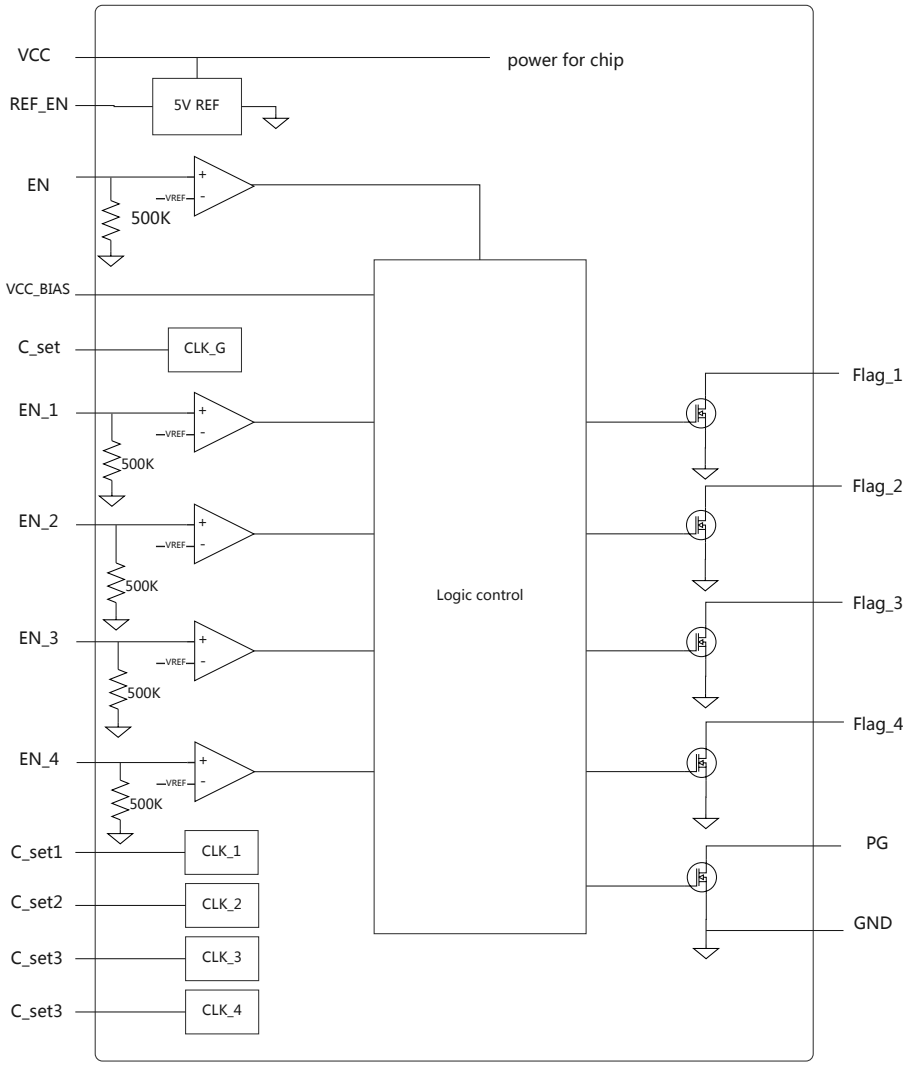
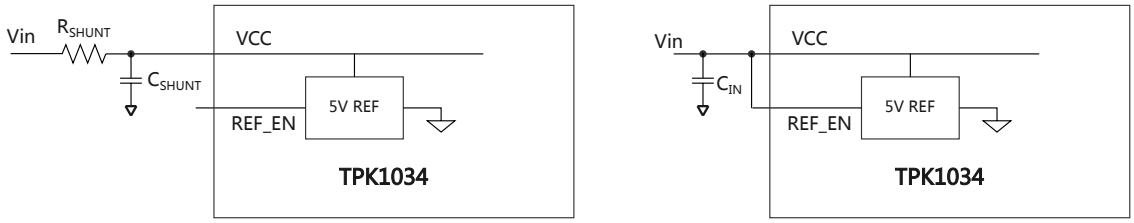


Figure 11. Functional Block Diagram

Feature Description

REF_EN

TPK1034 has a shunt reference design to support up to 22V supply voltage. The shunt reference is enabled by leaving REF_EN not connected, which will be pulled down internally, while an external resistor R_{SHUNT} is needed between the external power supply and VCC pin, as shown in below Figure 12(a). The shunt reference is designed at 5V to supply the TPK1034 internal circuit, and can also provide an external load up to 15mA. If the external power supply is 5V or lower, it is not necessary to enable the shunt reference, REF_EN can be connected to the VCC pin, as shown in Figure 12(b).



(a) Shunt reference enabled (b) Shunt reference disabled

Figure 12. Shunt Reference Circuit

Power Monitor

TPK1034 has four power monitor pins: EN1, EN2, EN3, EN4. The internal of each pin is a comparator with a high accurate reference voltage of 0.98 V. With the external divided resistors, each pin can monitor power supply above 0.98V. If the voltage of each pin falls below the falling threshold voltage, V_{IN_ENx}, the corresponding output, FLAGx, is low. In contrast, if the voltage of each pin rises above the rising threshold, the corresponding output turns high after an individual capacitor set delay time. There is overall EN, which should be enabled first, then the four channels can be functional, as the below figure shows.

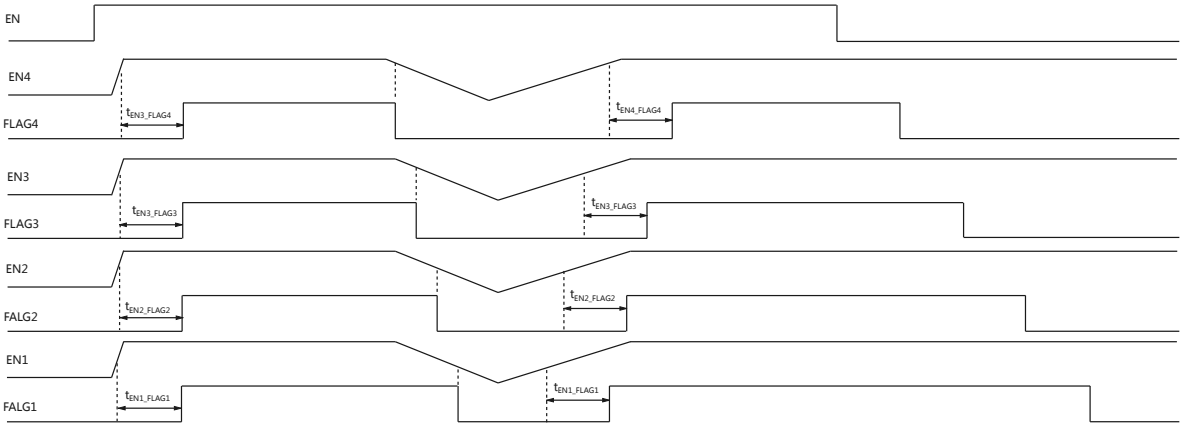


Figure 13. Power Monitor

Sequence

With the independent control of each channel and delay time set by individual capacitors, TPK1034 can achieve flexible power sequence control. The overall EN controls all channels, which should be enabled first, while if EN is low, all channel output turns low with a fixed pattern that from flag4 to flag3, then flag2 and flag1, after a delay time that is programmed by another capacitor. The below figure shows the channel sequence.

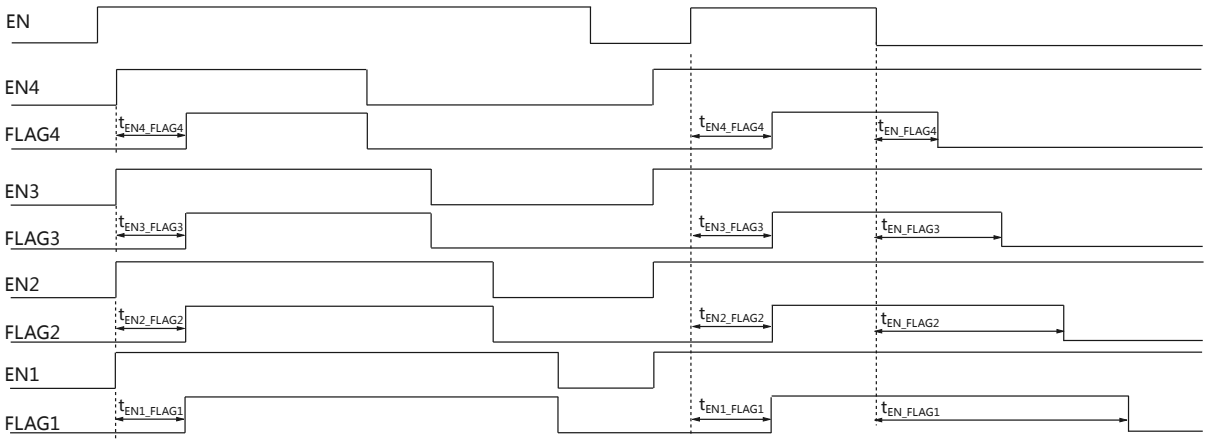


Figure 14. Channel Sequence

Timing

Each channel output high delay time is programmed by a capacitor for the corresponding channel, the delay time equation is

$$t_X = 14.8945\text{ms} \times C\_SET_X\,(\text{nF}) + 0.075\text{ms} \quad (1)$$

where, X is 1, 2, 3, or 4, and C_SETX is the corresponding capacitor.

The off delay time t5 has the same equation, while the capacitor is that at the C_SET pin.

PG

TPK1034 has power good indication, PG, and output. If all channel outputs, FLAG1 to FLAG4, are high, PG is high, otherwise, PG is low. PG is an open drain configuration, which should be pulled high externally.

VCC_BIAS

The VCC_BIAS pin can be supplied by a bias voltage before VCC powers on, to avoid FLAGx and PG not providing strong enough pull-down capability only during the VCC power-up period. An external 1MΩ to 10MΩ can be connected between VCC_BIAS and external bias voltage, which is used to limit the current flowing into the VCC_BIAS pin.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

TPK1034 is a four-channel power monitor and sequencer. Each channel has an independent enable control and individual capacitor-set delay time. The overall enabled control of all the channels, and all the channels off sequence delay time can be set by another capacitor. The channel output and PG are open-drain configurations with active high, which need to be pulled up.

Typical Application

Figure 15 shows the typical application schematic of the TPK1034 with shunt reference enabled

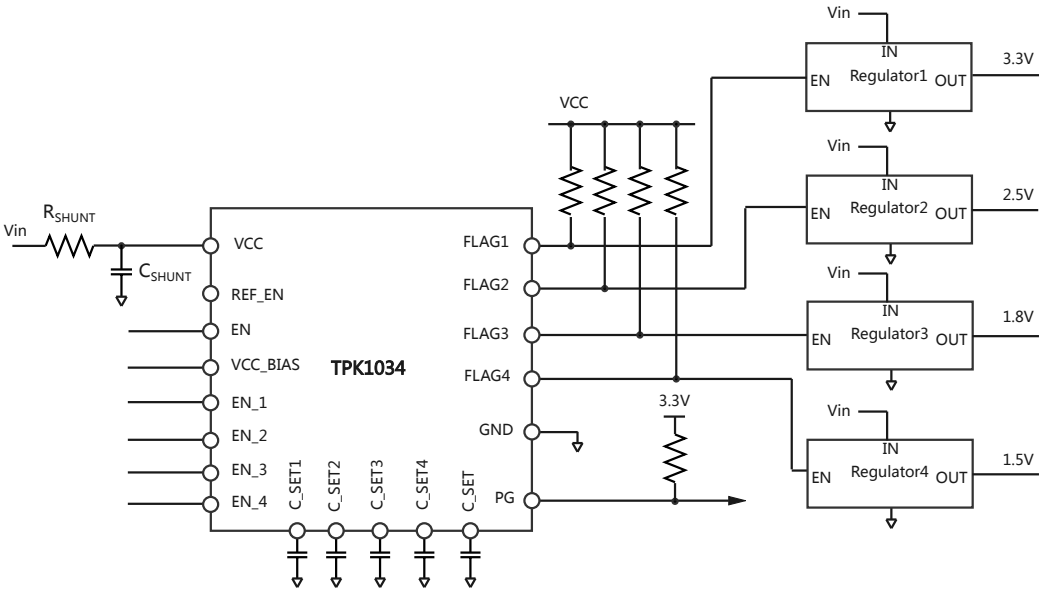


Figure 15. Typical Application Circuit

Shunt Reference Design Guide

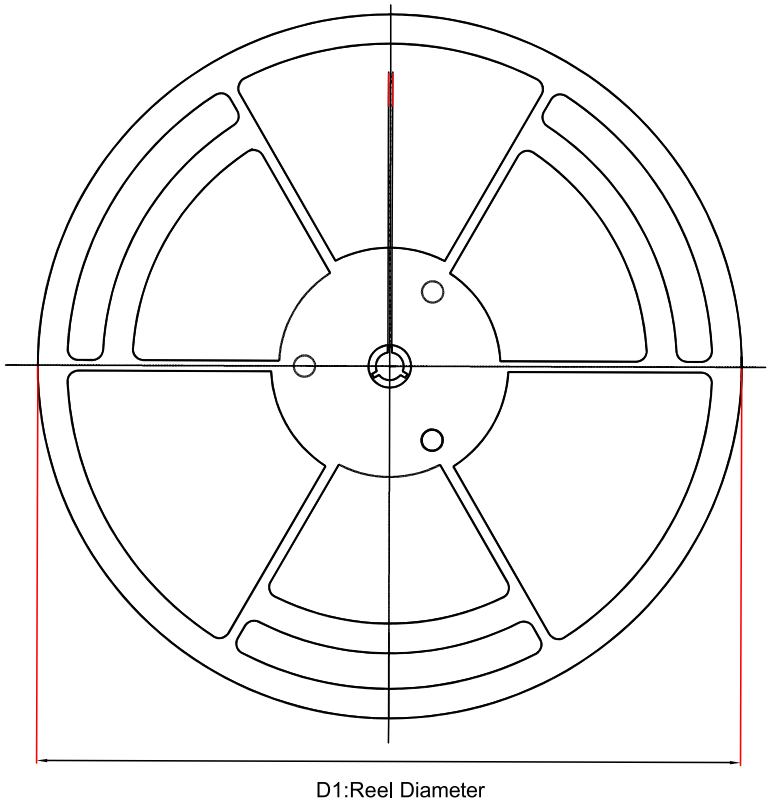
When shunt reference is enabled, VCC is regulated at 5 V if the input voltage is above 5 V. VCC is designed to provide up to 15 mA output capability, R_{SHUNT} is needed to limit the output current under different input voltage, C_{SHUNT} is needed for VCC regulation stability. Users can refer recommeded values of R_{SHUNT} and C_{SHUNT} in the below table.

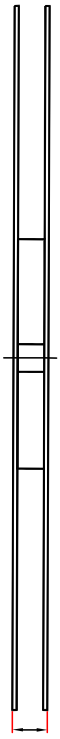
Table 2. R_{SHUNT} and C_{SHUNT} Guide

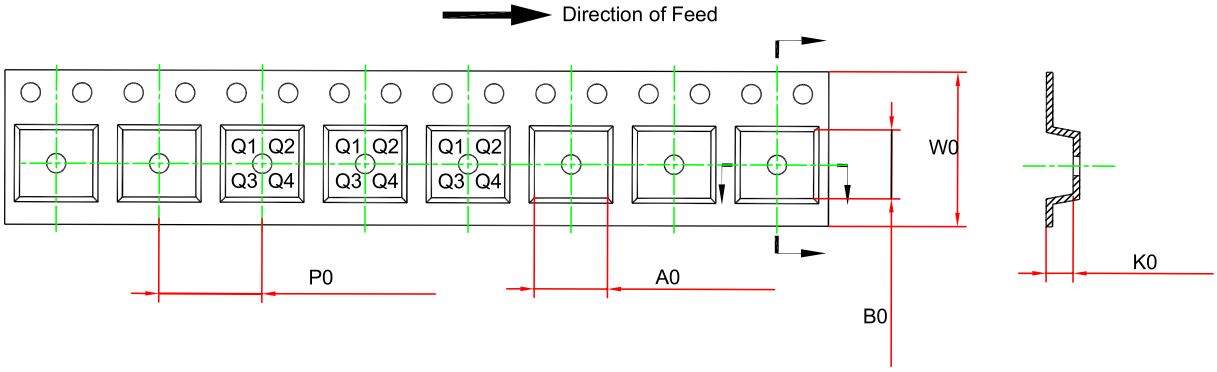
Vin	Recommended R_{SHUNT} at 15mA VCC Output Capability	Recommended C_{SHUNT}
5.5V	30Ω	1μF to 10μF

8V	190Ω	1μF to 10μF
11V	390Ω	1μF to 10μF
20V	1kΩ	1μF to 10μF

Tape and Reel Information





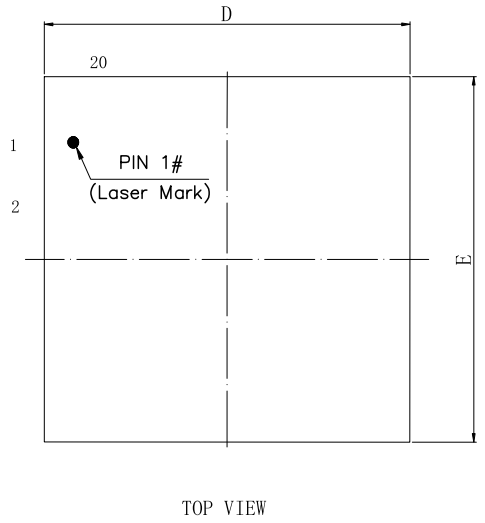


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPK1034-QF6R-S	QFN3.5x3.5-20	330.0	17.6	3.8	3.8	1.1	8.0	12.0	Q1

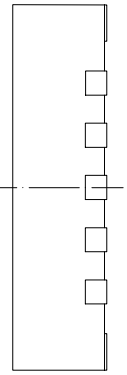
Package Outline Dimensions

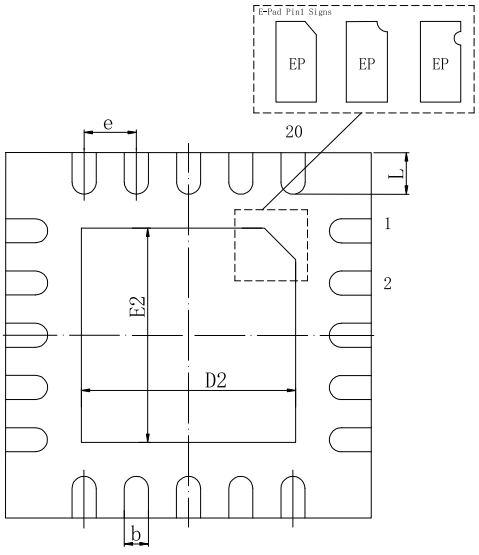
QFN3.5X3.5-20

Package Outline Dimensions QF6(QFN3.5X3.5-20-A)

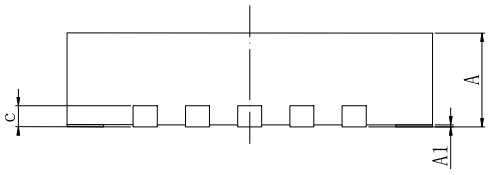


TOP VIEW





BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.180	0.300	0.007	0.012
c	0.203 REF		0.008 REF	
D	3.400	3.600	0.134	0.142
E	3.400	3.600	0.134	0.142
e	0.500 BSC		0.020 BSC	
L	0.250	0.450	0.010	0.018
D2	2.050	2.250	0.081	0.089
E2	2.050	2.250	0.081	0.089

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPK1034-QF6R-S	−40 to 125°C	QFN3.5x3.5-20	K1034	1	4000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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