

Features

- Input Voltage Range: 2.5 V to 5.5V
- Power-Up and Power-Down Sequence Control
- Single Enable Control Signal Input Channel
- Three Power Sequence Channels:
 - Open-Drain Output
 - Selectable Timing Options
 - Selectable Power-Down Sequence Options
- Support Cascaded Device Output
- Low Power Consumption
- Junction Temperature: -40°C to $+125^{\circ}\text{C}$
- Small SOT23-6 Package

Applications

- Video Surveillance
- Network Equipment and Servers
- Industrial Control
- FPGA/ASIC/CPLD Power Sequence Control
- Power Supply Sequence Control

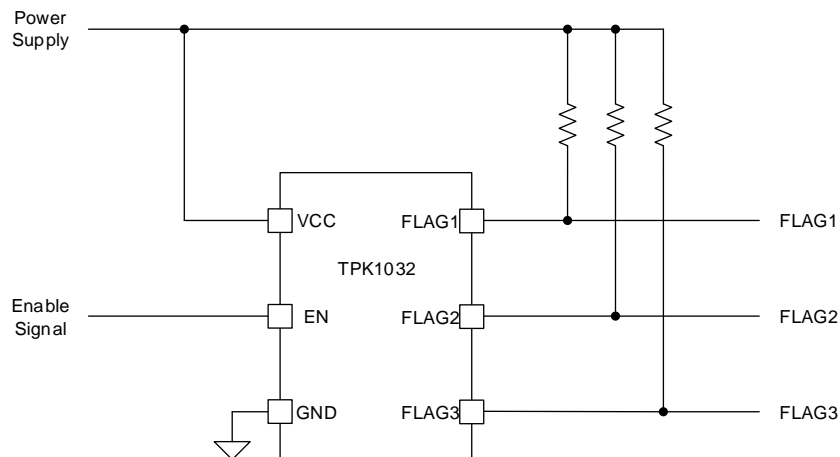
Description

The TPK1032 series products are simple power sequencers, which provide power-up and power-down sequence control of multi-channel power supplies. Furthermore, the TPK1032 series support maximum three devices cascaded to control sequence of nine-channel power rails in one system.

The TPK1032 series products have three open-drain output channels, and all the channels can be pulled up to any required voltage level equal or lower than V_{CC} . When the TPK1032 series are enabled with EN pin goes high, the three output channels turn to high with the sequence of FLAG1-FLAG2-FLAG3 after the selected delay period individually; When the TPK1032 series are disabled with EN pin goes low, the three output channels turn low one by one with the selected sequence after the selected delay period individually.

The TPK1032 series products provide SOT23-6 package with guaranteed junction temperature range (T_j) from -40°C to $+125^{\circ}\text{C}$.

Typical Application Schematic



Product Family Table

Part Number	Orderable Number	Package	Transport Media, Quantity	MSL	Marking information
TPK1032	TPK1032AAL1-S6TR	SOT23-6	3,000	MSL1	KAA
TPK1032	TPK1032ABL1-S6TR	SOT23-6	3,000	MSL1	KAB
TPK1032	TPK1032ACL1-S6TR	SOT23-6	3,000	MSL1	KAC
TPK1032	TPK1032ADL1-S6TR	SOT23-6	3,000	MSL1	KAD
TPK1032	TPK1032AEL1-S6TR	SOT23-6	3,000	MSL1	KAE
TPK1032	TPK1032AFL1-S6TR ⁽¹⁾	SOT23-6	3,000	MSL1	KAF

(1) Future product, contact 3PEAK factory for more information and sample.

TPK1032 XYL1-S6TR

X: Sequence Designator

Designator	Power-Up Sequence	Power-Down Sequence
A	FLAG1 – FLAG2 – FLAG3	FLAG3 – FLAG2 – FLAG1
B	FLAG1 – FLAG2 – FLAG3	FLAG3 – FLAG1 – FLAG2
C	FLAG1 – FLAG2 – FLAG3	FLAG2 – FLAG3 – FLAG1
D	FLAG1 – FLAG2 – FLAG3	FLAG2 – FLAG1 – FLAG3
E	FLAG1 – FLAG2 – FLAG3	FLAG1 – FLAG3 – FLAG2
F	FLAG1 – FLAG2 – FLAG3	FLAG1 – FLAG2 – FLAG3

Y: Delay Designator

Designator	t _{D1} (ms)	t _{D2} (ms)	t _{D3} (ms)	t _{D4} (ms)	t _{D5} (ms)	t _{D6} (ms)
A	11	11	11	11	11	11
B	30	30	30	30	30	30
C	60	60	60	60	60	60
D	120	120	120	120	120	120
E	2	2	2	2	2	2
F	16	16	16	16	16	16

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Revision History

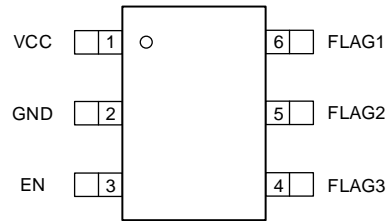
Date	Revision	Notes
2019/05/31	Rev. Pre	Preliminary Version
2019/08/31	Rev. A	Initial Release
2022/07/29	Rev. A.1	Update td ratio in EC table

Pin Configuration and Functions

TPk1032 Series

6-Pin SOT23

Top View



Pin Functions

NAME	PIN NUMBER	TYPE	DESCRIPTION
EN	3	I	Device enable pin.
FLAG1	6	O	Open-drain output pin.
FLAG2	5	O	Open-drain output pin.
FLAG3	4	O	Open-drain output pin.
GND	2	–	Ground reference pin.
VCC	1	I	Input power supply.

Specifications

Absolute Maximum Ratings

		MIN	MAX	UNIT
VCC, EN		-0.3	6	V
FLAG1, FLAG2, FLAG3		-0.3	6	V
T _J	Junction Temperature Range	-40	150	°C
T _{STG}	Storage Temperature Range	-65	150	°C
T _L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond the Absolute Maximum Ratings may permanently damage the device.

(2) All voltage values are with respect to GND.

ESD Ratings

		Condition	Minimum Level	UNIT
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	±1500	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	±500	V

Recommended Operating Conditions

		MIN	MAX	UNIT
VCC		2.5	5.5	V
EN		0	VCC + 0.3	V
FLAG1, FLAG2, FLAG3		0	VCC + 0.3	V
T _J	Junction Temperature Range	-40	125	°C

Thermal Information

PACKAGE	θ_{JA}	θ_{JC}	UNIT
SOT23-6	206	140	°C/W

Electrical Characteristics

$T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ (typical value at $T_J = +25^{\circ}\text{C}$), $V_{CC} = 3.3\text{ V}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply						
VCC	Input supply voltage		2.5		5.5	V
ICC	Operating quiescent current			55	100	μA
Enable						
$V_{\text{EN_TH}}$	EN pin threshold voltage		1	1.23	1.5	V
I_{EN}	EN pin pull-up current	$V_{\text{EN}} = 0\text{ V}$	5	6.5	8	μA
Open-Drain Output						
V_{OL}	FLAGx pin output low level	$I_{\text{FLAGx}} = 1.2\text{ mA}$	0		0.4	V
I_{FLAGx}	FLAGx pin leakage current	$V_{\text{FLAGx}} = 3.3\text{ V}$		0.3	1	μA
Power-Up Sequence						
t_{d1}	Timer delay 1 tolerance	All other timing options	-15%		15%	
		2-ms timing option	-20%		20%	
t_{d2}	Timer delay 2 tolerance	All other timing options	-15%		15%	
		2-ms timing option	-20%		20%	
t_{d3}	Timer delay 3 tolerance	All other timing options	-15%		15%	
		2-ms timing option	-20%		20%	
Power-Down Sequence						
t_{d4}	Timing delay 4 tolerance	All other timing options	-15%		15%	
		2-ms timing option	-20%		20%	
t_{d5}	Timing delay 5 tolerance	All other timing options	-15%		15%	
		2-ms timing option	-20%		20%	
t_{d6}	Timing delay 6 tolerance	All other timing options	-15%		15%	
		2-ms timing option	-20%		20%	
Timing Delay Tolerance						
$\frac{t_{dx} - 70\mu\text{s}}{t_{dx+1}}$	Ratio of timing delays	For $x = 1$ or 4 , 2-ms timing option	90%		110%	
$\frac{t_{dx} - 400\mu\text{s}}{t_{dx+1}}$	Ratio of timing delays	For $x = 1$ or 4 , all other timing options	95%		105%	
$\frac{t_{dx}}{t_{dx+1}}$	Ratio of timing delays	For $x = 2$ or 5	95%		105%	

Typical Performance Characteristics

$T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ (typical value at $T_J = +25^{\circ}\text{C}$), $V_{CC} = 3.3\text{ V}$, Delay = 10 ms, unless otherwise noted.

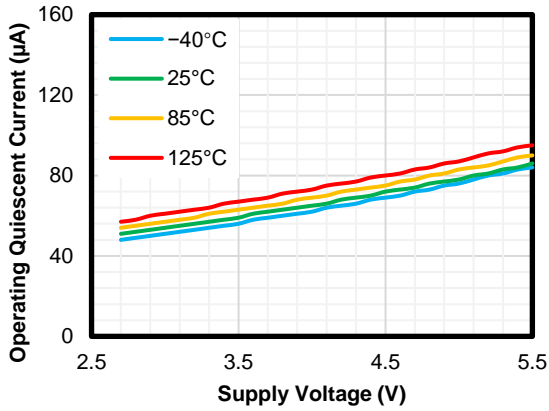


Figure 1 Quiescent Current vs Supply Voltage

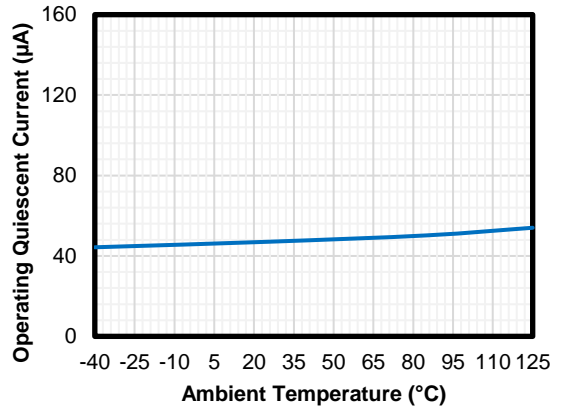


Figure 2 Quiescent Current vs Temperature

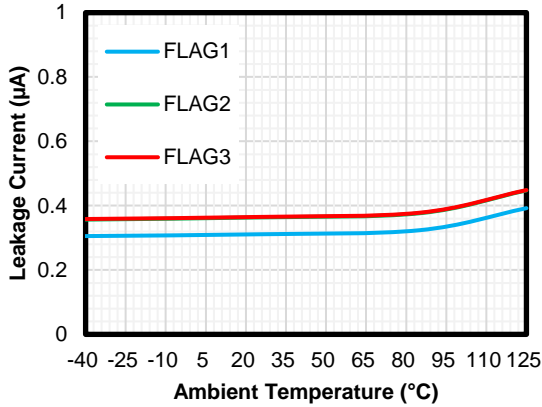


Figure 3 FLAGx Leakage Current vs Temperature

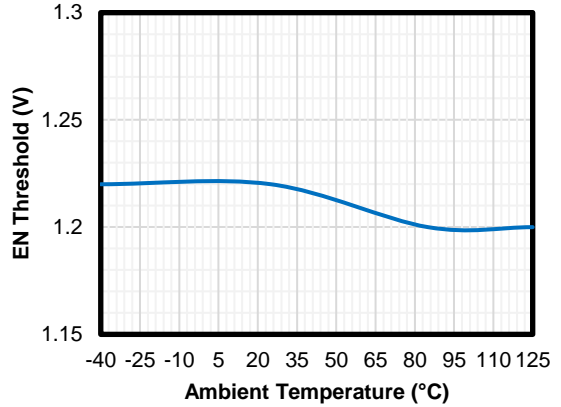


Figure 4 Enable Threshold vs Temperature

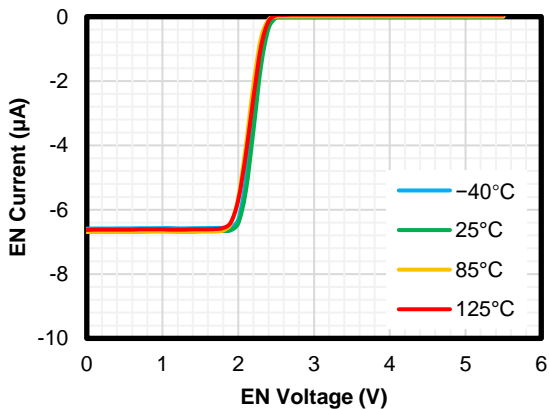


Figure 5 EN Input Current vs EN Voltage

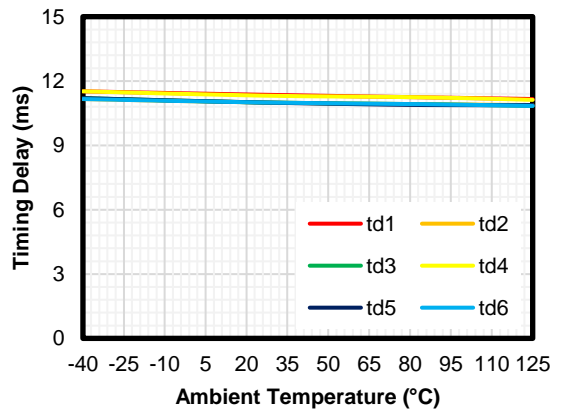


Figure 6 Timing Delay vs Temperature

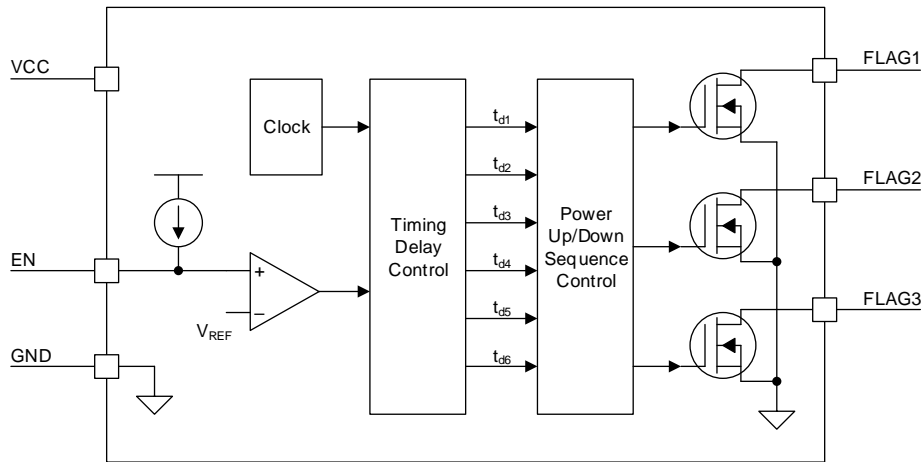
Detailed Description

Overview

The TPK1032 series products are simple power sequencers, which provide power-up and power-down sequence control of multi-channel power supplies. Furthermore, the TPK1032 series support maximum three devices cascaded to control sequence of nine-channel power rails in one system.

The TPK1032 series products have three open-drain output channels, and all the channels can be pulled up to any required voltage level equal or lower than V_{CC} . When the TPK1032 series are enabled with EN pin goes high, the three output channels turn to high with the sequence of FLAG1-FLAG2-FLAG3 after the selected delay period individually; When the TPK1032 series are disabled with EN pin goes low, the three output channels turn low one by one with the selected sequence after the selected delay period individually.

Functional Block Diagram



Feature Description

Enable (EN)

The timing sequence of TPK1032 series is controlled by the enable (EN) signal. When device powered up, all the flags keep low until the EN pin is pulled high. An internal comparator, with reference voltage connected at negative terminal, set the enable threshold precisely at 1.22 V. When the EN pin voltage is higher than the threshold, the power-up sequence starts.

With the precision enable threshold, the TPK1032 series can be enabled after a certain delay period set by external capacitor or a certain voltage value determined by external resistor divider.

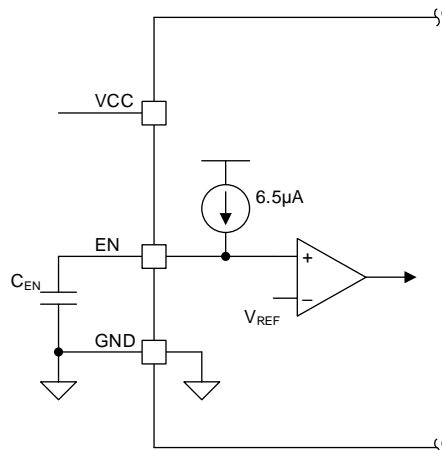


Figure 7 Using Capacitor at EN

Note: It is not recommended to connected EN to VCC directly. EN should be kept low before VCC is ready.

When using a capacitor at the EN pin (Figure 7), the enable delay period can be calculated by Equation 1:

$$t_{EN_DLY} = \frac{1.23V \times C_{EN}}{6.5\mu A} \tag{1}$$

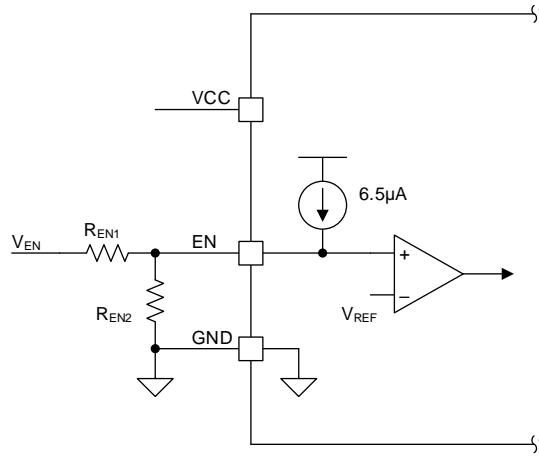


Figure 8 Using Resistor Divider at EN

When using the resistor divider at the EN pin (Figure 8), the resistor divider ratio can be calculated by Equation 2:

$$V_{EN} = V_{EN_TH} \times \frac{R_{EN1} + R_{EN2}}{R_{EN2}} - 6.5\mu A \times R_{EN1} \tag{2}$$

The TPK1032 series also implement the EN pin de-glitch function. When there are ripple across the enable threshold at the EN pin, the device will always reset if the EN pin falls below the threshold. The timing delay only start counting at the last EN rising threshold (Figure 9).

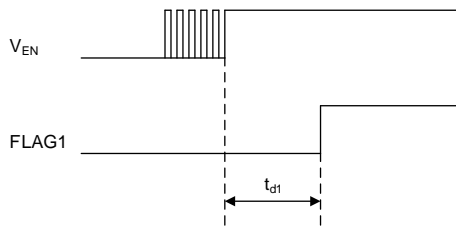


Figure 9 Enable De-glitch

Power Sequence (FLAGx)

When the TPK1032 series devices are enabled, all the output flags will be released sequentially. The timing delay period between two adjacent flags is determined by the device internal delay periods.

Figure 10 show the power sequences of the output flags.

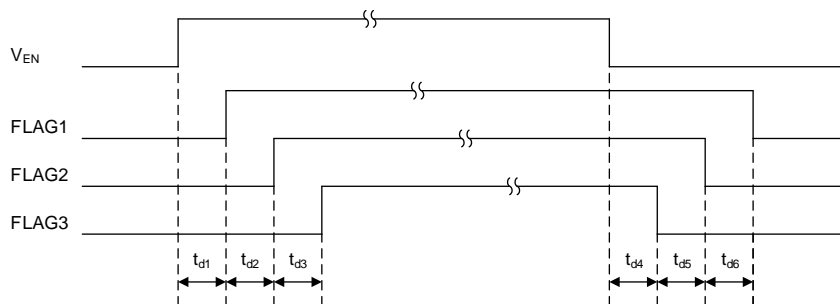


Figure 10 Power Up and Power Down Sequence

Power Sequence Interruption

When the enable signal keeps constant during the entire power up or power down sequence, the TPK1032 series devices will operate the whole sequence as shown in Figure 10. However, if the enable signal falling or rising edge comes during the power up or power down sequence, the device will enter the interrupt status and initialize a new power down or power up sequence.

Figure 11 show the power up sequence with EN interruption.

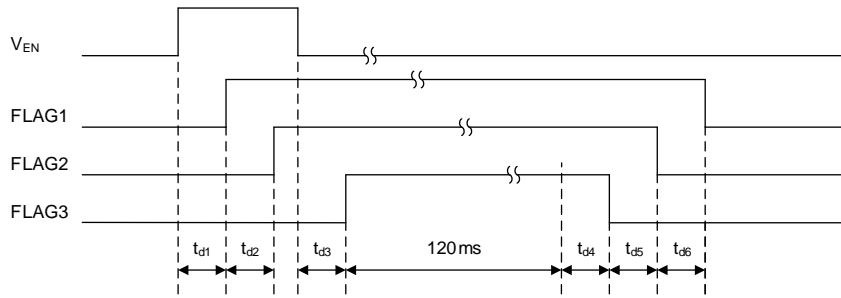


Figure 11 Interrupt of Power Up Sequence

Figure 12 show the power down sequence with EN interruption.

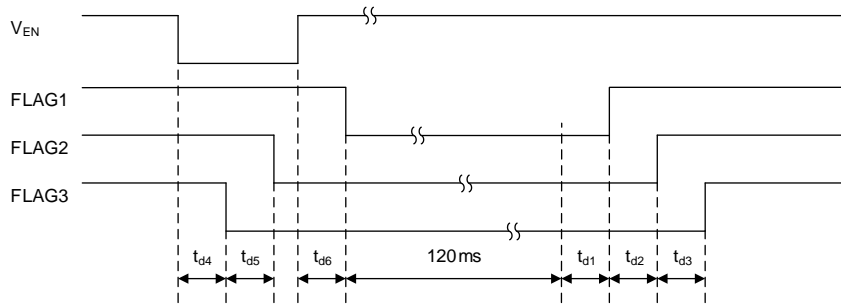


Figure 12 Interrupt of Power Down Sequence

Application and Implementation

NOTE

Information in the following applications sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPK1032 series products are 3-channel simple power sequencers, which provide power-up and power-down sequence control of multi-channel power supplies. The following application schematic shows a typical usage of the TPK1032 series.

Typical Application

Figure 13 and Figure 14 shows the typical application schematic of the TPK1032 series.

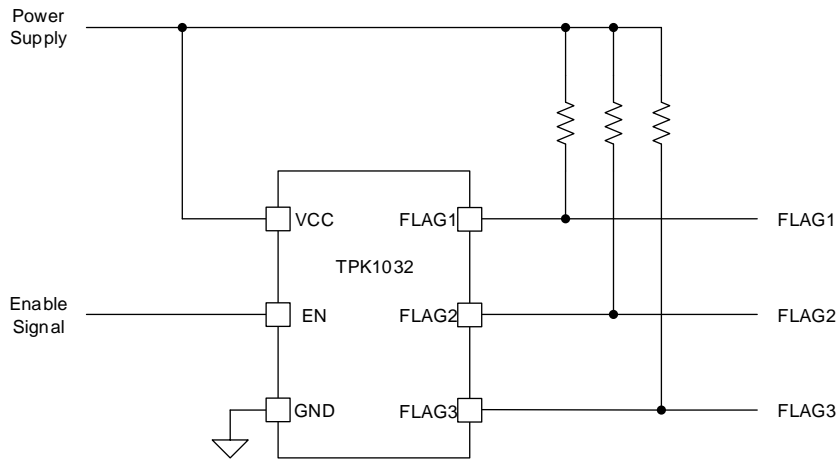


Figure 13 VCC and FLAGx with Same Power Rail

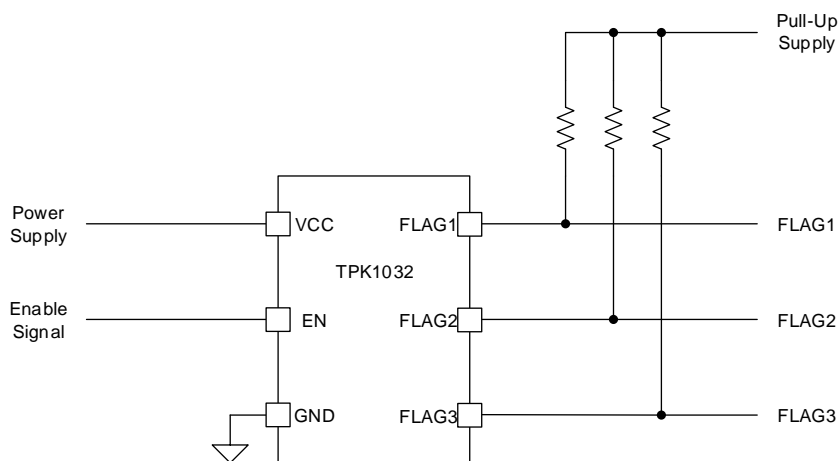


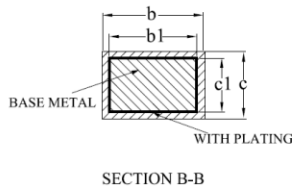
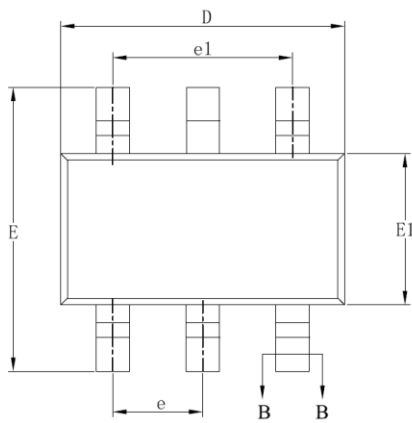
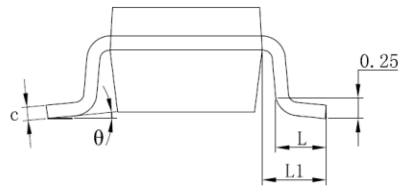
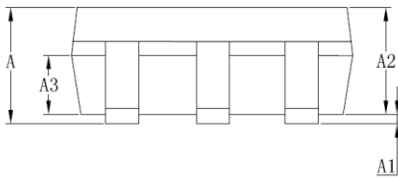
Figure 14 VCC and FLAGx with Different Power Rails

Layout Requirements

- FLAGx pull-up resistors, recommended 100 kΩ, should be placed closely to the flag output pins and the pull-up power supply. The traces should be equal to each other, and the trace length should be as short as possible.

Package Outline Dimensions

SOT23-6



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.25
A1	0.04	—	0.10
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.33	—	0.41
b1	0.32	0.35	0.38
c	0.15	—	0.19
c1	0.14	0.15	0.16
D	2.82	2.92	3.02
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95BSC		
e1	1.90BSC		
L	0.30	—	0.60
θ	0	—	8°

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