# 3-Channel Simple Power Sequencer with Adjustable Timing Control

## Features

- Input Voltage Range: 2.7 V to 5.5 V
- Power-up and Power-down Sequence Control
- Single Enable Control Signal Input Channel
- Three Power Sequence Channels:
  - Open-Drain Output
  - Adjustable Timing Controlled by Capacitor
  - Support Invert Output
- Support Cascaded Device Output
- Low Power Consumption
- Junction Temperature: −40°C to +125°C
- Small MSOP8 Package

## Applications

- Video Surveillance
- Network Equipment and Servers
- Industrial Control
- FPGA/ASIC/CPLD Power Sequence Control
- Multi-Channel Power Supply Sequence Control

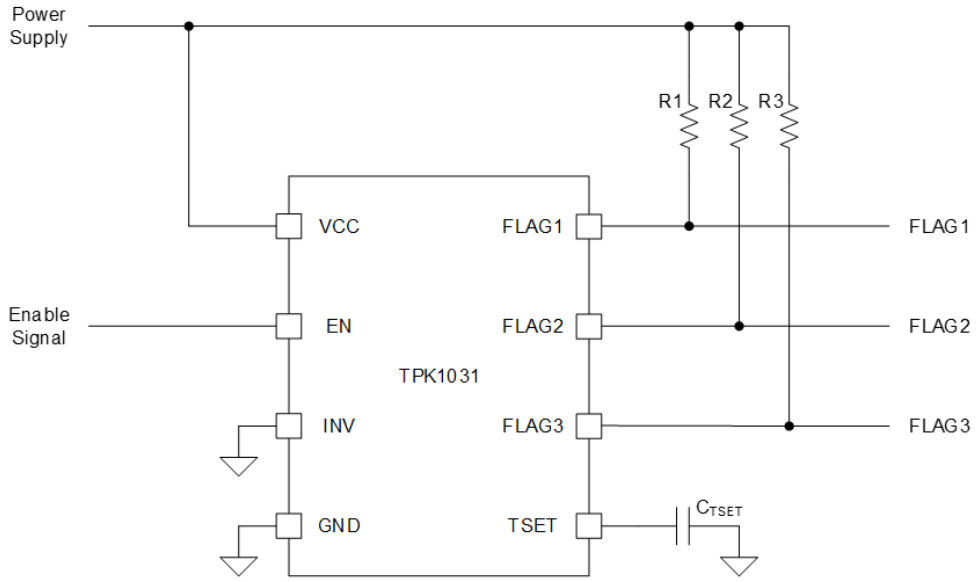
## Description

The TPK1031 is a series of simple power sequencers, providing power-up and power-down sequence control of multi-channel power supplies. Furthermore, the TPK1031 series supports a maximum of three devices cascaded to control the sequence of nine-channel power rails in one system.

The TPK1031 series has three open-drain output channels, and all the channels can be pulled up to any required voltage level equal to or lower than $V_{CC}$. When the TPK1031 series is enabled and the EN pin goes high, the three output channels toggle with the sequence of FLAG1-FLAG2-FLAG3 after the delay period is individually set by the external capacitor. When the TPK1031 series is disabled and the EN pin goes low, the three output channels toggle following a reverse sequence after the delay period is individually set by the external capacitor.

The TPK1031 series provides a small MSOP8 package with a guaranteed junction temperature range ($T_J$) from −40°C to +125°C.

## Typical Application Circuit



# Table of Contents

## Product Family Table

| Order Number | Package | Marking Information | MSL | Transport Media, Quantity |
|---|---|---|---|---|
| TPK1031L1-VS1R | MSOP8 | K1031 | 1 | Tape and Reel, 3000 |

## Revision History

| Date | Revision | Notes |
|---|---|---|
| 2019-05-31 | Rev.Pre.0 | Preliminary version. |
| 2019-08-31 | Rev.A.0 | Initial released version. |
| 2019-12-20 | Rev.A.1 | Upgraded the HBM and ESD ratings to ±2000 V (Page 6). |
| 2021-07-09 | Rev.A.2 | 1. Corrected the mistaken pin number of EN from 3 to 2 (Page 5).<br>2. Added Tape and Reel Information (Page 16). |
| 2024-12-23 | Rev.A.3 | Updated to a new datasheet format. |

## Pin Configuration and Functions

TPK1031 Series
MSOP8
Top View

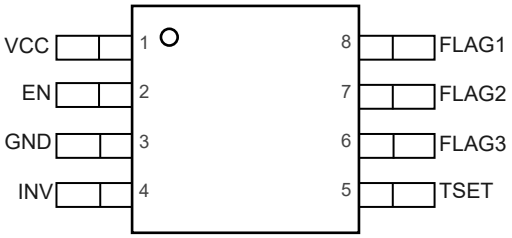



**Table 1. Pin Functions**

| Pin No. | Name | I/O | Description |
|---|---|---|---|
| 2 | EN | I | The enable pin of the device. |
| 8 | FLAG1 | O | The open-drain output pin. |
| 7 | FLAG 2 | O | The open-drain output pin. |
| 6 | FLAG 3 | O | The open-drain output pin. |
| 3 | GND | | The ground reference pin. |
| 4 | INV | I | The invert output set pin. |
| 5 | TSET | O | The delay time set pin. |
| 1 | VCC | I | The input power supply. |

# Specifications

## Absolute Maximum Ratings (1)

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| | $V_{CC}$, EN, INV, $T_{SET}$ | −0.3 | 6 | V |
| | FLAG1, FLAG2, FLAG3 | −0.3 | 6 | V |
| $T_J$ | Maximum Junction Temperature | −40 | 150 | °C |
| $T_{STG}$ | Storage Temperature Range | −65 | 150 | °C |
| $T_L$ | Lead Temperature (Soldering, 10 sec) | | 260 | °C |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
(2) All voltage values are with respect to GND.

## ESD, Electrostatic Discharge Protection

| Symbol | Parameter | Condition | Minimum Level | Unit |
|---|---|---|---|---|
| HBM | Human Body Model ESD | ANSI/ESDA/JEDEC JS-001 (1) | ±2000 | V |
| CDM | Charged Device Model ESD | ANSI/ESDA/JEDEC JS-002 (2) | ±500 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## Recommended Operating Conditions

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | | 2.7 | 5.5 | V |
| EN, INV, $T_{SET}$ | | 0 | $V_{CC}$ + 0.3 | V |
| FLAG1, FLAG2, FLAG3 | | 0 | $V_{CC}$ + 0.3 | V |
| $T_J$ | Junction Temperature Range | −40 | 125 | °C |

## Thermal Information

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| MSOP8 | 247 | 118 | °C/W |

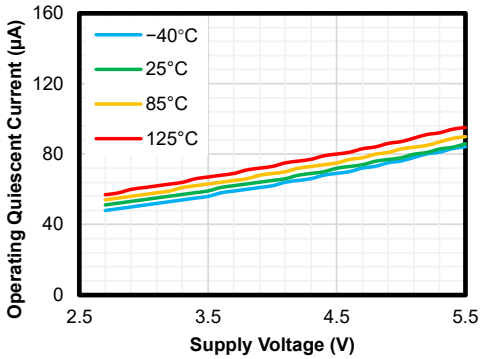
## Electrical Characteristics

All test conditions: $T_J$ = −40℃ to +125℃ (typical value at $T_J$ = +25℃), $V_{CC}$ = 3.3 V, unless otherwise noted.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| $V_{CC}$ | Input Supply Voltage | | 2.7 | | 5.5 | V |
| $I_{CC}$ | Operating Quiescent Current | INV = GND | | 55 | 100 | μA |
| | | INV = $V_{CC}$ | | 85 | 130 | μA |
| **Enable** | | | | | | |
| $V_{EN\_TH}$ | EN Pin Threshold Voltage | | 1 | 1.23 | 1.5 | V |
| $I_{EN}$ | EN Pin Pull-up Current | $V_{EN}$ = 0 V | 5 | 6.5 | 8 | μA |
| **Open-Drain Output** | | | | | | |
| $V_{OL}$ | FLAGx Pin Output Low Level | $I_{FLAGx}$ = 1.2 mA | 0 | | 0.4 | V |
| $I_{FLAGx}$ | FLAGx Pin Leakage Current | $V_{FLAGx}$ = 3.3 V | | 0.3 | 1 | μA |
| **Delay Time Setup** | | | | | | |
| $I_{TSET\_SOURCE}$ | $T_{SET}$ Pin Source Current | | 7 | 11 | 15 | μA |
| $I_{TSET\_SINK}$ | $T_{SET}$ Pin Sink Current | | 7 | 11 | 15 | μA |
| $V_{TSET\_H}$ | $T_{SET}$ Pin High-Level Threshold | | 1 | 1.14 | 1.4 | V |
| $V_{TSET\_L}$ | $T_{SET}$ Pin Low-Level Threshold | | 0.4 | 0.5 | 0.7 | V |
| $T_{CLK}$ | Clock Cycle | $C_{TSET}$ = 10 nF | 0.9 | 1.16 | 1.4 | ms |
| **Timing Delays** | | | | | | |
| $t_{d1}$, $t_{d4}$ | Timing Delays | | 9 | | 10 | Cycles |
| $t_{d2}$, $t_{d3}$, $t_{d5}$, $t_{d6}$ | Timing Delays | | | 8 | | Cycles |
| Inverting Output Setup | | | | | | |
| $V_{INV\_IH}$ | Invert Pin High-Level Input | | 90% | | | of $V_{CC}$ |
| $V_{INV\_IL}$ | Invert Pin Low-Level Input | | | | 10% | of $V_{CC}$ |

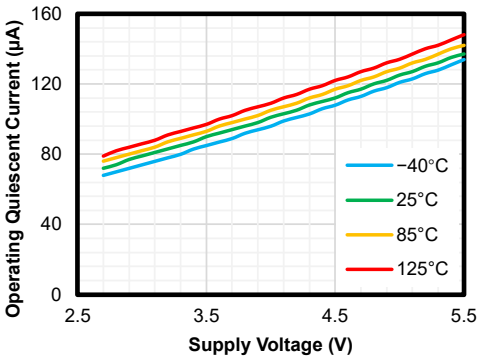
## Typical Performance Characteristics

All test conditions: $T_J$ = −40℃ to +125℃ (typical value at $T_J$ = +25℃), $V_{CC}$ = 3.3 V, unless otherwise noted.




INV = GND

**Figure 1. Quiescent Current vs. Supply Voltage**




INV = VCC

**Figure 2. Quiescent Current vs. Supply Voltage**

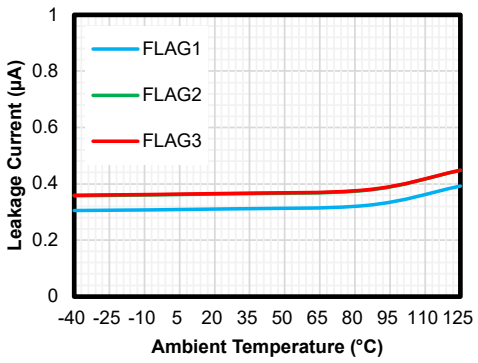



**Figure 3. FLAGx Leakage Current vs. Temperature**

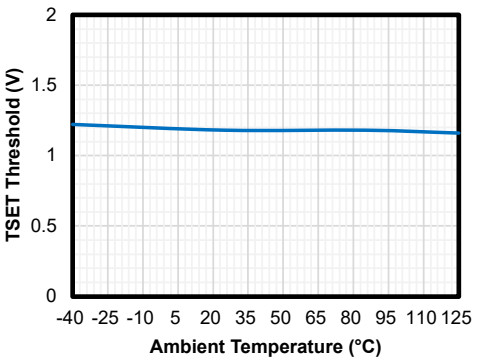
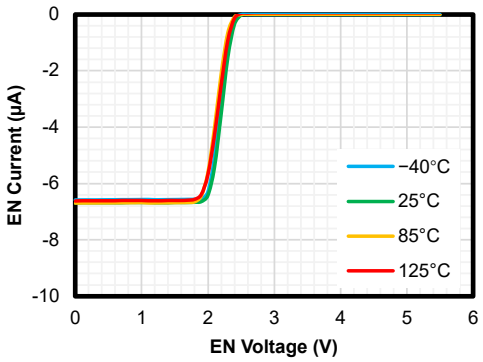
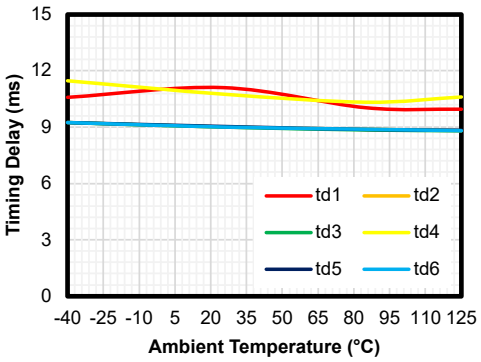



**Figure 4. $T_{SET}$ Threshold vs. Temperature**




INV = GND

**Figure 5. EN Input Current vs. EN Voltage**




$C_{TSET}$ = 10 nF

**Figure 6. Timing Delay vs. Temperature**

# Detailed Description

## Overview

The TPK1031 is a series of simple power sequencers, providing power-up and power-down sequence control of multi-channel power supplies. Furthermore, the TPK1031 series supports a maximum of three devices cascaded to control the sequence of nine-channel power rails in one system.

The TPK1031 series of products has three open-drain output channels, and all the channels can be pulled up to any required voltage level equal to or lower than $V_{CC}$. When the TPK1031 series is enabled and the EN pin goes high, the three output channels toggle with the sequence of FLAG1-FLAG2-FLAG3 after the delay period is individually set by the external capacitor. When the TPK1031 series is disabled and the EN pin goes low, the three output channels toggle following a reverse sequence after the delay period is individually set by the external capacitor.

## Functional Block Diagram

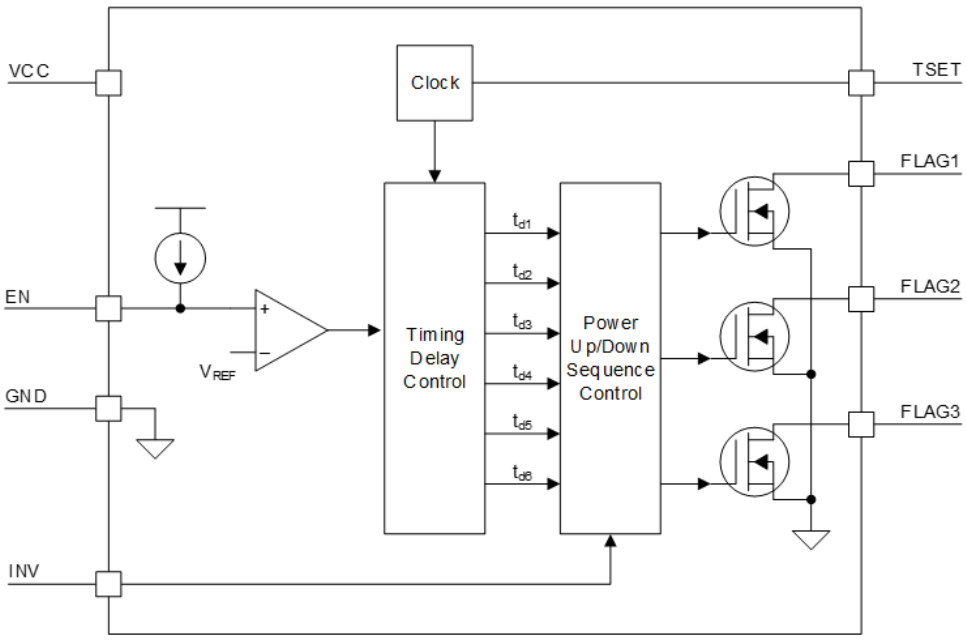



**Figure 7. Functional Block Diagram**

## Feature Description

### Device Enable (EN)

The timing sequence of the TPK1031 series is controlled by the enable (EN) signal. An internal comparator connected at the EN pin, with reference to the bandgap voltage, sets the enable threshold precisely at 1.23 V. With this precision enable threshold, the TPK1031 series can be enabled after a certain delay period set by an external capacitor or a certain voltage value determined by the external resistor divider.

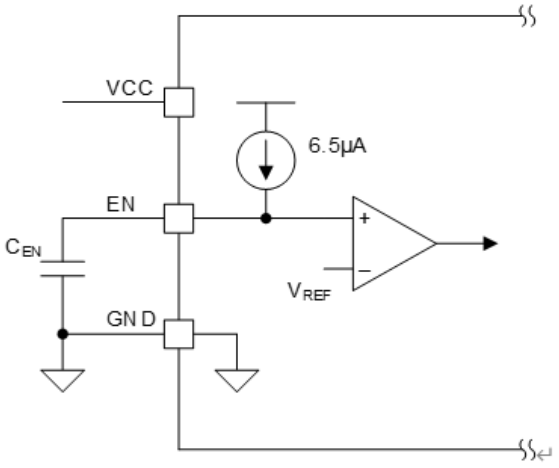



**Figure 8. Using Capacitor at EN**

When using a capacitor at the EN pin (Figure 8), the enable delay period can be calculated by Equation 1.

$$t_{EN\_DLY} = \frac{1.23\ V \times C_{EN}}{6.5\ \mu A} \quad (1)$$

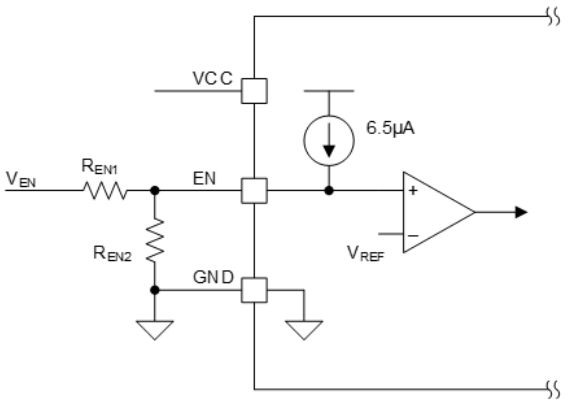



**Figure 9. Using Resistor Divider at EN**

When using the resistor divider at the EN pin (Figure 9), the resistor divider can be calculated by Equation 2.

$$V_{EN} = V_{EN\_TH} \times \frac{R_{EN1} + R_{EN2}}{R_{EN2}} - 6.5\ \mu A \times R_{EN1} \quad (2)$$

The TPK1031 series also implements the EN pin de-glitch function. When there are ripples across the enable threshold at the EN pin, the device always resets if the EN pin falls below the threshold. The timing delay only starts counting at the last EN rising threshold (Figure 10).

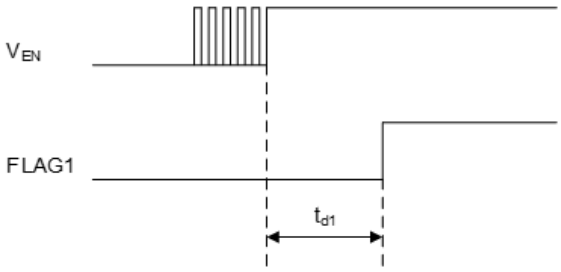



**Figure 10. Enable De-glitch (INV = Low)**

### Inverted Output (INV)

The voltage level of the TPK1031 series output flags is selectable high or low by setting the INV voltage.

When INV = low,

- Output flags turn to high sequentially after each timing delay period when the enable signal of the device comes.
- Output flags turn to low sequentially after each timing delay period when the disable signal of the device comes.

When INV = high,

- Output flags turn to low sequentially after each timing delay period when the enable signal of the device comes.
- Output flags turn to high sequentially after each timing delay period when the disable signal of the device comes.

### Adjustable Timing Delay

The delay period between the TPK1031 series output flags is adjustable with a small external capacitor $C_{TSET}$ at the $T_{SET}$ pin. The $T_{SET}$ pin charges/discharges the capacitor $C_{TSET}$ with an about ±11-μA source/sink current, $I_{TSET\_SOURCE}$ and $I_{TSET\_SINK}$, between the voltage threshold $V_{TSET\_H}$ and $V_{TSET\_L}$. The charging period, $T_{CHG}$, and discharging period, $T_{DISCHG}$, compose one delay clock cycle, $T_{CLK}$.

Figure 11 shows the delay clock cycle timing waveform.

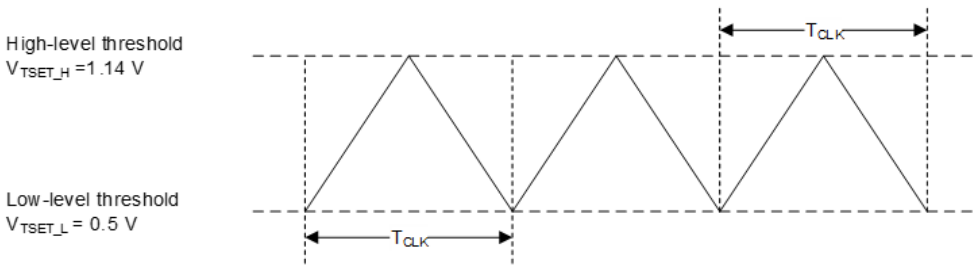



**Figure 11. Delay Clock Cycle Timing Waveform**

The delay clock period can be calculated by Equation 3.

$$T_{CLK} = \left( \frac{V_{TSET\_H} - V_{TSET\_L}}{I_{TSET\_SOURCE}} + \frac{V_{TSET\_H} - V_{TSET\_L}}{I_{TSET\_SINK}} \right) \times C_{TSET} \quad (3)$$

### Power Sequence (FLAGx)

When the TPK1031 series of devices is enabled, all the output flags are released sequentially. The timing delay period between two adjacent flags is determined by the product of each delay clock period and the internal delay clock counter.

Figure 12 and Figure 13 show the power sequences of the output flags.

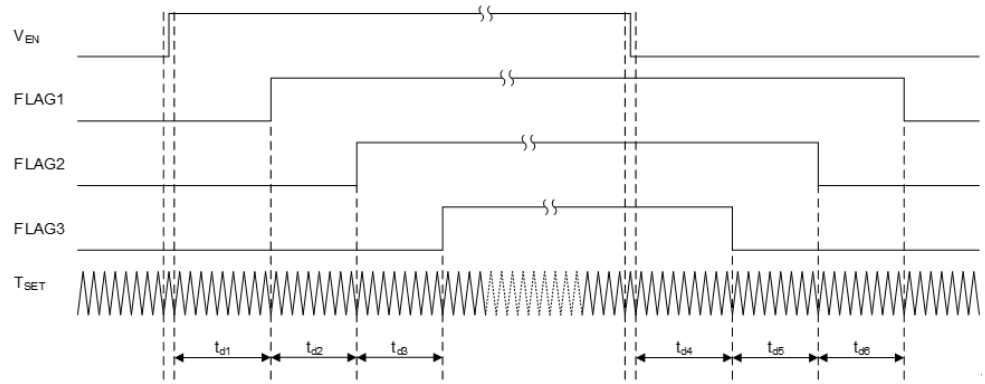



**Figure 12. Power Up and Power Down Sequence when INV = Low**

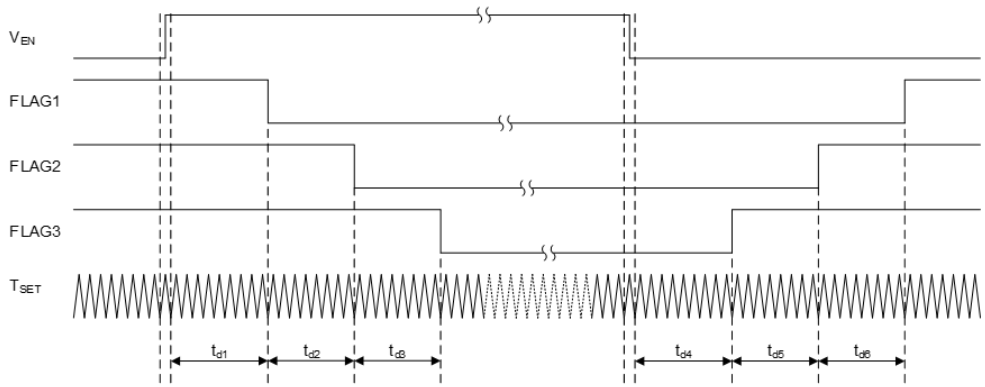



**Figure 13. Power Up and Power Down Sequence when INV = High**

### Power Sequence Interruption

When the enable signal keeps constant during the entire power-up or power-down sequence, the TPK1031 series operates the whole sequence as shown in Figure 12 and Figure 13. However, if the enable signal falling or rising edge comes during the power up or power down sequence, the device enters the interrupt status and initializes a new power down or power up sequence.

Figure 14 shows the power sequence with EN interruption when INV is low.

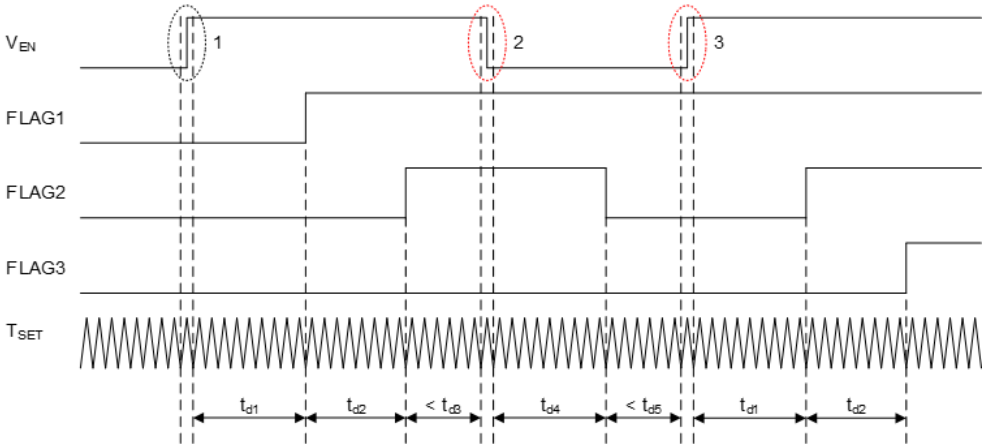



**Figure 14. Power Sequence Interruption when INV = Low**

Notes:

1. The enable signal of the device.
2. The enable interrupt during the power-up sequence.
3. The enable interrupt during the power-down sequence.

# Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## Application Information

The TPK1031 series is a 3-channel simple power sequencer, which provides power-up and power-down sequence control of multi-channel power supplies. The following application schematic shows a typical usage of the TPK1031 series.

## Typical Application

Figure 15 and Figure 16 show the typical application schematic of the TPK1031 series.

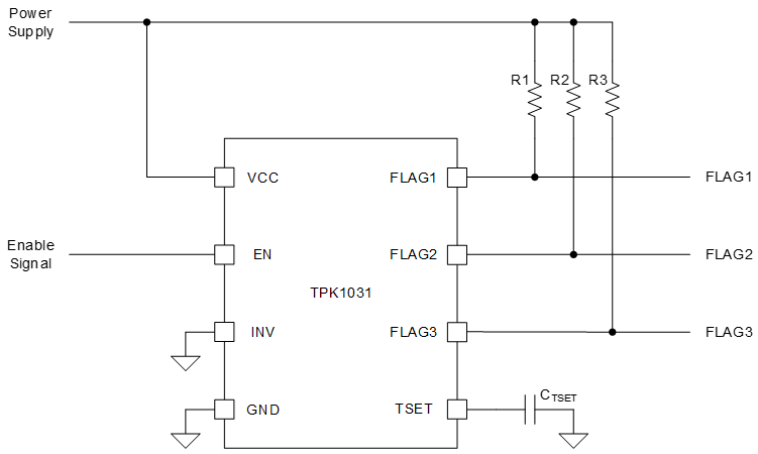



**Figure 15. $V_{CC}$ and FLAGx with the Same Power Rail**

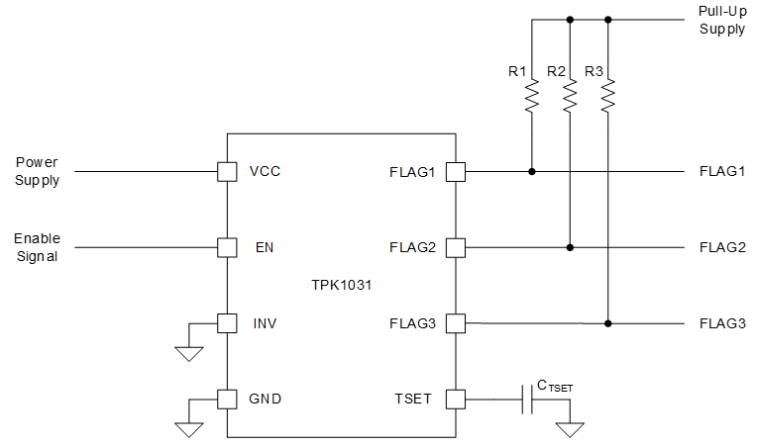



**Figure 16. $V_{CC}$ and FLAGx with Different Power Rails**

### Design Parameters

For this design example, use the parameters listed in Table 2.

**Table 2. Design Parameters**

| Parameters | Value |
|---|---|
| Power Supply Voltage Range, $V_{CC}$ | 2.7 V to 5.5 V |
| Enable Signal Voltage | LOW (< 10% of $V_{CC}$), HIGH (>90% of $V_{CC}$) |
| Pull-up Resistors, R1, R2, R3 | 100 kΩ |
| Timing Delay Capacitor, $C_{TSET}$ (1) | 10 nF |
| $t_{d1}$, $t_{d4}$ (1) | 10.44 ms to 11.60 ms |
| $t_{d2}$, $t_{d3}$, $t_{d6}$, $t_{d6}$ (1) | 9.28 ms |

(1) See Adjustable Timing Delay section for more details

### Application Waveform

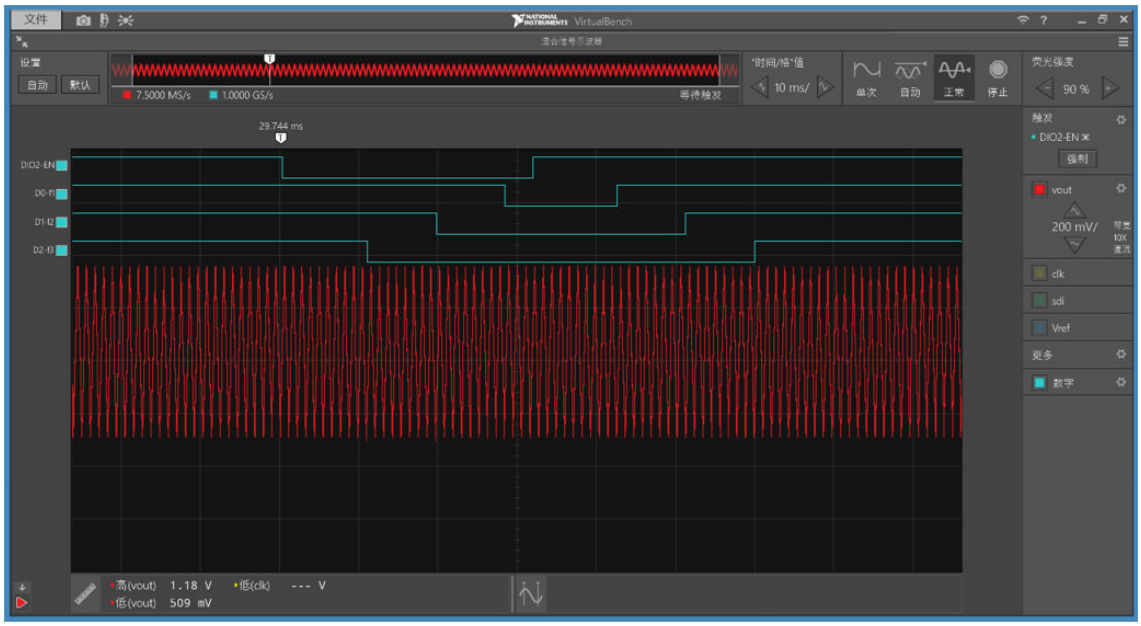



**Figure 17. Power up and Power down Sequence**

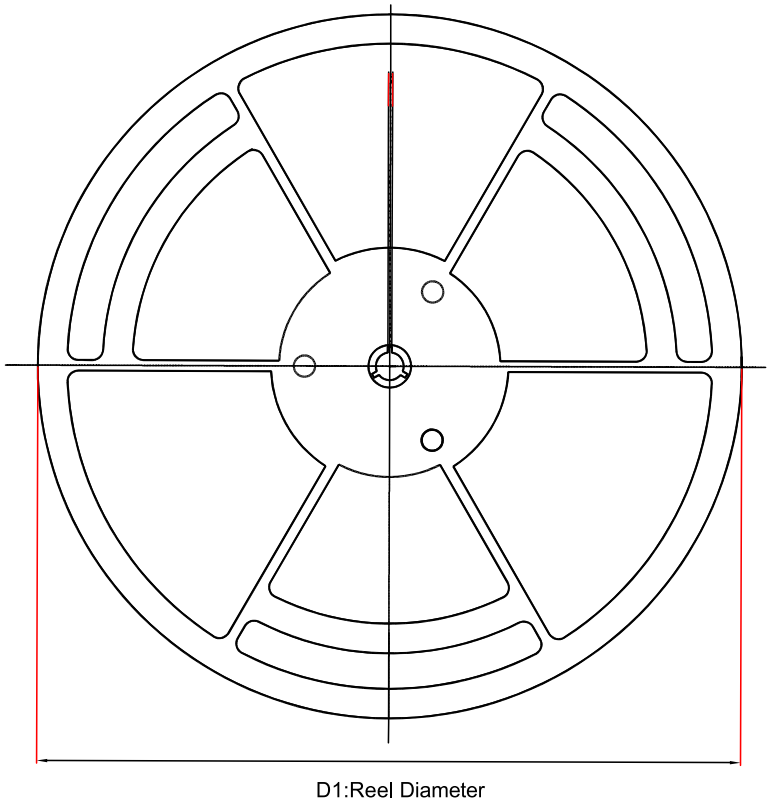
INV = GND

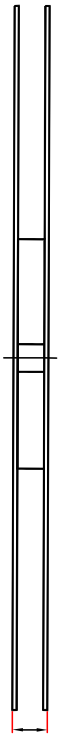
# Layout

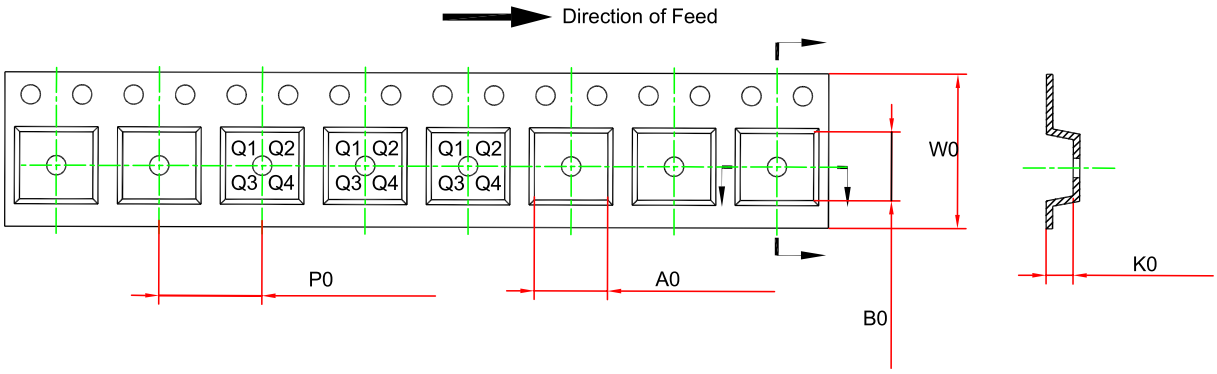
## Layout Requirements

- The FLAGx pull-up resistors, recommended 100 kΩ, should be placed close to the flag output pins and the pull-up power supply. The traces should be equal to each other, and the trace length should be as short as possible.
- The timing delay capacitor should be placed as close as possible to the $T_{SET}$ pin, and the straight trace without via is recommended.

## Tape and Reel Information



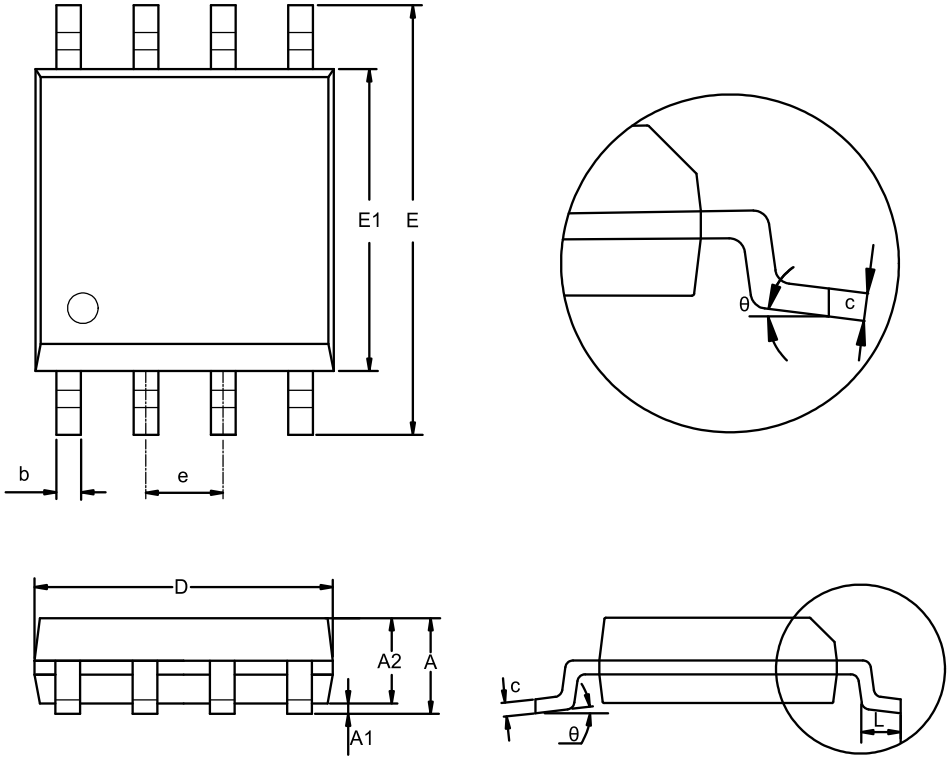




| Order Number | Package | D1 (mm) | W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | W0 (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|
| TPK1031L1-VS1R | MSOP8 | 330 | 17.6 | 5.2 | 3.3 | 1.5 | 8 | 12 | Q1 |

## Package Outline Dimensions

### MSOP8

Package Outline Dimensions VS1(MSOP-8-A)




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.800 | 1.100 | 0.031 | 0.043 |
| A1 | 0.020 | 0.150 | 0.001 | 0.006 |
| A2 | 0.750 | 0.950 | 0.030 | 0.037 |
| b | 0.250 | 0.380 | 0.010 | 0.015 |
| c | 0.090 | 0.230 | 0.004 | 0.009 |
| D | 2.900 | 3.100 | 0.114 | 0.122 |
| E | 4.700 | 5.100 | 0.185 | 0.201 |
| E1 | 2.900 | 3.100 | 0.114 | 0.122 |
| e | 0.650 BSC | | 0.026 BSC | |
| L | 0.400 | 0.800 | 0.016 | 0.031 |
| θ | 0 | 8° | 0 | 8° |

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

## Order Information

| Order Number | Operating Temperature Range | Package | Marking Information | MSL | Transport Media, Quantity | Eco Plan |
|---|---|---|---|---|---|---|
| TPK1031L1-VS1R | −40°C to 125°C | MSOP8 | K1031 | 1 | Tape and Reel, 3000 | Green |

**Green**: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

# IMPORTANT NOTICE AND DISCLAIMER



**Performance Information.** Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

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