3-V_{RMS} Audio Line Driver with Integrated Charge Pump

Features

- 3-V_{RMS} Output into 2.5-kΩ Load with 5-V Supply
- 2-V_{RMS} Output into 2.5-kΩ Load with 3.3-V Supply
- Integrated Charge Pump Generates Negative Supply Rail
- SNR Enhanced
- PVDD Power-off Delay Function
- Low THD+N: 0.001%
- Drives 600-Ω Load
- Stable with 220-pF Capacitive Load
- Pop-Free under-Voltage Protection (TPF632C/605C)
- Pop-Free Enable Control
- –40°C to 85°C Operation Range
- Robust 2-kV (Output-Pin) HBM ESD Rating on All Pins
- Robust 1.5-kV CDM ESD Rating
- Green, Popular-Type Package

Applications

- Set-Top Box
- Blue-Ray and HD DVD Players
- PDP TV and LCD TV

Description

The 3PEAK TPF632C, TPF 605C and TPF607C are 3-V_{RMS} pop-free stereo line drivers with an integrated charge pump generating the negative supply rail which allows the removal of the output DC-blocking capacitors. The devices are capable of driving 3-V_{RMS} into a 2.5-kΩ load with a single 5-V supply voltage. The TPF632C has differential inputs, the TPF605C/607C support single-ended inputs, and all use external resistors for flexible gain setting.

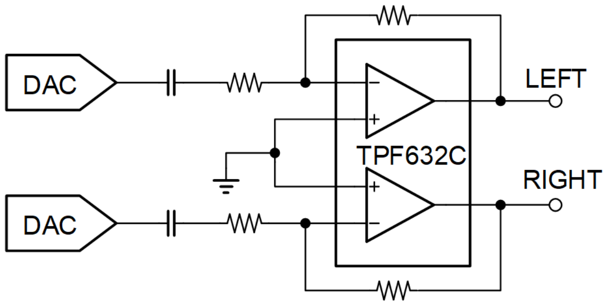
The 3PEAK TPF632C, TPF605C, and TPF607C have built-in enable/shutdown control for pop-free on/off control. The TPF632C and TPF605C have an external under-voltage detector that mutes the output when the monitored voltage droops below the set value. The use of the TPF632C/605C/607C in audio products reduces component counts considerably compared to traditional methods of generating a 3-V_{RMS} output.

The devices need only a single 5-V supply to generate an 8.5-V_{PP} output, while the traditional op-amp requires a split-rail power supply to achieve the same. The devices are ideal for single-supply electronics where size and cost are critical design parameters.

Audio Line Drivers

Part Number	Package	Remarks
TPF632C	TSSOP14	5-V/3.3-V, differential inputs
TPF605C	EMSOP10 DFN2X2-10	5-V/3.3-V, single-ended inputs
TPF607C	MSOP10	Single-ended inputs, no UVP control

Typical Application Circuit



Typical Application Circuit of TPF632C

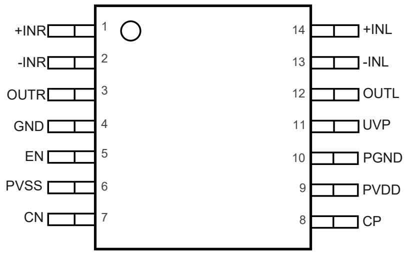
Table of Contents

Revision History

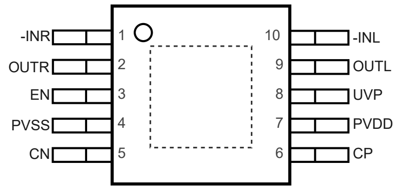
Date	Revision	Notes
2017-08-04	Rev.A.0	Initial version.
2018-08-17	Rev.A.1	Released version.
2019-03-19	Rev.A.2	• Added the DFN2X2-10 package for the TPF605C; • Changed the ESD HBM specification from 8 kV to 2 kV, and CDM specification from 2 kV to 1.5 kV, due to the change of the testing standard; • Added the EN pin description with an internal 100-k resistor.
2021-02-28	Rev.A.3	• Adjusted the V_{UVP} specification: – V_{DD} = 3.3 V, 1.15 V (Min), 1.35 V (Max); – V_{DD} = 5 V, 1.20 V (Min), 1.38 V (Max). • Changed the I_{ENL} specification from 1 μA to 2.2 μA (Max).
2025-10-21	Rev.A.4	• The following updates are all about the new datasheet formats or typos, and the actual product remains unchanged. – Updated the gain of the low-pass filtering in Table 2

Pin Configuration and Functions

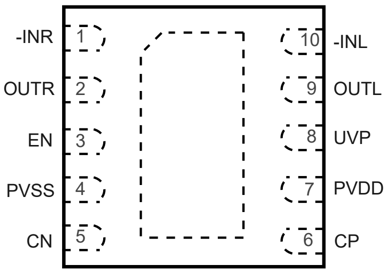
TPF632C
TSSOP14
Top View



TPF605C
EMSOP10
Top View



TPF605C
DFN2X2-10
Top View



TPF607C
MSOP10
Top View

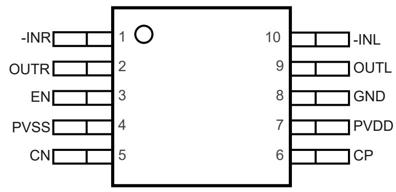


Table 1. Pin Functions

Pin No.				Name	I/O	Description
TSSOP14	**EMSOP10**	**DFN2X2-10**	**MSOP10**			
1				+INR	I	Positive input of the right channel OPAMP.
2	1	1	1	−INR	I	Negative input of the right channel OPAMP.
3	2	2	2	OUTR	O	Output of the right channel OPAMP.
4			8	GND	P	Ground.
5	3	3	3	EN	I	Enable. When left open, it is pulled high through an internal 100-kW resistor.
6	4	4	4	PVSS	P	Negative supply generated with the integrated charge pump.
7	5	5	5	CN	I/O	Negative terminal of the flying capacitor of the charge.
8	6	6	6	CP	I/O	Positive terminal of the flying capacitor of the charge.
9	7	7	7	PVDD	P	Positive supply.
10				PGND	P	Ground for the charge pump.
11	8	8		UVP	I	Under-voltage protection input.
12	9	9	9	OUTL	O	Output of the left channel OPAMP.

Pin No.				Name	I/O	Description
13	10	10	10	−INL	I	Negative input of the left channel OPAMP.
14				+INL	I	Positive input of the left channel OPAMP.

Specifications

Absolute Maximum Ratings (1)

	Parameter	Min	Max	Unit
	Supply Voltage: $V^+ - V^-$		6.0	V
V_{IN}	Input Voltage	$V^- - 0.3$	$V^+ + 0.3$	V
	Input Current: +IN, –IN, SHDN (2)	−10	10	mA
	EN Pin Voltage	V^-	V^+	V
I_O	Output Current: OUT	−20	20	mA
	Output Short-Circuit Duration (3)		Indefinite	
T_A	Operating Temperature Range	−40	125	°C
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range	–65	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500 mV beyond the power supply, the input current should be limited to less than 10 mA.
(3) A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	MIL-STD-883H Method 3015.8	2	kV
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	1.5	kV

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
TSSOP14	130	49	°C/W
MSOP10	120	45	°C/W
EMSOP10	70	10	°C/W
DFN2X2-10	94	65	°C/W

Electrical Characteristics

All test conditions: T_A = 27°C, V_{DD} = 5 V, R_L= 2.5 kΩ, C_{PUMP} = C_{PVSS} = 1 μF, C_{IN} = 10 μF, R_{IN} = 10 kΩ, R_{FB} = 20 kΩ, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply Voltage Range		2.7		5.5	V
V_{OS}	Output Offset Voltage	Input grounded, unity gain	−4		4	mV
I_Q	Quiescent Current	No load		4.6		mA
$I_{Q (off)}$	Supply Current in Shutdown				0.33	mA
V_O	Output Voltage	V_{DD} = 3.3 V, f = 1 kHz, THD = 1%	2.05			V_{RMS}
		V_{DD} = 5 V, f = 1 kHz, THD = 1%	3.05			V_{RMS}
THD + N	Total Harmonic Distortion plus Noise	V_O = 3 V_{RMS}, f = 1 kHz		0.001		%
V_{ENH}	High-Level Threshold Voltage (EN)	V_{DD} = 3.3 V, EN low-to-high transition	1			V
		V_{DD} = 5 V, EN low-to-high transition	1			V
V_{ENL}	Low-Level Threshold Voltage (EN)	V_{DD} = 3.3 V, EN high-to-low transition			0.5	V
		V_{DD} = 5 V, EN low-to-high transition			0.6	V
$\lvert I_{ENH} \rvert$	High-Level Input Current (EN)	V_{DD} = 5 V, V_I = V_{DD}			0.1	μA
$\lvert I_{ENL} \rvert$	Low-Level Input Current (EN)	V_{DD} = 5 V, V_I = 0 V			2.2	μA
X_{TALK}	Crosstalk	V_O = 3 V_{RMS}, f = 1 kHz		−110		dB
I_{SC}	Short-Circuit Current	V_{DD} = 5 V		20		mA
R_{IN}	Input Resistor Range		1	10	47	kΩ
SR	Slew Rate			5		V/μs
C_L	Maximum Capacitive Load				220	pF
C_F	Flying Capacitor		0.1	0.33	2.2	μF
V_N	Noise Output Voltage	BW = 20 Hz to 20 kHz		4.3		μV_{RMS}
SNR	Signal-to-Noise Ratio	V_O = 3 V_{RMS}, f = 1 kHz, BW = 20 kHz		117		dB
GBW	Unity Gain Bandwidth	No load		10		MHz
A_{VOL}	Open-Loop Voltage Gain	No load		130		dB
V_{UVP}	External under-Voltage Detection	V_{DD} = 3.3 V	1.15	1.23	1.35	V
		V_{DD} = 5 V	1.20	1.27	1.38	V
I_{HYS}	External under-Voltage Detection Hysteresis Current			4.7		μA
F_{CP}	Charge Pump Frequency			330		kHz

Typical Performance Characteristics

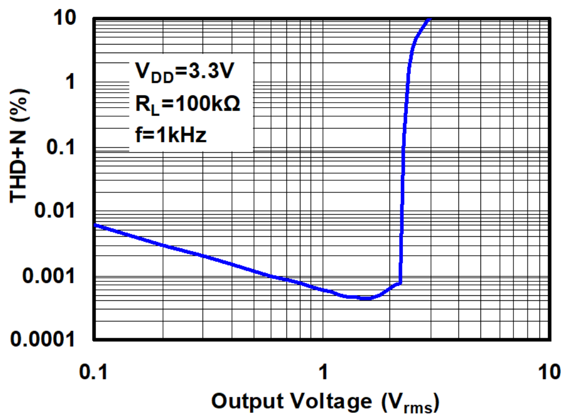


Figure 1. Total Harmonic Distortion + Noise vs. Output Voltage

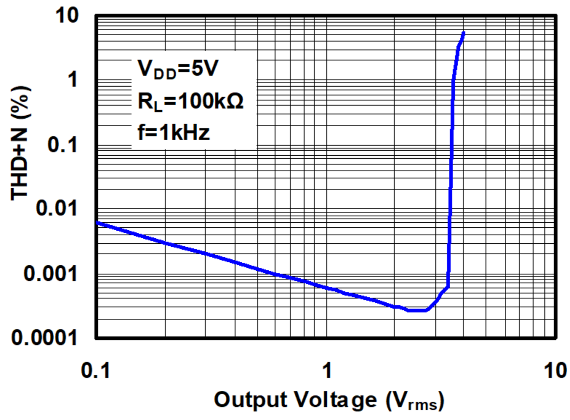


Figure 2. Total Harmonic Distortion + Noise vs. Output Voltage

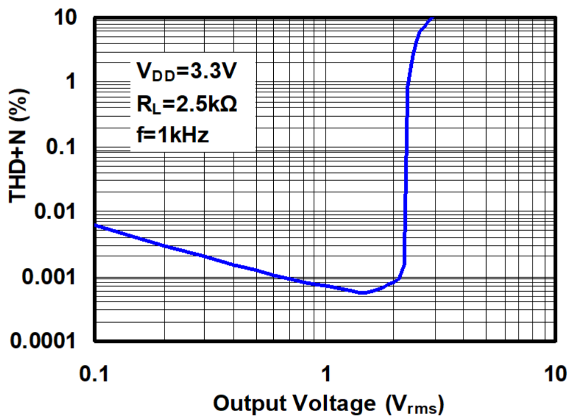


Figure 3. Total Harmonic Distortion + Noise vs. Output Voltage

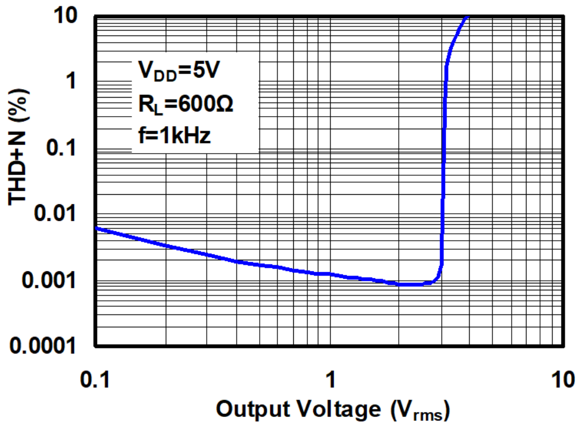


Figure 4. Total Harmonic Distortion + Noise vs. Output Voltage

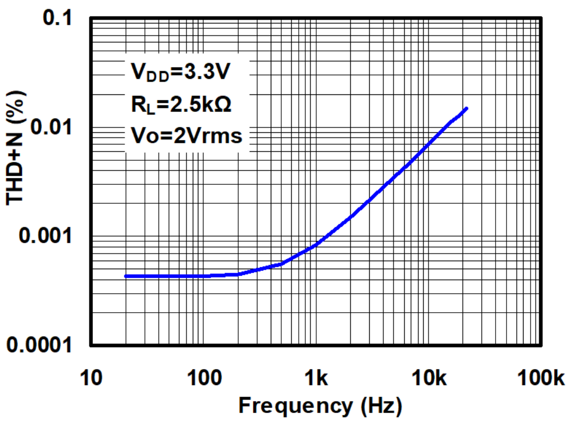


Figure 5. Total Harmonic Distortion + Noise vs. Frequency

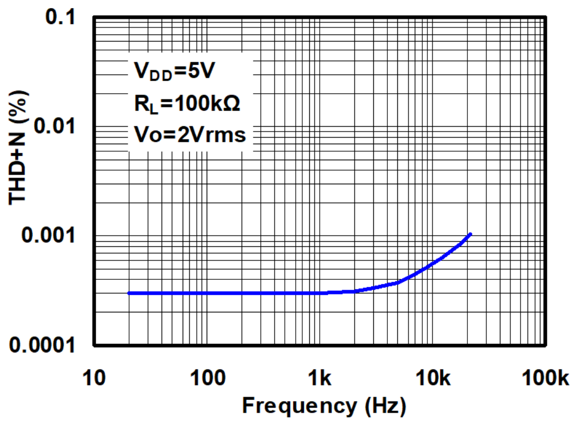


Figure 6. Total Harmonic Distortion + Noise vs. Frequency

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

Typical application circuits are shown in Figure 12 and Figure 13. The TPF632C/605C/607C operate from a single-supply voltage PVDD. The integrated charge pump generates a negative supply –PVDD at the PVSS pin. The Line driving amplifiers work with dual supplies: PVDD and –PVDD. Therefore, the DC level of the audio output is designed to be 0 V. The DC-blocking capacitor typically seen in a single-supplied driver is unnecessary.

The supply range of the TPF632C/605C/607C is from 2.7 V to 5.5 V. For a 3-V_{RMS} output, the recommended supply voltage is 5 V. For a 2-V_{RMS} output, the recommended supply voltage is 3.3 V.

R_{IN} of 2.5 kΩ and R_{FB} of 5 kΩ set the inverting gain of 2. Because of the exceptional noise performance of the TPF632C/605C/607C, the dominant noise source is actually from R_{IN}. To get better noise performance, lower input resistance and feedback resistance are used.

Integrated Charge Pump

The integrated charge pump in the TPF632C/605C/607C generates the negative power supply from a single-supply PVDD. A flying capacitor for the charge pump is applied between CP and CN. Meanwhile, a decoupling capacitor is applied between PVSS and GND. The typical value for the flying capacitor is 0.33 µF. The typical value of the decoupling capacitor is the same as or larger than that of the flying capacitor. Low-ESR capacitors are recommended for the flying capacitor and decoupling capacitor.

Audio Signal Amplification Gain Setting

The TPF632C/605C/607C are mainly applied to amplify/buffer audio signals and drive audio lines with very low distortion. Typical application circuits with inverting gain are shown in Figure 7.

Non-inverting amplification of audio signals is also possible with the same low distortion.

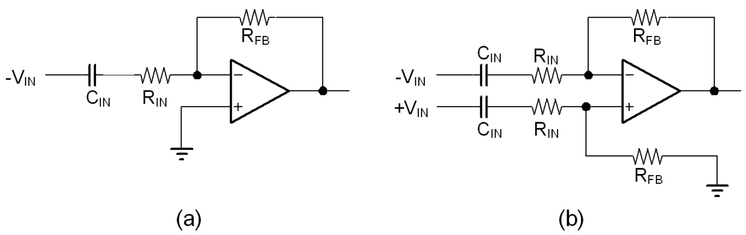


Figure 7. Typical Application Circuit of TPF632C

AC-Coupling Input Capacitors

With the integrated charge pump that generates negative rail, the TP632C/605C/607C are used to amplify audio signals, so the output DC voltage is 0 V. This usually requires the DC voltage of the input signal to be 0 V. If the input signal has a DC level other than 0 V, an AC-coupling capacitor is necessary to block the DC voltage.

The AC-coupling capacitor essentially forms a high-pass filter at the input. The cut-off frequency of the filter has to be low enough not to distort the input audio signal. For an inverting amplifier shown in Figure 7, the cut-off frequency is calculated as follows:

$$f_C = \frac{1}{2\pi R_{IN} C_{IN}} \quad (1)$$

If the required maximum cut-off frequency is known, the minimum AC-coupling capacitances are determined by:

$$C_{IN} \geq \frac{1}{2\pi R_{IN} f_C} \quad (2)$$

Adding Low-Pass Filtering to the Gain

If the low-pass filtering is necessary in addition to the audio signal amplification, a second-order filter is implemented as shown in Figure 8. The choice of C3, R1, R2, and R3 is based on the gain setting requirements and the AC-coupling cut-off frequency as discussed above. C1, C2, and C4 are calculated depending on the bandwidth. Example choices of R and C are listed in Table 2. If the first-order filtering satisfies the performance requirements, C2 and C4 are simply removed to lower the component counts.

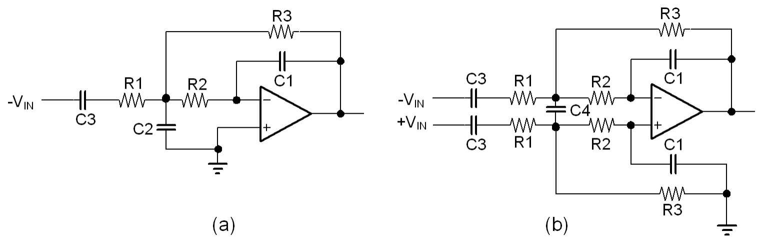


Figure 8. Second-Order Filter with Gain: (a) Single-Ended Input; (b) Differential Input

Table 2. Example RC Setting at Different Gains

Gain	R1	R2	R3	C1	C2	C3	C4
G = 4	2.5 kΩ	2.5 kΩ	10 kΩ	120 pF	1 nF	2.2 µF	360 pF
G = 5	2.4 kΩ	2.4 kΩ	12 kΩ	91 pF	750 pF	2.2 µF	390 pF
G = 7.5	2 kΩ	2 kΩ	15 kΩ	75 pF	750 pF	4.7 µF	390 pF

Pop-Free Power up and Power down

During power-up or power-down, the input device that provides audio sources experiences a significant DC-level shift. The charging of the input capacitor causes pop noise because of the DC shift. It is recommended that the TPF632C/605C/607C be disabled (EN low) during power-up and power-down, and keep disabled until the charging of the input capacitor is complete. The sequence of EN control is illustrated below.

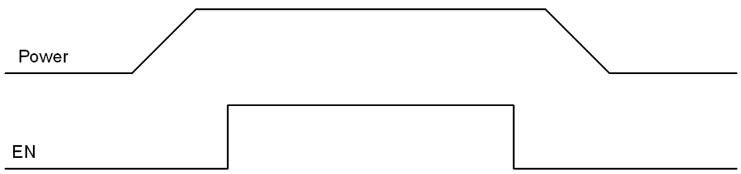


Figure 9. The Sequence of EN Control

Under-Voltage Protection

When unexpected power-off happens, the host may have insufficient time to disable the TPF632C/605C/607C before the pop noise is generated. Therefore, the integrated under-voltage protection circuits are used to mute and disable the TPF632C/605C/607C when the monitored supply voltage droops below a certain voltage.

The recommended connection is shown below. V_{SUPPLY} is the monitored supply voltage. The threshold voltage at the UVP pin is 1.23 V. R3 sets the hysteresis voltage, and is usually much larger than R1 and R2. The turn-on threshold and hysteresis can be calculated as follows:

$V_{TH} = 1.23\ V \times (R1 + R2) / R2$ (3)

Hysteresis = $4.7\ \mu A \times R3 \times (R1 + R2) / R2$ (4)

when

$R3 >> R1, R2$ (5)

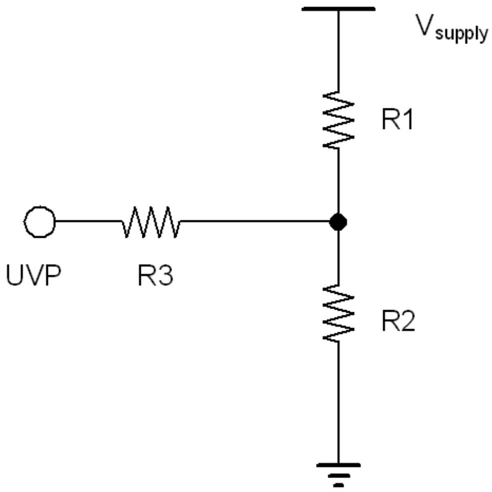


Figure 10. Under-Voltage Protection Circuits

ESD

The TPF632C/605C/607C have reverse-biased ESD protection diodes on all inputs and outputs. Input and output pins are biased no more than 300 mV beyond either supply rail.

Driving Large Capacitive Load

The TPF632C/605C/607C are designed to drive large capacitive loads up to 220 pF directly. When driving larger capacitive loads with the TPF632C/605C/607C, a small series resistor at the output (R_{ISO} in Figure 11) improves the phase margin and stability of the feedback loop by making the output loads resistive at the higher frequency. Usually, R_{ISO} of 50 Ω is sufficient.

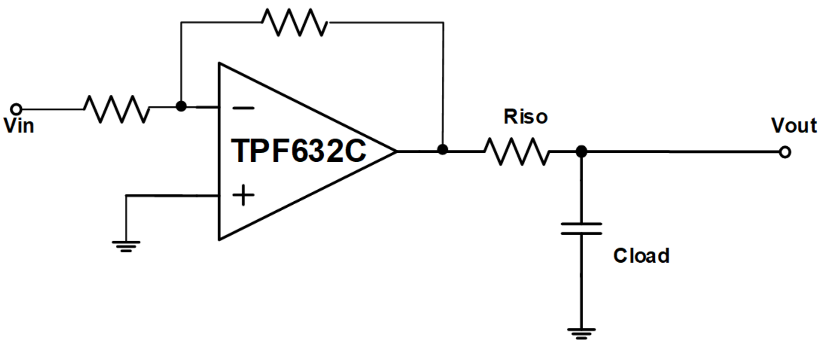


Figure 11. Driving Circuits

Power Supply Layout and Bypass

The power supply pin of the TPF632C/605C/607C has a local bypass capacitor (i.e., 0.01 μF to 0.1 μF) within 2 mm for high-frequency performance. It can also use a bulk capacitor (i.e., 1 μF or larger) within 100 mm to provide large and slow currents. This bulk capacitor can be shared with other analog parts.

The ground layout improves the performance by decreasing the amount of stray capacitances and noise at the inputs and outputs of OPA. To decrease stray capacitances, PC board lengths and resistor leads are minimized, and external components are placed as close to the pins of the op amps as possible.

Proper Board Layout

To ensure optimum performance at the PCB level, the design of the board layout must be careful. To avoid leakage currents, the surface of the board is kept clean and free of moisture. The coating of the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board.

Keeping supply traces short and properly bypassing the power supplies minimizes power supply disturbances caused by output current variations, such as when driving an AC signal into a heavy load. Bypass capacitors are connected as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and inputs of the amplifier. It is recommended that signal traces be kept at least 5 mm from supply lines to minimize coupling.

A variation in temperature across the PCB causes a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, resistors are oriented so that heat sources warm both ends equally. Input signal paths contain matching numbers and types of components to match the number and type of thermocouple junctions. For example, dummy components, such as zero-value resistors, are used to match real resistors in the opposite input paths. Matching components are located in close proximity and oriented in the same manner. Ensure that leads are of equal length so that thermal conduction is in equilibrium. Keeping heat sources on the PCB far away from the amplifier input circuitry is practical.

A ground plane is highly recommended. The ground plane reduces EMI noise and helps maintain a constant temperature across the circuit board.

Typical Application

Figure 12 and Figure 13 show the typical application schematics.

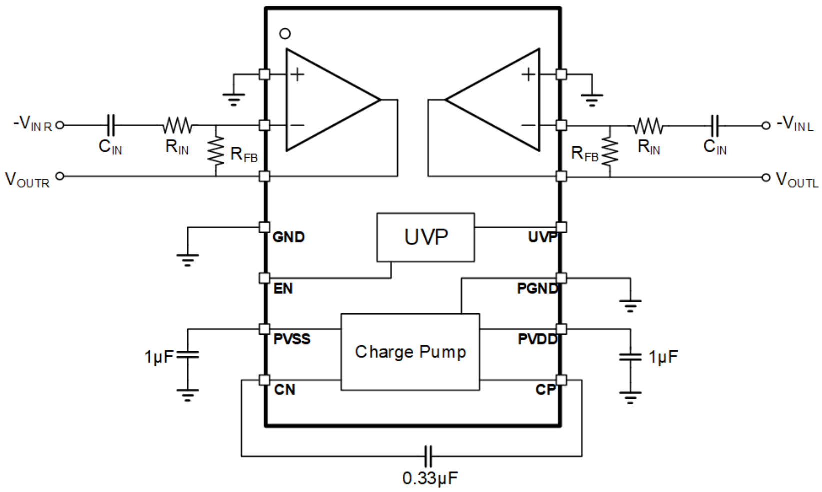
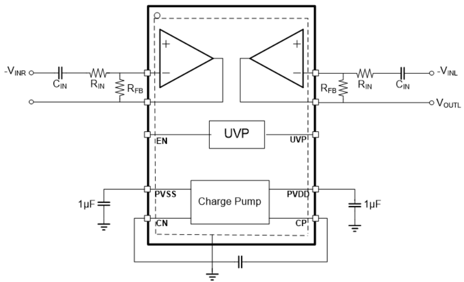


Figure 12. Typical Application Circuit of TPF632C



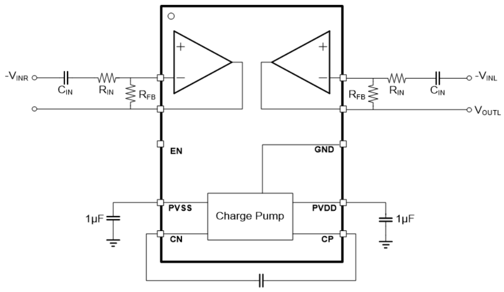
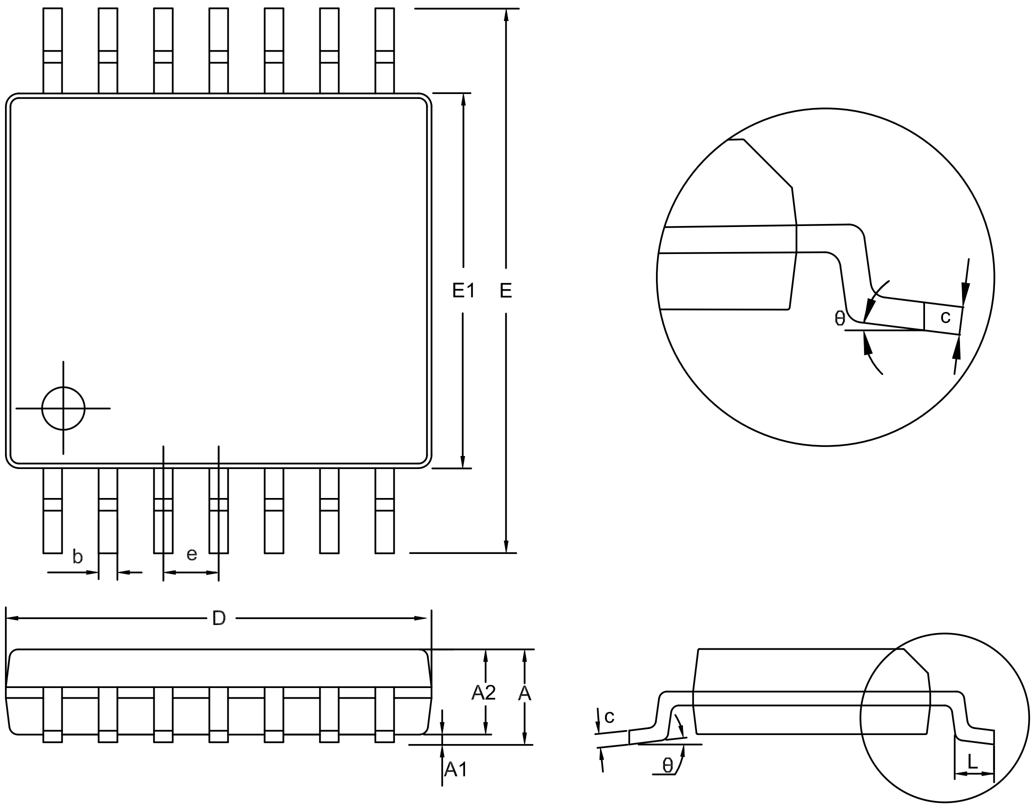


Figure 13. Typical Application Circuit of TPF605C (Left) and TPF607C (Right)

Package Outline Dimensions

TSSOP14

Package Outline Dimensions TS2(TSSOP-14-A)



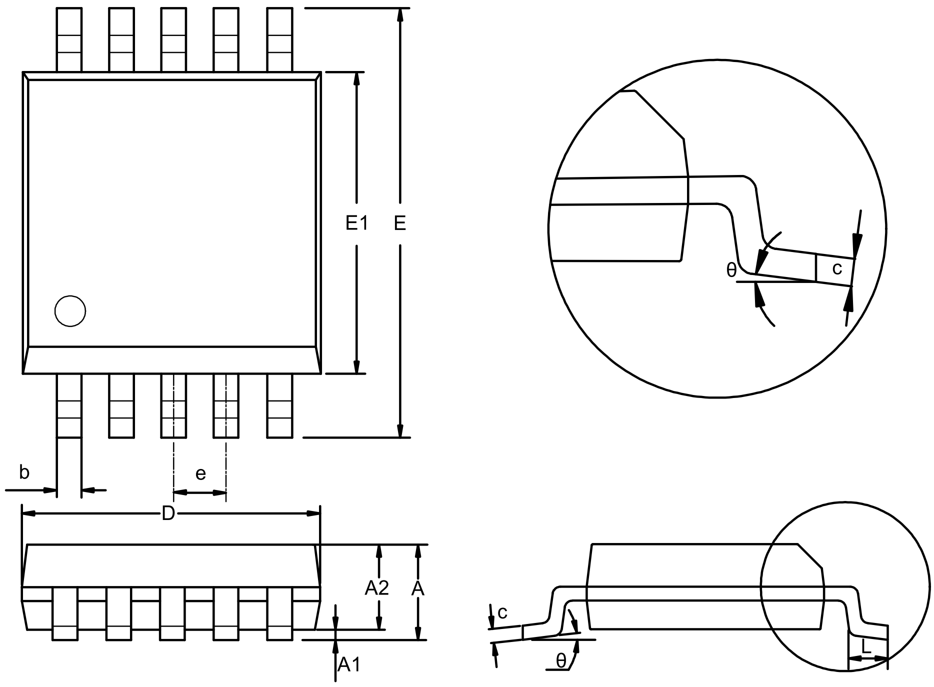
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

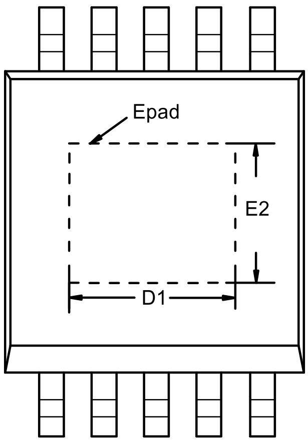
NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

EMSOP10

Package Outline Dimensions EV2(EMSOP-10-A)





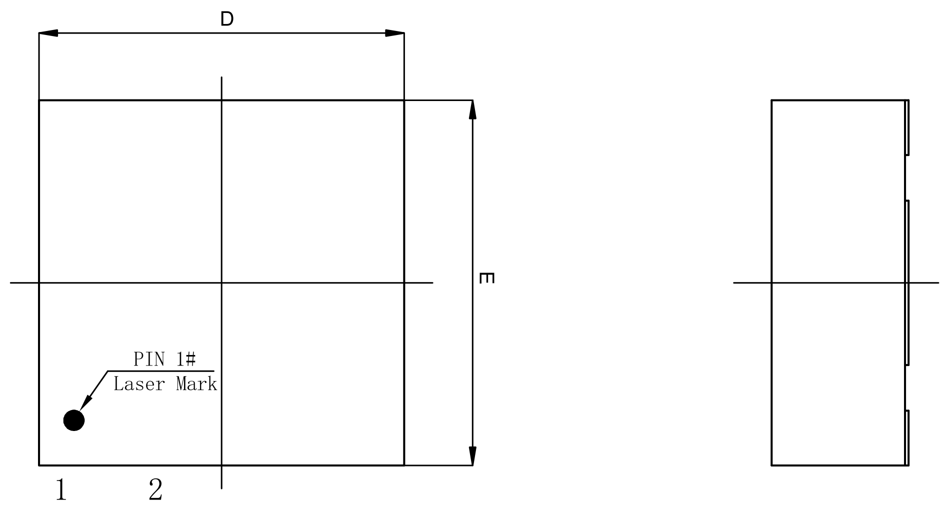
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	1.100	0.031	0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
D1	1.700	1.900	0.067	0.075
E	4.700	5.100	0.185	0.201
E1	2.900	3.100	0.114	0.122
E2	1.450	1.650	0.057	0.065
e	0.500 BSC		0.020 BSC	
L	0.400	0.800	0.016	0.031
θ	0	8°	0	8°

NOTES

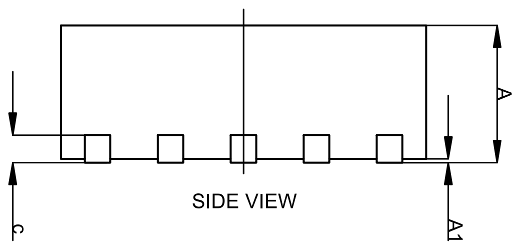
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

DFN2X2-10

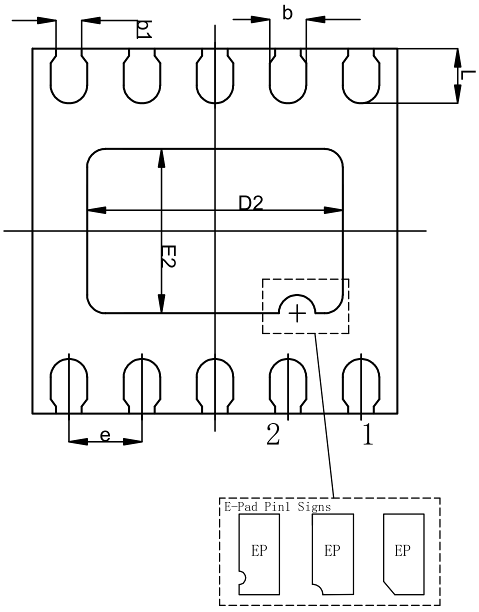
Package Outline Dimensions DFF(DFN2X2-10-A)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

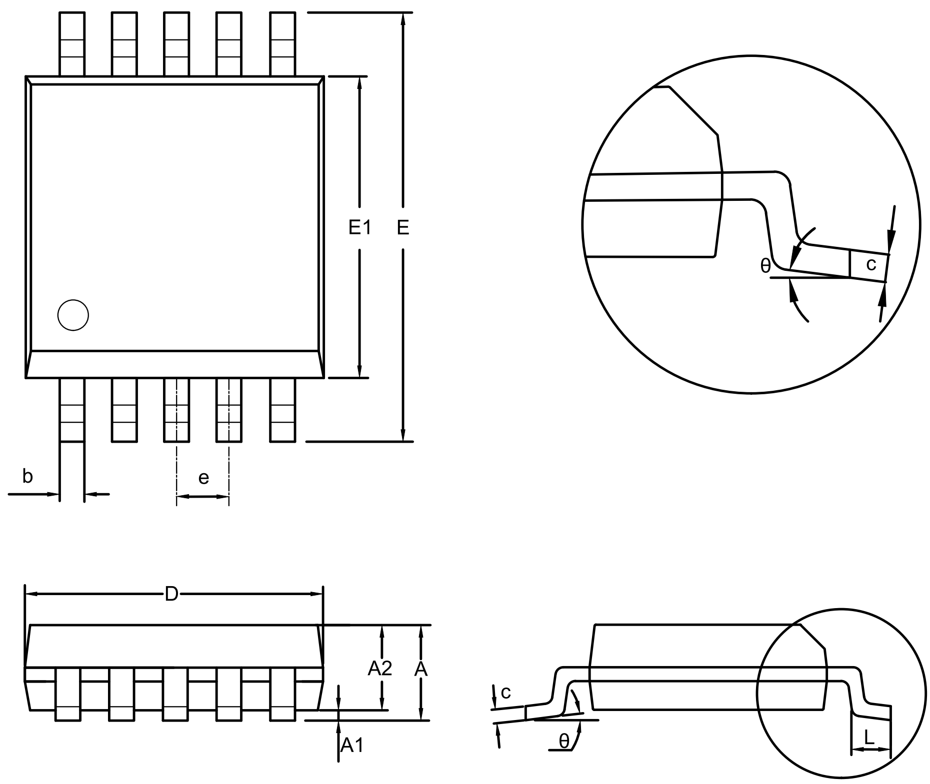
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.150	0.250	0.006	0.010
c	0.150	0.250	0.006	0.010
D	1.900	2.100	0.075	0.083
D2	1.300	1.500	0.051	0.059
E	1.900	2.100	0.075	0.083
E2	0.800	1.000	0.031	0.039
e	0.400 BSC		0.016 BSC	
L	0.250	0.350	0.010	0.014

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

MSOP10

Package Outline Dimensions VS2(MSOP-10-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	1.100	0.031	0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	4.700	5.100	0.185	0.201
E1	2.900	3.100	0.114	0.122
e	0.500 BSC		0.020 BSC	
L	0.400	0.800	0.016	0.031
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPF632C-TR	−40 to 85°C	TSSOP14	TPF632C	MSL3	Tape and Reel, 3000	Green
TPF605C-VR	−40 to 85°C	EMSOP10	TPF605C	MSL3	Tape and Reel, 3000	Green
TPF605C-DFFR (1)	−40 to 85°C	DFN2X2-10	05C	MSL3	Tape and Reel, 3000	Green
TPF607C-VR (1)	−40 to 85°C	MSOP10	TPF607C	MSL3	Tape and Reel, 3000	Green

(1) End of life.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

IMPORTANT NOTICE AND DISCLAIMER

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