

Features

- Wide Power Supply: +3.0V to +5.5V Single Supply
- Robust ESD Rating: >8kV HBM, >2kV CDM
- Green Product, MSOP8 Package

Video Filter:

- HDTV Video Filter Support Composite 1080p/60
- Optimized 6th-order Butterworth Video reconstruction filter:
 - ◆ HD Channel: -3dB BW 52MHz
- Support Multiple Input Biasing:
 - ◆ Transparent Clamping for DC restoration
 - ◆ Provide 80-mV Level-Shift when DC-Coupled
- 6dB Gain(2V/V), Rail to Rail Output
- AC- or DC-Coupled Output Driving Dual Video Loads (75Ω)

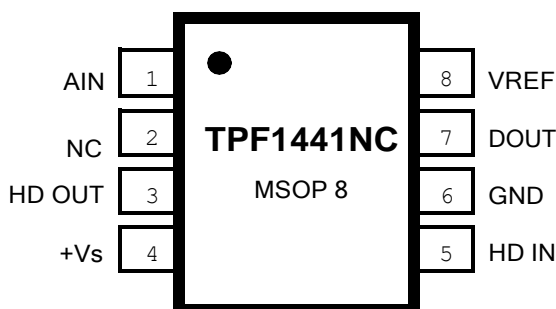
Comparator:

- Fast Response Time: 40 ns Propagation Delay
- Internal Hysteresis Ensures Clean Switching
- Push-Pull, CMOS/TTL Compatible Output
- Same DC clamping circuit as video input.

Applications

- Video Signal Amplification
- Set-Top Box Video Driver
- TV、DVD Player Video Buffer
- Video Buffer for Portable or USB-Powered Video Devices
- HDTV

Pin Configuration (Top View)



Description

The TPF1441NC is a low power, 52M HD composite video filter and comparator on a single chip. Drawing less than 11.5mA supply current over the full operating temperature range, TP1441NC operates from a single 3.0V to 5.5V power supply.

TPF1441NC integrates high-performance low-cost 52MHz composite video reconstruction filter, however it has very low power consumption. The filter is sixth-order Butterworth characteristics that are useful as digital-to-analog converter (DAC) reconstruction filters or as analog-to-digital converter (ADC) anti-aliasing filters. The HD filters can actually support 720p/1080p CVI/TVI/AHD platform.

The TPF1441NC's on-board comparator incorporates 3PEAK's proprietary and patented design techniques to achieve the ultimate combination of high-speed (40ns propagation delay under 3.0~5.5V wide supply range) and low power consumption , The internal input hysteresis eliminates output switching due to internal input noise voltage, reducing current draw. The PUSH-PULL output supports rail-to-rail output swing, and interfaces with CMOS/TTL logic.

TPF1441NC is available in MSOP-8 package (TP1441NC-VR). Its operation temperature range is from -40°C to +85°C.

Related Resources

AN-1201: Application notes of TPF1XX

Pin Name	Pin Function
AIN	Non-Inverting Input of the Comparator
NC	Not connect
HD OUT	HD video output, LPF = 52 MHz
+Vs	Positive Power Supply
HD IN	HD video input, LPF = 52 MHz
GND	Ground
DOUT	Comparator Output
VREF	Inverting Input of Comparator

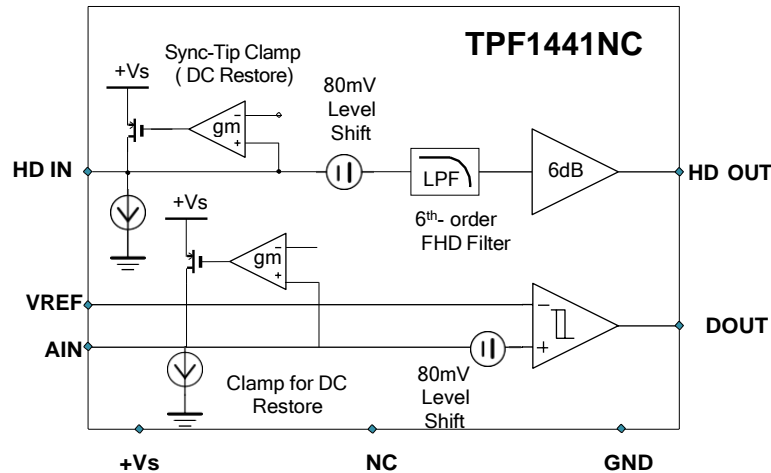
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Revision History

Date	Revision	Notes
2017/10/15	Rev.A.0	Initial Version
2018/10/30	Rev.A.1	Released Version

Function Block



Order Information

Order Number	Operating Temperature Range	Package	Marking Information	Transport Media, Quantity
TPF1441NC-VR	-40 to 85°C	8-Pin MSOP	TPF1441NC	Tape and Reel, 3000

Absolute Maximum Ratings*

Parameters		Value	Units
Power Supply, V_{DD} to GND		6.0	V
V_{IN}	Input Voltage	$V_{DD} + 0.3V$ to GND - 0.3V	
I_O	Output Current	65	mA
T_J	Maximum Junction Temperature	150	°C
T_A	Operating Temperature Range	-45 to 85	°C
T_{STG}	Storage Temperature Range	-65 to 150	°C
TL	Lead Temperature (Soldering 10 sec)	300	°C
θ_{JA}	8-Lead MSOP	210	°C/W

* **Note:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(1) This data was taken with the JEDEC low effective thermal conductivity test board.

(2) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	8	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	2	kV

Electrical Characteristics

All test condition is $V_{DD} = 3.3V$, $T_A = +25^{\circ}C$, $R_L = 150\Omega$ to GND, unless otherwise noted.

SYMBOL	PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Input Electrical Specifications							
V_{DD}	Supply Voltage Range			3.0		5.5	V
I_{DD}	Quiescent current (I_Q) ⁽¹⁾		$V_{DD} = 3.3V$, $V_{IN} = 500mV$, no load		9		mA
			$V_{DD} = 5.0V$, $V_{IN} = 500mV$, no load		10		mA
$I_{CLAMP-DOWN}$	Clamp Discharge Current		$V_{IN}=300mV$, measure current	0.6	2.64	4.8	μA
$I_{CLAMP-UP}$	Clamp Charge Current		$V_Y = -0.2V$		-1.7		mA
V_{CLAMP}	Input Voltage Clamp ⁽²⁾		$I_Y = -100\mu A$	0		+40	mV
R_{IN}	Input Impedance		$0.5V < V_Y < 1V$		3		M Ω
AV	Voltage Gain		$V_{IN}=0.5V, 1V$ or $2V$ $R_L=150\Omega$ to GND	5.91	6.02	6.06	dB
V_{OLS}	Output Level Shift Voltage		$V_{IN} = 0V$, no load, input referred	54	80	124	mV
V_{OL}	Output Voltage Low Swing		$V_{IN} = -0.3V$, $R_L = 75\Omega$		0.058		V
V_{OH}	Output Voltage High Swing		$V_{IN} = 3.3V$, $R_L = 75\Omega$ to GND (dual load)		3.24		V
PSRR	Power Supply Rejection Ratio		$\Delta V_{DD} = 3.3V$ to $3.6V$		61		dB
			$\Delta V_{DD} = 5.0V$ to $5.5V$, 50Hz		67		dB
I_{SC}	Short-circuit current		$V_{IN} = 2V$, 10Ω , output to GND		65		mA
			$V_{IN} = 0.1V$, output short to V_{DD}		65		mA
AC Electrical Specifications							
f_{-1dB}	-1dB Bandwidth	HD Channel	$R_L = 150\Omega$		41.5		MHz
f_{-3dB}	-3dB Bandwidth	HD Channel	$R_L = 150\Omega$		52		MHz
dG	Differential Gain		Video input range 1V		0.4		%
dP	Differential Phase		Video input range 1V		0.7		°
THD	Total Harmonic Distortion	HD Channel	$f=10MHz$, $V_{OUT}=1.4V_{PP}$		0.15		%
			$f=22MHz$, $V_{OUT}= 1.4V_{PP}$		0.6		%
D/DT	Group Delay Variation	HD Channel	$f = 100kHz$ to $27MHz$		2.2		ns
			$f = 100kHz$ to $60MHz$		6.0		ns
SNR	Signal-to-Noise Ratio	HD Channel	$f= 100kHz$ to $60MHz$		64		dB
R_{OUT_AC}	Output Impedance		$f = 10MHz$		0.5		Ω

*Note: (1). 100% tested at $T_A=25^{\circ}C$.

(2). Comparator Clamp has the same specification.

Electrical Characteristics-Comparator Part

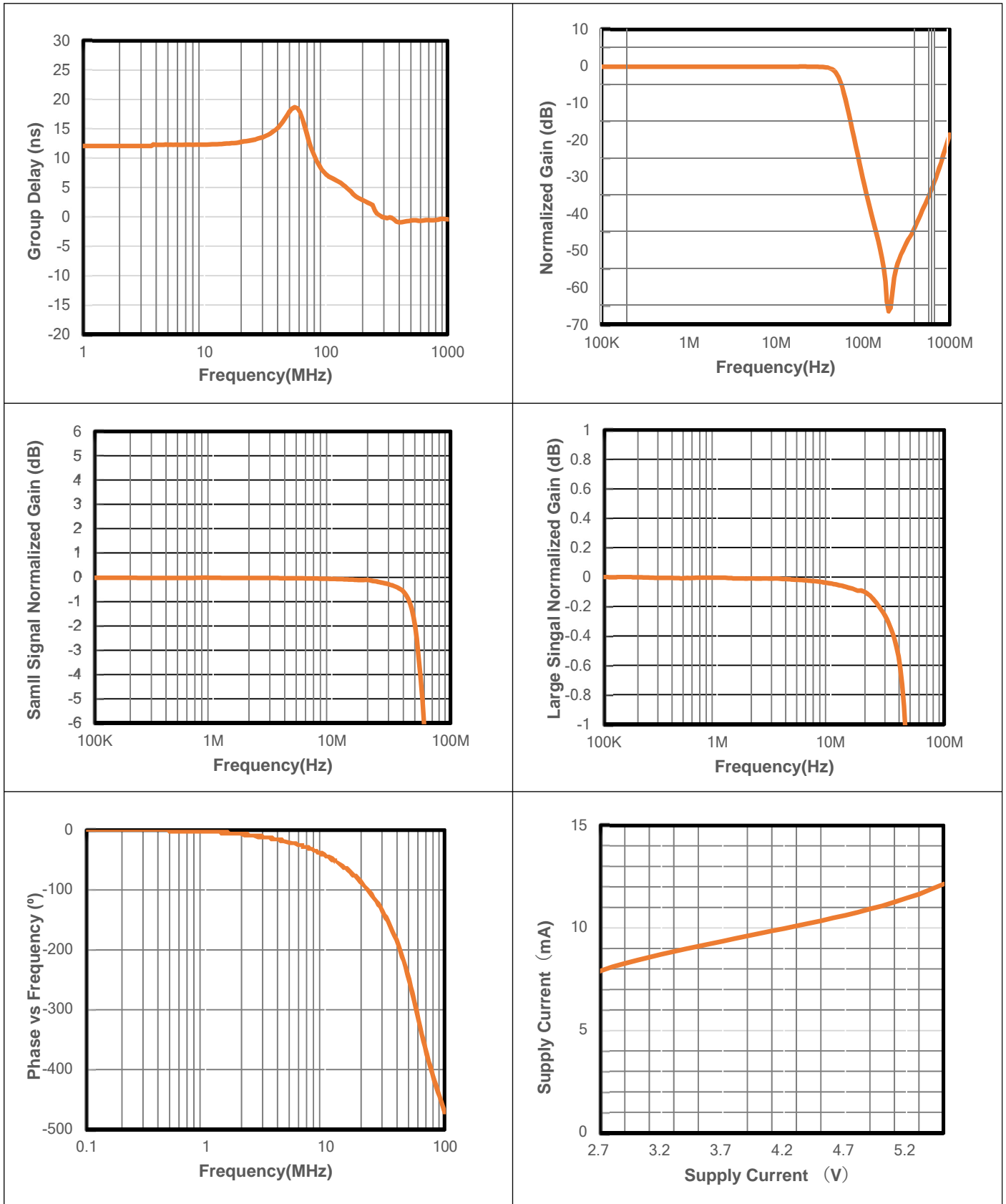
All test condition is VDD = 3.3V, TA = +25°C, CL =15pF, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{DD}	Supply Voltage		3		5.5	V
V _{OS}	Input Offset Voltage ^{Note 1}	V _{CM} = 1.2V		80		mV
V _{OS} TC	Input Offset Voltage Drift ^{Note 1}	V _{CM} = 1.2V		0.3		μV/°C
V _{HYST}	Input Hysteresis Voltage ^{Note 1}	V _{CM} = 1.2V		6		mV
V _{OH}	High-Level Output Voltage	I _{OUT} = -1mA	V _{DD} - 0.3			V
V _{OL}	Low-Level Output Voltage	I _{OUT} = 1mA			V _{SS} + 0.3	V
I _{SC}	Output Short-Circuit Current	Sink or source current		5		mA
t _R	Rising Time			7		ns
t _F	Falling Time			7		ns
T _{PD+}	Propagation Delay (Low-to-High)	VREF = 1.65V		36		ns
T _{PD-}	Propagation Delay (High-to-Low)	VREF = 1.65V		42		ns
T _{PDSKEW}	Propagation Delay Skew	VREF = 1.65V		4		ns

Note 1: The input offset voltage is the average of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.

Typical Performance Characteristics

All test condition is VDD = 3.3V, TA = +25°C, RL = 150Ω to GND, unless otherwise noted.



Application Information

The TPF1441NC is targeted for systems that require 1 channel high-definition (HD) video outputs. Although it can be used for numerous other applications, the needs and requirements of the video signal are the most important design parameters of the TPF1441NC. The TPF1441NC incorporates many features not typically found in integrated video parts while consuming very low power.

Internal Sync Clamp

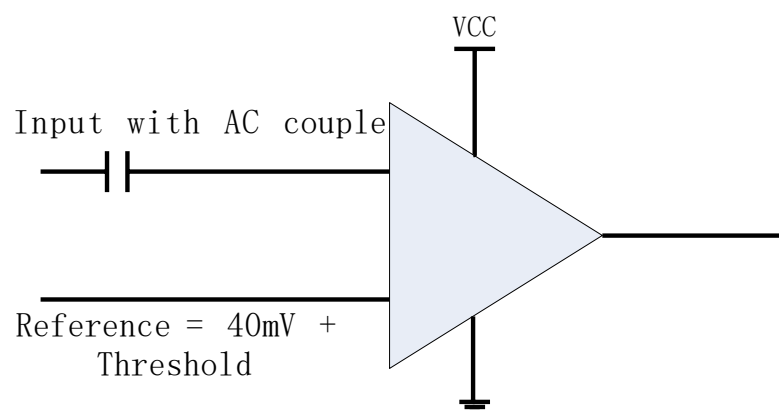
The typical embedded video DAC operates from a ground referenced single supply. This becomes an issue because the lower level of the sync pulse output may be at a 0V reference level to some positive level. The problem is presenting a 0V input to most single supply driven amplifiers will saturate the output stage of the amplifier resulting in a clipped sync tip and degrading the video image. A larger positive reference may offset the input above its positive range.

The TPF1441NC features an internal sync clamp and offset function to level shift the entire video signal to the best level before it reaches the input of the amplifier stage. These features are also helpful to avoid saturation of the output stage of the amplifier by setting the signal closer to the best voltage range.

The simplified block diagram of the TPF1441NC is on Page-2. The AC coupled video sync signal is pulled negative by a current source at the input of the comparator amplifier. When the sync tip goes below the comparator threshold the output comparator is driven negative, The PMOS device turns on clamping sync tip to near ground level. The network triggers on the sync tip of video signal.

Comparator Internal Clamp

TPF1441NC integrates a comparator, which supports UTC function monolithically. Because of the distortion of the control signal transmitted over a long cable, the rising/falling edges would become slower and the amplitude would be attenuated. Furthermore the DC component may be shifted due to inconsistent DC ground level between sending and receiving devices. In a traditional design, the reference of the comparator needs to be manually changed accordingly. In order to solve this application problem, TPF1441NC implements a new feature on the input of comparator which clamps the bottom level of the input signal to 40.0 mV. Therefore, there is no need to consider the DC shift issue when choosing reference level, making the choice of reference level easier. Note that, to use this feature, the input must be AC-coupled and the capacitor selection is based on the control signal bandwidth. Typically a 0.1uF capacitor is used..



Droop Voltage and DC Restoration

Selection of the input AC-coupling capacitance is based on the system requirements. A typical sync tip width of a 64µs NTSC line is 4µs during which clamp circuit restores its DC level. In the remaining 60µs period, the voltage droops because of a small constant 2.0µA sinking current. If the AC-coupling capacitance is 0.1µF, the maximum droop voltage is about 1mV which is restored by the clamp circuit. The maximum pull-up current of the clamp circuit is 1.7mA. For a 4µs sync tip width and 0.1µF capacitor, the maximum restoration voltage is about 80mV.

The line droop voltage will increase if a smaller AC-coupling capacitance is used. For the same reason, if larger capacitance is used the line droop voltage will decrease. Table 1 is droop voltage and maximum restoration voltage of the clamp for typical capacitance.

CAP VALUE (nF)	DROOP IN 60µs (mV)	CHARGE IN 4µs (mV)
100	1.2	68
1,000	0.12	6.8

Table 1. Maximum restoration voltage and droop voltage of Y signals for different capacitance

Low Pass Filter--Sallen Key

The Sallen Key is a classic low pass configuration. This provides a very stable low pass function, and in the case of the TPF1441NC, the six-pole roll-off at around 52MHz. The six-pole function is accomplished with an RC low pass network placed in series with and before the Sallen Key.

Output Couple

TPF1441NC output could support both “AC Couple” and “DC Couple”, if use “AC Couple”, this capacitor is typically between 220-µF and 1000-µF, although 470-µF is common. This value of this capacitor must be this large to minimize the line tilt (droop) and/or field tilt associated with ac-coupling as described previously in this document.

The TPF1441NC internal sync clamp makes it possible to DC couple the output to a video load, eliminating the need for any AC coupling capacitors, thereby saving board space and additional expense for capacitors. This makes the TPF1441NC extremely attractive for portable video applications. Additionally, this solution completely eliminates the issue of field tilt in the lower frequency. The trade-off is the supply current could be bigger. Typical load current for AC coupled is around 1mA, compared to typical 11.5mA used when DC coupling.

Output Drive Capability and Power Dissipation

With the high output drive capability of the TPF1441NC, it is possible to exceed the +125°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for an application to determine if load conditions or package types need to be modified to assure operation of the amplifier in a safe operating area. The maximum power dissipation allowed in a package is determined according to Equation:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{JA}$$

Where:

TJMAX = Maximum junction temperature

TAMAX = Maximum ambient temperature

Θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or: for sourcing:

$$PD_{MAX} = V_s \times I_{SMAX} + (V_s - V_{OUT}) \times \frac{V_{OUT}}{R_L}$$

Where:

VS = Supply voltage

ISMAX = Maximum quiescent supply current

VOU = Maximum output voltage of the application

RLOAD = Load resistance tied to ground

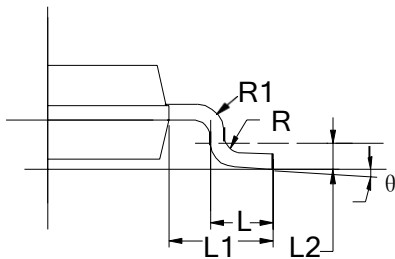
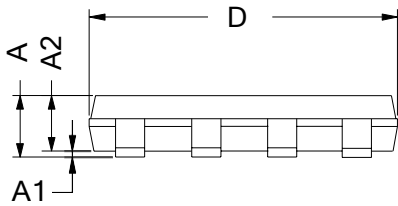
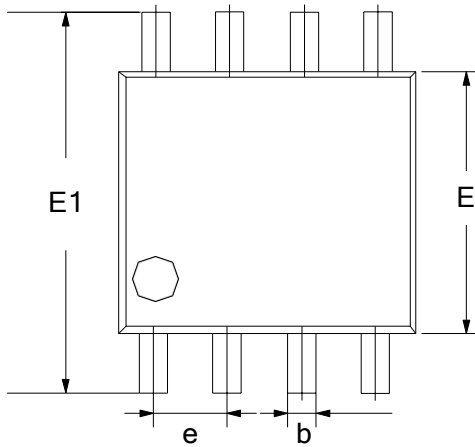
By setting the two PDMAX equations equal to each other, we can solve the output current and RLOAD to avoid the device overheat.

Power Supply Bypassing Printed Circuit Board Layout

As with any modern operational amplifier, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as short as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, a single 4.7 μ F tantalum capacitor in parallel with a 0.1 μ F ceramic capacitor from VS+ to GND will suffice.

Package Outline Dimensions

MSOP-8



Symbol	Dimensions In Millimeters	
	Min	Max
A	0.800	1.200
A1	0.000	0.200
A2	0.750	0.950
b	0.30 TYP	
C	0.15 TYP	
D	2.900	3.100
e	0.65 TYP	
E	2.900	3.100
E1	4.700	5.100
L	0.400	0.800
L1	0.95 TYP	
L2	0.25 TYP	
θ	0°	6°

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