8-CH PDM to TDM Converter

Features

- System Features:
  - 4/8 Channels of PDM Audio Inputs from Digital Microphones
  - 16×, 32×, or 64× Decimation Ratio of PDM to PCM Audio Data
  - 24-bit Data Sampling to Support High SPL Microphones
  - 126 dB A-weighted SNR
  - 4/8/12/16/24/48/96/192 kHz Output Sampling Rate
  - Bit Clock Rates of 64×, 128×, 256×, or 512× Output Sampling Rate
  - Dual Pins Can Output PDM Clocks Generated from the Identical Source
  - Automatic PDM Clock Generation
  - Automatic Power-down if BCLK Removed
- Programmable Channel Settings
  - Gain Calibration with 0.07-dB Resolution
  - Phase Calibration with 163-ns Resolution
- Audio Interface Features
  - PDM Input, TDM or I^2S Output
  - Output Slot Width: 16 bits, 24 bits, or 32 bits
  - Support Slave I^2S or TDM2/4/8/16 (cascaded)
  - Configurable TDM Slot Routing and Sizes
- Control Interface Features
  - Selectable I^2C Software Control or Hardware Mode Operation
  - Support I^2C Bus Speed: 100 Kbps, 400 Kbps, or 1 Mbps
- Power Features
  - I/O Supply Voltage from 1.70 V to 3.63 V
  - DVDD Supply Voltage from 1.70 V to 1.98 V
  - 2.5 mA DVDD Operating Current for 4/8-ch at 48 kHz Sampling Rate & 1.8 V Supply
  - < 5-μA Typical DVDD Shutdown Current
- Ambient Temperature: –40°C to +85°C
- 0.50 mm Pitch QFN3X3-16

Applications

- Microphone Arrays
- Conference System
- Education System
- AI Mobile Computing
- Notebook/Pad
- Smart Speakers
- A/V Surveillance System

Description

The TPDA7008 is a high-performance converter that converts Pulse Density Modulation (PDM) input streams to one Pulse Code Modulation(PCM) output stream. And the audio PCM data can be sent through the serial audio interface of Time Division Multiplexing (TDM) or I^2S. The PDM data can be from up to eight digital microphones or other PDM sources.

The TPDA7008 features some advanced integrated designs of programmable channel gain and phase, high-pass filter (HPF), bi-quad filters, and low-latency filters that improve audio performance. With these excellent performance functions, the TPDA7008 becomes a suitable choice of hardware peripheral in entire audio systems, particularly in far-field microphone arrays for voice acquisition and algorithm processing.

Functional Block Diagram

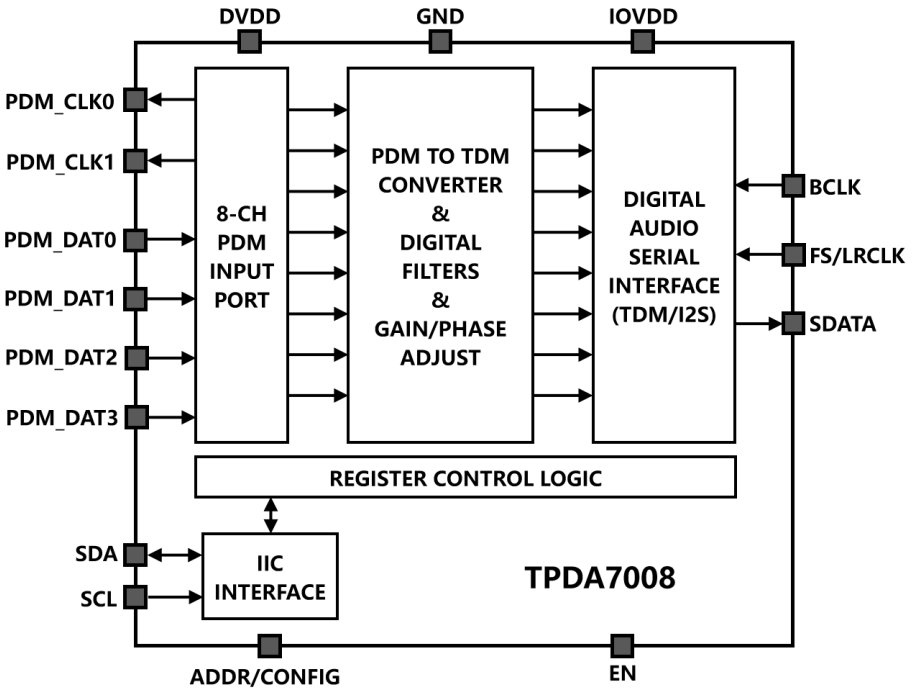


Table of Contents

Product Family Table

Order Number	Function	Marker	MSL	Package
TPDA7008-QFNR	Support up to 8 PDM MICs	PT8	3	QFN3x3-16
TPDA7004-QFNR	Support up to 4 PDM MICs	PT4	3	QFN3x3-16

Revision History

Date	Revision	Notes
2025-10-28	Rev.A.0	Released version

Pin Configuration and Functions

TPDA7008
QFN3x3-16 Package
Top View

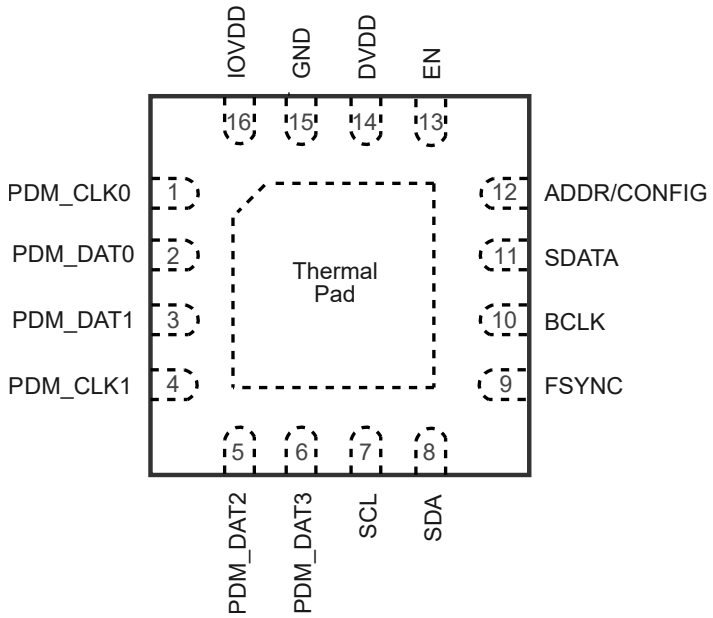


Table 1. Pin Functions: TPDA7008

Pin No.	Name	I/O	Description
1	PDM_CLK0	OUT	PDM Output Clock 0.
2	PDM_DAT0	IN	PDM Input Data 0.
3	PDM_DAT1	IN	PDM Input Data 1.
4	PDM_CLK1	OUT	PDM Output Clock 1.
5	PDM_DAT2	IN	PDM Input Data 2.
6	PDM_DAT3	IN	PDM Input Data 3.
7	SCL	IN	I^2C Serial Clock Input.
8	SDA	IN/OUT	I^2C Data In or Out.
9	FSYNC	IN	I^2S/TDM Frame Sync or Left/Right Clock.
10	BCLK	IN	I^2S/TDM Bit Clock.
11	SDATA	OUT	I^2S/TDM Serial Data Output.
12	ADDR/CONFIG	IN	I2C Address or Standalone Configuration Selection.
13	EN	IN	Chip Enable.

Pin No.	Name	I/O	Description
			Ground this pin to disable the device and put it in low power mode. Apply IOVDD to this pin to enable normal operation. All register settings are preserved when the device is disabled. However, the bit clock counters, and the audio data resets, which is the same as performing a soft reset.
14	DVDD	IN	Internal Core Digital Power Supply.
15	GND	IN/OUT	Ground.
16	IOVDD	IN	Digital Input/Output Power Supply.
-	Thermal Pad	-	Thermal Pad. The thermal/exposed pad must be grounded by soldering it to a grounded copper pad of equivalent size on the PCB.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Vmax_dvdd	DVDD to Ground		1.98	V
Vmax_iovdd	IOVDD to Ground		3.63	V
VDDio	Digital inputs	GND − 0.3	IOVDD + 0.3	V
T_A	Maximum Operating Ambient Temperature Range	−40	85	℃
T_J	Junction Temperature Range	−40	125	℃
T_S	Storage Temperature Range	−65	150	℃

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD (Electrostatic Discharge Protection)

Parameter		Condition	Value	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±7	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
Power Supplies					
DVDD	DVDD to Ground			1.98	V
IOVDD	IOVDD to Ground			3.63	V
VDD_IN	Digital Inputs	GND − 0.3		IOVDD + 0.3	V
Temperature Range					
T_A	Maximum Operating Ambient Temperature Range	−40.0		85.0	°C
T_J	Junction Temperature Range	−40.0		125.0	°C
T_S	Storage Temperature Range	−65.0		150.0	°C

Electrical Characteristics

All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Supply Voltage						
IOVDD	Supply for Input/Output (I/O) Circuitry, including pads and level shifters		1.7		3.63	V
DVDD	Supply for Digital Circuitry		1.7	1.8	1.98	V
IOVDD Pin Current						
IOVDD Pin Current	Operation State	IOVDD = 3.3 V		2.5		mA
	Operation State	IOVDD = 1.8 V		1.1		mA
	Shutdown Current	Power applied, frame and bit clocks applied, and then device placed into power-down state by software ctrl flow		1.2		μA
	Shutdown Current	Power applied, frame and bit clocks applied, and then device placed into power-down state by hardware ctrl way		4.0		μA
DVDD Pin Current						
DVDD Pin Current	Operation State	DVDD = 1.8 V, 8 channels, 48 kHz f_S		2.35		mA
	Operation State	DVDD = 1.8 V, 4 channels, 48 kHz f_S		2.26		mA
	Operation State	DVDD = 1.8 V, 8 channels, 16 kHz f_S		0.82		mA
	Operation State	DVDD = 1.8 V, 4 channels, 16 kHz f_S		0.79		mA
	Shutdown Current	Power-down mode using either method by software or hardware		3.0		μA
Digital Input						
VIH	High Level (VIH)		0.7 × IOVDD			V
VIL	Low Level (VIL)				0.3 × IOVDD	V
IIH	High Level (IIH)	Digital input pins with pull-down resistor			2.5	μA
IIL	Low Level (IIL) at 0 V	Digital input pins with pull-down resistor			1.0	μA
C_I	Guaranteed by Design			3.5		pF

Parameter		Conditions	Min	Typ	Max	Unit
Output Voltage						
VOH	High Level (VOH)	Source current when output is high (IOH) = 1 mA	0.85 × IOVDD			V
VOL	Low Level (VOL)	Source current when output is low (IOL) = 1 mA			0.1 × IOVDD	V
Output Pin Current						
Out Pin Current	IOVDD = 1.8 V	Drive strength setting 2.5 mA		0.7		mA
		Drive strength setting 5 mA		1.4		mA
		Drive strength setting 10 mA		2.8		mA
		Drive strength setting 15 mA		4.2		mA
	IOVDD = 3.3 V	Drive strength setting 2.5 mA		2.5		mA
		Drive strength setting 5 mA		5.0		mA
		Drive strength setting 10 mA		10.0		mA
		Drive strength setting 15 mA		15.0		mA

Audio Characteristics

DVDD = 1.70 V to 1.98 V, IOVDD = 1.70 V to 3.63 V, T_A = 25°C, and pins set to low drive setting, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Audio Performance						
DR	Dynamic Range	20 Hz to 20 kHz, −60 dB input, A-weighted filter (rms), relative to 0 dBFS output		126.0		dB
SNR	Signal-to-Noise-Ratio	A-weighted filter, fifth-order input, relative to 0 dBFS output		126.0		dB
Decimation Ratio		DC to 0.45 × output sampling rate	16×	64×	64×	
FR	Frequency Response		−0.003		0.14	dB
Stop Band				0.72 × f_S		
Stop Band Attenuation			72.7			dB
Group Delay		0.02 f_S input signal, 64× decimation	3.71	3.71	3.71	FSYNC cycles
Group Delay		0.02 f_S input signal, 32× decimation	3.82	3.82	3.82	FSYNC cycles
Group Delay		0.02 f_S input signal, 16× decimation	3.24	3.24	3.24	FSYNC cycles
Gain	PDM to PCM		−0.8	0.0	0.7	dB
Start-Up Time		After power-up reset and initialization code runs	63.0	64.0	64.0	FSYNC cycles
Bit Resolution		Internal and output	16.0	24.0	32.0	bit
Interchannel Phase	Phase calibration		0		255	PDM_CLK cycle
High-Pass Filter −3dB Point				3.8		Hz
Clock						
FS	Sync Clock		8.0	48.0	192.0	KHz
BCLK	Bit Clock		0.512	12.288	24.576	MHz
PDM_CLK			0.512	3.072	6.144	MHz

AC Timing Requirements

Specifications are subject to change without notice.

Table 2. I²C Timing Specification

Symbol	Parameter Description	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0		1000	kHz
t_{SCLH}	SCL pulse width high	0.26			us
t_{SCLL}	SCL pulse width low	0.5			us
t_{SCS}	Start and repeated start condition setup time	0.26			us
t_{SCH}	Start condition hold time	0.26			us
t_{DS}	Data setup time	50			ns
t_{DH}	Data hold time	0		0.45	us
t_{SCLR}	SCL rise time			120	ns
t_{SCLF}	SCL hold time			120	ns
t_{SDR}	SDA Rise Time			120	ns
t_{SDF}	SDA fall time			120	ns
t_{BFT}	Bus-Free time between stop and start	0.5			us
t_{SUSTO}	Stop condition setup time	0.26			us

I2C Timing

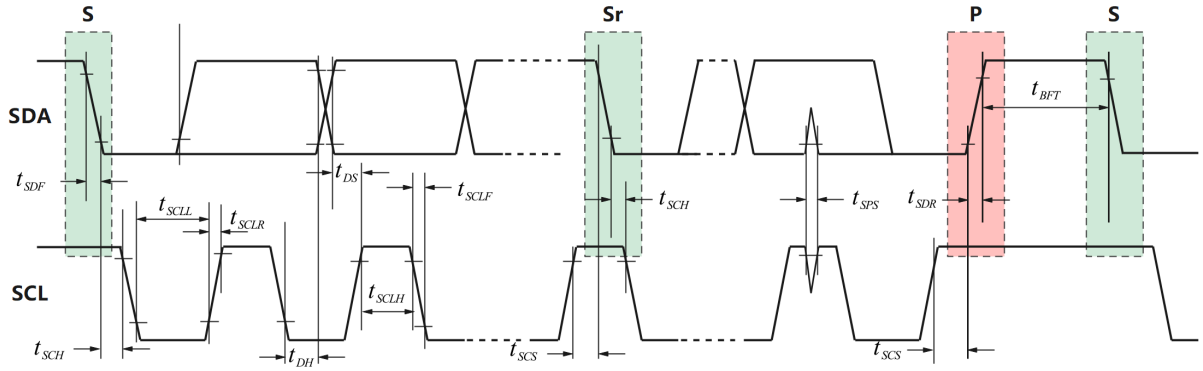


Figure 1. I2C Timing

Table 3. PDM Microphone Input Timing Specification

Symbol	Parameter	Min	Typ	Max	Unit
t_{RISS}	DATA Input Setup before PDMCLK	9.0			ns
t_{RIHS}	DATA Input Hold after PDMCLK	3.0			ns

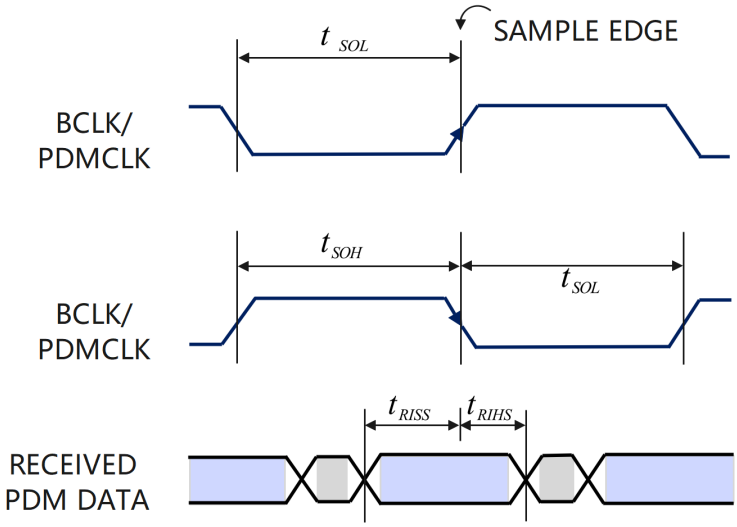


Figure 2. PDM Timing

Table 4. I2S/TDM Timing Specification

Symbol	Parameters Description	Min	Max	Unit
I2S Slave Timing Requirements				
f_{FSYNC}	FSYNC/LRCLK frequency		192K	Hz
t_{FSYNC}	FSYNC/LRCLK period	5.21		ns
f_{BCLK}	BCLK frequency, sample rate from 4KHz to 192KHz		24.576M	Hz
t_{BCLK}	BCLK period	40.7		ns
t_{BIL}	BCLK low pulse width, at BCLK=24.576MHz	18		ns
t_{BIH}	BCLK high pulse width, at BCLK=24.576MHz	18		ns
t_{LIS}	FSYNC setup to BCLK input rising edge, at FSYNC=192KHz	10		ns
t_{LIH}	FSYNC hold from BCLK input rising edge, at FSYNC=192KHz	10		ns
t_{SOD}	SDATA out Delay After BCLK falling Edge, 25pF load over all level of IOVDD, all temperature ranges and skews, with default drive strength =10mASDATA delay from BCLK output falling edge, 25 pf load over entire range of IOVDD, all temperatures and skews, default drive strength of 10 mA		15.28	ns
	IOVDD = 3.3 V ± 10%, drive strength set to 2.5 mA, with 25 pF load		14.62	ns
	IOVDD = 3.3 V ± 10%, drive strength set to 5 mA, with 25 pF load		12.25	ns
	IOVDD = 3.3 V ± 10%, drive strength set to 10 mA, with 25 pF load		11.21	ns
	IOVDD = 3.3 V ± 10%, drive strength set to 15 mA, with 25 pF load		11.01	ns
	IOVDD = 1.8 V ± 10%, drive strength set to 2.5 mA, with 25 pF load		24.06	ns
	IOVDD = 1.8 V ± 10%, drive strength set to 5 mA, with 25 pF load		18.98	ns
	IOVDD = 1.8 V ± 10%, drive strength set to 10 mA, with 25 pF load		15.28	ns
	IOVDD = 1.8 V ± 10%, drive strength set to 15 mA, with 25 pF load		14.73	ns

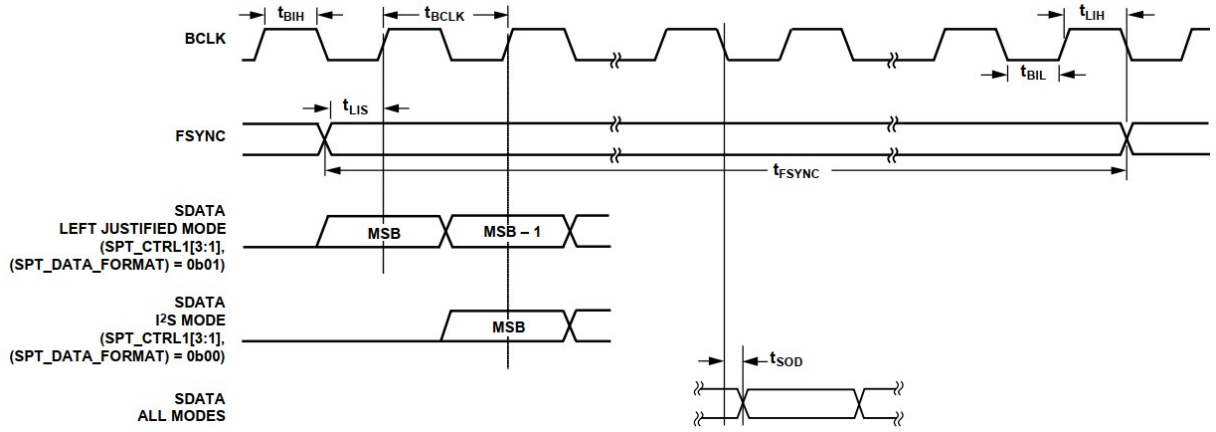


Figure 3. I2S/TDM Slave Timing

Table 5. Power-up Sequence Timing

Parameter		Min	Max	Unit
t_{POR}	Both power supplies can be applied at the same time or the IOVDD must be applied first, then the DVDD at any point after	0		ms

(1) The test data is based on bench tests and design simulation.

Typical Audio Characteristic Figures

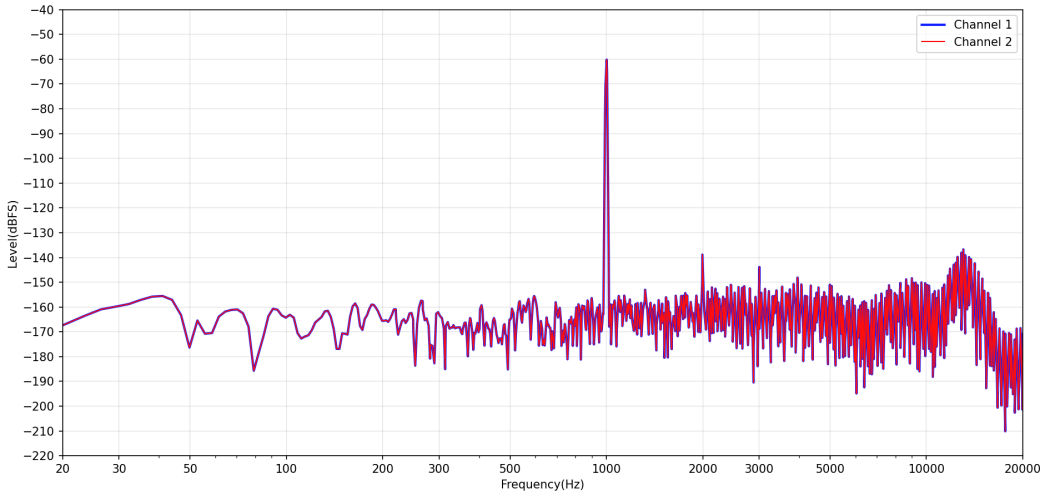


Figure 4. FFT@48KSample Rate

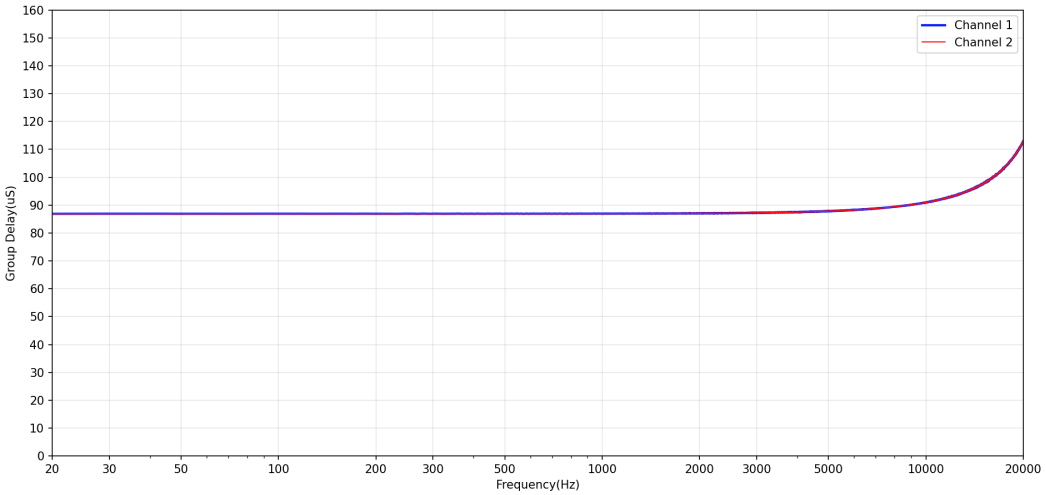


Figure 5. Group Delay@48K Sample Rate

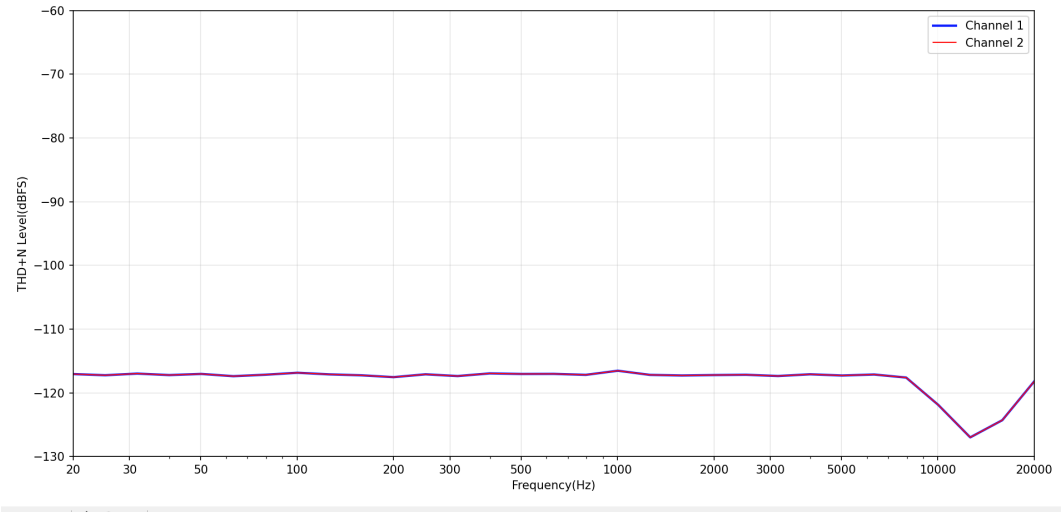


Figure 6. THD+N vs. Frequency

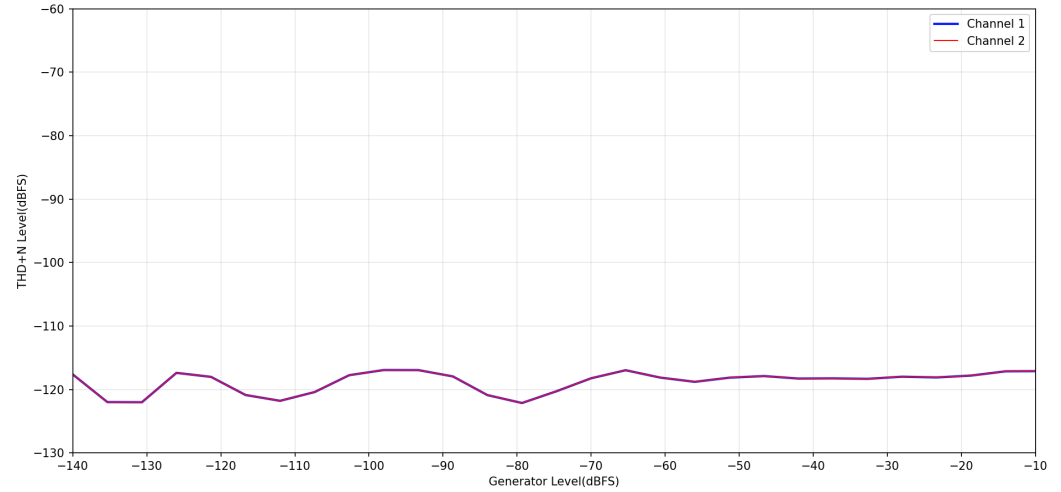


Figure 7. THD+N vs. Level

Detailed Description

Overview

The TPDA7008 provides up to 8 channels of decimation from a 1-bit PDM source to 24-bit PCM data. The down sampling ratio can be set at 64 ×, 32 ×, and 16 ×(f_S), with f_S being the PCM output sampling rate. Note that all PDM channels decimate at the same ratio. The 24-bit down sampled PCM audio output via standard I2S or TDM format.

PDM Interface

The input sources for the TPDA7008 can be any device that has PDM output interface, such as a digital microphone. The output pins of these microphones can connect directly to the input pins of the TPDA7008. The TPDA7008 has two separate PDM_CLKx outputs that are replications of the same signal to allow easier drive of multiple sources. Each PDM_CLKx can be disabled individually. The PDM_DATx input pins are connected to the data output of the PDM sources. Internally, there are 8 channels, Channel 0 to Channel 7. The mapping of PDM_DATx inputs to the internal channels is detailed in the following Table 6:

Table 6. PDM Data Channel Mapping

Input Pin	PDM CLK Edge	Internal Channel
PDM_DAT0	Falling	0
PDM_DAT0	Rising	1
PDM_DAT1	Falling	2
PDM_DAT1	Rising	3
PDM_DAT2	Falling	4
PDM_DAT2	Rising	5
PDM_DAT3	Falling	6
PDM_DAT3	Rising	7

Power-up Sequency and Initialization

The TPDA7008 requires two power supplies to function: the IOVDD and the DVDD. Both power supplies can be applied at the same time. If the power supplies are applied at different times, the IOVDD must be applied first and then the DVDD at any point after. There are no timing restrictions.

After the power supplies have stabilized, the device initializes and is ready to accept incoming I2S clocks or I2C commands based on the mode of operation.

After the initialization is complete, and I2S clocks are applied, it takes 16 full frame sync cycles to begin sending out PDM clocks.When the PDM clocks start, and after another 48 frame sync cycles, the PDM data shows up on the SDATA pin.

The TPDA7008 can operate in two modes of operation: hardware standalone mode or software I2C control mode.

Clocking

After power is applied and the power-up initialization is complete, the device is ready to accept TDM or I2S clocks. At that point, it takes 16 full-frame sync cycles for the device to fully initialize and start sending PDM clocks. If during normal operation the bit clock is removed, the PDM_CLKx outputs stop immediately, and the TPDA7008 enters a lower power state

automatically. See the Power-down State section for more details. When the clocks resume, the TPDA7008 relocks to the bit clock and adjusts the PDM_CLKx outputs accordingly. The length of time before the PDM clock outputs resume is 4 frames ± 1 frame to lock to the incoming signal. If the format of the clock signal changes, the TPDA7008 detects this change at the end of the frame and stops the PDM clock outputs. Then, the device reconfigures and resumes sending PDM clocks with no user intervention. Again, the length of time before the PDM clock outputs resume usually takes 4 frames ±1 frame to lock to the incoming signal.

The TPDA7008 requires a BCLK rate that is a minimum of 64× the frame sync (FSYNC) sample rate. BCLK rates of 128×, 256×, and 512×, and the FSYNC rate are also supported. The TPDA7008 automatically detects the ratio between BCLK and FSYNC and generates a PDM clock output at 64 × the FSYNC rate by default. If lower decimation ratios are selected in Register 0x05, DEC_RATIO_CLK_MAP, the PDM output clock rate corresponds with the DEC_RATIO bits setting. The minimum sampling rate is 4 kHz, and the maximum sampling rate is 192 kHz. The PDM clock range is 256 kHz to 6.144 MHz. Internally, all processing is done at the PDM_CLK rate.

The two PDM clock outputs, PDM_CLK0 and PDM_CLK1, are separate buffered outputs of the same clock. However, the incoming PDM data is clocked in using the signal present at the actual clock pin and not the internal clock going out to the pin. The reason for this is to allow the clock rise time to be slowed by the external capacitance in a similar manner to the PDM data signal. It is recommended to associate the incoming PDM data with the clock output that is actually connected to the PDM microphone. The DEC_RATIO_CLK_MAP register, Register 0x05, is used to assign one of the two clocks to each PDM data input.

Power-down State

The TPDA7008 can be placed into a power-down state by using one of two methods available. The preferred method is by using register writes to place the device into the lowest possible power-down state. However, when the TPDA7008 operates in standalone mode, use the second method, which uses the enable pin (EN).

With a system controller, when entering the low power state, disable the PDM clocks and disable the channel outputs by writing a zero to Register 0x04. Then, the frame and bit clocks can be removed (stopped) to place the device in the power-down state. Allow enough time for the I2C write to complete before stopping the clocks. A minimum of one full frame after the I2C write completes is enough wait time. It is not necessary to lower the EN pin, it does not lower the power draw any further. See Table 7 for more details.

Table 7. Entering the Power-Down State Using Register Writes

Step	Action
1	Write a zero into Register 0x04
2	Wait at least one frame period
3	Stop the frame and bit clocks

When the TPDA7008 is in standalone mode, the device can be placed into the power-down state by applying a low signal to the EN pin and then waiting a minimum of one full frame to place the device into the power-down state. See Table 8 for more details.

Table 8. Entering the Power-Down State when Operating in Standalone Mode

Step	Action
1	Apply a low voltage to the EN pin
2	Wait at least one frame period
3	Stop the frame and bit clocks

To come out of the power-down mode, the order for restarting the clocks vs. enabling the device does not matter. Enabling the device refers to either raising the EN pin or enabling the device by writing to Register 0x04.

Hardware Standalone Mode

Because all channels default to enable and output, the device can be used with the default control settings without I2C and with any setting of the ADDR/CONFIG pin, except for hardware mode. If the ADDR/CONFIG pin is left open, the device is in standalone hardware mode and I2C communications are not possible. See Table 12 for details on the ADDR/CONFIG pin settings. In standalone hardware mode, the settings of the I2C SCL pin and SDA pin can select different functionality by changing the state of some registers from their default. See Table 9 for details of the differences from the default settings.

Table 9. Hardware/Standalone Mode Settings: Changes from Default Setting

SCL Pin	SDA Pin	Operation Settings	PDM Clock Settings: Enabled	Channel Enables	Drive Strength
HIGH	HIGH	4-channel	PDM CLK1 disabled	CH4/5, CH6/7 disabled	Default setting: 10
HIGH	LOW	8-channel high drive	PDM CLK0/1 enabled	All channels enabled	SDATA_DS=11, PDM_CLK0_DS=11, PDM_CLK0_DS=11
LOW	HIGH	6-channel	PDM CLK0/1 enabled	CH6/7 disabled	Default setting: 10
LOW	LOW	6-channel high drive	PDM CLK0/1 enabled	CH6/7 disabled	SDATA_DS=11, PDM_CLK0_DS=11, PDM_CLK0_DS=11

To achieve the lowest power in standalone hardware mode operation when a BCLK is present, the EN pin is still functional and can be pulled low, placing the device into a low power mode. The EN pin also performs a soft reset but does not reset any of the register settings. Stopping the bit clock also places the device into a low-power state. See the Clocking section for more details.

Serial Audio Output Interface

The TPDA7008 supports I2S and TDM serial output formats. Up to 16 TDM slots can be used. TDM slot widths of 16 bits, 24 bits, and 32 bits are supported. Any internal channel can be routed to any output slot via the SPT_Cx_SLOT bits. By default, each channel is routed to the same number slot. For example, Channel 1 goes to Slot 1 and Channel 6 goes to Slot 6. Each channel can be set to drive during its set slot or not drive (tristate high impedance mode) via its respective SPT_Cx_DRV bit. I2S mode or TDM mode selection is via the SPT_SAI_MODE bit (Bit 0) in the SPT_ CTRL1 register. The SDATA pin is in tristate high impedance mode, except when the port is driving serial data by default. It is possible for two or more channels to be set to the same TDM slot. In that case, the lowest channel number wins and drives its data into the slot. The data of the other channel never appears anywhere. There is no cross-checking of register settings to prevent the user from doing this, but the device is not damaged, only the data is missing from the output.

The SPT_CTRL1 register, SPT_SAI_MODE bit (Bit 0) sets the serial port audio interface mode. The two modes are stereo and TDM. The primary difference between these two modes is the format of the frame sync clock that is expected and the polarity of the active edge of the clock.

With the SPT_SAI_MODE bit set to 0, and the SPT_LRCLK_POL bit (Bit 1, Register SPT_CTRL2) set to 0, the serial port is in stereo mode with the clock polarity set to normal. In this mode, only two channels of data are expected to be sent. The frame starts with the falling edge of the frame sync, and the expected duty cycle is 50% high and 50% low. Channel 0 sends out its data when the clock is low, and as soon as the frame sync goes high, the data from Channel 0 is stopped, and Channel 1 begins sending. Both edges of the frame sync clock are used.

With the SPT_SAI_MODE bit set to 1, and the SPT_LRCLK_ POL bit set to 0, the serial port is in TDM mode with the clock polarity set to normal. In this mode, there can be as few as a single channel transmitted or as many as 8 channels spread out across 16 data slots of a TDM-16 format.

The TPDA7008 can support four different bit clock rates of 64×, 128×, 256×, or 512× the output sampling rate. These bit clock rates are combined with the three different TDM slot sizes of 16-bit or 32-bit slots, selected in the SPT_CTRL1 register, Bits[5:4] (SPT_SLOT_WIDTH), to result in 12 combinations of TDM formats that are supported. See Table 10.

Table 10. Number of Slots in Supported TDM Bit Clock Ratio vs. Slot Width Setting

	Slot Width		
Bit Clock Ratio	**16-Bit Slot**	**24-Bit Slot**	**32-Bit Slot**
64×f_S	4	2	2
128×f_S	8	4	4
256×f_S	16	8	8
512×f_S	32	16	16

Note that as soon as the next frame sync edge is detected, the TPDA7008 restarts from Slot 0, and only TDM-16 or less is supported for placing data into a TDM slot. Data cannot be placed into slots above 16. The TPDA7008 can be configured to tristate all unused TDM slots.

In TDM mode, the frame sync is expected to be a positive-going pulse that is at least one bit clock period wide. The falling edge is not important and is not looked at as long as it is low long enough to meet the timing specification read as a low before going back high. The frame starts with the rising edge of this pulse. The data is clocked out according to the slot width and data format specified in the SPT_CTRL1 register, Register 0x07. The TPDA7008 continues to send data until all active channels are sent and then the device waits for the next frame sync clock edge to start sending the next set of frame samples. If TDM-16 is used and the TPDA7008 is set to output Channel 0 to Channel 7 into Slot 0 to Slot 7, the TPDA7008 can tristate for the remainder of the frame, allowing another TPDA7008 to output its 8 channels onto Slot 8 to Slot 15. These slots do not have to be consecutive. The two devices may interleave their respective data if properly set up to do this. The serial port can be set up to only drive when there is data to drive into a data slot. If one or more of the eight channels is not used, the channel can be assigned to drive a slot or tristate during that data slot in the TDM data stream, which is done using Bit 0 in the SPT_Cx registers.

The SPT_LRCLK_POL bit, left/right clock polarity, can be set to 1 and the bit inverts the expected frame clock. In stereo mode with the SPT_LRCLK_POL bit set to 1, Channel 0 is sent out when the frame sync is high so the start of the frame is a low-to-high transition. In TDM mode, with the SPT_LRCLK_POL bit set to 1, the expected frame sync pulse is negative-going so that the frame starts with the high-to-low transition.

The SPT_DATA_FORMAT bits (Bits[3:1]) in the SPT_CTRL1 register allow for the justification of the data within the 32-bit data slot. The left-justified mode, delayed by one bit clock period, and the right-justified modes for 24-bit and 16-bit data word sizes are all supported.

I2C Interface

The TPDA7008 supports a 2-wire serial bus (I2C-compatible) shared across multiple peripherals. Two signals, serial data (SDA) and serial clock (SCL), carry information between the TPDA7008 and the system I2C master controller. The TPDA7008 is always a slave on the bus and cannot initiate a data transfer. Each slave device is identified by a unique address. The address byte format is shown in Table 11 with the LSBs of the address determined by the state of the ADDR/CONFIG pin (see Table 12). The address resides in the first 7 bits of the I2C write. The LSB of this byte sets either a read or write operation. Logic Level 1 corresponds to a read operation, and Logic Level 0 corresponds to a write operation.

Table 11. I2C Device Address Byte Format

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	1	0	1	bit2	bit1	R/W

Table 12. ADDR/CONFIG Pin Options By Hardware Connection

I2C Address Bit2	I2C Address Bit1	ADDR/CONFIG Pin Configuration
1	1	Tie to IOVDD
0	0	Tie to GND
1	0	Pull high to IOVDD via a 47Kohm resistor
0	1	Pull low to GND via a 47Kohm resistor
Hardware Mode	Hardware Mode	Open

Output Pin Drive Strength

All output pins have configurable output drive strength that can be set via their respective control registers. Drive strengths of 2.5 mA, 5 mA, 10 mA, and 15 mA at 3.3 V IOVDD are possible. The serial data output pin functions in slave mode at all valid sample rates, provided that the external circuit design provides sufficient electrical signal integrity. When operating at IOVDD = 1.8 V nominal, take care to achieve sufficient timing margins at BCLK frequencies over 12.288 MHz. The capacitance of the bit clock and SDATA signal lines on the PCB, along with the length of the trace, enters into the calculation of this timing margin.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPDA7008 is generally used for the audio system with insufficient PDM interfaces, and can not connect enough PDM sources. In addition, to facilitate the PCB layout, the TPDA7008 uses digital micphones instead of analog micphones associated with ADCs in the scheme for the multiple micphones algorithm.

Typical Applications

Typical Application 1

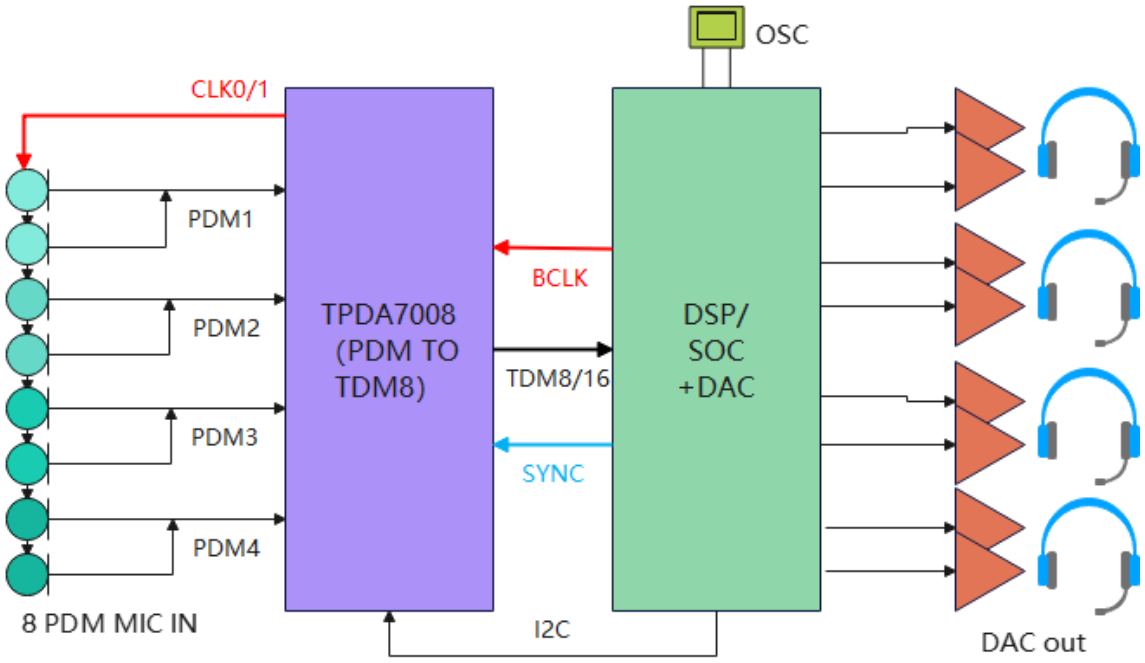


Figure 8. Multi Mic-array for DSP/SOC, which lacks PDM input pins

For some DSP or SOC, which has only 1 or 2 PDM inputs, while its application requires to support more than 4, or even 8 MIC inputs. Using the TPDA7008 can save the data and clock pin for this kind of DSP/SOC, even with 2 pcs of the TPDA7008, we can support 16 PDM microphones input, while using just a single data lane of TDM16 mode. Refer to the above figure to see more.

Typical Application 2

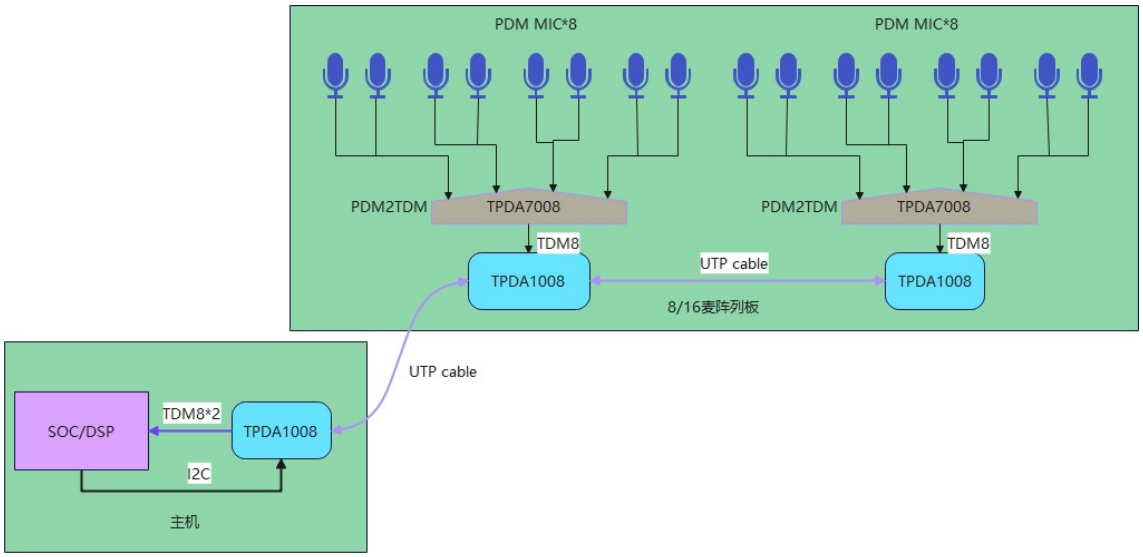


Figure 9. Distributed Mic-array System Implemented with TPDA7008 + ASN Network

For a distributed recording and playback application in a conference system/education system, the TPDA7008 provides one effective solution for multi-channel voice acquisition up to 8/16 PDM microphones, it uses a single data lane TDM to the consequent receiver, like ASN/A2B/HSMT, etc. The above figure shows a conference system block diagram.

Register Table

Offset	Name	Bits	Settings	Description	Reset	Type
0x00	VENDOR_ID	[7:0]	Not applicable	Vendor ID Register.	0xEA	RO
0x01	DEVICE_ID1	[7:0]	Not applicable	Device ID 1 Register.	0x70	RO
0x02	DEVICE_ID2	[7:0]	Not applicable	Device ID 2 Register.	0x08	RO
0x03	ANALOG_STATUS	[7:0]	Not applicable	Analog Status Register.	0x00	RO
0x04	ENABLES	[7:6]		Reserved	0x3F	R/W
		5	- 0 1	PDM Clock 1 Enable Diabled Enabled		
		4	- 0 1	PDM Clock 0 Enable Diabled Enabled		
		3	- 0 1	PDM Data 3 Enable Diabled Enabled		
		2	- 0 1	PDM Data 2 Enable Diabled Enabled		

Offset	Name	Bits	Settings	Description	Reset	Type
		1	-	PDM Data 1 Enable
			0	Diabled
			1	Enabled
		0	-	PDM Data 0 Enable
			0	Diabled
			1	Enabled
0x06	HPF_CONTROL	[7:1]		Reserved	0xD0	R/W
		0	-	High-pass Filter Enable
			0	Diabled
			1	Enabled
0x07	SPT_CTRL1	7		Reserved	0x41	R/W
		6	-	Tristate Enable for Unassigned Slots
			0	Diabled
			1	Enabled
		[5:4]	-	Serial Port Width
			00	32BIT
			01	16BIT
			10	24BIT
		[3:1]	-	Selects serial port data delay from left/right/frame
			-	clock transition
			001	Left justified, delay by 0
			000	I2S mode, delay by 1
			010	Delay by 8
			011	Delay by 12
			100	Delay by 16
		0	-	Serial Audio Interface
			0	Stereo
			1	TDM
0x08	SPT_CTRL2	[7:2]		Reserved	0x00	R/W
		1	-	Selects serial port left/right frame clock polarity
			0	Normal
			1	Inverted
		0	-	Selects serial port bit clock polarity
			0	Capture on rising edge
			1	Capture on falling edge
0x09	SPT_C0	[7:4]	-	Serial Port Channel 0 Slot Selection	0x01	R/W
			0000	Slot 0
			0001	Slot 1
			0010	Slot 2
			0011	Slot 3
			0100	Slot 4
			0101	Slot 5
			0110	Slot 6

Offset	Name	Bits	Settings	Description	Reset	Type
			0111	Slot 7		
			1000	Slot 8		
			1001	Slot 9		
			1010	Slot 10		
			1011	Slot 11		
			1100	Slot 12		
			1101	Slot 13		
			1110	Slot 14		
			1111	Slot 15		
		[3:1]		Reserved		
		0	-	Serial Port Channel 0 Drive Select		
			0	Not driven		
			1	Driving selected slot		
0x0A	SPT_C1	[7:4]	-	Serial Port Channel 1 Slot Selection	0x11	R/W
			0000	Slot 0		
			0001	Slot 1		
			0010	Slot 2		
			0011	Slot 3		
			0100	Slot 4		
			0101	Slot 5		
			0110	Slot 6		
			0111	Slot 7		
			1000	Slot 8		
			1001	Slot 9		
			1010	Slot 10		
			1011	Slot 11		
			1100	Slot 12		
			1101	Slot 13		
			1110	Slot 14		
			1111	Slot 15		
		[3:1]		Reserved		
		0	-	Serial Port Channel 1 Drive Select		
			0	Not driven		
			1	Driving selected slot		
0x0B	SPT_C2		-	Serial Port Channel 2 Slot Selection	0x21	R/W
			0000	Slot 0		
			0001	Slot 1		
			0010	Slot 2		
			0011	Slot 3		
		[7:4]	0100	Slot 4		
			0101	Slot 5		
			0110	Slot 6		
			0111	Slot 7		
			1000	Slot 8		
			1001	Slot 9		

Offset	Name	Bits	Settings	Description	Reset	Type
			1010	Slot 10		
			1011	Slot 11		
			1100	Slot 12		
			1101	Slot 13		
			1110	Slot 14		
			1111	Slot 15		
		[3:1]		Reserved		
			-	Serial Port Channel 2 Drive Select		
		0	0	Not driven		
			1	Driving selected slot		
0x0C	SPT_C3	[7:4]	-	Serial Port Channel 3 Slot Selection	0x31	R/W
			0000	Slot 0		
			0001	Slot 1		
			0010	Slot 2		
			0011	Slot 3		
			0100	Slot 4		
			0101	Slot 5		
			0110	Slot 6		
			0111	Slot 7		
			1000	Slot 8		
			1001	Slot 9		
			1010	Slot 10		
			1011	Slot 11		
			1100	Slot 12		
			1101	Slot 13		
			1110	Slot 14		
			1111	Slot 15		
		[3:1]		Reserved		
		0	-	Serial Port Channel 3 Drive Select		
			0	Not driven		
			1	Driving selected slot		
0x0D	SPT_C4	[7:4]	-	Serial Port Channel 4 Slot Selection	0x41	R/W
			0000	Slot 0		
			0001	Slot 1		
			0010	Slot 2		
			0011	Slot 3		
			0100	Slot 4		
			0101	Slot 5		
			0110	Slot 6		
			0111	Slot 7		
			1000	Slot 8		
			1001	Slot 9		
			1010	Slot 10		
			1011	Slot 11		
			1100	Slot 12		

Offset	Name	Bits	Settings	Description	Reset	Type
			1101	Slot 13		
			1110	Slot 14		
			1111	Slot 15		
		[3:1]		Reserved		
		0	-	Serial Port Channel 4 Drive Select		
			0	Not driven		
			1	Driving selected slot		
0x0E	SPT_C5	[7:4]	-	Serial Port Channel 5 Slot Selection	0x51	R/W
			0000	Slot 0		
			0001	Slot 1		
			0010	Slot 2		
			0011	Slot 3		
			0100	Slot 4		
			0101	Slot 5		
			0110	Slot 6		
			0111	Slot 7		
			1000	Slot 8		
			1001	Slot 9		
			1010	Slot 10		
			1011	Slot 11		
			1100	Slot 12		
			1101	Slot 13		
			1110	Slot 14		
			1111	Slot 15		
		[3:1]		Reserved		
		0	-	Serial Port Channel 5 Drive Select		
			0	Not driven		
			1	Driving selected slot		
0x0F	SPT_C6	[7:4]	-	Serial Port Channel 6 Slot Selection	0x61	R/W
			0000	Slot 0		
			0001	Slot 1		
			0010	Slot 2		
			0011	Slot 3		
			0100	Slot 4		
			0101	Slot 5		
			0110	Slot 6		
			0111	Slot 7		
			1000	Slot 8		
			1001	Slot 9		
			1010	Slot 10		
			1011	Slot 11		
			1100	Slot 12		
			1101	Slot 13		
			1110	Slot 14		
			1111	Slot 15		

Offset	Name	Bits	Settings	Description	Reset	Type
		[3:1]		Reserved		
		0	-	Serial Port Channel 6 Drive Select		
			0	Not driven		
			1	Driving selected slot		
0x10	SPT_C7	[7:4]	-	Serial Port Channel 7 Slot Selection	0x71	R/W
			0000	Slot 0		
			0001	Slot 1		
			0010	Slot 2		
			0011	Slot 3		
			0100	Slot 4		
			0101	Slot 5		
			0110	Slot 6		
			0111	Slot 7		
			1000	Slot 8		
			1001	Slot 9		
			1010	Slot 10		
			1011	Slot 11		
			1100	Slot 12		
			1101	Slot 13		
			1110	Slot 14		
			1111	Slot 15		
		[3:1]		Reserved		
		0	-	Serial Port Channel 7 Drive Select		
			0	Not driven		
			1	Driving selected slot		
0x11	DRIVE_STRENGTH	[7:6]		Reserved	0x2A	R/W
		[5:4]	-	PDM_CLK1 Output Pad Drive Strength Control		
			00	2.5 mA/3.3 V		
			01	5 mA/3.3 V		
			10	10 mA/3.3 V		
			11	15 mA/3.3 V		
		[3:2]	-	PDM_CLK0 Output Pad Drive Strength Control		
			00	2.5 mA/3.3 V		
			01	5 mA/3.3 V		
			10	10 mA/3.3 V		
			11	15 mA/3.3 V		
		[1:0]	-	SDATA Output Pad Drive Strength Control		
			00	2.5 mA/3.3 V		
			01	5 mA/3.3 V		
			10	10 mA/3.3 V		
			11	15 mA/3.3 V		
0x12	RESETS	[7:2]		Reserved	0x00	R/W
		1	-	Software Reset Including Register Settings		
			0	Running		

Offset	Name	Bits	Settings	Description	Reset	Type
			1	In reset		
		0	-	Software Reset Not Including Register Settings		
			0	Running		
			1	In reset		
0x13	PDM_0_GCAL	[7:4]	-	PDM0 Slot0 Gain Calibration(dB)	0x00	R/W
			0000	0		
			0001	-0.068		
			0010	-0.135		
			0011	-0.202		
			0100	-0.268		
			0101	-0.333		
			0110	-0.398		
			0111	-0.463		
			1000	0		
			1001	0.068		
			1010	0.136		
			1011	0.206		
			1100	0.275		
			1101	0.346		
			1110	0.417		
			1111	0.486		
		[3:0]	-	PDM0 Slot1 Gain Calibration(dB)		
			0000	0		
			0001	-0.068		
			0010	-0.135		
			0011	-0.202		
			0100	-0.268		
			0101	-0.333		
			0110	-0.398		
			0111	-0.463		
			1000	0		
			1001	0.068		
			1010	0.136		
			1011	0.206		
			1100	0.275		
			1101	0.346		
			1110	0.417		
			1111	0.486		
0x14	PDM_1_GCAL	[7:4]	-	PDM1 Slot0 Gain Calibration(dB)	0x00	R/W
			0000	0		
			0001	-0.068		
			0010	-0.135		
			0011	-0.202		
			0100	-0.268		
			0101	-0.333		

Offset	Name	Bits	Settings	Description	Reset	Type
			0110	-0.398		
			0111	-0.463		
			1000	0		
			1001	0.068		
			1010	0.136		
			1011	0.206		
			1100	0.275		
			1101	0.346		
			1110	0.417		
			1111	0.486		
		[3:0]	-	PDM1 Slot1 Gain Calibration(dB)		
			0000	0		
			0001	-0.068		
			0010	-0.135		
			0011	-0.202		
			0100	-0.268		
			0101	-0.333		
			0110	-0.398		
			0111	-0.463		
			1000	0		
			1001	0.068		
			1010	0.136		
			1011	0.206		
			1100	0.275		
			1101	0.346		
			1110	0.417		
			1111	0.486		
0x15	PDM_2_GCAL	[7:4]	-	PDM2 Slot0 Gain Calibration(dB)	0x00	R/W
			0000	0		
			0001	-0.068		
			0010	-0.135		
			0011	-0.202		
			0100	-0.268		
			0101	-0.333		
			0110	-0.398		
			0111	-0.463		
			1000	0		
			1001	0.068		
			1010	0.136		
			1011	0.206		
			1100	0.275		
			1101	0.346		
			1110	0.417		
			1111	0.486		
		[3:0]	-	PDM2 Slot1 Gain Calibration(dB)		

Offset	Name	Bits	Settings	Description	Reset	Type
			0000	0		
			0001	-0.068		
			0010	-0.135		
			0011	-0.202		
			0100	-0.268		
			0101	-0.333		
			0110	-0.398		
			0111	-0.463		
			1000	0		
			1001	0.068		
			1010	0.136		
			1011	0.206		
			1100	0.275		
			1101	0.346		
			1110	0.417		
			1111	0.486		
0x16	PDM_3_GCAL	[7:4]	-	PDM3 Slot0 Gain Calibration(dB)	0x00	R/W
			0000	0		
			0001	-0.068		
			0010	-0.135		
			0011	-0.202		
			0100	-0.268		
			0101	-0.333		
			0110	-0.398		
			0111	-0.463		
			1000	0		
			1001	0.068		
			1010	0.136		
			1011	0.206		
			1100	0.275		
			1101	0.346		
			1110	0.417		
			1111	0.486		
		[3:0]	-	PDM3 Slot1 Gain Calibration(dB)		
			0000	0		
			0001	-0.068		
			0010	-0.135		
			0011	-0.202		
			0100	-0.268		
			0101	-0.333		
			0110	-0.398		
			0111	-0.463		
			1000	0		
			1001	0.068		
			1010	0.136		
			1011	0.206		

Offset	Name	Bits	Settings	Description	Reset	Type
			1100 1101 1110 1111	0.275 0.346 0.417 0.486		
0x17	CHANNEL_DELAY_CODE_0	[7:0]		PDM0 Slot0 Phase Delay Code from 0~255 Cycles, Cycles Step is PDMCLK	0x00	R/W
0x18	CHANNEL_DELAY_CODE_1	[7:0]		PDM0 Slot1 Phase Delay Code from 0~255 Cycles, Cycles Step is PDMCLK	0x00	R/W
0x19	CHANNEL_DELAY_CODE_2	[7:0]		PDM1 Slot0 Phase Delay Code from 0~255 Cycles, Cycles Step is PDMCLK	0x00	R/W
0x1A	CHANNEL_DELAY_CODE_3	[7:0]		PDM1 Slot1 Phase Delay Code from 0~255 Cycles, Cycles Step is PDMCLK	0x00	R/W
0x1B	CHANNEL_DELAY_CODE_4	[7:0]		PDM2 Slot0 Phase Delay Code from 0~255 Cycles, Cycles Step is PDMCLK	0x00	R/W
0x1C	CHANNEL_DELAY_CODE_5	[7:0]		PDM2 Slot1 Phase Delay Code from 0~255 Cycles, Cycles Step is PDMCLK	0x00	R/W
0x1D	CHANNEL_DELAY_CODE_6	[7:0]		PDM3 Slot0 Phase Delay Code from 0~255 Cycles, Cycles Step is PDMCLK	0x00	R/W
0x1E	CHANNEL_DELAY_CODE_7	[7:0]		PDM3 Slot1 Phase Delay Code from 0~255 Cycles, Cycles Step is PDMCLK	0x00	R/W

Reference Schematic

PDM Digital Microphone Circuits

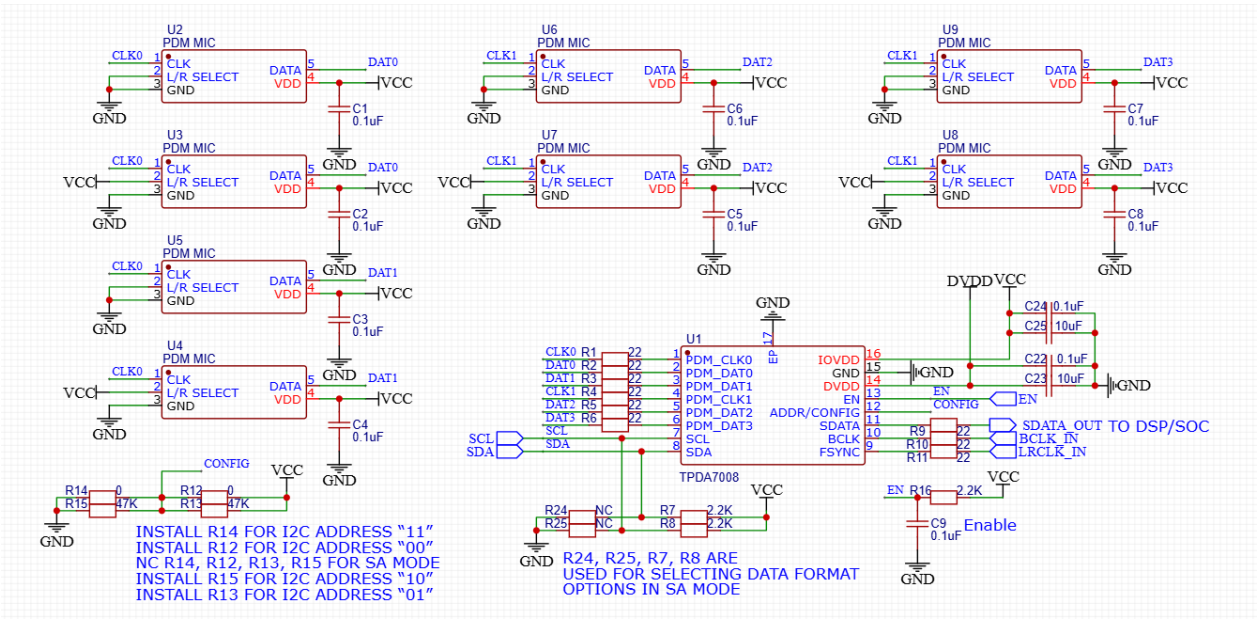
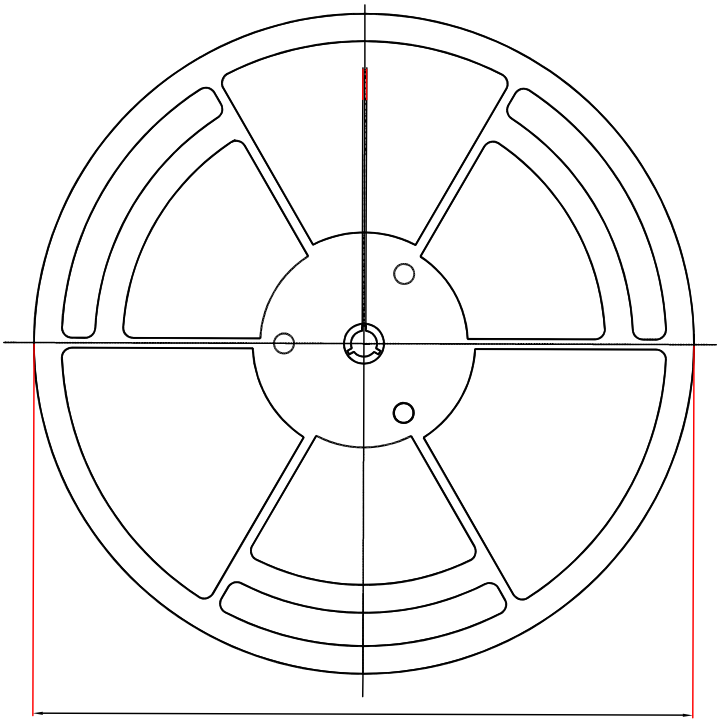
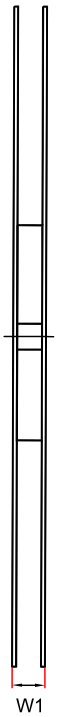
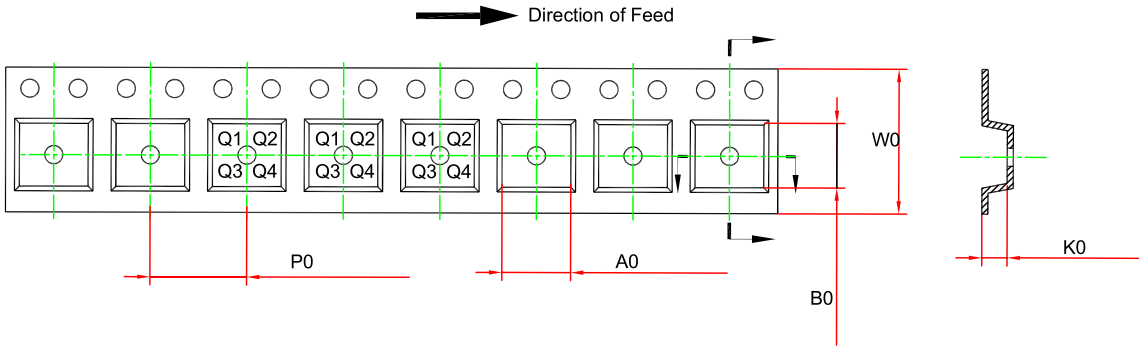


Figure 10. 8-Digital Microphones Connections to the TPDA7008

Tape and Reel Information





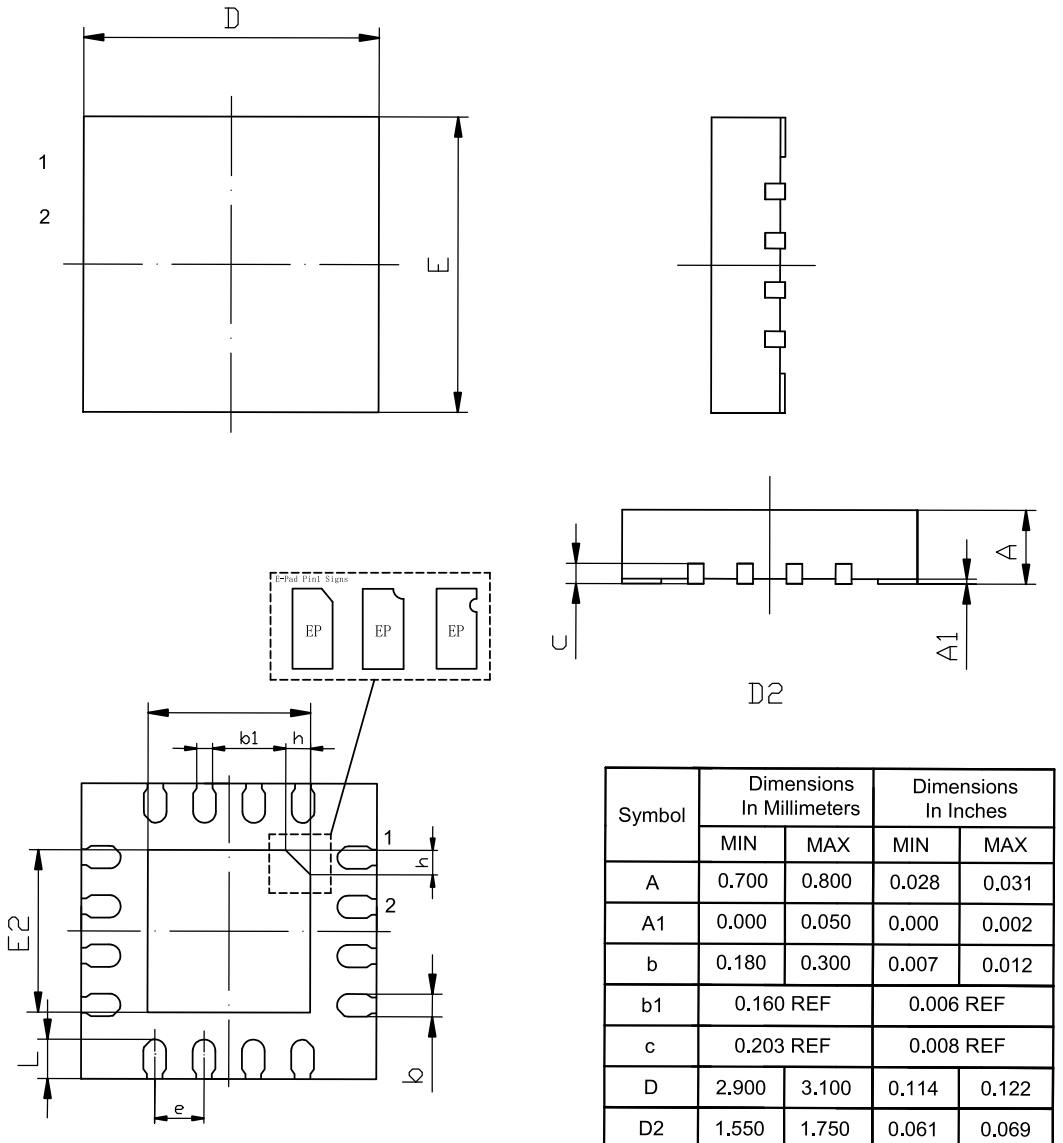


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPDA7008-QFNR	QFN3X3-16	330	17.6	3.3	3.3	1.1	8	12	Q1
TPDA7004-QFNR	QFN3X3-16	330	17.6	3.3	3.3	1.1	8	12	Q1

Package Outline Dimensions

QFN3X3-16

Package Outline Dimensions QFN(QFN3X3-16-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.180	0.300	0.007	0.012
b1	0.160 REF		0.006 REF	
c	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D2	1.550	1.750	0.061	0.069
E	2.900	3.100	0.114	0.122
E2	1.550	1.750	0.061	0.069
e	0.500 BSC		0.020 BSC	
L	0.250	0.450	0.010	0.018
h	0.200	0.300	0.008	0.012

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPDA7008-QFNR	−40 to 85°C	QFN3X3-16	PT8	MSL3	Tape and Reel, 4000	Green
TPDA7004-QFNR	−40 to 85°C	QFN3X3-16	PT4	MSL3	Tape and Reel, 4000	Green

Evaluation board information

Order Number	Description	Eco Plan
EVM_TPDA700X	Evaluation board for TPDA7008/TPDA7004	Green
EVM_TPDA700X_KIT	Evaluation board for TPDA7008/TPDA7004 with USB to IIC emulator	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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