Micropower, Single-Supply Comparator and Precision Reference IC

Features

- Single-Supply Voltage Range: +2.5 V to +5.5 V
- Very Low Supply Current (33 µA for TPCMP511 and 45 µA for TPCMP512)
- Low Input Bias Current: 2 nA maximum
- Low Offset Voltage: ±7 mV maximum
- 450-ns Propagation Delay
- Rail-to-Rail Inputs
- −40°C to 125°C Operation Range
- Voltage Reference Offers:
  - 20ppm/°C (typ) Temperature Coefficient
  - ±0.4% (max) Initial Accuracy
  - Stable for 0 to 100-nF Capacitive Loads

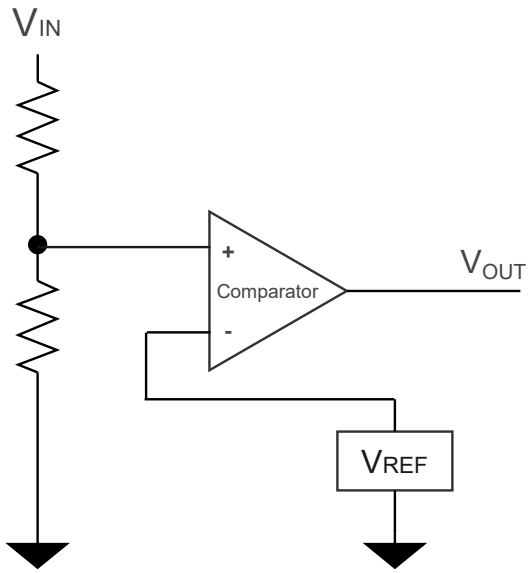
Applications

- Precision Battery Management
- Window Comparators
- Level Translators
- Digital Line Receivers

Description

The comparator features rail-to-rail input and output, with a common-mode input voltage range that extends 250 mV beyond the supply rails. Input bias current is typically 1.0 pA, and input offset voltage is typically 0.5 mV. Internal hysteresis ensures clean output switching, even with slow-moving input signals. The output stage features a unique design that limits supply current surges while switching, virtually eliminating supply glitches typical of many other comparators. This design also minimizes overall power consumption under dynamic conditions. The comparator outputs have rail-to-rail, push-pull output stages sinks and sources up to 95 mA. The propagation delay is 450 ns, even with the low-operating supply current. The device features an on-chip 1.23-V reference.

Typical Application Circuit



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Revision History

Date	Revision	Notes
2025-12-10	Rev.A.0	Initial version.
2026-01-23	Rev.A.1	The following updates are all about the new datasheet formats or typos, and the actual product remains unchanged. Updated Thermal Information for WLCSP: changed θ_{JA} from 201°C/W to 263.3°C/W and changed θ_{JC} from 24°C/W to 41.9°C/W. Added the TPCMP512 in the datasheet: • Updated Typical Application Circuit • Added Pin Configuration and Functions for TPCMP512-DF4R • Added Thermal Information for DFN2X2-8 • Updated Functional Block Diagram • Added Quiescent Current for TPCMP512 in Electrical Characteristics • Added Tape and Reel Information for TPCMP512-DF4R • Added Package Outline Dimensions for DFN2X2-8 • Added Order Information for TPCMP512-DF4R

Pin Configuration and Functions

TPCMP511-WLPR
WLCSP
Top View

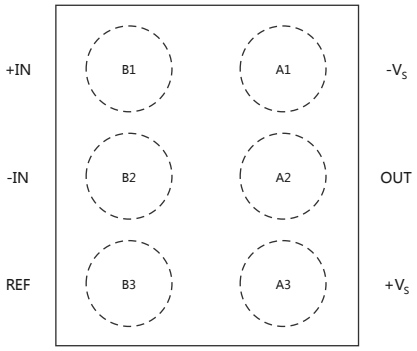


Table 1. Pin Functions: TPCMP511-WLPR

Pin No.	Name	I/O	Description
A1	$-V_S$	−	Negative power supply.
A2	OUT	O	Output.
A3	$+V_S$	−	Positive power supply.
B1	+IN	I	Non-inverting input.
B2	−IN	I	Inverting input.
B3	REF	-	Reference voltage output

TPCMP512-DF4R
DFN2X2-8
Top View

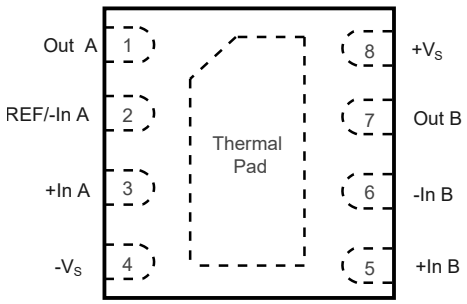


Table 2. Pin Functions: TPCMP512-DF4R

Pin No.	Name	I/O	Description
1	Out A	O	Output.
2	REF/−In A	−	Inverting input and Reference voltage output.
3	+In A	I	Non-inverting input.
4	$-V_S$	−	Negative power supply.
5	+In B	I	Non-inverting input.
6	−In B	I	Inverting input.
7	Out B	O	Output.
8	$+V_S$	−	Positive power supply.
Thermal Pad	Thermal Pad	-	Exposed Thermal Pad. The exposed pad is tied to the $-V_S$.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
	Supply Voltage, $(+V_S) – (-V_S)$	−0.3	6	V
	Input Voltage	$(-V_S) – 0.3$	$(+V_S) + 0.3$	V
	Input Current: +IN, −IN (2)	−10	10	mA
	Output Voltage	$(-V_S) – 0.3$	$(+V_S) + 0.3$	V
	Comparator Output Short-Circuit Duration (3)		Indefinite	
	Reference Output Short-Circuit Duration (3)		Indefinite	
T_J	Maximum Junction Temperature		150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	–65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The inputs are protected by ESD protection diodes to the positive and negative power supply. If the input extends more than 500 mV beyond the positive or negative power supply, the input current should be limited to less than 10 mA.
(3) A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many comparators are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
V_S	Supply Voltage, $(+V_S) – (-V_S)$	2.5		5.5	V

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
WLCSP	263.3	41.9	°C/W
DFN2X2-8	100	60	°C/W

Electrical Characteristics

All test conditions: V_S = 5 V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Supply						
I_Q	Quiescent Current	V_S = 5 V, No Load, Output High, V_{INP} = 1 V, V_{INN} = 0 V, T_A = −40°C to 125°C, TPCMP511		33	100	μA
		V_S = 5 V, No Load, Output High, V_{INP} = 1 V, V_{INN} = 0 V, T_A = −40°C to 125°C, TPCMP512		45	100	μA
		V_S = 5 V, No Load, Output Low, V_{INP} = 0 V, V_{INN} = 1 V, T_A = −40°C to 125°C, TPCMP511		33	100	μA
		V_S = 5 V, No Load, Output Low, V_{INP} = 0 V, V_{INN} = 1 V, T_A = −40°C to 125°C, TPCMP512		45	100	μA
		V_S = 2.7 V, No Load, Output High, V_{INP}= 1 V, V_{INN} = 0 V, T_A = −40°C to 125°C, TPCMP511		32	100	μA
		V_S = 2.7 V, No Load, Output High, V_{INP}= 1 V, V_{INN} = 0 V, T_A = −40°C to 125°C, TPCMP512		45	100	μA
		V_S = 2.7 V, No Load, Output Low, V_{INP} = 0 V, V_{INN} = 1 V, T_A = −40°C to 125°C, TPCMP511		32	100	μA
		V_S = 2.7 V, No Load, Output Low, V_{INP} = 0 V, V_{INN} = 1 V, T_A = −40°C to 125°C, TPCMP512		45	100	μA
PSRR	Power Supply Rejection Ratio	V_S = 2.5 V to 5.5 V, V_{CM} = 0 V, T_A = −40°C to 125°C	67	80		dB
Input Characteristics						
V_{OS}	Input Offset Voltage (1)	V_S = 5 V, V_{CM} = 0 V	−5	±0.5	5	mV
		V_S = 5 V, V_{CM} = 0 V, T_A = −40°C to 125°C	−7		7	mV
V_{OS} TC	Input Offset Voltage Drift (2)	V_S = 5 V, V_{CM} = 0 V, T_A = −40°C to 125°C			30	μV/°C
V_{OS}	Input Offset Voltage (1)	V_S = 2.5 V, V_{CM} = 0 V	−5		5	mV
		V_S = 2.5 V, V_{CM} = 0 V, T_A = −40°C to 125°C	−7	±1	7	mV
V_{OS} TC	Input Offset Voltage Drift (2)	V_S = 2.5 V, V_{CM} = 0 V, T_A = −40°C to 125°C			30	μV/°C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{HYST}	Input Hysteresis Voltage (1)	V_S = 5 V, V_{CM} = 0 V		2.5		mV
V_{HYST}	Input Hysteresis Voltage (1)	V_S = 2.5 V, V_{CM} = 0 V		2.5		mV
I_B	Input Bias Current	V_S = 5 V, V_{CM} = 0 V, T_A = −40°C to 125°C	−2000	±1	2000	pA
		V_S = 5 V, V_{CM} = 2.5 V, T_A = −40°C to 125°C	−2000		2000	pA
I_{OS}	Input Offset Current	V_S = 5 V, V_{CM} = 0 V	−1000	±0.5	1000	pA
		V_S = 5 V, V_{CM} = 0 V, T_A = −40°C to 125°C	−2000	±0.5	2000	pA
		V_S = 5 V, V_{CM} = 2.5 V	−1000		1000	pA
		V_S = 5 V, V_{CM} = 2.5 V, T_A = −40°C to 125°C	−2000	±0.5	2000	pA
C_{IN}	Input Capacitance	Either input over vcm range		2.5		pF
CMRR	Common-mode Rejection Ratio	V_S = 5 V, V_{CM} = 0 V to 5 V, T_A = −40°C to 125°C	60	65		dB
V_{CM}	Common-mode Input Voltage Range	V_S = 5 V	−0.25		5.25	V
		V_S = 5 V, T_A = −40°C to 125°C	0		5	V
Output						
V_{OL}	Output Voltage Swing from Negative Rail	V_S = 5 V, I_{SINK} = 8 mA			300	mV
		V_S = 5 V, I_{SINK} = 8mA, T_A = −40°C to 125°C		250	350	mV
		V_S = 2.7 V, I_{SINK} = 3.5 mA			160	mV
		V_S = 2.7 V, I_{SINK} = 3.5 mA, T_A = −40°C to 125°C		150	200	mV
V_{OH}	Output Voltage Swing from Positive Rail	V_S = 5 V, I_{SOURCE} = 8 mA			150	mV
		V_S = 5 V, I_{SOURCE} = 8 mA, T_A = −40°C to 125°C		120	200	mV
		V_S = 2.7 V, I_{SOURCE} = 3.5 mA			120	mV
		V_S = 2.7 V, I_{SOURCE} = 3.5 mA, T_A = −40°C to 125°C		100	150	mV
I_{SOURCE}	Source Current	V_S = 5 V, T_A = −40°C to 125°C		95		mA
		V_S = 2.7 V, T_A = −40°C to 125°C		35		mA
I_{SINK}	Sink Current	V_S = 5 V, T_A = −40°C to 125°C		95		mA
		V_S = 2.7 V, T_A = −40°C to 125°C		35		mA
Switching Characteristics (3)						
T_{PLH}	Propagation Delay Time, Low to High	V_S = 2.7 V, V_{CM} = V_S/2, 50mV overdrive, C_L= 15 pF		450		ns
		V_S = 2.7 V, V_{CM} = V_S/2, 100mV overdrive, C_L= 15 pF		400		ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		V_S = 5 V, V_{CM} = V_S/2, 50mV overdrive, C_L= 15 pF		450		ns
		V_S = 5 V, V_{CM} = V_S/2, 100mV overdrive, C_L= 15 pF		400	450	ns
T_{PHL}	Propagation Delay Time, High to Low	V_S = 2.7 V, V_{CM} = V_S/2, 50mV overdrive, C_L= 15 pF		450		ns
		V_S = 2.7 V, V_{CM} = V_S/2, 100mV overdrive, C_L= 15 pF		400		ns
		V_S = 5 V, V_{CM} = V_S/2, 50mV overdrive, C_L= 15 pF		450		ns
		V_S = 5 V, V_{CM} = V_S/2, 100mV overdrive, C_L= 15 pF		400	450	ns
T_R	Rise Time	V_S = 5 V, C_L= 15 pF, Output from 20% to 80%		40		ns
T_R	Rise Time	V_S = 5 V, C_L= 50 pF, Output from 20% to 80%		50		ns
T_R	Rise Time	V_S = 5 V, C_L= 200 pF, Output from 20% to 80%		80		ns
T_F	Fall Time	V_S = 5 V, C_L= 15 pF, Output from 80% to 20%		40		ns
T_F	Fall Time	V_S = 5 V, C_L= 50 pF, Output from 80% to 20%		50		ns
T_F	Fall Time	V_S = 5 V, C_L= 200 pF, Output from 80% to 20%		80		ns
T_{ON}	Power-up Time	V_S = 5 V, The time between VCC exceed 2.7V and the output is in a valid logic state.		20		µs
Reference						
V_{REF}	Reference Voltage, 0.4%	Initial at 25°C	1.225	1.23	1.235	V
V_{REF}TC	Output Voltage Temperature Coefficient	−40°C to 85°C		20	100	ppm/°C
		−40°C to 125°C		20	100	ppm/°C
ΔV_{REF}/ ΔV_S	Line Regulation	2.5V ≤ V_S≤ 5.5V, T_A = −40°C to 125°C		50	200	µV/V
ΔV_{REF}/ ΔI_{REF}	Load Regulation	Sourcing: 0µA~500µA, T_A = −40°C to 125°C		2	4	µV/µA
		Sinking: -500µA~0µA, T_A = −40°C to 125°C		3.5	6	µV/µA
I_{SC}	Output Short-Circuit Current	V_{REF}= −V_S or V_S, T_A = 25°C		4		mA
Noise Voltage	Peak to Peak Noise	f = 0.1Hz to 10Hz, T_A = 25°C		17		µVpp

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Noise Voltage	RMS Noise	f = 10Hz to 10kHz, T_A = 25°C		42		μV
Ripple Rejection	$\Delta V_{REF}/\Delta V_{CC}$	V_{CC} = 5V ±100mV, f = 120Hz, T_A = 25°C		86		dB
T_{HYST}	Thermal Hysteresis	T_A = 25°C		130		ppm
C_{LOAD}	Capacitive Load	T_A = −40°C to 125°C			100	nF
T_{REF}	Turn-on Settling Time	To Vref=1% of final value, T_A = 25°C		200		μs

(1) The input offset voltage is the average of the input-referred trip points.
(2) Provided by bench tests and design simulation.
(3) Delay time is measured from the mid-point of the input to the mid-point of the output.
(4) Provided by design simulation.

Typical Performance Characteristics

All test conditions: V_S = 5 V, V_{CM} = 2.5 V, unless otherwise noted.

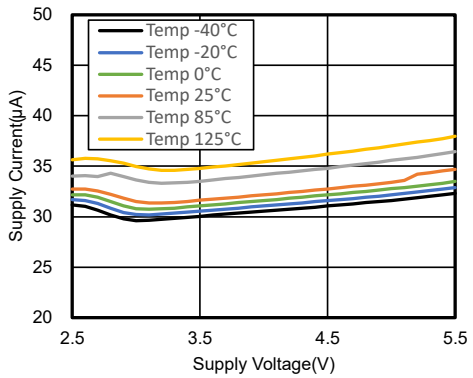


Figure 1. Supply Current vs. Supply Voltage, Output High, TPCMP511

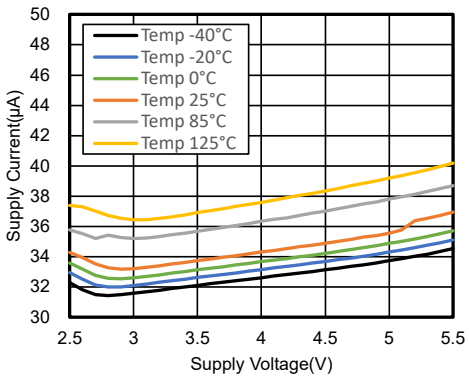


Figure 2. Supply Current vs. Temperature, TPCMP511

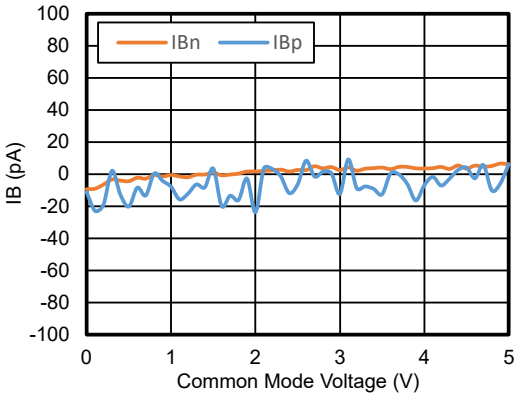


Figure 3. IB vs. Common-Mode Voltage

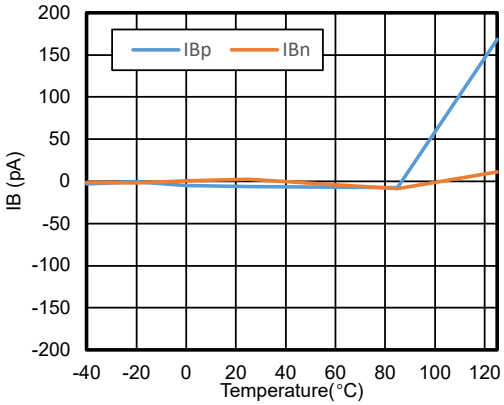


Figure 4. IB vs. Temperature

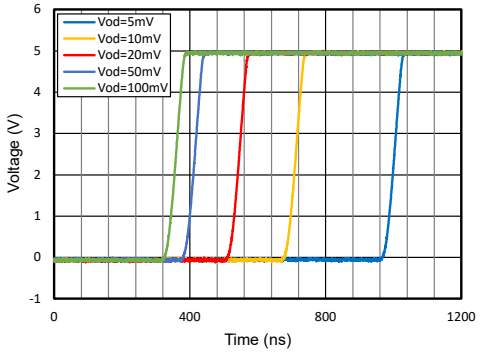


Figure 5. Propagation Delay, Low to High, 5 V

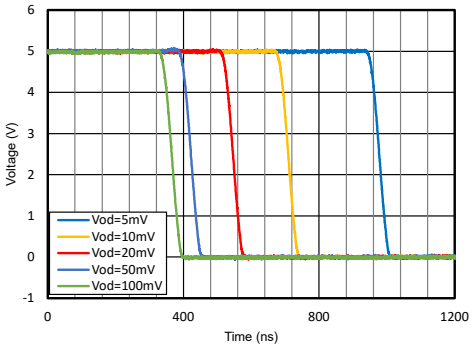


Figure 6. Propagation Delay, High to Low, 5 V

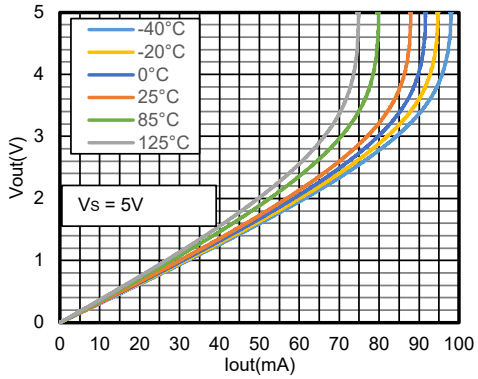


Figure 7. Output Voltage vs. Output Sinking Current, 5 V

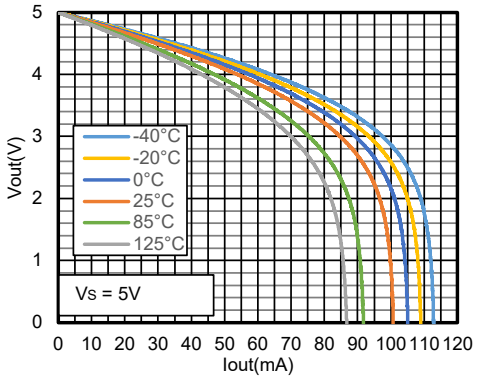


Figure 8. Output Voltage vs. Output Sourcing Current, 5 V

Detailed Description

Overview

The comparators feature rail-to-rail inputs and outputs, with a common-mode input voltage range that extends 250 mV beyond the supply rails. Input bias current is typically 1.0 pA, and input offset voltage is typically 0.5 mV. Internal hysteresis ensures clean output switching, even with slow-moving input signals. The output stage features a unique design that limits supply current surges while switching, virtually eliminating supply glitches typical of many other comparators. This design also minimizes overall power consumption under dynamic conditions. The comparator outputs have rail-to-rail, push-pull output stages sinks and sources up to 95 mA. The propagation delay is 450 ns, even with the low-operating supply current. The device features an on-chip 1.23-V reference.

Functional Block Diagram

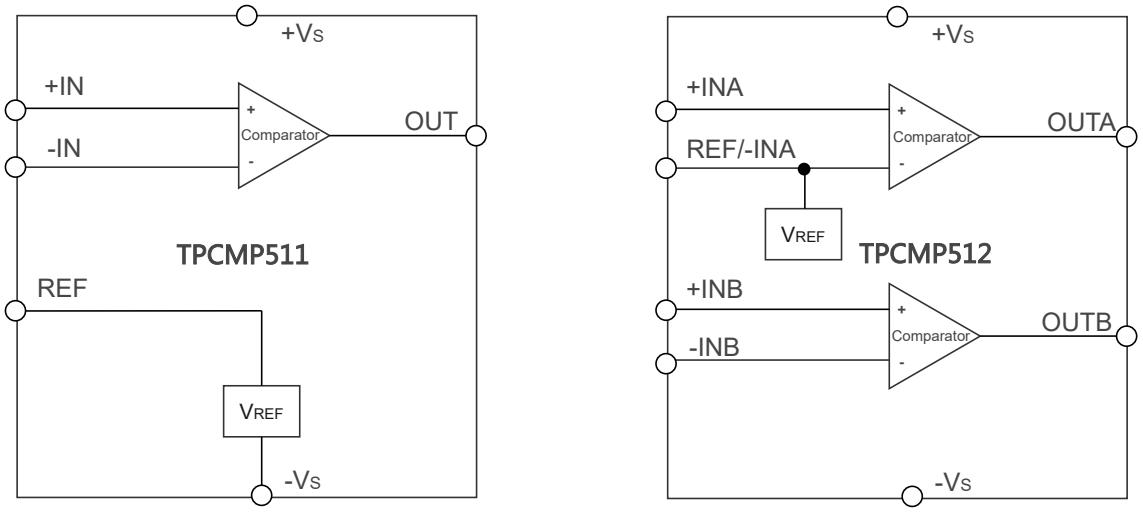


Figure 9. Functional Block Diagram

Application and Implementation

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Typical Application

Over-voltage Detection

The device is an ideal candidate to be used as over-voltage detection shown in Figure 10. The input signal is compared with the reference voltage through a resistor divider to generate a comparator logic output. When the divided input voltage exceeds the reference voltage, the comparator output goes high to indicate an over-voltage fault.

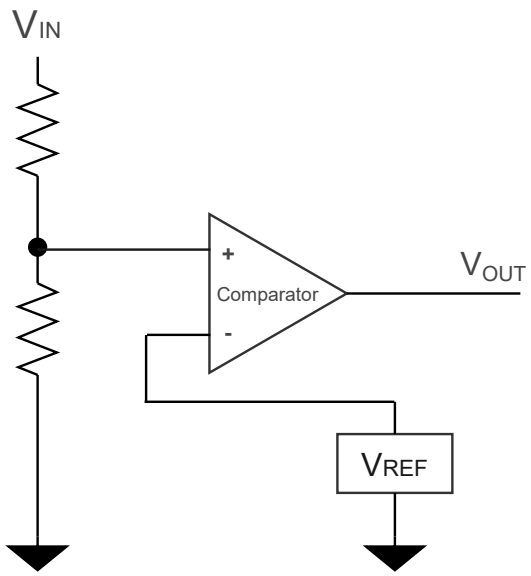
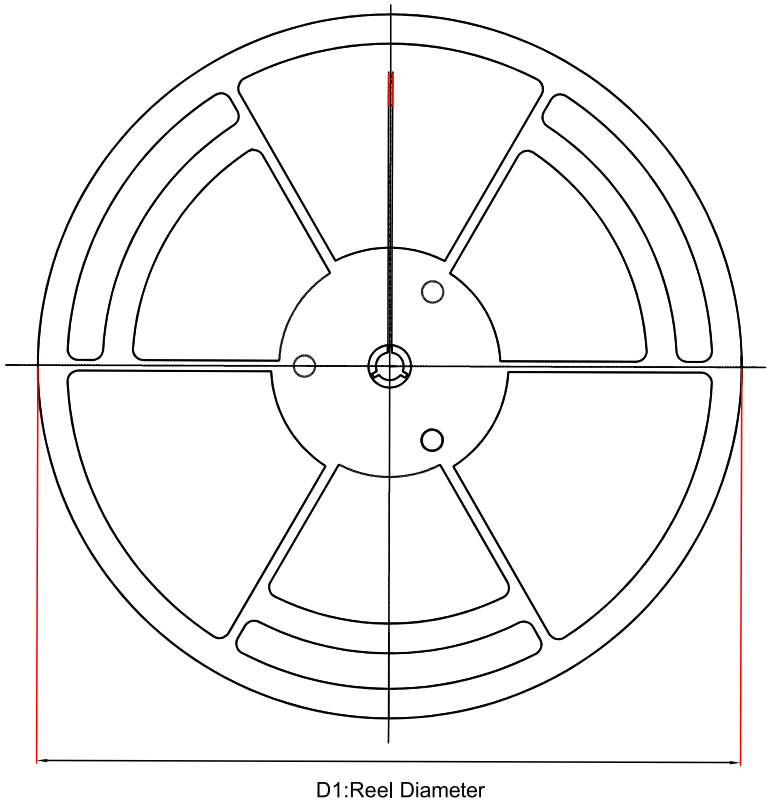
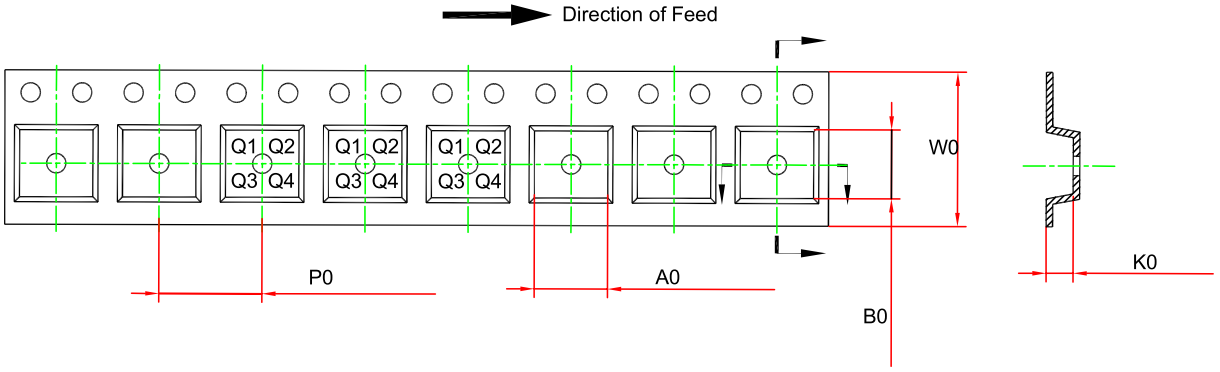


Figure 10. Typical Application Circuit

Tape and Reel Information





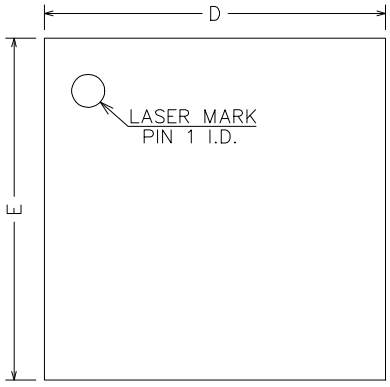
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm) (1)	B0 (mm) (1)	K0 (mm) (1)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPCMP511-WLPR	WLCSP	178	12.5	1.18	1.68	0.83	4	8	Q1
TPCMP512-DF4R	DFN2X2-8	180	12.5	2.15	2.15	0.88	4	8	Q1

(1) The value is for reference only. Contact the 3PEAK factory for more information.

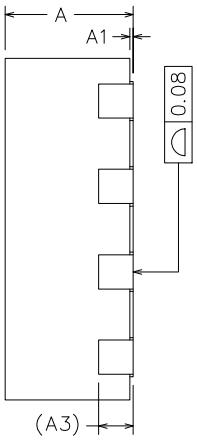
Package Outline Dimensions

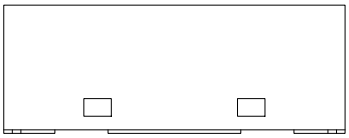
DFN2X2-8

Package Outline Dimensions DF4(DFN2X2-8-I)

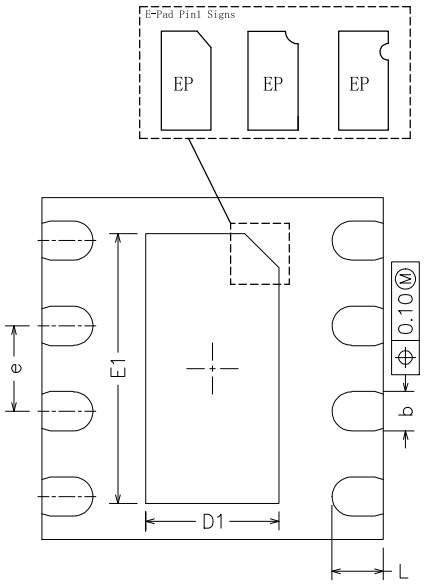


Top View





Side View



Bottom View

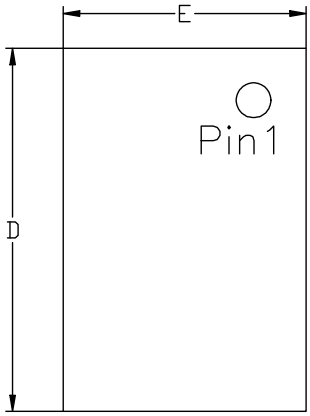
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.200	0.300	0.008	0.012
A3	0.150	0.250	0.006	0.010
D	1.950	2.050	0.077	0.081
D1	0.750	0.850	0.030	0.033
E	1.950	2.050	0.077	0.081
E1	1.550	1.650	0.061	0.065
e	0.500 BSC		0.020BSC	
L	0.250	0.350	0.010	0.014

NOTES

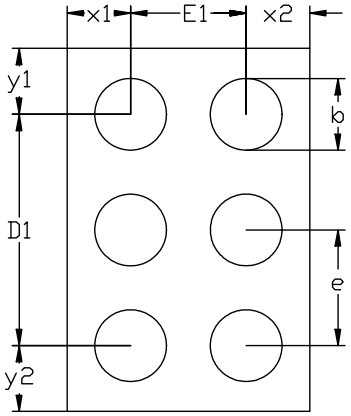
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

WLCSP

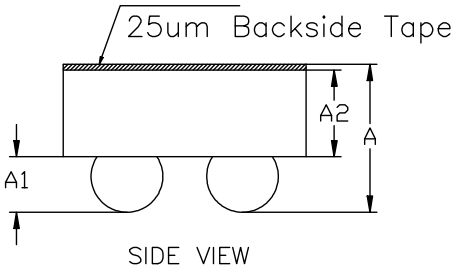
Package Outline Dimensions WLP(WLCSP-A)



TOP VIEW
(MARK SIDE)



BOTTOM VIEW
(BALL SIDE)



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.595	0.685	0.023	0.027
A1	0.220	0.260	0.009	0.010
A2	0.350	0.400	0.014	0.016
D	1.540	1.600	0.061	0.063
D1	1.000BSC		0.039	
E	1.020	1.080	0.040	0.043
E1	0.500BSC		0.020	
b	0.290	0.330	0.011	0.013
e	0.500BSC		0.020	
x1	0.275REF		0.011	
x2	0.275REF		0.011	
y1	0.285REF		0.011	
y2	0.285REF		0.011	

NOTES:
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPCMP511-WLPR	−40 to 125°C	WLCSP	C51	MSL1	Tape and Reel,3000	Green
TPCMP512-DF4R	−40 to 125°C	DFN2X2-8	C52	MSL3	Tape and Reel,3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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