14-Bit, 250MSPS, Ultralow-Power ADC

Features

- Maximum Sample Rate: 250 MSPS
- Ultralow Power with 1.8-V Single Supply
- Programmable Data Rate:
  - 337-mW Total Power at 160 MSPS
  - 448-mW Total Power at 250 MSPS
- High Dynamic Performance:
  - SNR: 71.0dBFS at 170 MHz
  - SFDR: 84dBc at 170 MHz
- Output Interface:
  - Double Data Rate (DDR) LVDS with Programmable Swing and Strength
  - Standard Swing: 350 mV
  - Low Swing: 200 mV
  - Default Strength: 100 Ω Termination
  - 2x Strength: 50 Ω Termination
  - 1.8-V Parallel CMOS Interface Also Supported
- Programmable Gain up to 6dB for SNR/SFDR Trade-Off
- DC Offset Correction
- Supports Low Input Clock Amplitude Down To 200 mVPP
- Package: QFN7×7-48

Applications

- Wireless Communications Infrastructure
- Software Defined Radio

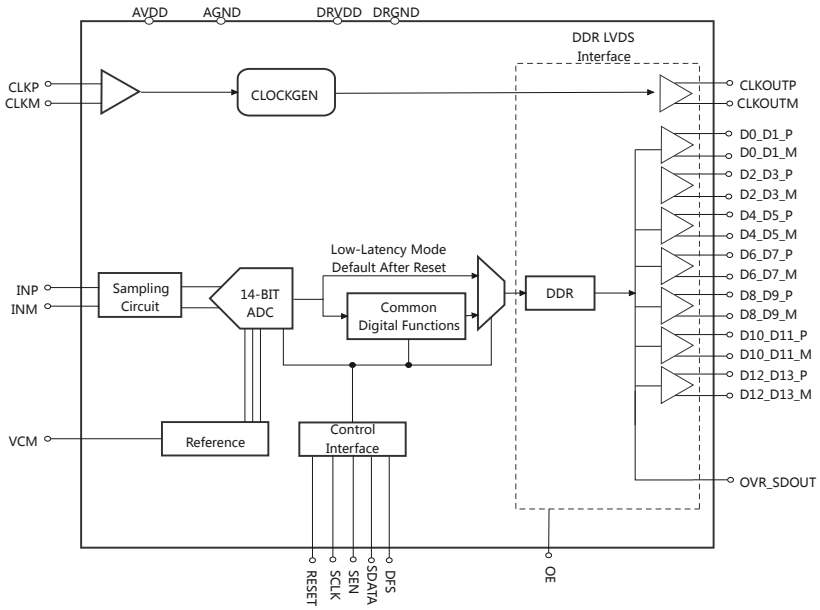
Description

The TPC703120 is a 14-bit analog-to-digital converter (ADC) with sampling rates up to 250MSPS. These devices use innovative design techniques to achieve high dynamic performance, while consuming extremely low power at 1.8-V supply. The device is well-suited for multi-carrier, wide bandwidth communications applications.

The TPC703120 has fine gain options that can be used to improve SFDR performance at lower full-scale input ranges, especially at high input frequencies. They include a DC offset correction loop that can be used to cancel the ADC offset. At lower sampling rates, the ADC automatically operates at scaled-down power with no loss in performance.

The TPC703120 is available in a compact QFN7×7-48 package and is specified over the industrial temperature range (–40 °C to +85 °C).

Functional Block Diagram



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Product Family Table

Order Number	Resolution	Throughput	Package	Interface
TPC703120-FE5R	14	250M	QFN7X7-48	DDR LVDS,PARA CMOS

Revision History

Date	Revision	Notes
2026-06-15	Rev.A.0	initial release.

Pin Configuration and Functions

TPC703120 LVDS Pinout
QFN7×7-48 Package
Top View

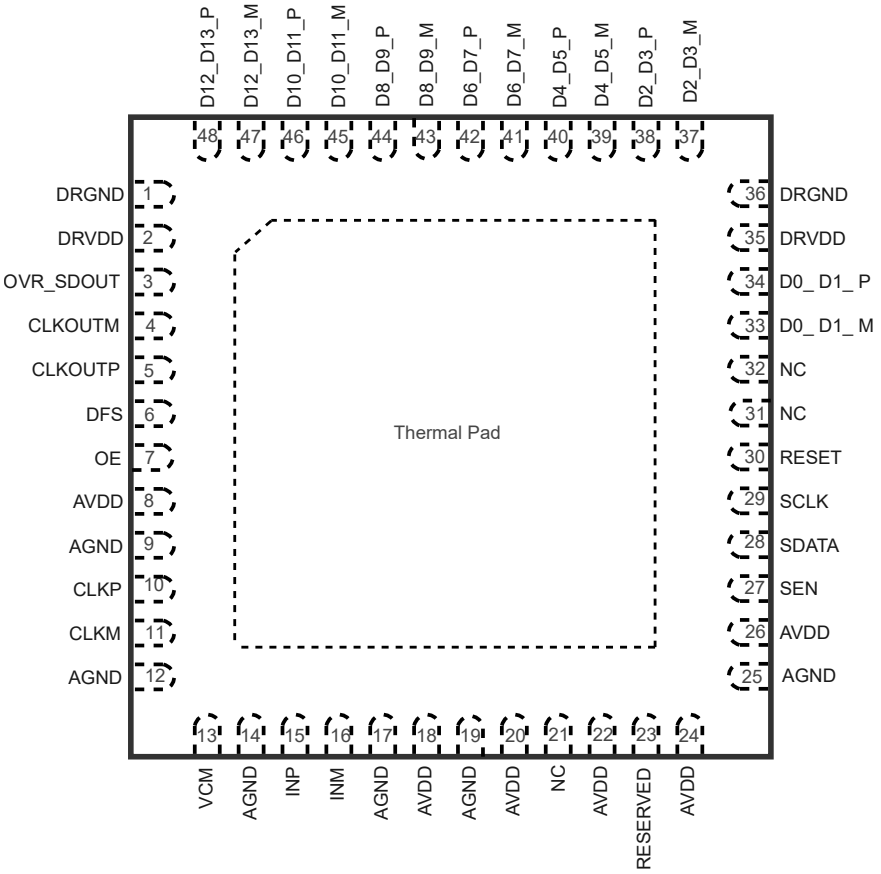


Table 1. Pin Functions: TPC703120 Pin Assignments (LVDS Mode)

Pin		Type (1)	Description
Name	Number		
AVDD	8, 18, 20, 22, 24, 26	I	Analog power supply
AGND	9, 12, 14, 17, 19, 25	I	Analog ground
CLKP	10	I	Differential clock input, positive
CLKM	11	I	Differential clock input, negative
INP	15	I	Differential analog input, positive
INM	16	I	Differential analog input, negative
VCM	13	O	Outputs the common-mode voltage (0.95 V) that can be used externally to bias the analog input pins.

Pin		Type (1)	Description
Name	Number		
RESET	30	I	Serial interface RESET input. When using the serial interface mode, the internal registers must be initialized through hardware RESET by applying a high pulse on this pin or by using the software reset option; refer to the Serial Interface section. When RESET is tied high, the internal registers are reset to the default values. In this condition, SEN can be used as an analog control pin. RESET has an internal 180-kΩ pull-down resistor.
SCLK	29	I	This pin functions as a serial interface clock input when RESET is low. When RESET is high, SCLK has no function and should be tied to ground. This pin has an internal 180-kΩ pull-down resistor.
SDATA	28	I	This pin functions as a serial interface data input when RESET is low. When RESET is high, SDATA functions as a STANDBY control pin (see Table 10). This pin has an internal 180-kΩ pull-down resistor.
SEN	27	I	This pin functions as a serial interface enable input when RESET is low. When RESET is high, SEN has no function and should be tied to AVDD. This pin has an internal 180-kΩ pull-up resistor to AVDD.
OE	7	I	Output buffer enable input, active high; this pin has an internal 180-kΩ pull-up resistor to DRVDD.
DFS	6	I	Data format select input. This pin sets the DATA FORMAT (twos complement or offset binary) and the LVDS/CMOS output interface type. See Table 8 for detailed information.
RESERVED	23	I	Digital control pin, reserved for future use
CLKOUTP	5	O	Differential output clock, true
CLKOUTM	4	O	Differential output clock, complement
D0_D1_P	34	O	Differential output data D0 and D1 multiplexed, true
D0_D1_M	33	O	Differential output data D0 and D1 multiplexed, complement
D2_D3_P	38	O	Differential output data D2 and D3 multiplexed, true
D2_D3_M	37	O	Differential output data D2 and D3 multiplexed, complement
D4_D5_P	40	O	Differential output data D4 and D5 multiplexed, true
D4_D5_M	39	O	Differential output data D4 and D5 multiplexed, complement
D6_D7_P	42	O	Differential output data D6 and D7 multiplexed, true
D6_D7_M	41	O	Differential output data D6 and D7 multiplexed, complement
D8_D9_P	44	O	Differential output data D8 and D9 multiplexed, true
D8_D9_M	43	O	Differential output data D8 and D9 multiplexed, complement
D10_D11_P	46	O	Differential output data D10 and D11 multiplexed, true
D10_D11_M	45	O	Differential output data D10 and D11 multiplexed, complement
D12_D13_P	48	O	Differential output data D12 and D13 multiplexed, true

Pin		Type (1)	Description
Name	Number		
D12_D13_M	47	O	Differential output data D12 and D13 multiplexed, complement
OVR_SDOUT	3	O	This pin functions as an out-of-range indicator after reset, when register bit READOUT = 0, and functions as a serial register readout pin when READOUT = 1.
DRVDD	2, 35	I	1.8V digital and output buffer supply
DRGND	1, 36, PAD	I	Digital and output buffer ground
NC	31, 32		Do not connect
Thermal Pad	Thermal Pad	-	The Thermal Pad is connected to DRGND.

(1) I is input, O is output.

TPC703120 CMOS Pinout
QFN7 × 7-48 Package
Top View

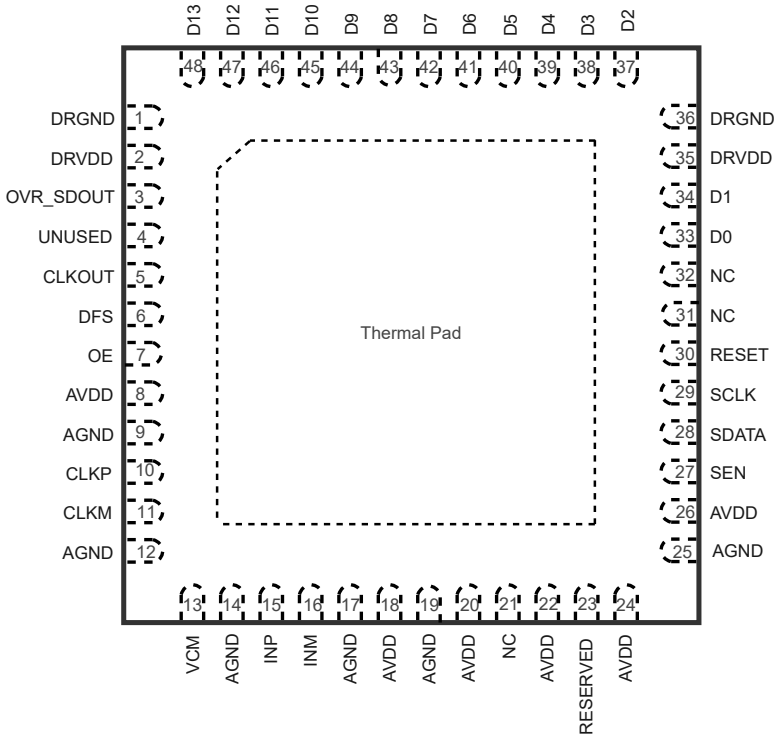


Figure 1.

Table 2. Pin Functions: TPC703120 Pin Assignments (CMOS Mode)

Pin		Type (1)	Description
Name	Number		
AVDD	8, 18, 20, 22, 24, 26	I	1.8V analog power supply
AGND	9, 12, 14, 17, 19, 25	I	Analog ground
CLKP	10	I	Differential clock input, positive
CLKM	11	I	Differential clock input, negative
INP	15	I	Differential analog input, positive
INM	16	I	Differential analog input, negative
VCM	13	O	Outputs the common-mode voltage (0.95 V) that can be used externally to bias the analog input pins.
RESET	30	I	Serial interface RESET input.

Pin		Type (1)	Description
Name	Number		
			When using the serial interface mode, the internal registers must initialize through hardware RESET by applying a high pulse on this pin or by using the software reset option; refer to the Serial Interface section. When RESET is tied high, the internal registers are reset to the default values. In this condition, SEN can be used as an analog control pin. RESET has an internal 180-kΩ pull-down resistor.
SCLK	29	I	This pin functions as a serial interface clock input when RESET is low. When RESET is high, SCLK has no function and should be tied to ground. This pin has an internal 180-kΩ pull-down resistor.
SDATA	28	I	This pin functions as a serial interface data input when RESET is low. When RESET is high, SDATA functions as a STANDBY control pin (see Table 10). This pin has an internal 180-kΩ pull-down resistor.
SEN	27	I	This pin functions as a serial interface enable input when RESET is low. When RESET is high, SEN has no function and should be tied to AVDD. This pin has an internal 180-kΩ pull-up resistor to AVDD.
OE	7	I	Output buffer enable input, active high; this pin has an internal 180kΩ pull-up resistor to DRVDD.
DFS	6	I	Data format select input. This pin sets the DATA FORMAT (twos complement or offset binary) and the LVDS/CMOS output interface type. See Table 8 for detailed information.
RESERVED	23	I	Digital control pin, reserved for future use
CLKOUTP	5	O	Differential output clock, true
CLKOUTM	4	O	Differential output clock, complement
D0	33	O	14-bit CMOS output data
D1	34	O	14-bit CMOS output data
D2	37	O	14-bit CMOS output data
D3	38	O	14-bit CMOS output data
D4	39	O	14-bit CMOS output data
D5	40	O	14-bit CMOS output data
D6	41	O	14-bit CMOS output data
D7	42	O	14-bit CMOS output data
D8	43	O	14-bit CMOS output data
D9	44	O	14-bit CMOS output data
D10	45	O	14-bit CMOS output data
D11	46	O	14-bit CMOS output data
D12	47	O	14-bit CMOS output data
D13	48	O	14-bit CMOS output data

Pin		Type (1)	Description
Name	Number		
OVR_SDOUT	3	O	This pin functions as an out-of-range indicator after reset, when register bit READOUT = 0, and functions as a serial register readout pin when READOUT = 1.
DRVDD	2, 35	I	1.8V digital and output buffer supply
DRGND	1, 36, PAD	I	Digital and output buffer ground
NC	31, 32		Do not connect
Thermal Pad	Thermal Pad	-	The Thermal Pad is connected to DRGND.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Analog Voltage	Analog Input Voltage to GND	GND − 0.3	VDD + 0.3	V
Digital Voltage	Digital Input Voltage to AGND	GND − 0.3	VDD + 0.3	V
Supply Voltage	AVDD/DRVDD to GND	−0.3	2.1	V
T_J	Maximum Junction Temperature		125	°C
T_A	Operating Temperature Range	−40	85	°C
T_{STG}	Storage Temperature Range	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	3	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Power Supply (VDD to GND)	1.7	1.8	1.9	V
Power Supply (DRVDD to GND)	1.7	1.8	1.9	V
Analog Inputs				
Differential Input Voltage Range (1)		2		VPP
Input Common-mode Voltage		VCM±0.05		V
Maximum Analog Input Frequency with 2VPP Input Amplitude		400		MHz
Maximum Analog Input Frequency with 1VPP Input Amplitude		800		MHz
Clock Input				
TPC703120				
Low-speed Mode Enabled	20		80	MSPS
Low-speed Mode Disabled	> 80		250	MSPS
Input clock amplitude differential (VCLKP – VCLKM)				
Sine Wave, Ac-coupled	0.2	1.5		VPP
LVPECL, Ac-coupled		1.6		VPP
LVDS, Ac-coupled		0.7		VPP

Parameter		Min	Typ	Max	Unit
LVCMOS, Single-ended, Ac-coupled			1.8		V
Input Clock Duty Cycle					
Low-speed Mode Enabled		40	50	60	%
Low-speed Mode Disabled		35	50	65	%
Digital Outputs					
C_{LOAD}	Maximum External Load Capacitance from Each Output Pin to DRGND		5		pF
R_{LOAD}	Differential Load Resistance between the LVDS Output Pairs (LVDS mode)		100		Ω
T_A	Operating Free-air Temperature	–40		+85	°C

(1) With 0dB gain

Thermal Information

Package Type	θ_{JA}	θ_{JB}	θ_{JCTOP}	Unit
QFN7×7-48	34.3	7.09	11.24	°C/W

Electrical Characteristics: TPC703120

All test conditions: AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, –1dBFS differential analog input, 1dB gain, and DDR LVDS interface. Minimum and maximum values are across the full temperature range: TMIN = –40°C to TMAX = +85°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
	Resolution				14	Bits
	SNR (signal-to-noise ratio), LVDS	fIN = 10MHz		72.7		dBFS
		fIN = 70MHz		72.2		dBFS
		fIN = 100MHz		71.8		dBFS
		fIN = 170MHz		71		dBFS
		fIN = 300MHz		69.9		dBFS
	SINAD (signal-to-noise and distortion ratio), LVDS	fIN = 10MHz		71.4		dBFS
		fIN = 70MHz		70.3		dBFS
		fIN = 100MHz		69.2		dBFS
		fIN = 170MHz		69.5		dBFS
		fIN = 300MHz		67.7		dBFS
SFDR	Spurious-free Dynamic Range	fIN = 10MHz		89.0		dBc
		fIN = 70MHz		81.0		dBc
		fIN = 100MHz		76.1		dBc
		fIN = 170MHz		83.1		dBc
		fIN = 300MHz		75.4		dBc
THD	Total Harmonic Distortion	fIN = 10MHz		84.8		dBc
		fIN = 70MHz		77.7		dBc
		fIN = 100MHz		74.2		dBc
		fIN = 170MHz		78.6		dBc
		fIN = 300MHz		73.9		dBc
HD2	Second-harmonic Distortion	fIN = 10MHz		88.0		dBc
		fIN = 70MHz		82.7		dBc
		fIN = 100MHz		83.0		dBc
		fIN = 170MHz		82.3		dBc
		fIN = 300MHz		74.4		dBc
HD3	Third-harmonic Distortion	fIN = 10MHz		89.5		dBc
		fIN = 70MHz		80.0		dBc
		fIN = 100MHz		75.0		dBc
		fIN = 170MHz		82.3		dBc
		fIN = 300MHz		86.9		dBc
	Worst Spur	fIN = 10MHz		102.4		dBc

Parameter		Conditions	Min	Typ	Max	Unit
	(other than second and third harmonics)	fIN = 70MHz		96.6		dBc
		fIN = 100MHz		97.6		dBc
		fIN = 170MHz		96.5		dBc
		fIN = 300MHz		94.4		dBc
	Input Overload Recovery	Recovery to within 1% (of final value) for 6dB overload with sine-wave input		1		Clock cycles
PSRR	AC Power-supply Rejection Ratio	For 100mVPP signal on AVDD supply, up to 10MHz		> 30		dB
ENOB	Effective Number of Bits	fIN = 170MHz		11.4		LSBs
DNL	Differential Nonlinearity	fIN = 170MHz	−0.95	±0.5	0.95	LSBs
INL	Integrated Nonlinearity	fIN = 170MHz	−5	±2	5	LSBs

Electrical Characteristics (continued): General

All test conditions: AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, –1dBFS differential analog input, 1dB gain, and DDR LVDS interface. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, unless otherwise noted.

Parameter		Min	Typ	Max	Unit
	Differential input voltage range		2		VPP
	Differential input resistance (at DC)		> 1		MΩ
	Differential input capacitance		4		pF
	Analog input bandwidth		550		MHz
V_{CM}	Common-mode output voltage		0.95		V
	VCM output current capability		4		mA
	Offset error	-15	5	15	mV
	Temperature coefficient of offset error		0.003		mV/°C
E_{GREF}	Gain error as a result of internal reference inaccuracy alone	-2		2	%FS
E_{GCHAN}	Gain error of channel alone		–0.2		%FS
	Temperature coefficient of EGCHAN		0.001		Δ%/°C
	IAVDD Analog supply current		159.0	170.0	mA
	IDRVDD (1) Output buffer supply current LVDS interface with 100 Ω external termination Low LVDS swing (200 mV)		62.0		mA
	IDRVDD Output buffer supply current LVDS interface with 100 Ω external termination Standard LVDS swing (350 mV)		85.0	110.0	mA
	IDRVDD output buffer supply current (1)(2) CMOS interface (2) 8pF external load capacitance fIN = 2.5MHz		75.0		mA
	Analog power		286.2		mW
	LVDS interface, low LVDS swing		153		mW
	Digital power CMOS interface (2) 8pF external load capacitance fIN = 2.5MHz		135.0		mW
	Global power-down		2		mW
	Standby		62.0	79.2	mW

(1) The maximum DRVDD current with CMOS interface depends on the actual load capacitance on the digital output lines. Note that the maximum recommended load capacitance on each digital output line is 10pF.

(2) In CMOS mode, the DRVDD current scales with the sampling frequency, the load capacitance on output pins, and the input frequency.

Digital Characteristics

All test conditions: AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, –1dBFS differential analog input, 1dB gain, and DDR LVDS interface. Minimum and maximum values are across the full temperature range: TMIN = –40°C to TMAX = +85°C, unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Unit
Digital Inputs (RESET, SCLK, SDATA, SEN, OE)					
High-level input voltage	RESET, SCLK, SDATA, and SEN support 1.8 V and 3.3 V CMOS logic levels	1.3			V
Low-level input voltage				0.4	V
High-level input voltage	OE only supports 1.8 V CMOS logic levels	1.3			V
Low-level input voltage				0.4	V
High-level input current: SDATA, SCLK (1)	VHIGH = 1.8 V		10		µA
High-level input current: SEN	VHIGH = 1.8 V		0		µA
Low-level input current: SDATA, SCLK	VLOW = 0 V		0		µA
Low-level input current: SEN	VLOW = 0 V		10		µA
Digital Outputs (CMOS INTERFACE: D0 TO D13, OVR_SDOUT)					
High-level output voltage	Iload = 1 mA	DRVDD – 0.15	DRVDD		V
Low-level output voltage	Iload= 1 mA		0	0.15	V
Digital Outputs (LVDS INTERFACE: DA0P/M TO DA13P/M, DB0P/M TO DB13P/M, CLKOUTP/M)					
High-level output voltage (2) VODH	Standard swing LVDS	270	+350	420	mV
Low-level output voltage (2) VODL	Standard swing LVDS	−420	–350	-270	mV
High-level output voltage (2) VODH	Low swing LVDS		+200		mV
Low-level output voltage (2) VODL	Low swing LVDS		−200		mV
Output common-mode voltage VOCM			1.05		V

(1) SDATA and SCLK have an internal 180kΩ pull-down resistor.

(2) With an external 100Ω termination.

Timing Characteristics

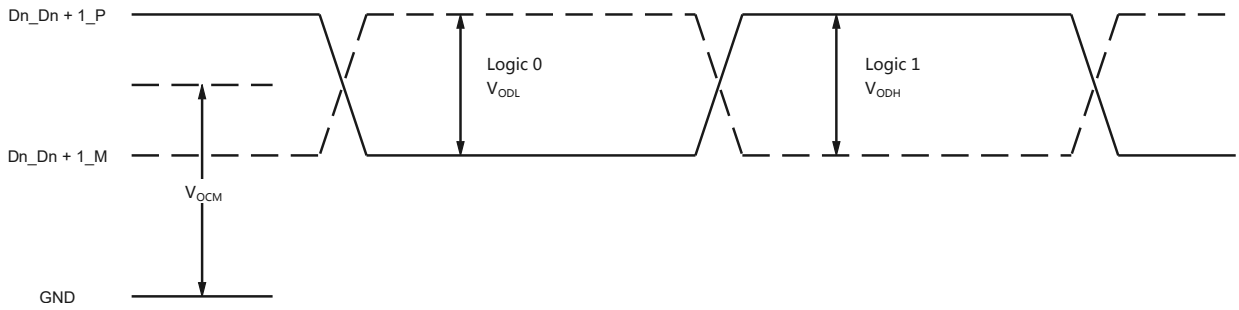


Figure 2. LVDS Output Voltage Levels

(1) With external 100-Ω termination.

Timing Requirements: LVDS and CMOS Modes (1)

All test conditions: AVDD = 1.8 V, DRVDD = 1.8 V, sampling frequency = 250 MSPS, sine wave input clock, CLOAD = 5pF (2) , and R_{LOAD} = 100Ω (3) .Minimum and maximum values are across the full temperature range: TMIN = –40°C to TMAX = +85°C, AVDD = 1.8 V, and DRVDD = 1.7 V to 1.9 V, unless otherwise noted

Parameter		Conditions	Min	Typ	Max	Unit
t_A	Aperture delay		0.6	0.8	1.2	ns
	Variation of aperture delay	Between two devices at the same temperature and DRVDD supply		±100		ps
t_J	Aperture jitter			100		f_S rms
	Wakeup time	Time to valid data after coming out of STANDBY mode		5	25	µs
		Time to valid data after coming out of PDN GLOBAL mode		100	500	µs
	ADC latency (4)	Low-latency mode (default after reset)		10		Clock cycles
		Low-latency mode disabled (gain enabled, offset correction disabled)		16		Clock cycles
		Low-latency mode disabled (gain and offset correction enabled)		17		Clock cycles
DDR LVDS MODE (5)(6)						
t_{SU}	Data setup time (3)	Data valid (7) to zero-crossing of CLKOUTP (Sample Rate=250M)	0.75	1.2		ns
t_H	Data hold time (3)	Zero-crossing of CLKOUTP to data becoming invalid (7) (Sample Rate=250M)	0.35	0.7		ns
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over *1MSPS ≤ sampling frequency ≤ 250MSPS*	3.0	4.4	5.4	ns
	Variation of t_{PDI}	Between two devices at the same temperature and DRVDD supply		±0.6		ns

(1) Timing parameters are ensured by design and characterization but are not production tested.
(2) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground.
(3) R_{LOAD} is the differential load resistance between the LVDS output pair.
(4) At higher frequencies, t_{PDI} is greater than one clock period and overall latency = ADC latency + 1.
(5) Measurements are done with a transmission line of 100Ω characteristic impedance between the device and the load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(6) The LVDS timings are unchanged for low latency disabled and enabled.
(7) Data valid refers to a logic high of 1.26 V and a logic low of 0.54 V.

Timing Requirements: LVDS and CMOS Modes (continued)

All test conditions: AVDD = 1.8 V, DRVDD = 1.8 V, sampling frequency = 250 MSPS, sine wave input clock, C_{LOAD} = 5 pF (2), and R_{LOAD} = 100 Ω (3). Minimum and maximum values are across the full temperaturerange: TMIN = –40°C to TMAX = +85°C, AVDD = 1.8 V, and DRVDD = 1.7 V to 1.9 V, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
DDR LVDS MODE (continued)						
LVDS bit clock duty cycle		Duty cycle of differential clock, (CLKOUTP – CLKOUTM) *1MSPS ≤ sampling frequency ≤ 250MSPS*	49	54	56	%
t_{RISE}, t_{FALL}	Data rise time, Data fall time	Rise time measured from –100mV to +100mV Fall time measured from +100mV to –100mV *1MSPS ≤ sampling frequency ≤ 250MSPS*		0.07		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from – 100mV to +100mV Fall time measured from +100mV to – 100mV *1MSPS ≤ sampling frequency ≤ 250MSPS*		0.14		ns
t_{OE}	Output enable (OE) to data delay	Time to valid data after OE becomes active		60	100	ns
Parallel CMOS MODE (8)(9)						
t_{START}	Input clock to data delay	Input clock rising edge cross-over to start of data valid (10)			3.2	ns
t_{DV} Data valid time		Time interval of valid data (10)	2.5	3.7		ns
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over *1MSPS ≤ sampling frequency ≤ 200MSPS*	3.7	5.5	7.6	ns
Output clock duty cycle		Duty cycle of output clock, CLKOUT *1MSPS ≤ sampling frequency ≤ 200MSPS*	49	53	56	%
t_{RISE}, t_{FALL}	Data rise time, Data fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD *1 ≤ sampling frequency ≤ 250MSPS*		0.21		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD *1 ≤ sampling frequency ≤ 200MSPS*		0.35		ns
t_{OE}	Output enable (OE) to data delay	Time to valid data after OE becomes active		20	40	ns

(8) For f_S > 200MSPS, it is recommended to use an external clock for data capture instead of the device output clock signal (CLKOUT).

(9) Low latency mode enabled.

(10) Data valid refers to a logic high of 1.26 V and a logic low of 0.54 V.

Table 3. LVDS Timing Across Sampling Frequencies

Sampling Frequency (MSPS)	Setup Time (ns)			Hold Time (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX
230	0.8	1.5		0.35	0.6	
200	1.1	1.8		0.35	0.6	
185	1.3	2.0		0.35	0.6	
160	1.6	2.4		0.35	0.6	
125	2.2	3.3		0.35	0.6	
80	3.9	5.5		0.35	0.6	

Table 4. CMOS Timing Across Sampling Frequencies (Low Latency Enabled)

Sampling Frequency (MSPS)	Timing Specified with Respect to Output Clock								
	t_{SETUP} (ns)			t_{HOLD} (ns)			t_{PDI} (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
200	1.6	2.3		1.3	2.6		3.7	4.5	7.6
185	1.8	2.5		1.4	2.7		3.7	4.5	7.6
160	2.1	3.0		1.6	3.2		3.7	4.5	7.6
125	2.5	3.5		2.4	4.4		3.7	4.5	7.6
80	4.4	6.0		4	6.4		3.7	4.5	7.6

Table 5. CMOS Timing Across Sampling Frequencies (Low Latency Disabled)

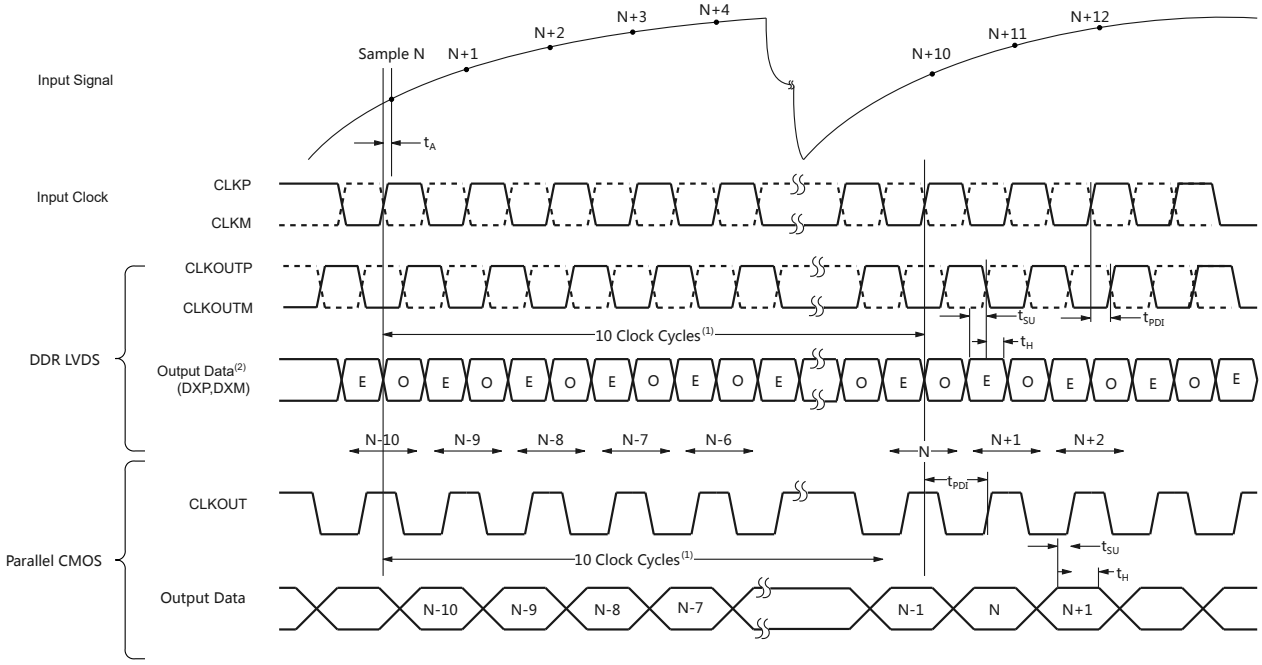
Sampling Frequency (MSPS)	Timing Specified with Respect to Output Clock								
	t_{SETUP} (ns)			t_{HOLD} (ns)			t_{PDI} (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
200	1.6	2.3		1.3	2.6		3.7	4.5	7.6
185	1.8	2.5		1.4	2.7		3.7	4.5	7.6
160	2.1	3.0		1.6	3.2		3.7	4.5	7.6
125	2.5	3.5		2.4	4.4		3.7	4.5	7.6
80	4.4	6.0		4	6.4		3.7	4.5	7.6

Table 6. CMOS Timing Across Sampling Frequencies (Low Latency Enabled)

Sampling Frequency (MSPS)	Timing Specified with Respect to Input Clock					
	t_{START} (ns)			t_{DV} (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX
250			3.2	2.5	3.7	
230			3.0	2.7	4.0	
200			2.6	3.2	4.6	
185			-0.4	3.5	5.0	
170			-1.3	3.9	5.6	

Table 7. CMOS Timing Across Sampling Frequencies (Low Latency Disabled)

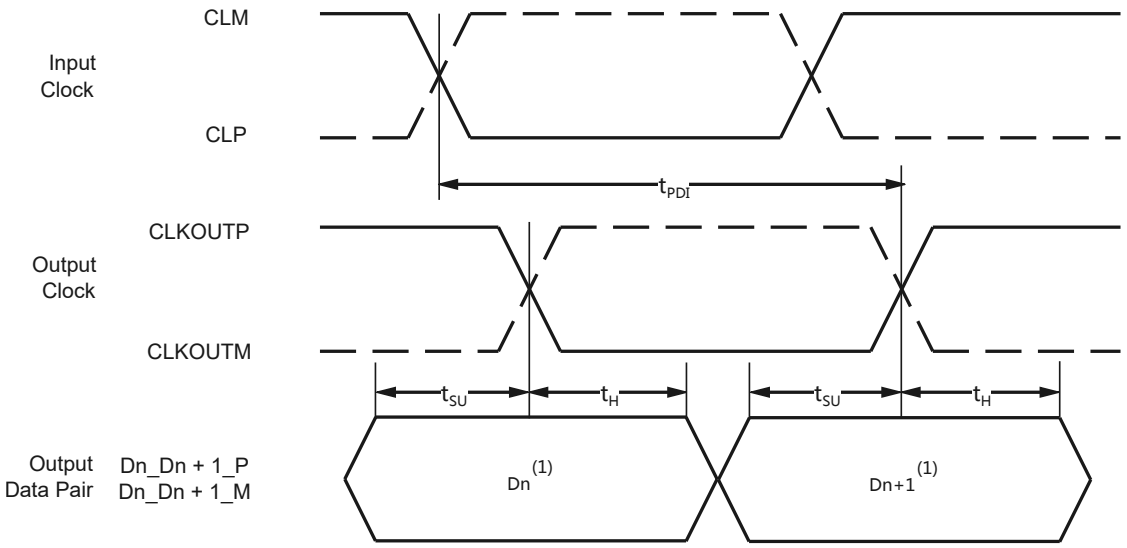
Sampling Frequency (MSPS)	Timing Specified with Respect to Input Clock					
	t_{START} (ns)			t_{DV} (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX
250			3.2	2.5	3.7	
230			3.0	2.7	4.0	
200			2.6	3.2	4.6	
185			-0.4	3.5	5.0	
170			-1.3	3.9	5.6	



(1) ADC latency in low-latency mode. At higher sampling frequencies, tDPI is greater than one clock cycle which then makes the overall latency = ADC latency + 1.

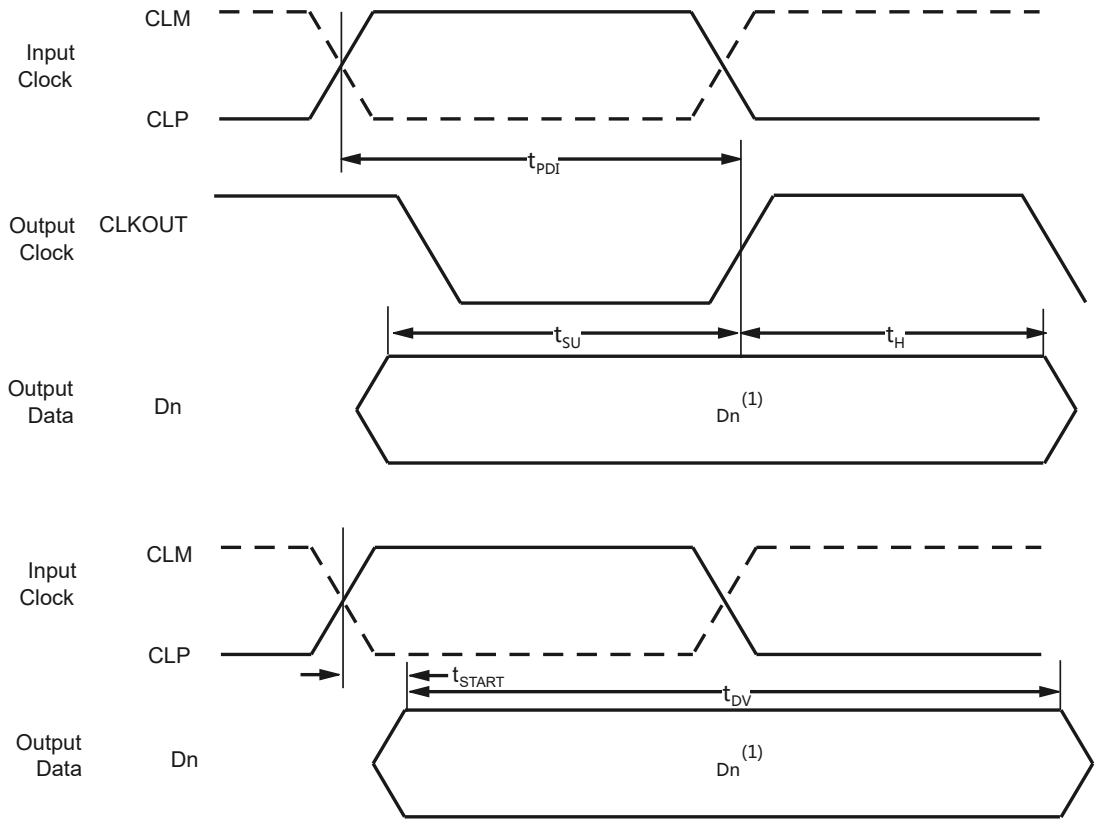
(2) E = Even bits (D0, D2, D4, etc). O = Odd bits (D1, D3, D5, etc).

Figure 3. Latency Diagram



(1) Dn = bits D0, D2, D4, etc. Dn + 1 = Bits D1, D3, D5, etc.

Figure 4. LVDS Mode Timing



(1) Dn = bits D0, D1, D2, etc.

Figure 5. CMOS Mode Timing

Typical Performance Characteristics

All test conditions: At +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5VPP differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, 1dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT. Note that after reset, the device is in 0dB gain mode, unless otherwise noted

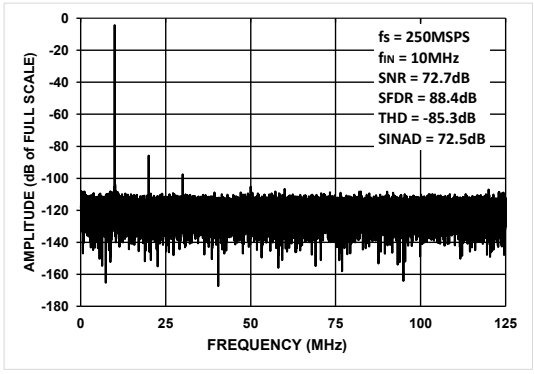


Figure 6. FFT(10 MHz)

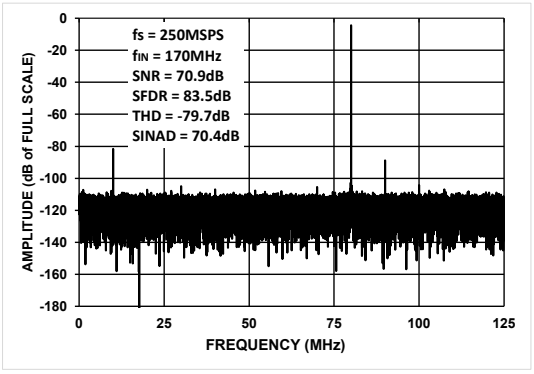


Figure 7. FFT(170 MHz)

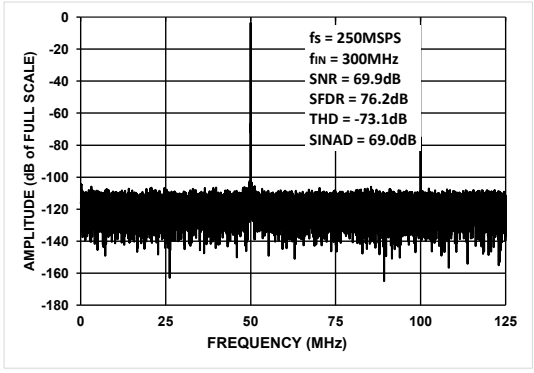


Figure 8. FFT(300 MHz)

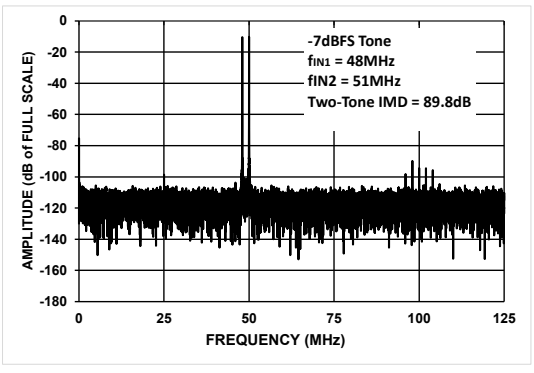


Figure 9. FFT (TWO-TONE)

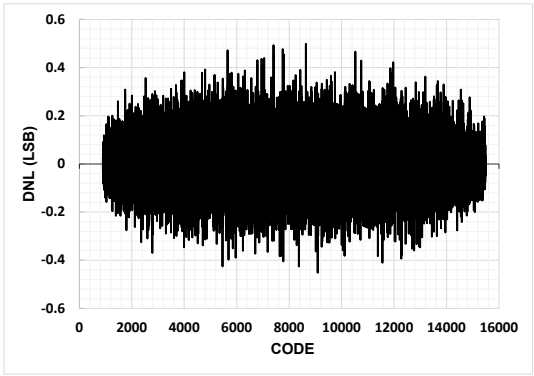


Figure 10. DNL

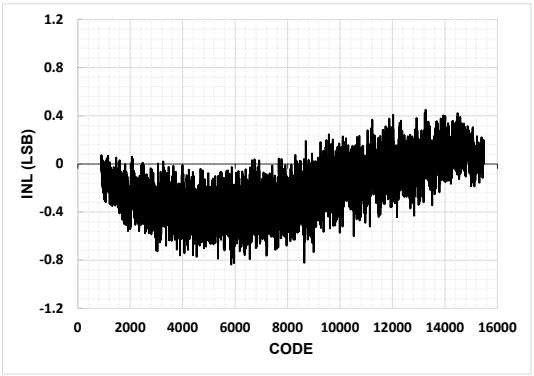


Figure 11. INL

Detailed Description

Functional Block Diagram

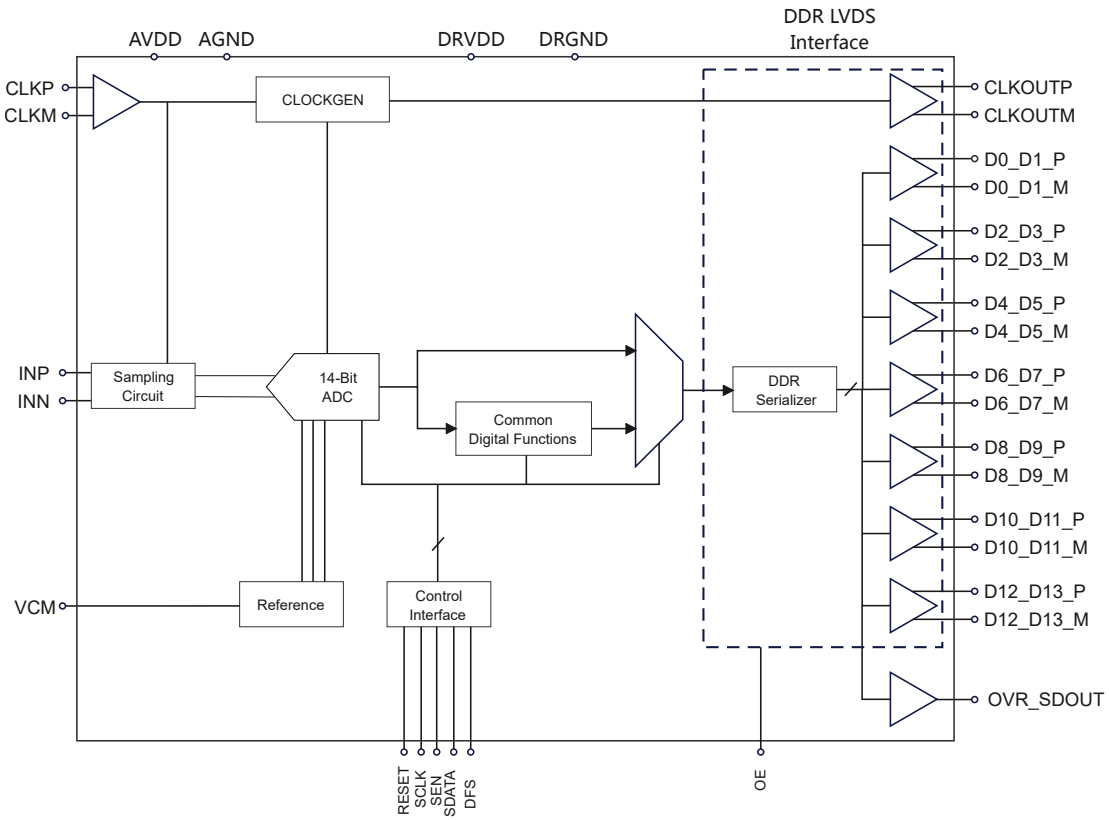


Figure 12. TPC703120 Block Diagram

Device Configuration

The TPC703120 has several modes that can be configured using a serial programming interface, as described in Table 8, Table 9, and Table 10. In addition, the devices have two dedicated parallel pins for quickly configuring commonly used functions. The parallel pins are DFS (analog 4-level control pin) and OE (digital control pin). The analog control pins can be easily configured using a simple resistor divider (with 10% tolerance resistors).

Table 8. DFS: Analog Control Pin

Voltage Applied On DFS	Description (Data Format/Output Interface)
0, +100mV/–0mV	Twos complement/DDR LVDS
(3/8) AVDD ± 100mV	Twos complement/parallel CMOS
(5/8) AVDD ± 100mV	Offset binary/parallel CMOS
AVDD, +0mV/– 100mV	Offset binary/DDR LVDS

Table 9. OE: Digital Control Pin

Voltage Applied On OE	Description
0	Output data buffers disabled
AVDD	Output data buffers enabled

When the serial interface is not used, the SDATA pin can also be used as a digital control pin to place the device in standby mode. To enable this, the RESET pin must be tied high. In this mode, SEN and SCLK do not have any alternative functions. Keep SEN tied high and SCLK tied low on the board.

Table 10. SDATA: Digital Control Pin

Voltage Applied On SDATA	Description
0	Normal operation
Logic high	Device enters standby

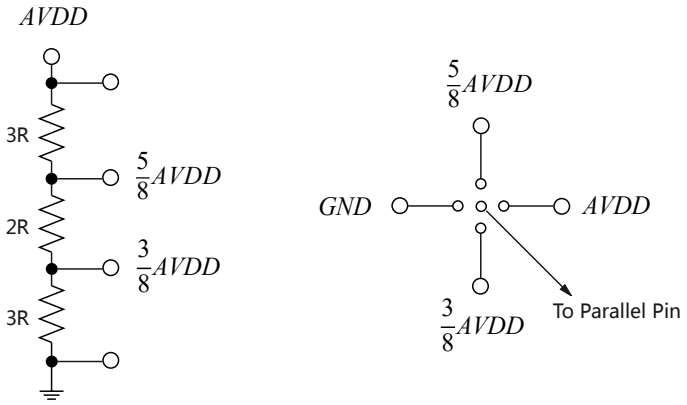
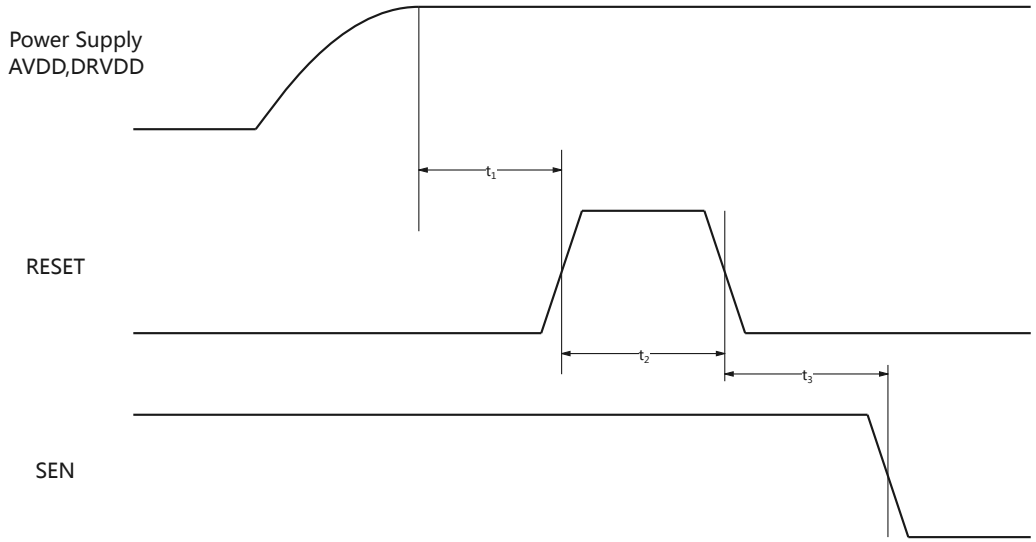


Figure 13. Simplified Diagram to Configure DFS Pin

Reset Timing Characteristics



Note: A high pulse on the RESET pin is required in the serial interface mode in case of initialization through hardware reset. For parallel interface operation, RESET must be permanently tied high.

Figure 14. Reset Timing Diagram

Reset Timing Requirements (1)

All test conditions: at +25°C and minimum and maximum values across the full temperature range: TMIN = –40°C to TMAX = +85°C, unless otherwise noted.

Parameter		Test Conditions	Min	Typ	Max	Unit
t_1	Power-on delay	Delay from power-up of AVDD and DRVDD to RESET pulse active	1			ms
t_2	Reset pulse width	Pulse width of the active RESET signal that resets the serial registers	10			ns
					1 (2)	µs
t_3		Delay from RESET disable to SEN active	100			ns

(1) Timing parameters are ensured by design and characterization but are not production tested.
(2) The reset pulse is needed only when using the serial interface configuration. If the pulse width is greater than 1 µs, the device can enter the parallel configuration mode briefly and then return back to serial interface mode.

Register Summary

The analog-to-digital converter (ADC) has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), and SDATA (serial interface data) pins. Serial shift of bits

into the device is enabled when SEN is low. Serial data SDATA are latched at every falling edge of SCLK when SEN is active (low). The serial data are loaded into the register at every 16th SCLK falling edge when SEN is low. In case the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse. The first eight bits form the register address and the remaining eight bits are the register data. The interface can work with SCLK frequency from 20MHz down to very low speeds (a few Hertz) and also with non-50% SCLK duty cycle.

Register Initialization

After power-up, the internal registers must be initialized to the default values. This initialization can be accomplished in one of two ways:

1. Either through a hardware reset by applying a high pulse on the RESET pin (of width greater than 10 ns)
2. By applying a software reset. When using the serial interface, set the RESET bit (D7 in register 00h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

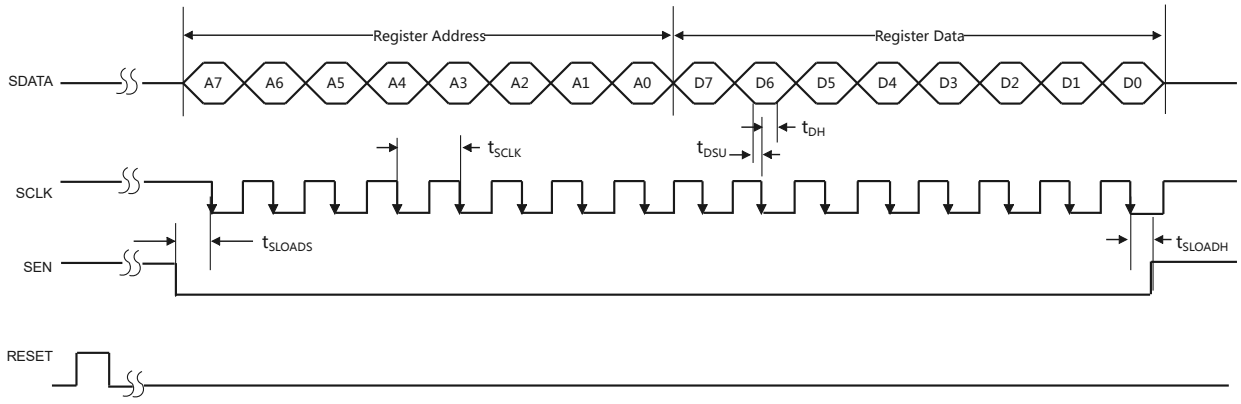


Figure 15. Serial Interface Timing

Serial Interface Timing Characteristics

All test conditions: at +25°C, minimum and maximum values across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C,AVDD = 1.8 V, and DRVDD = 1.8 V, unless otherwise noted.

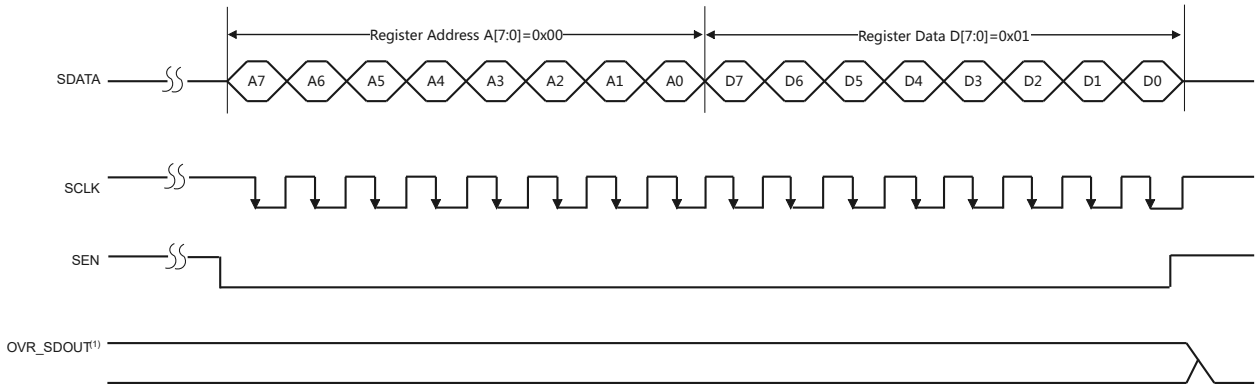
Parameter		Min	Typ	Max	Unit
f_{SCLK}	SCLK frequency (equal to 1/t_{SCLK})	> dc		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DSU}	SDATA setup time	25			ns
t_{DH}	SDATA hold time	25			ns

Serial Register Readout

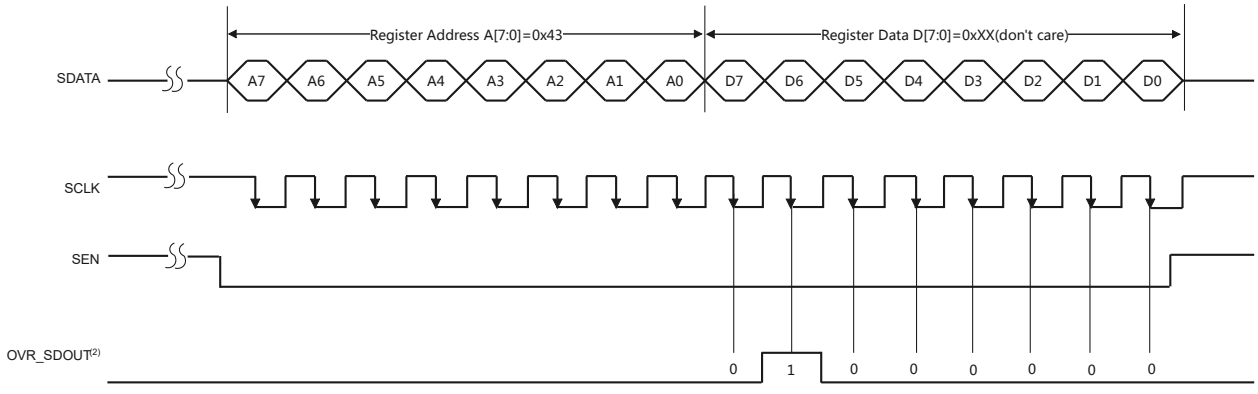
The serial register readout function allows the contents of the internal registers to be read back on the OVR_SDOUT pin. This readback may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

After power-up and device reset, the OVR_SDOUT pin functions as an over-range indicator pin by default. When the readout mode is enabled, OVR_SDOUT outputs the contents of the selected register serially:

1. Set the READOUT register bit to '1'. This setting puts the device in serial readout mode and disables any further writes to the internal registers **except** the register at address 0. Note that the READOUT bit itself is also located in register 0. The device can exit readout mode by writing READOUT = 0. Only the contents of the register at address 0 cannot be read in the register readout mode.
2. Initiate a serial interface cycle specifying the address of the register (A7 to A0) whose content has to be read.
3. The device serially outputs the contents (D7 to D0) of the selected register on the OVR_SDOUT pin.
4. The external controller can latch the contents at the falling edge of SCLK.
5. To exit the serial readout mode, the reset register bit READOUT = 0 enables writes into all registers of the device. At this point, the OVR_SDOUT pin becomes an over-range indicator pin.



a) Enable Serial Readout (READOUT = 1)



b) Read Contents of Register 0x43. This Register Has Been Initialized with 0x40 (device is put in global power-down mode).

(1) The OVR_SDOUT pin functions as OVR (READOUT = 0).
(2) The OVR_SDOUT pin functions as a serial readout (READOUT = 1).

Serial Register Map

Summarizes the functions supported by the serial interface.

Register Address	Default Value After Reset	Register Data							
A[7:0] (Hex)	D[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
00	00	0	0	0	0	0	0	RESET	READOUT
01	00	LVDS SWING						0	0
03	00	0	0	0	0	0	0	HIGH PERF MODE 1	
25	00	GAIN				DISABLE GAIN	TEST PATTERNS		
26	00	0	0	0	0	0	0	LVDS CLKOUT STRENGTH	LVDS DATA STRENGTH
3D	00	DATA FORMAT		EN OFFSET CORR	0	0	0	0	0
3F	00	CUSTOM PATTERN HIGH D[13:6]							
40	00	CUSTOM PATTERN D[5:0]						0	0
41	00	LVDS CMOS		CMOS CLKOUT STRENGTH		EN CLKOUT RISE	CLKOUT RISE POSN		EN CLKOUT FALL
42	00	CLKOUT FALL POSN		0	0	DIS LOW LATENCY	STBY	0	0
43	00	0	PDN GLOBAL	0	PDN OBUF	0	0	EN LVDS SWING	
BF	00	OFFSET PEDESTAL						0	0
CF	00	FREEZE OFFSET CORR	0	OFFSET CORR TIME CONSTANT				0	0
DF	00	0	0	LOW SPEED		0	0	0	0

Description of Serial Registers

For best performance, two special mode register bits must be enabled: HI PERF MODE 1

Table 11. Register Address 00h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	RESET	READOUT

Bits[7:2] **Always write '0'**

Bit 1 **RESET: Software reset applied**

This bit resets all internal registers to the default values and self-clears to 0 (default = 1).

Bit 0 **READOUT: Serial readout**

This bit sets the serial readout of the registers.

0 = Serial readout of registers disabled; the OVR_SDOUT pin functions as an over-voltage indicator.

1 = Serial readout enabled; the OVR_SDOUT pin functions as a serial data readout.

Table 12. Register Address 01h (Default = 00h)

7	6	5	4	3	2	1	0
LVDS SWING						0	0

Bits[7:2] **LVDS SWING: LVDS swing programmability (1)**
000000 = Default LVDS swing; ±350mV with external 100Ω termination
011011 = LVDS swing increases to ±410mV
110010 = LVDS swing increases to ±465mV
010100 = LVDS swing increases to ±570mV
111110 = LVDS swing decreases to ±200mV
001111 = LVDS swing decreases to ±125mV

Bits[1:0] **Always write '0'**

(1) The EN LVDS SWING register bits must be set to enable LVDS swing control.

Table 13. Register Address 03h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HI PERF MODE 1	

Bits[7:2] **Always write '0'**

Bits[1:0] **HI PERF MODE 1: High performance mode 1**
00 = Default performance after reset
01 = Do not use
10 = Do not use
11 = For best performance across sampling clock and input signal frequencies, set the HIGH PERF MODE 1 bits

Table 14. Register Address 25h (Default = 00h)

7	6	5	4	3	2	1	0
GAIN				DISABLE GAIN	TEST PATTERNS		

Bits[7:4] **GAIN: Gain programmability**
These bits set the gain programmability in 0.5dB steps.

0000 = 0dB gain (default after reset)
0001 = 0.5dB gain
0010 = 1.0dB gain
0011 = 1.5dB gain
0100 = 2.0dB gain
0101 = 2.5dB gain
0110 = 3.0dB gain
0111 = 3.5dB gain
1000 = 4.0dB gain
1001 = 4.5dB gain
1010 = 5.0dB gain
1011 = 5.5dB gain
1100 = 6.0dB gain

Bit 3 **DISABLE GAIN: Gain setting**
This bit sets the gain.

0 = Gain enabled; gain is set by the GAIN bits only
if low-latency mode is disabled.
1 = Gain disabled

Bits[2:0] **TEST PATTERNS: Data capture**

These bits verify data capture.
000 = Normal operation
001 = Outputs all 0s
010 = Outputs all 1s
011 = Outputs toggle pattern
In the TPC7031, output data D[13:0] is an alternating sequence of *01010101010101* and *10101010101010*.
In the TPC7021, output data D[11:0] is an alternating sequence of *010101010101* and *101010101010*.
100 = Outputs digital ramp
In the TPC7031, output data increments by one LSB (14-bit) every clock cycle from code 0 to code 16383
In the TPC7021, output data increments by one LSB (12-bit) every clock cycle from code 0 to code 4095
101 = Output custom pattern (use registers 3Fh and 40h for setting the custom pattern)
110 = Unused
111 = Unused

Table 15. Register Address 26h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LVDS CLKOUT STRENGTH	LVDS DATA STRENGTH

Bits[7:2] **Always write '0'**

Bit 1 **LVDS CLKOUT STRENGTH: LVDS output clock buffer strength**

This bit determines the external termination to be used with the LVDS output clock buffer.
0 = 100Ω external termination (default strength)
1 = 50Ω external termination (2x strength)

Bit 0 **LVDS DATA STRENGTH: LVDS data buffer strength**

This bit determines the external termination to be used with all of the LVDS data buffers.
0 = 100Ω external termination (default strength)
1 = 50Ω external termination (2x strength)

Table 16. Register Address 3Dh (Default = 00h)

7	6	5	4	3	2	1	0
DATA FORMAT		EN OFFSET CORR	0	0	0	0	0

Bits[7:6] **DATA FORMAT: Data format selection**

These bits selects the data format.
00 = The DFS pin controls data format selection
10 = Twos complement
11 = Offset binary

Bit 5 **ENABLE OFFSET CORR: Offset correction setting**

This bit sets the offset correction.

0 = Offset correction disabled

1 = Offset correction enabled

Bits[4:0] **Always write '0'**

Table 17. Register Address 3Fh (Default = 00h)

7	6	5	4	3	2	1	0
CUSTOM PATTERN D13	CUSTOM PATTERN D12	CUSTOM PATTERN D11	CUSTOM PATTERN D10	CUSTOM PATTERN D9	CUSTOM PATTERN D8	CUSTOM PATTERN D7	CUSTOM PATTERN D6

Bits[7:0] **CUSTOM PATTERN**

These bits set the custom pattern.

Table 18. Register Address 40h (Default = 00h)

7	6	5	4	3	2	1	0
CUSTOM PATTERN D5	CUSTOM PATTERN D4	CUSTOM PATTERN D3	CUSTOM PATTERN D2	CUSTOM PATTERN D1	CUSTOM PATTERN D0	0	0

Bits[7:2] **CUSTOM PATTERN**

These bits set the custom pattern.

Bits[1:0] **Always write '0'**

Table 19. Register Address 41h (Default = 00h)

7	6	5	4	3	2	1	0
LVDS CMOS		CMOS CLKOUT STREGNTH		EN CLK RISE	CLKOUT RISE POSN		EN CLKOUT FALL

Bits[7:6] **LVDS CMOS: Interface selection**

These bits select the interface.

00 = The DFS pin controls the selection of either LVDS or CMOS interface

10 = The DFS pin controls the selection of either LVDS or CMOS interface

01 = DDR LVDS interface

11 = Parallel CMOS interface

Bits[5:4] **CMOS CLKOUT STRENGTH**

Controls strength of CMOS output clock only.

00 = Maximum strength (recommended and used for specified timings)

01 = Medium strength

10 = Low strength

11 = Very low strength

Bits 3 **ENABLE CLKOUT RISE**

0 = Disables control of output clock rising edge

1 = Enables control of output clock rising edge

Bits[2:1] **CLKOUT RISE POSN: CLKOUT rise control**

Controls position of output clock rising edge

LVDS interface:

00 = Default position (timings are specified in this condition)

01 = Setup reduces by 500ps, hold increases by 500ps

10 = Data transition is aligned with rising edge

11 = Setup reduces by 200ps, hold increases by 200ps

CMOS interface:

00 = Default position (timings are specified in this condition)

01 = Setup reduces by 100ps, hold increases by 100ps

10 = Setup reduces by 200ps, hold increases by 200ps

11 = Setup reduces by 1.5ns, hold increases by 1.5ns

Bit 0 **ENABLE CLKOUT FALL**

0 = Disables control of output clock fall edge

1 = Enables control of output clock fall edge

Table 20. Register Address 42h (Default = 00h)

7	6	5	4	3	2	1	0
CLKOUT FALL CTRL		0	0	DIS LOW LATENCY	STBY	0	0

Bits[7:6] **CLKOUT FALL CTRL**

Controls position of output clock falling edge

LVDS interface:

00 = Default position (timings are specified in this condition)

01 = Setup reduces by 400ps, hold increases by 400ps

10 = Data transition is aligned with rising edge

11 = Setup reduces by 200ps, hold increases by 200ps

CMOS interface:

00 = Default position (timings are specified in this condition)

01 = Falling edge is advanced by 100ps

10 = Falling edge is advanced by 200ps

11 = Falling edge is advanced by 1.5ns

Bits[5:4] **Always write '0'**

Bits 3 **DIS LOW LATENCY: Disable low latency**

This bit disables low-latency mode

0 = Low latency mode is enabled. Digital functions such as gain, test patterns and offset correction are disabled

1 = Low-latency mode is disabled. This setting enables the digital functions.

Bit 2 **STBY: Standby mode**

This bit sets the standby mode.

0 = Normal operation

1 = Only the ADC and output buffers are powered down; internal reference is active; wake-up time from standby is fast

Bits[1:0] **Always write '0'**

Table 21. Register Address 43h (Default = 00h)

7	6	5	4	3	2	1	0
0	PDN GLOBAL	0	PDN OBUF	0	0	EN LVDS SWING	

Bit 7 **Always write '0'**

Bit 6 **PDN GLOBAL: Power-down**
This bit sets the state of operation.
0 = Normal operation
1 = Total power down; the ADC, internal references, and output buffers are powered down; slow wake-up time.

Bit 5 **Always write '0'**

Bit 4 **PDN OBUF: Power-down output buffer**
This bit set the output data and clock pins.
0 = Output data and clock pins enabled
1 = Output data and clock pins powered down and put in high- impedance state

Bits[3:2] **Always write '0'**

Bits[1:0] **EN LVDS SWING: LVDS swing control**
00 = LVDS swing control using LVDS SWING register bits is disabled
01 = Do not use
10 = Do not use
11 = LVDS swing control using LVDS SWING register bits is enabled

Table 22. Register Address BFh (Default = 00h)

7	6	5	4	3	2	1	0
OFFSET PEDESTAL						0	0

Bits[7:2] **OFFSET PEDESTAL**
These bits set the offset pedestal.
When the offset correction is enabled, the final converged value after the offset is corrected is the ADC mid-code value. A pedestal can be added to the final converged value by programming these bits.

BITS VALUE	PEDESTAL
011111	31LSB
011110	30LSB
011101	29LSB
000000	0LSB
111111	– 1LSB
111110	–2LSB
100000	–32LSB

Bits[1:0] **Always write '0'**

Table 23. Register Address CFh (Default = 00h)

7	6	5	4	3	2	1	0
FREEZE OFFSET CORR	BYPASS OFFSET CORR	OFFSET CORR TIME CONSTANT				0	0

Bit 7 **FREEZE OFFSET CORR**

This bit sets the freeze offset correction.

0 = Estimation of offset correction is not frozen (bit EN OFFSET CORR must be set)

1 = Estimation of offset correction is frozen (bit EN OFFSET CORR must be set). When frozen, the last estimated value is used for offset correction every clock cycle.

Bit 6 **Always write '0'**

OFFSET CORR TIME CONSTANT

Bits[5:2] These bits set the offset correction time constant for the correction loop time constant in number of clock cycles.

value	TIME CONSTANT
0000	1M
0001	2M
0010	4M
0011	8M
0100	16M
0101	32M
0110	64M
0111	128M
1000	256M
1001	512M
1010	1G
1011	2G

Bits[1:0] **Always write '0'**

Bits[1:0] Always write '0'

Table 24. Register Address DFh (Default = 00h)

7	6	5	4	3	2	1	0
0	0	LOW SPEED			0	0	0

Bits[7:1] **Always write '0'**

Bit 0 **LOW SPEED: Low-speed mode**

00, 01, 10 = Low-speed mode disabled (default state after reset); this setting is recommended for sampling rates greater than 80MSPS.

11 = Low-speed mode enabled; this setting is recommended for sampling rates less than or equal to 80MSPS.

Digital Output Information

Digital Output Information

The TPC703120 provides either 14-bit data, respectively, and an output clock synchronized with the data.

Output Interface

Two output interface options are available: double data rate (DDR) LVDS and parallel CMOS. They can be selected using the LVDS CMOS serial interface register bit or using the DFS pin.

DDR LVDS Outputs

In this mode, the data bits and clock are output using low-voltage differential signal (LVDS) levels. Two data bits are multiplexed and output on each LVDS differential pair, as shown in Figure 16.

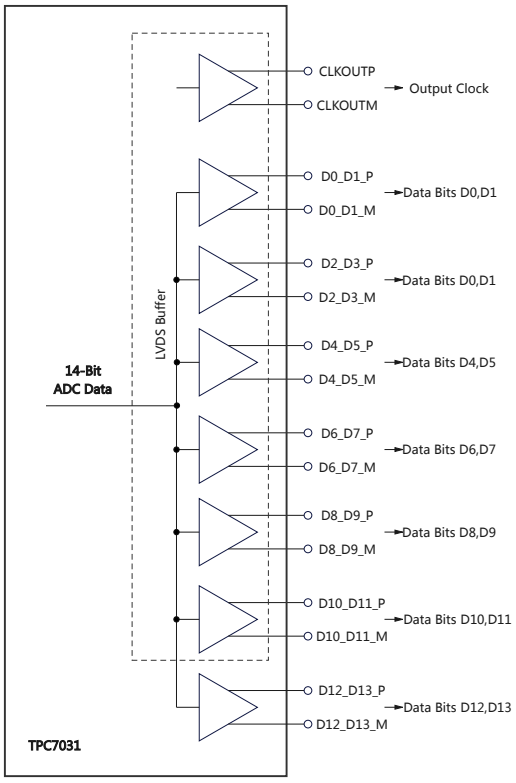


Figure 16. TPC703120 LVDS Data Outputs

Even data bits (D0, D2, D4, etc.) are output at the falling edge of CLKOUTP and the odd data bits (D1, D3, D5, etc.) are output at the rising edge of CLKOUTP. Both the rising and falling edges of CLKOUTP must be used to capture all 14 data bits, as shown in Figure 17.

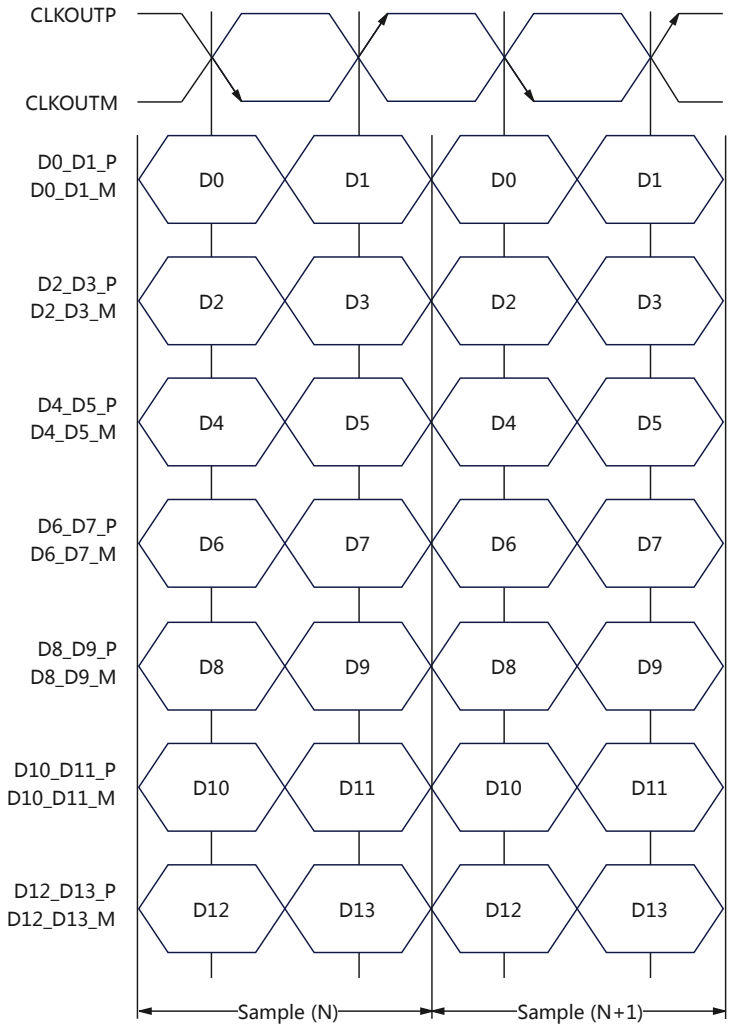


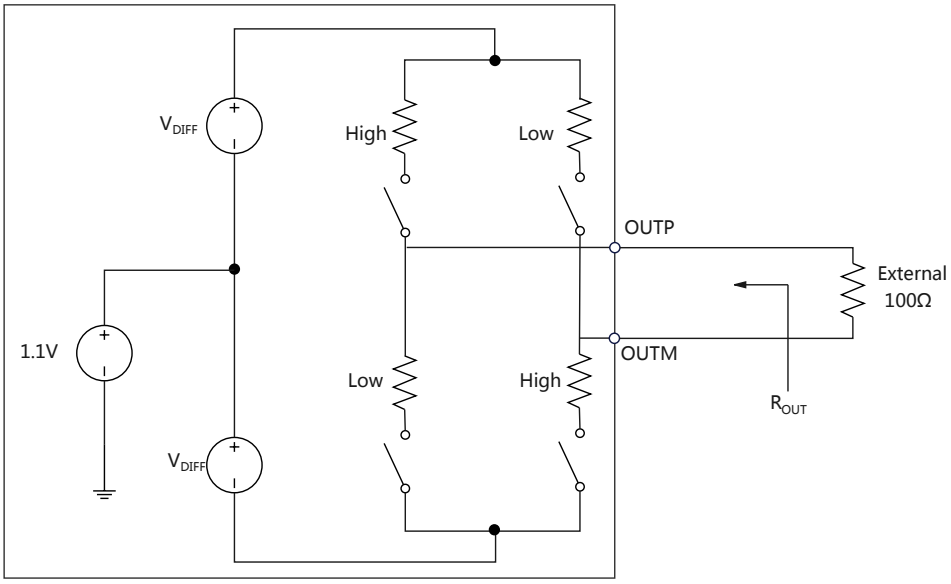
Figure 17. DDR LVDS Interface

LVDS Output Data and Clock Buffers

The equivalent circuit of each LVDS output buffer is shown in Figure 18. After reset, the buffer presents an output impedance of 100 Ω to match with the external 100 Ω termination.

The VDIFF voltage is nominally 350 mV, resulting in an output swing of ±350 mV with 100 Ω external termination. The VDIFF voltage is programmable using the LVDS SWING register bits from ±125 mV to ±570 mV.

Additionally, a mode exists to double the strength of the LVDS buffer to support 50 Ω differential termination. This mode can be used when the output LVDS signal is routed to two separate receiver chips, each using a 100 Ω termination. The mode can be enabled using the LVDS DATA STRENGTH and LVDS CLKOUT STRENGTH register bits for data and output clock buffers, respectively. The buffer output impedance behaves in the same way as a source-side series termination. By absorbing reflections from the receiver end, it helps to improve signal integrity.



NOTE: Use the default buffer strength to match 100 Ω external termination (ROUT = 100 Ω). To match with a 50 Ω external termination, set the LVDS STRENGTH bit (ROUT = 50 Ω).

Figure 18. LVDS Buffer Equivalent Circuit

Parallel CMOS Interface

In CMOS mode, each data bit is output on a separate pin as the CMOS voltage level, for every clock cycle. The rising edge of the output clock CLKOUT can be used to latch data in the receiver. Figure 19 depicts the CMOS output interface.

Switching noise (caused by CMOS output data transitions) can couple into the analog inputs and degrade SNR.The coupling and SNR degradation increases as the output buffer drive is made stronger. To minimize this degradation, the CMOS output buffers are designed with controlled drive strength. The default drive strengthensures a wide data stable window (even at 250MSPS) is provided so the data outputs have minimal loadcapacitance. It is recommended to use short traces (one to two inches or 2.54 cm to 5.08 cm) terminated with less than 5-pF load capacitance, as shown in Figure 20.

For sampling frequencies greater than 200 MSPS, it is recommended to use an external clock to capture data. The delay from input clock to output data and the data valid times are specified for higher sampling frequencies. These timings can be used to delay the input clock appropriately and use it to capture data.

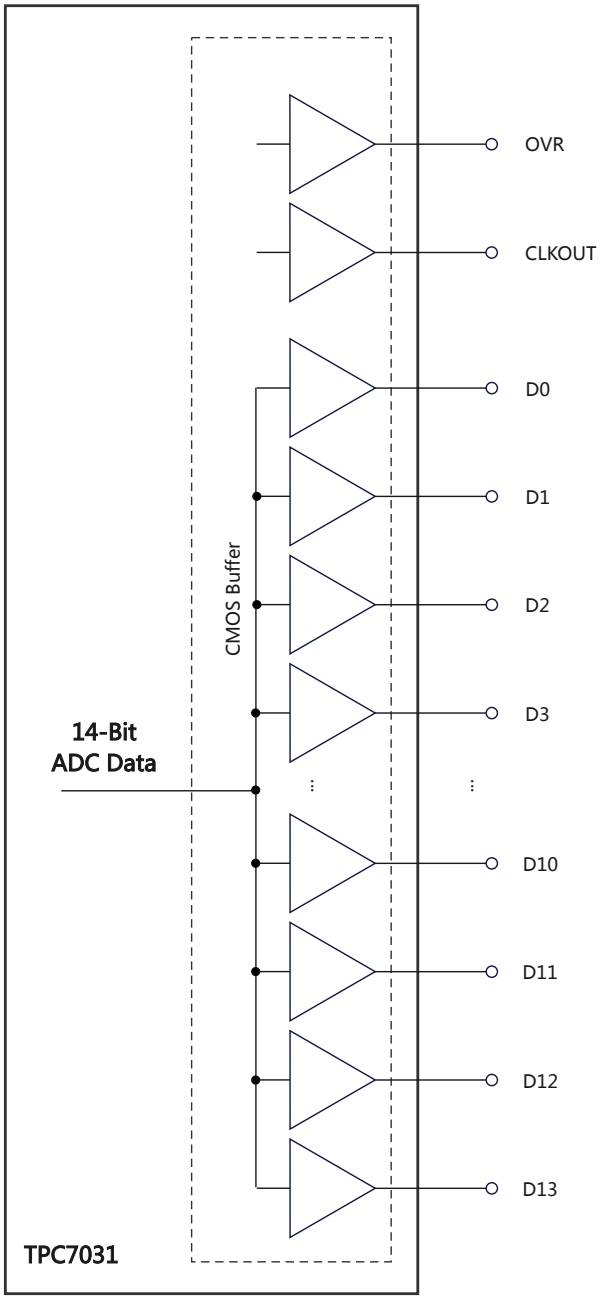


Figure 19. CMOS Output Interface

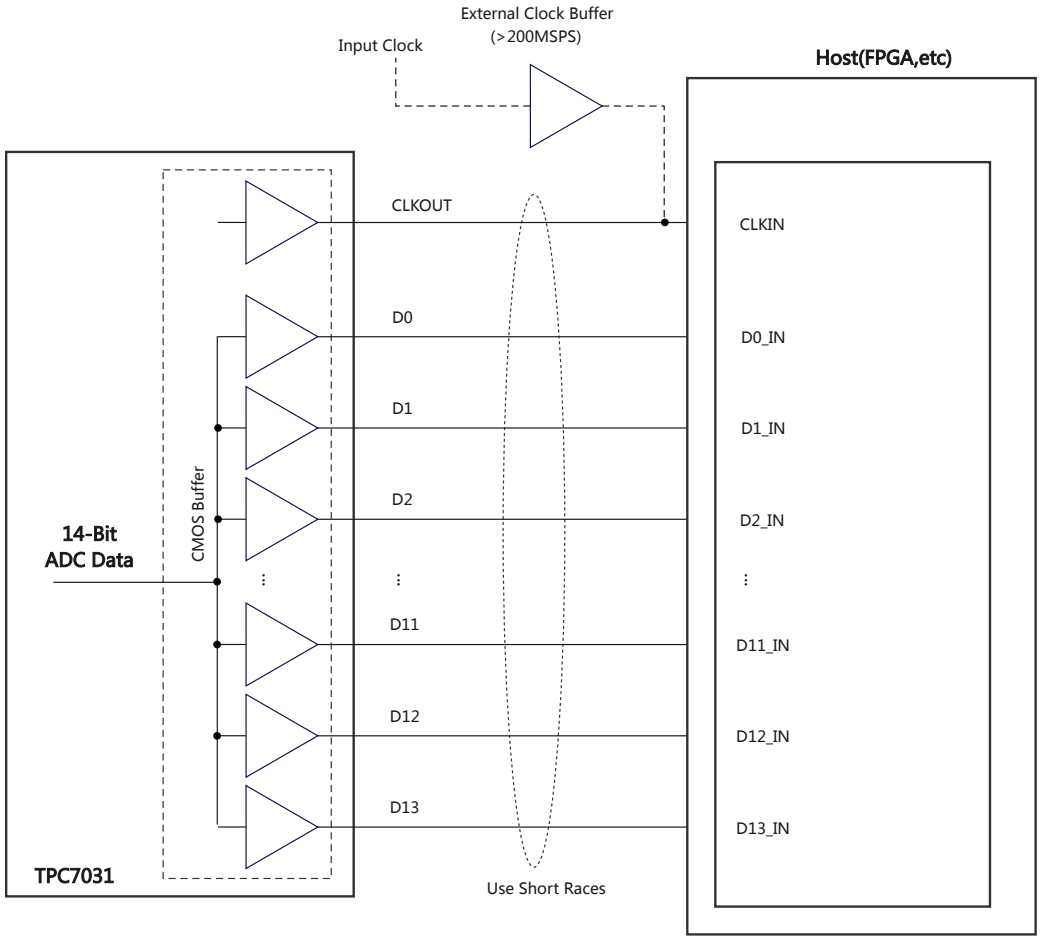


Figure 20. Using the CMOS Data Outputs

Input Over-Voltage Indication (OVR Pin)

The device features an OVR pin that provides information regarding analog input overload. At any clock cycle, if the sampled input voltage exceeds the positive or negative full-scale range, the OVR pin goes high. It remains high as long as the overload condition persists. The OVR pin is implemented as a CMOS output buffer, powered by the DRVDD supply, and operates independently of the output data interface type (DDR LVDS or CMOS).

For a positive overload, the D[13:0] output data bits are 3FFFh in offset binary output format and 1FFFh in twos complement output format. For a negative input overload, the output code is 0000h in offset binary output format and 2000h in twos complement output format.

Output Data Format

Two output data formats are supported: twos complement and offset binary. They can be selected using the DATA FORMAT serial interface register bit or controlling the DFS pin in parallel configuration mode. In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application information

Analog Inputs

The analog input consists of a switched-capacitor-based, differential, sample-and-hold architecture. This differential topology results in very good AC performance even for high input frequencies at high sampling rates. The INP and INM pins must be externally biased around a common-mode voltage of 0.95 V, available on the VCM pin. For a full-scale differential input, each input INP and INM pin must swing symmetrically between (VCM + 0.5 V) and (VCM – 0.5 V), resulting in a 2VPP differential input swing. The input sampling circuit has a high 3dB bandwidth that extends up to 550 MHz (measured from the input pins to the sampled voltage).

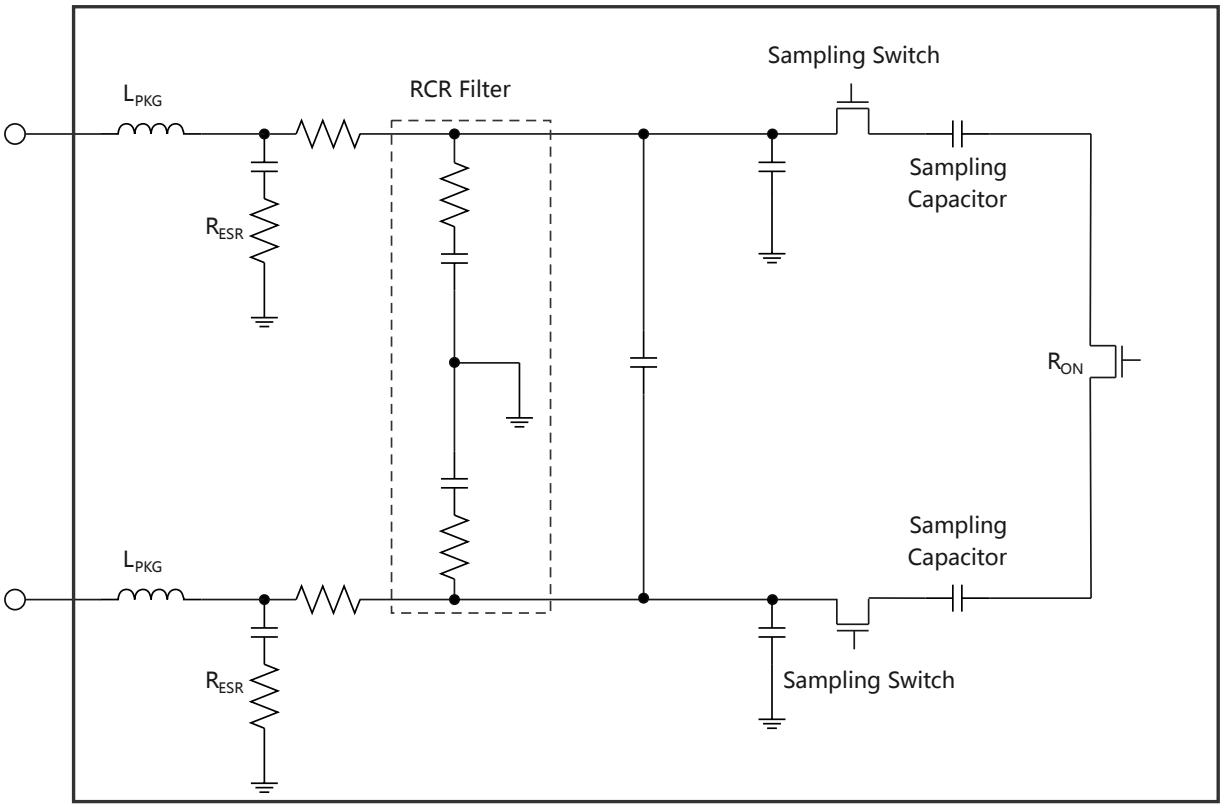


Figure 21. Analog Input Equivalent Circuit

Driving Circuit

Two example driving circuit configurations are shown in Figure 22 and Figure 23 —one optimized for low bandwidth and the other one for high bandwidth to support higher input frequencies. In Figure 22, an external R-C-R filter with 3.3 pF is used to help absorb sampling glitches. The R-C-R filter limits the bandwidth of the drive circuit, making it suitable for low input frequencies (up to 250MHz). Transformers such as ADT1-1WT or WBC1-1 can be used up to 250 MHz.

For higher input frequencies, the R-C-R filter can be dropped. Together with the lower series resistors (5 Ω to 10 Ω), this drive circuit provides higher bandwidth to support frequencies up to 500 MHz. A transmission line transformer such as ADTL2-18 can be used.

Note that both the drive circuits have been terminated by 50 Ω near the ADC side. The termination is accomplished by a 25 Ω resistor from each input to the 0.95 V common-mode (VCM) from the device. This termination allows the analog inputs to be biased around the required common-mode voltage.

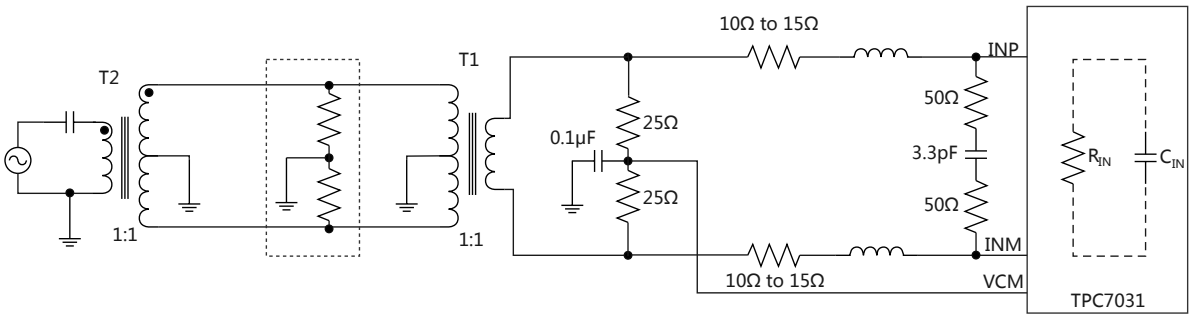


Figure 22. Drive Circuit with Low Bandwidth (for Low Input Frequencies)

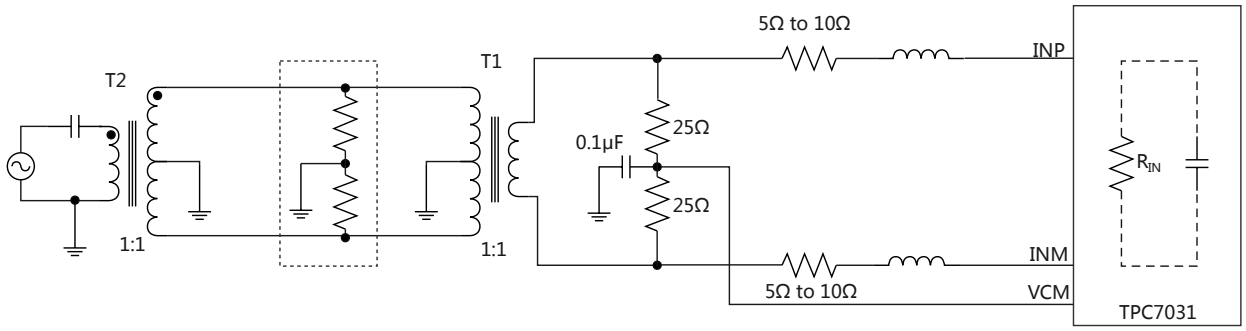


Figure 23. Drive Circuit with High Bandwidth (For High Input Frequencies)

Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This technique improves the common-mode noise immunity and even-order harmonic rejection. A 5 Ω to 15 Ω resistor in series with each input pin is recommended to damp out ringing caused by package parasitics. It is also necessary to present low impedance (less than 50 Ω) for the common-mode switching currents. This impedance can be achieved by using two resistors from each input terminated to the common-mode voltage (VCM).

Note that the device includes an internal R-C filter from each input to ground. The purpose of this filter is to absorb the glitches caused by the opening and closing of the sampling capacitors. The cutoff frequency of the R-C filter involves a trade-off. A lower cutoff frequency (larger C) absorbs glitches better, but also reduces the input bandwidth and the maximum input frequency that can be supported. On the other hand, with no internal R-C filter, high input frequency can be supported but now the sampling glitches must be supplied by the external driving circuit. The inductance of the package bond wires limits the ability of the external driving circuit to support the sampling glitches.

In the TPC703120, the R-C component values have been optimized while supporting high input bandwidth (550 MHz). However, in applications where very high input frequency support is not required, filtering of the glitches can be improved further with an external R-C-R filter;

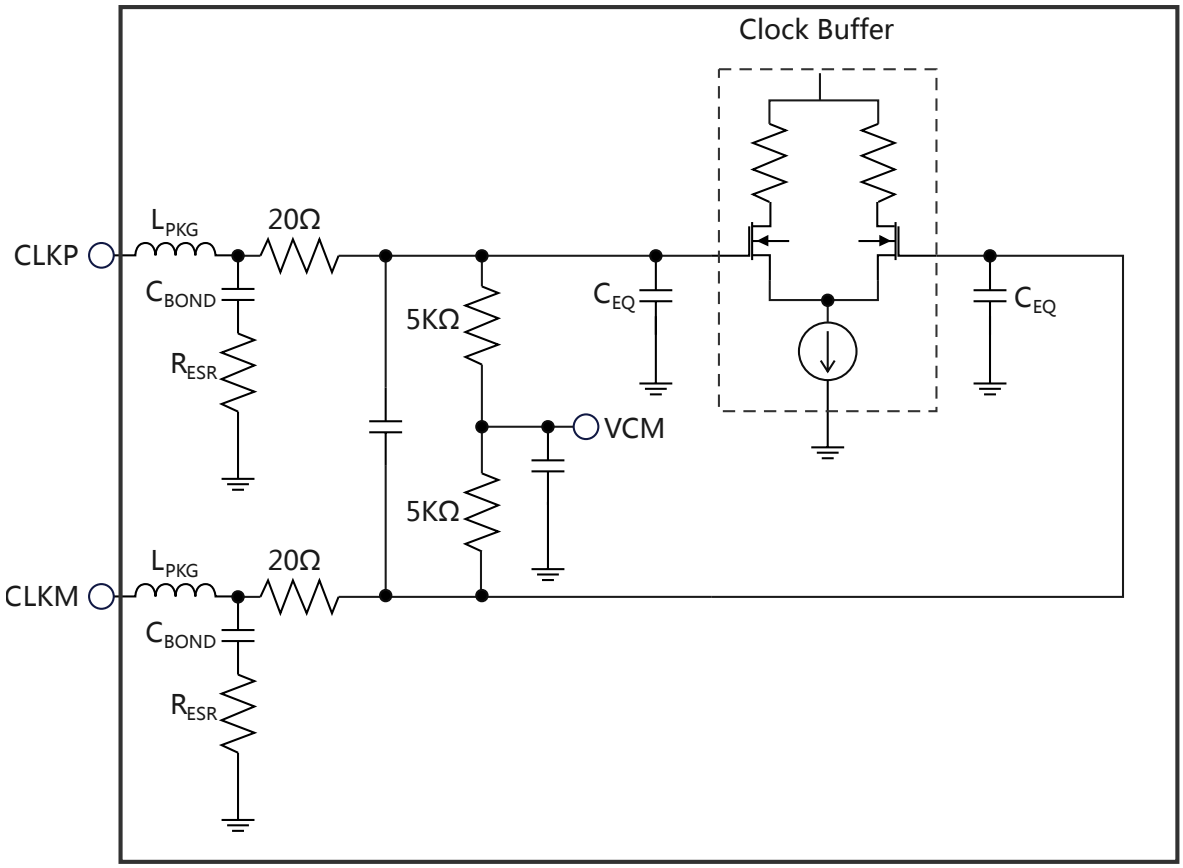
In addition, the drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched impedance to the source. While designing the drive circuit, the ADC impedance must be considered.

Input Common-Mode

To ensure a low-noise, common-mode reference, the VCM pin is filtered with a 0.1-µF low-inductance capacitor connected to ground. The VCM pin is designed to directly drive the ADC inputs. Each ADC input pin sinks a common-mode current of approximately 0.6 µA per MSPS of clock frequency.

Clock Input

The TPC703120 clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to VCM using internal 5-kΩ resistors. This setting allows the use of transformer-coupled drive circuits for sine-wave clock or ac-coupling for LVPECL and LVDS clock sources. Figure 24 shows an equivalent circuit for the input clock.



Note: C_{EQ} is 1 pF to 3 pF and is the equivalent input capacitance of the clock buffer.

Figure 24. Input Clock Equivalent Circuit

Single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-µF capacitor, as shown in Figure 25. For best performance, the clock inputs must be driven differentially, reducing susceptibility to common-mode noise. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input. Figure 26 shows a differential circuit.

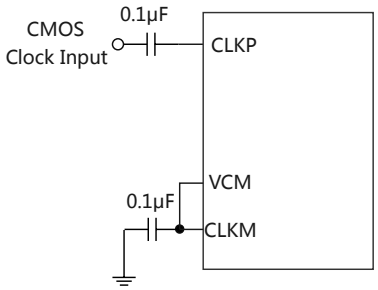


Figure 25. Single-Ended Clock Driving Circuit

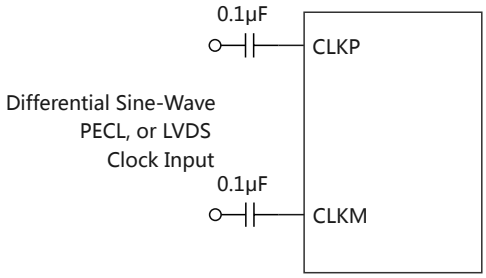


Figure 26. Differential Clock Driving Circuit

Digital Functions and Low Latency Mode

The device has several useful digital functions such as test patterns, gain, and offset correction. All of these functions require extra clock cycles for operation and increase the overall latency and power of the device. Alternately, the device has a low-latency mode in which the raw ADC output is routed to the output data pins with a latency of 10 clock cycles. In this mode, the digital functions are bypassed. Figure 27 shows more details of the processing after the ADC.

The device is in low-latency mode after reset. In order to use any of the digital functions, first the low-latency mode must be disabled by setting the DIS LOW LATENCY register bit to '1'. After this, the respective register bits must be programmed as described in the following sections and in the Serial Register Map section.

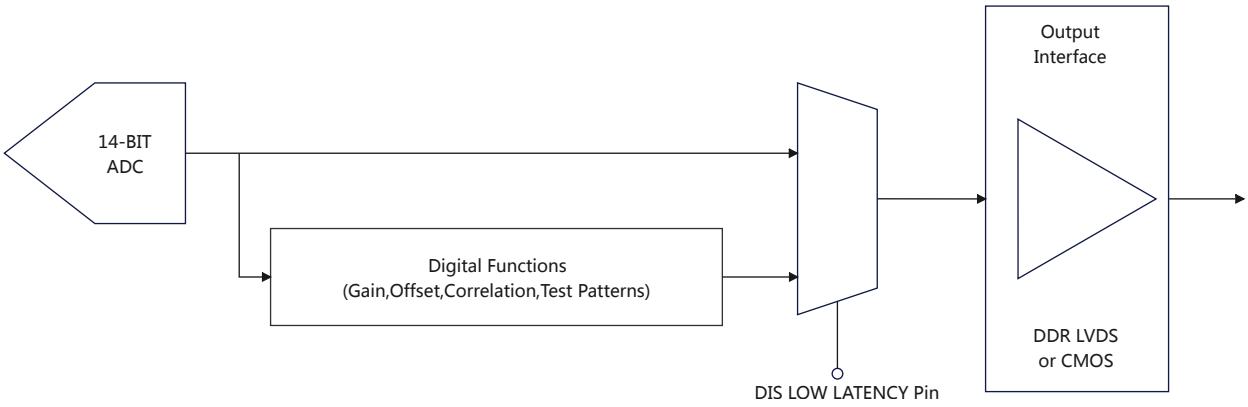


Figure 27. Digital Processing Block Diagram

Gain for SFDR/SNR Trade-Off

The TPC703120 includes gain settings that can be used to get improved SFDR performance. The gain is programmable from 0dB to 6dB (in 0.5 dB steps) using the GAIN register bits. For each gain setting, the analog input full-scale range scales proportionally, please refer to Table 25.

The SFDR improvement is achieved at the expense of SNR; for each gain setting, the SNR degrades approximately between 0.5 dB and 1 dB. The SNR degradation is reduced at high input frequencies. As a result, the gain is very useful at high

input frequencies because the SFDR improvement is significant with marginal degradation in SNR. Therefore, the gain can be used to trade-off between SFDR and SNR.

After a reset, the device is in low-latency mode and gain function is disabled. To use gain:

- First, disable the low-latency mode (DIS LOW LATENCY = 1).
- This setting enables the gain and puts the device in a 0 dB gain mode.
- For other gain settings, program the GAIN bits.

Table 25. Full-Scale Range Across Gains

Gain (dB)	Type	Full-Scale (VPP)
0	Default after reset	2
1	Programmable gain	1.78
2	Programmable gain	1.59
3	Programmable gain	1.42
4	Programmable gain	1.26
5	Programmable gain	1.12
6	Programmable gain	1.00

Offset Correction

The TPC703120 has an internal offset correction algorithm that estimates and corrects DC offset up to ±10 mV. The correction can be enabled using the EN OFFSET CORR serial register bit. Once enabled, the algorithm estimates the channel offset and applies the correction every clock cycle. The time constant of the correction loop is a function of the sampling clock frequency. The time constant can be controlled using the OFFSET CORR TIME CONSTANT register bits, refer to Table 26.

After the offset is estimated, the correction can be frozen by setting FREEZE OFFSET CORR = 1. Once frozen, the last estimated value is used for the offset correction of every clock cycle. Note that offset correction is disabled by default after reset.

After a reset, the device is in low-latency mode and offset correction is disabled. To use offset correction:

• First, disable the low-latency mode (DIS LOW LATENCY = 1).

• Then set EN OFFSET CORR to '1' and program the required time constant.

Table 26. Time Constant of Offset Correction Loop

Offset Corr Time Constant	Time Constant, TCCLK (Number of Clock Cycles)	Time Constant, TCCLK × 1/fS (sec)(1)
0000	1M	4 ms
0001	2M	8 ms
0010	4M	16.7 ms
0011	8M	33.5 ms
0100	16M	67 ms
0101	32M	134 ms
0110	64M	268 ms

Offset Corr Time Constant	Time Constant, TCCLK (Number of Clock Cycles)	Time Constant, TCCLK × 1/fS (sec)(1)
0111	128M	537 ms
1000	256M	1.1 s
1001	512M	2.15 s
1010	1G	4.3 s
1011	2G	8.6 s
1100	Reserved	—
1101	Reserved	
1110	Reserved	
1111	Reserved	—

Power Down

The TPC703120 has three power-down modes: power-down global, standby, and output buffer disable.

Power-Down Global

In this mode, the entire chip (including the ADC, internal reference, and the output buffers) is powered down, resulting in reduced total power dissipation of about 5 mW. The output buffers are in a high-impedance state. The wake-up time from the global power-down to data becoming valid in normal mode is typically 100μs. To enter the global power-down mode, set the PDN GLOBAL register bit.

Standby

In this mode, only the ADC is powered down and the internal references are active, resulting in a fast wake-up time of 5 μs. The total power dissipation in standby mode is approximately 80 mW. To enter the standby mode, set the STBY register bit.

Output Buffer Disable

The output buffers can be disabled and put in a high-impedance state; wakeup time from this mode is fast, approximately 100 ns. This can be controlled using the PDN OBUF register bit or using the OE pin.

Layout

Layout Guideline

Ground

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned.

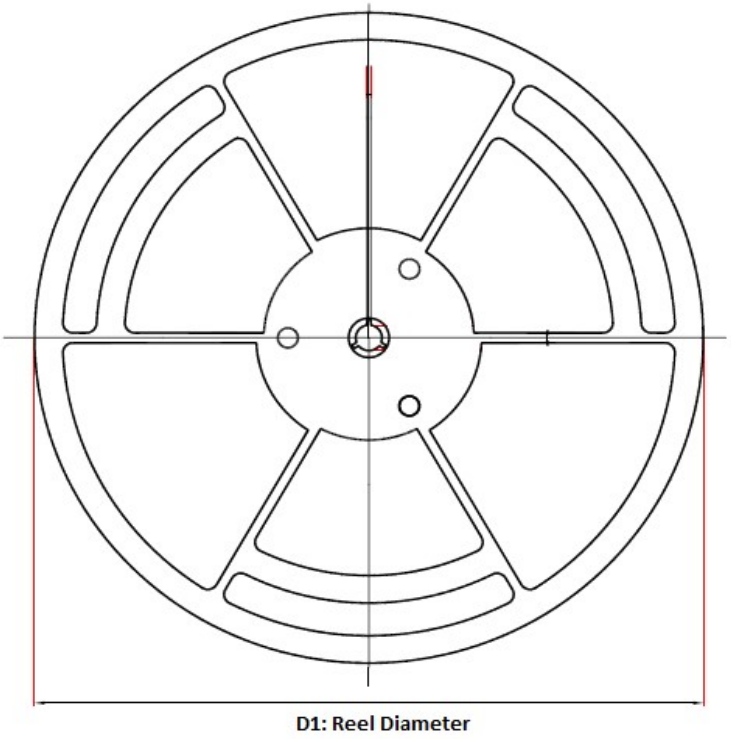
Power Supply Decoupling

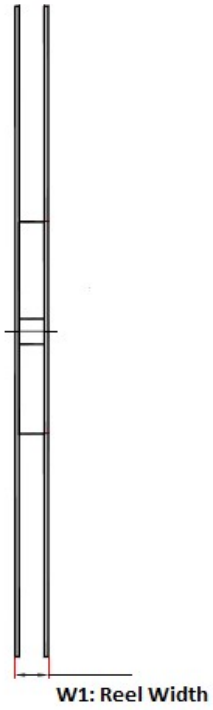
Decoupling capacitors can help filter external power-supply noise, so the optimum number of capacitors depends on the actual application. The decoupling capacitors should be placed very close to the converter supply pins.

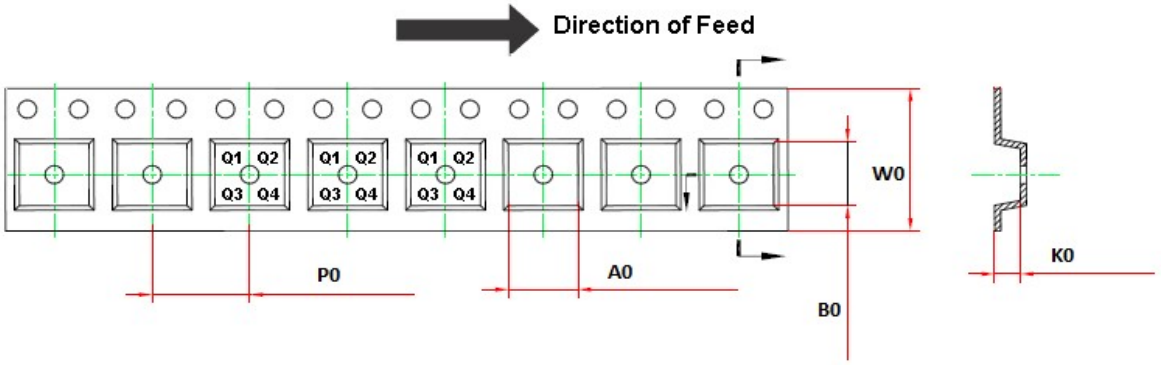
E-PAD

In addition to providing a path for heat dissipation, the Power PAD is also electrically internally connected to the digital ground. Therefore, it is necessary to solder the exposed pad to the ground plane for best thermal and electrical performance.

Tape and Reel Information





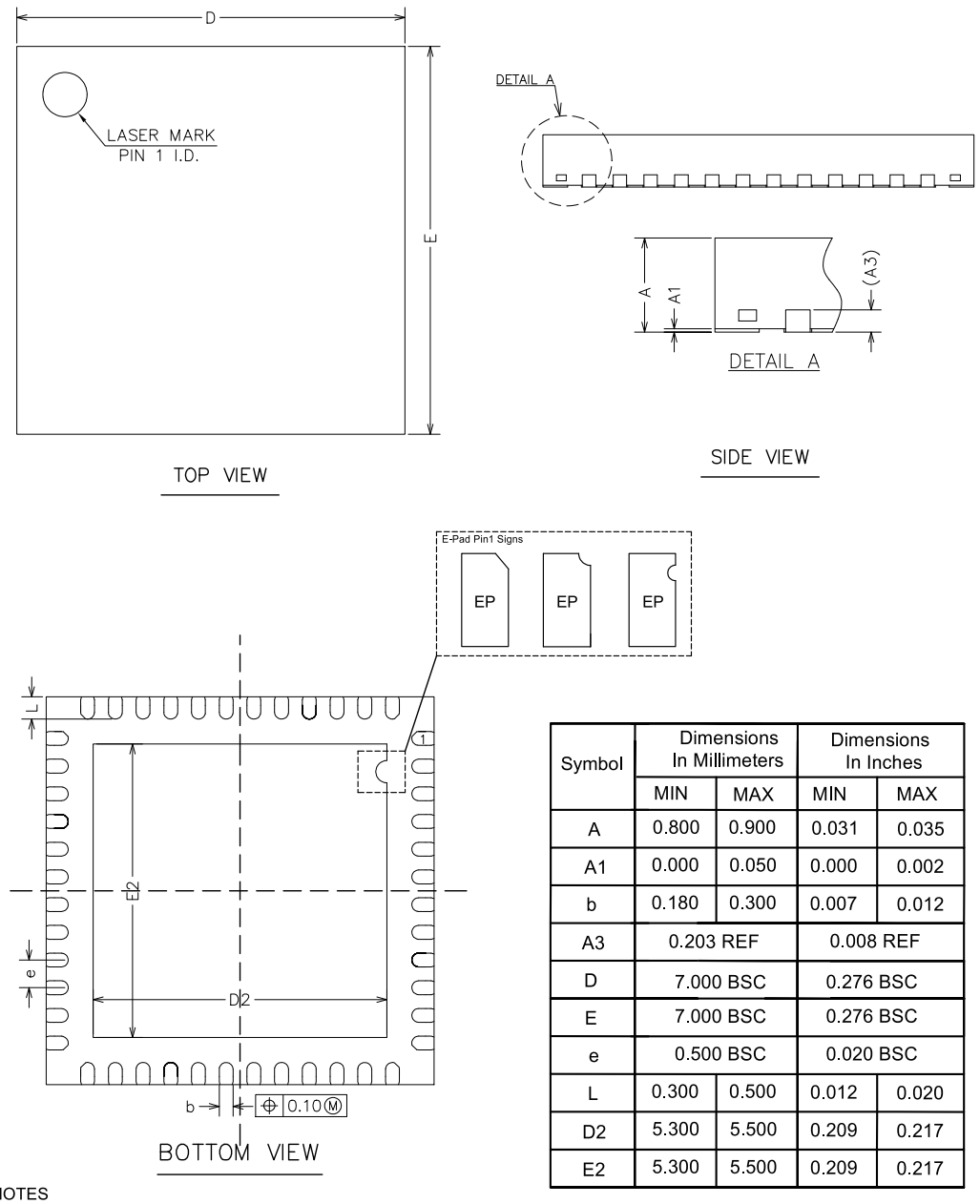


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPC703120-FE5R	QFN7X7-48	329	20.8	7.25	7.25	1.1	12	16	Q2

Package Outline Dimensions

QFN7X7-48

Package Outline Dimensions FE5(QFN7X7-48-G)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.031	0.035
A1	0.000	0.050	0.000	0.002
b	0.180	0.300	0.007	0.012
A3	0.203 REF		0.008 REF	
D	7.000 BSC		0.276 BSC	
E	7.000 BSC		0.276 BSC	
e	0.500 BSC		0.020 BSC	
L	0.300	0.500	0.012	0.020
D2	5.300	5.500	0.209	0.217
E2	5.300	5.500	0.209	0.217

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPC703120-FE5R	−40 to 85°C	QFN7X7-48	703120	3	T&R, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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