12-Channel, 8-kSPS, 16-Bit, Highly Integrated Sigma-Delta ADC

Features

- ADC Performance:
  - Analog Multiplexer with 6-full Differential or 12-single Ended Inputs
  - Programmable Gain: 1 to 128
  - Programmable Data Rates: 2.5 SPS to 8 kSPS
  - Digital Filter: Simultaneous 50-Hz and 60-Hz Rejection at ≤ 20 SPS with Low-Latency Digital Filter
- Integrated Functions:
  - Dual-Matched Programmable Current Sources for Sensor Excitation: 10 μA to 2000 μA
  - Internal Reference: 2.5 V
  - Internal Oscillator
  - Internal Temperature Sensor
  - Extended Fault Detection Circuits
  - Self-Offset and System Calibration
  - GPIO and GPO Pins with External Mux Control
- Digital Interface
  - 3-/4- wire SPI-Compatible Interface with CRC Checking
- Digital Supply: 2.7 V to 5 V
- Package: TQFP5x5-32
- Operating Temperature Range: −40°C to +125°C

Applications

- Process Control: PLC/DCS Modules
- Voltage, Current, Temperature, and Pressure Measurement Flow Meters
- Temperature Controllers
- Medical and Scientific Instrumentation

Description

The TPC62412 is a precision 12-channel, multiplexed ADC with integrated PGA and many other features, offering accurate measurement for low-bandwidth input signals, and lower-system cost and component count.

The device has a 16-bit delta-sigma converter, with configurable data rates. There is a sinc5 filter for optimized noise performance, and low-latency filter for fast settling with 50-/60-Hz rejection for noisy industrial environments.

A low-noise programmable gain amplifier provides 1 to 128 gain options to amplify low-level signals.

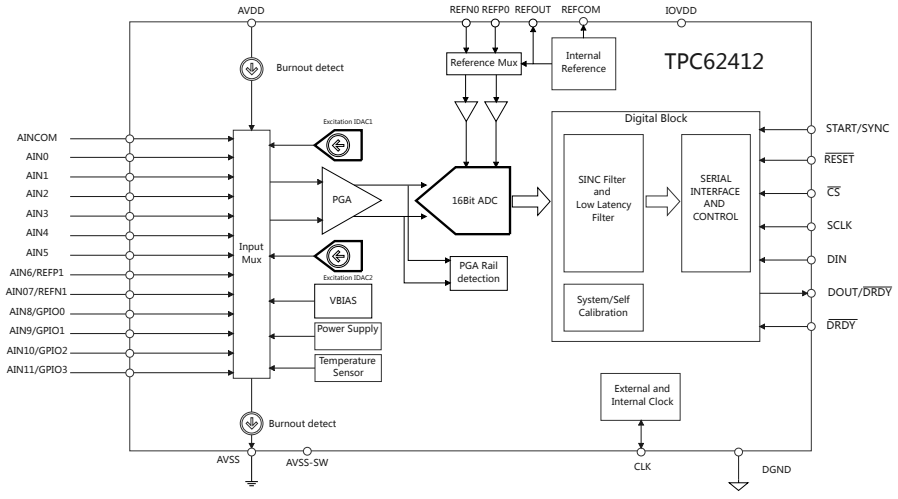
Additionally, the device integrates a precision 2.5-V bandgap reference and an integrated oscillator.

Two programmable excitation current sources are available for easy RTD biasing for temperature measurement.

Finally, more features such as burn out, CRC, voltage bias, system monitoring, and GPIOs are integrated.

The device is available in the TQFP5X5-32 package.

Typical Application Circuit



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Product Family Table

Order Number	ADC resolution	ADC channel	Temperature Range	Package
TPC62412-QPER	16	12	−40℃ to 125℃	TQFP5X5-32

Revision History

Date	Revision	Notes
2025-02-10	Rev.A.0	Initial released.

Pin Configuration and Functions

TPC62412
TQFP 5X5-32
Top View

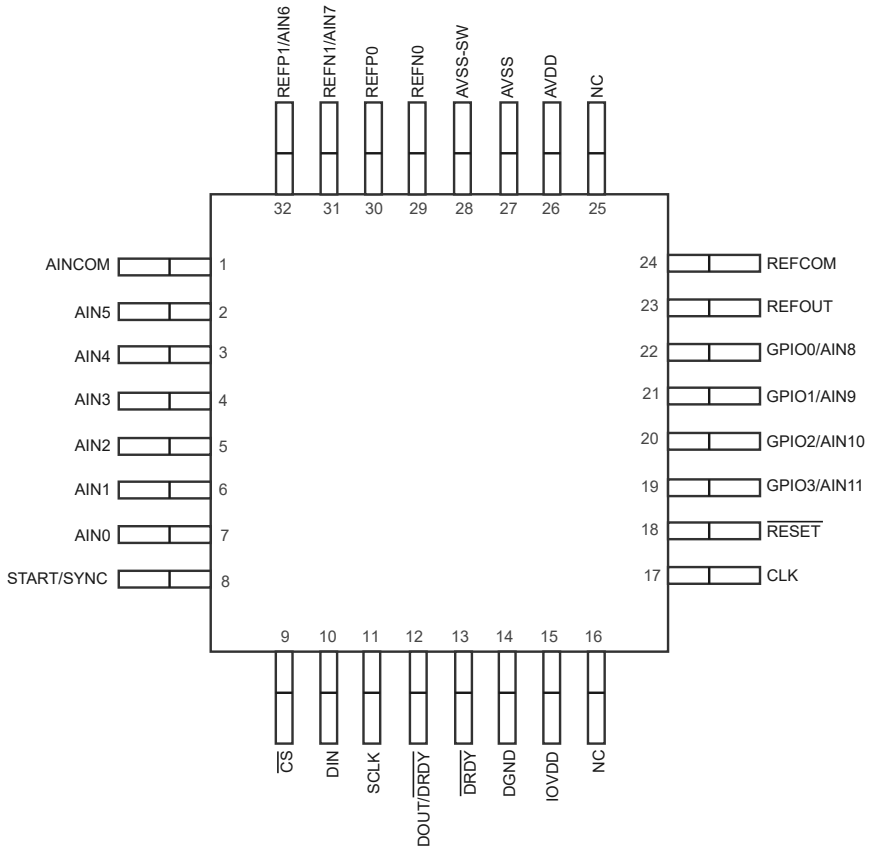


Table 1. Pin Functions

Pin		Function	Description (1)
Pin No.	Name		
1	AINCOM	Analog input	Common analog input for single-ended measurements
2	AIN5	Analog input	Analog input 5
3	AIN4	Analog input	Analog input 4
4	AIN3	Analog input	Analog input 3
5	AIN2	Analog input	Analog input 2
6	AIN1	Analog input	Analog input 1
7	AIN0	Analog input	Analog input 0
8	START/SYNC	Digital input	Start conversion
9	$\overline{CS}$	Digital input	Chip select; active low

Pin		Function	Description (1)
Pin No.	Name		
10	DIN	Digital input	Serial data input
11	SCLK	Digital input	Serial clock input
12	DOUT/$\overline{\text{DRDY}}$	Digital output	Serial data output combined with data ready; active low
13	$\overline{\text{DRDY}}$	Digital output	Data ready; active low
14	DGND	Digital ground	Digital ground
15	IOVDD	Digital supply	Digital I/O power supply. In case IOVDD is not tied to DVDD, connect a 100-nF (or larger) capacitor to DGND.
16	NC	—	Leave unconnected or connect to AVSS
17	CLK	Digital input	External clock input. Connect to DGND to use the internal oscillator.
18	$\overline{\text{RESET}}$	Digital input	Reset; active low
19	GPIO3/AIN11	Analog input/output	General-purpose I/O (2); analog input 11
20	GPIO2/AIN10	Analog input/output	General-purpose I/O (2); analog input 10
21	GPIO1/AIN9	Analog input/output	General-purpose I/O (2); analog input 9
22	GPIO0/AIN8	Analog input/output	General-purpose I/O (2); analog input 8
23	REFOUT	Analog output	Positive voltage reference output. Connect a 1-µF to 47-µF capacitor to REFCOM if the internal voltage reference is enabled.
24	REFCOM	Analog output	Negative voltage reference output. Connect to AVSS.
25	NC	—	Leave unconnected or connect to AVSS
26	AVDD	Analog supply	Positive analog power supply. Connect a 330-nF (or larger) capacitor to AVSS.
27	AVSS	Analog supply	Negative analog power supply
28	AVSS-SW	Analog supply	Negative analog power supply; low-side switch. Connect to AVSS.
29	REFN0	Analog input	Negative external reference input 0
30	REFP0	Analog input	Positive external reference input 0
31	REFN1/AIN7	Analog input	Negative external reference input 1; analog input 7
32	REFP1/AIN6	Analog input	Positive external reference input 1; analog input 6

(1) General-purpose inputs and outputs use logic levels based on the analog supply.

Specifications

Absolute Maximum Ratings (1)

		Min	Max	Unit
Supply Voltage	AVDD to AVSS	−0.3	5.5	V
	AVSS to DGND	−2.8	0.3	V
	DVDD to DGND	−0.3	3.9	V
	IOVDD to DGND	−0.3	5.5	V
Analog Input Voltage	AINx, GPIOx, REFPx, REFNx, REFCOM	AVSS – 0.3	AVDD + 0.3	V
Digital Input Voltage	$\overline{CS}$, SCLK, DIN, DOUT/$\overline{DRDY}$, $\overline{DRDY}$, START, $\overline{RESET}$, CLK	DGND – 0.3	IOVDD + 0.3	V
Input Current	Continuous, AVSS-SW, REFN0, REFOUT	−100	100	mA
	Continuous, all other pins except power-supply pins	−10	10	mA
T_A	Operating Temperature Range	−40	125	°C
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±7000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Test Conditions	Min	Typ	Max	Units
Power Supply						
AVDD	Analog Power Supply	AVDD to AVSS	3		5.5	V
		AVSS to DGND	−2.5	0	0	V
		AVDD to DGND	1.5		5.5	V
DVDD	Digital Power Supply	IOVDD to DGND	2		5.5	V
		IOVDD to AVSS	2		8	V
$V_{(AINx)}$	Absolute Input Voltage	PGA Bypassed	AVSS − 0.05		AVDD + 0.05	V
		PGA Enabled, Gain = 1 to 8	AVSS + 0.15		AVDD − 0.35	V
		PGA Enabled, Gain =16 to 128				V
V_{IN}	Differential Input Voltage	$V_{IN} = V_{AINP} - V_{AINN}$	$-V_{REF}$/Gain		V_{REF}/Gain	V
Voltage Reference Input						
V_{REF}	Absolute Differential Input Voltage		1		AVDD − AVSS	V
$V_{(REFNx)}$	Absolute Negative Reference Voltage	REF BUF Bypassed	AVSS		$V_{(REFPx)}$− 1	V
		REF BUF Enable	AVSS + 0.5		$V_{(REFPx)}$ − 1	V
$V_{(RFEFPx)}$	Absolute Positive Reference Voltage	REF BUF Bypass	$V_{(REFNx)}$ + 1		AVDD + 0.05	V
		REF BUF Enable	$V_{(REFNx)}$+ 1		AVDD − 0.5	V
External Clock Source						
f_{CLK}	External Clock Frequency		2	4.096	4.5	MHz
	Duty Cycle		40	50	60	%
Internal Clock Source						
f_{CLK}	Clock Frequency			4.096		MHz
	Accuracy		−2		2	%
General Purpose Inputs						
	GPIO Input Voltage		AVSS − 0.05		AVDD + 0.05	V
Digital Inputs						
	Digital Input Voltage		DGND		IOVDD	V
Temperature Range						
T_J	Operating Junction Temperature		−40		125	℃

Thermal Information

Package Type	θ_{JA}	$\theta_{JC(top)}$	θ_{JB}	Unit
TQFP5X5-32	70.56	19.2	45.07	°C/W

Electrical Characteristics

All minimum/maximum specifications at T_A = −40℃ to +125℃ and all typical specifications at T_A = 25℃, AVDD = 3.0 V to 5.5 V, IOVDD = 3.3 V, AVSS = 0 V, unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Units
Analog Input					
Differential Input Impedance	AVDD = 5.5 V, PGA Gain = 1 T_A = −40°C to +85°C	1.834	3.427		GΩ
	AVDD = 5.5 V, PGA Gain = 2 T_A = −40°C to +85°C	1.316	2.621		
	AVDD = 5.5 V, PGA Gain = 4 T_A = −40°C to +85°C	0.811	1.417		
	AVDD = 5.5 V, PGA Gain = 8 T_A = −40°C to +85°C	0.500	0.798		
	AVDD = 5.5 V, PGA Gain = 16 T_A = −40°C to +85°C	0.272	0.426		
	AVDD = 5.5 V, PGA Gain = 32 T_A = −40°C to +85°C	0.157	0.231		
	AVDD = 5.5 V, PGA Gain = 64 T_A = −40°C to +85°C	0.129	0.206		
	AVDD = 5.5 V, PGA Gain = 128 T_A = −40°C to +85°C	0.104	0.191		
PGA					
Gain Settings			1, 2, 4, 8, 16, 32, 64, 128		
Startup Time	Enabling the PGA in conversion mode		190		µs
System Performance					
Resolution		16			Bits
Data Rate		2.5		8 k	SPS
INL (Best Fit)	PGA bypassed, T_A = 25°C V_{CM} = AVDD/2		2.5	±10	ppm_{FSR}
	PGA gain = 1 to 8 V_{CM} = AVDD/2		5		
	PGA gain = 16 to 128 V_{CM} = AVDD/2		6		
Input Offset Voltage	T_A = 25°C, PGA bypassed	–188	78	170	µV
	T_A = 25°C, PGA enabled, gain = 1	–205	81	200	
	T_A = 25°C, PGA enabled, gain = 2	–100	15	100	
	T_A = 25°C, PGA enabled, gain = 4	–50	15	–50	
	T_A = 25°C, PGA enabled, gain = 8	–30	5	30	

Parameter	Test Conditions	Min	Typ	Max	Units
	T_A = 25°C, PGA enabled, gain = 16	–20	6	20	
	T_A = 25°C, PGA enabled, gain = 32 to 128	–15	5	15	
	T_A = 25°C, PGA bypassed, after internal vos calibration	on the order of noisepp at the set DR			
	T_A = 25°C, PGA enabled, gain = 1 to 128, after internal offset calibration	on the order of noisepp at the set DR			
	T_A = 25°C, PGA bypassed, global chop enabled	–2.3	0.1	2.2	µV
	T_A = 25°C, PGA enabled, gain = 1, global chop enabled	–2.3	0.1	2.2	
Offset Drift	AVDD = 5.5 V, PGA bypassed		21		nV/°C
	AVDD = 5.5 V, PGA Gain = 1 T_A = −40°C to +85°C		200	715	
	AVDD = 5.5 V, PGA Gain = 2 T_A = −40°C to +85°C		82	275	
	AVDD = 5.5 V, PGA Gain = 4 T_A = −40°C to +85°C		55	160	
	AVDD = 5.5 V, PGA Gain = 8 T_A = −40°C to +85°C		42	105	
	AVDD = 5.5 V, PGA Gain = 16 T_A = −40°C to +85°C		31	75	
	AVDD = 5.5 V, PGA Gain = 32 T_A = −40°C to +85°C		18	55	
	AVDD = 5.5 V, PGA Gain = 64 T_A = −40°C to +85°C		17	51	
	AVDD = 5.5 V, PGA Gain = 128 T_A = −40°C to +85°C		21	50	
	AVDD = 5.5 V, PGA bypassed or enable, Global chop		0.5		
Gain Error (Exclude Voltage Reference Error)	T_A = 25°C, PGA bypassed	−0.06	0.01	0.06	%FSR
	T_A = 25°C, PGA Gain = 1	−0.06	0.01	0.06	
	T_A = 25°C, PGA Gain = 2	−0.10	0.02	0.11	
	T_A = 25°C, PGA Gain = 4	−0.13	0.02	0.13	
	T_A = 25°C, PGA Gain = 8	−0.17	0.04	0.17	
	T_A = 25°C, PGA Gain = 16	−0.17	0.03	0.17	
	T_A = 25°C, PGA Gain = 32	−0.17	0.04	0.18	
	T_A = 25°C, PGA Gain = 64	−0.17	0.04	0.18	
	T_A = 25°C, PGA Gain = 128	−0.17	0.04	0.18	
Gain Drift	AVDD = 5.5 V, PGA bypassed		0.4		ppm/°C

Parameter	Test Conditions	Min	Typ	Max	Units
(Exclude Voltage Reference Error)	AVDD = 5.5 V, PGA Gain = 1 T_A = −40°C to +85°C		0.6	1.6	
	AVDD = 5.5 V, PGA Gain = 2 T_A = −40°C to +85°C		0.5	1.3	
	AVDD = 5.5 V, PGA Gain = 4 T_A = −40°C to +85°C		0.6	1.6	
	AVDD = 5.5 V, PGA Gain = 8 T_A = −40°C to +85°C		0.5	1.5	
	AVDD = 5.5 V, PGA Gain = 16 T_A = −40°C to +85°C		0.8	2.4	
	AVDD = 5.5 V, PGA Gain = 32 T_A = −40°C to +85°C		1.3	3.5	
	AVDD = 5.5 V, PGA Gain = 64 T_A = −40°C to +85°C		1.4	3.8	
	AVDD = 5.5 V, PGA Gain = 128 T_A = −40°C to +85°C		1.5	4.4	
Noise (Input-referred)	PGA Gain = 128, DR = 2.5 SPS, Sinc^3 filter		60		nV_{RMS}
NMRR Normal-mode Rejection Ratio	f_{IN} = 50 Hz or 60 Hz (±1 Hz), DR = 10 SPS, Sinc^3 filter		88		dB
	f_{IN} = 50 Hz or 60 Hz (±1 Hz), DR = 10 SPS, Sinc^3 filter, external f_{CLK} = 4.096 MHz		102		
	f_{IN} = 50 Hz or 60 Hz (±1 Hz), DR = 20 SPS, low-latency filter		79		
	f_{IN} = 50 Hz or 60 Hz (±1 Hz), DR = 20 SPS, low-latency filter, external f_{CLK} = 4.096 MHz		94		
	f_{IN} = 50 Hz (±1 Hz), DR = 50 SPS, Sinc^3 filter		87		
	f_{IN} = 50 Hz (±1 Hz), DR = 50 SPS, Sinc^3 filter, external f_{CLK} = 4.096 MHz		102		
	f_{IN} = 60 Hz (±1 Hz), DR = 60 SPS, Sinc^3 filter		89		
	f_{IN} = 60 Hz (±1 Hz), DR = 60 SPS, sinc^3 filter, external f_{CLK} = 4.096 MHz		106		
CMRR Common-mode Rejection Ratio	At DC	104	122		dB
	f_{CM} = 50 Hz or 60 Hz (±1 Hz), DR = 2.5 SPS to 10 SPS, Sinc^3 filter		122		
	f_{CM} = 50 Hz or 60 Hz (±1 Hz), DR = 2.5 SPS, 5 SPS, 10 SPS, 20 SPS, low-latency filter		111		

Parameter	Test Conditions	Min	Typ	Max	Units
PSRR Power-supply Rejection Ratio	AVDD at DC	83	95		
	AVDD at 50 Hz or 60 Hz		90		
Voltage Reference Inputs					
Absolute Input Current	Reference buffers disabled, external V_{REF} = 2.5 V, REFP1/REFN1 inputs		1.6		uA/V
	Reference buffers enabled, external V_{REF} = 2.5 V, REFP1/REFN1 inputs		0.3		nA
Internal Voltage Reference					
V_{REF}	Output Voltage		2.5		V
Accuracy	T_A = 25°C, AVDD = 3.3 V	–0.1%	±0.03%	0.1%	
Temperature Drift	T_A= −40 to 125°C		5		ppm/°C
Output Current	sink and source	–1		1	mA
Short-circuit Limit Current	sink or source		4		mA
PSRR Power-supply Rejection Ratio	AVDD at DC		89		dB
Load Regulation	Load Current = −1 to 1 mA		150		µV/mA
Startup Time	1-µF capacitor on REFOUT, 0.001% settling		2		ms
Capacitive Load Stability (1)	Capacitor on REFOUT	1		47	µF
Reference Noise	f =0.1 to 10 Hz, 1 µF capacitor on REFOUT		9		μV_{PP}
Internal Oscillator					
f_{CLK}	Frequency		4.096		MHz
	Accuracy	−1.5%		1.5%	
Excitation Current Sources (IDACs)					
Current Setting		10, 50, 100, 250, 500, 750, 1000, 1500, 2000			µA
Compliance Voltage	10 µA to 750 µA, 0.1% deviation	AVSS		AVDD - 0.4	V
	1 mA to 2 mA, 0.1% deviation	AVSS		AVDD - 0.6	V
Accuracy (Each IDAC)	T_A = 25°C, 10 µA to 100 µA	–5%	±0.7%	5%	
	T_A = 25°C, 250 µA to 2 mA	–3%	±0.5%	3%	
Current Mismatch betwewn IDACs	T_A = 25°C, 10 µA to 100 µA		0.15%	0.80%	
	T_A = 25°C, 250 µA to 750 µA		0.10%	0.60%	
	T_A = 25°C, 1 mA to 2 mA		0.07%	0.40%	
Temperature Drift (Each IDAC)	10 µA to 750 µA		20		ppm/°C
	1 m to 2 mA		10		
Temperature Drift Matching Between IDACs	10 µA to 100 µA		3		ppm/°C
	250 µA to 2 mA		2		

Parameter	Test Conditions	Min	Typ	Max	Units
Startup Time			25		µs
BIAS Voltage					
V_{BIAS}	Output Voltage Settings		(AVDD+AVSS)/2, (AVDD+AVSS)/12		V
Output Impedance			380		Ω
Startup Time	Capacitive load on all selected analog inputs C_{LOAD} = 1 µF, 0.1% settling		2.8		ms
Burnout Current Sources (BOCS)					
Current Setting			0.2, 1, 10		µA
Accuracy	0.2 µA		±8%		
	1 µA		±4%		
	10 µA		±2%		
PGA Rail Detection					
Positive Rail Threshold	Refer to the output of the PGA		AVDD – 0.15		V
Negative Rail Threshold	Refer to the output of the PGA		AVSS + 0.15		V
Reference Detection					
Threshold 1			0.3		V
Threshold 2			1/3 * (AVDD – AVSS)		V
Threshold 2 Accuracy	T_A = 25℃	–3%	±1%	3%	
Pull-together Resistance			1		MΩ
Supply Voltage Monitors					
Accuracy	(AVDD – AVSS) / 4 monitor		±1%		
	DVDD / 4 monitor		±1%		
Temperature Sensor					
Output Voltage	T_A = 25°C		130		mV
Temperature Coefficient			431		µV/°C
Accuracy			±2		°C
Low-side Power Switch					
R_{ON}	On Resistance		1.3	3	Ω
Current Through Switch			75		mA
GPIOs					
V_{IL}	Logic input level, low	AVSS – 0.05		0.3*AVDD	V
V_{IH}	Logic input level, high	0.7*AVDD		AVDD + 0.05	V
V_{OL}	Logic output level, low, I_{OL}= 1 mA	AVSS		0.2*AVDD	V
V_{OH}	Logic output level, high, I_{OH}= 1 mA	0.8*AVDD		AVDD	V
Digital Interface					
V_{IL}	Logic input level, low	DGND		0.3*IOVDD	V
V_{IH}	Logic input level, high	0.7*IOVDD		IOVDD	V

Parameter	Test Conditions	Min	Typ	Max	Units
V_{OL}	Logic output level, low, I_{OL}= 1 mA	DGND		0.2*IOVDD	V
V_{OH}	Logic output level, high, I_{OH}= 1 mA	0.8*IOVDD		IOVDD	V
Input Current	DGND ≤ $V_{Digital\ Input}$ ≤ IOVDD	−1		1	uA
Power Dissipation (T_A = 25°C, AVDD = IOVDD = 3.3 V, Internal Reference with buffer enabled, IDACs Disabled, VBIAS Disabled, Flags Disabled, Internal Oscillator, 1k SPS Data Rates, V_{IN} = 0 V)					
I_{AVDD}	Power-down mode		33	50	uA
	Standby mode, PGA bypassed		0.8	1.5	mA
	Conversion mode, PGA bypassed		0.86	1.6	
	Conversion mode, PGA enabled, gain = 1, 2		0.88	1.6	
	Conversion mode, PGA enabled, gain = 4, 8		0.93	1.8	
	Conversion mode, PGA enabled, gain = 16, 32		0.97	1.9	
	Conversion mode, PGA enabled, gain = 64		1.08	1.99	
	Conversion mode, PGA enabled, gain = 128		1.26	2.25	
P_D Power Dissipation	Conversion mode, PGA enabled, gain = 1		3.3		mW

Timing Specifications

Timing Requirements (1)

All minimum/maximum specifications at T_J = −40℃ to +125℃ and all typical specifications at T_J = 25℃, IOVDD = 2 V to 5.5 V, DOUT = 20 pF to DGND, unless otherwise noted.

Parameter		Min	Max	Unit (2)
Serial Interface				
$t_{d(CSSC)}$	Delay time, first SCLK rising edge after $\overline{CS}$ falling edge	20		ns
$t_{d(SCCS)}$	Delay time, $\overline{CS}$ rising edge after final SCLK falling edge	20		ns
$t_{w(CSH)}$	Pulse duration, $\overline{CS}$ high	30		ns
$t_{c(SC)}$	SCLK period	100		ns
$t_{w(SCH)}$	Pulse duration, SCLK high	40		ns
$t_{w(SCL)}$	Pulse duration, SCLK low	40		ns
$t_{su(DI)}$	Setup time, DIN valid before SCLK falling edge	15		ns
$t_{h(DI)}$	Hold time, DIN valid after SCLK falling edge	20		ns
$t_{d(CMD)}$	Delay time, between bytes or commands	0		ns
Reset Pin				
$t_{w(RSL)}$	Pulse duration, $\overline{RESET}$ low	4		t_{CLK}
$t_{d(RSSC)}$	Delay time, first SCLK rising edge after $\overline{RESET}$ rising edge (or 7th SCLK falling edge of RESET command)	4096		t_{CLK}
START/SYNC Pin				
$t_{w(STH)}$	Pulse duration, START/SYNC high	4	1765	t_{CLK}
$t_{w(STL)}$	Pulse duration, START/SYNC low	4		t_{CLK}
$t_{su(STDR)}$	Setup time, START/SYNC falling edge (or 7th SCLK falling edge of STOP command) before DRDY falling edge to stop further conversions (continuous conversion mode)	32		t_{CLK}
Reading Conversion Data without Rdata Command				
$t_{h(SCDR)}$	Hold time, SCLK low before DRDY falling edge (3)	28		t_{CLK}
$t_{d(DRSC)}$	Delay time, SCLK rising edge after DRDY falling edge (3)	4		t_{CLK}

(1) Parameters are guaranteed by design.
(2) $t_{CLK} = 1 / f_{CLK}$.
(3) Only applicable when reading data without the RDATA command. All commands can be sent without any SCLK to $\overline{DRDY}$ signal timing restrictions.

Switching Characteristics (1)

All minimum/maximum specifications at T_J = −40℃ to +125℃ and all typical specifications at T_J = 25℃,

IOVDD = 2 V to 5.5 V, DOUT = 20 pF to DGND, unless otherwise noted.

Parameter		Min	Typ	Max	Unit (2)
$t_{p(CSDO)}$	Propagation delay time, $\overline{CS}$ falling edge to DOUT driven	0		25	ns
$t_{p(SCDO)}$	Propagation delay time, SCLK rising edge to valid new DOUT	3		30	ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{CS}$ rising edge to DOUT high impedance	0		25	ns
$t_{p(STDR)}$	Propagation delay time, START/SYNC rising edge (or first SCLK rising edge of any command or data read) to $\overline{DRDY}$ rising edge			2	t_{CLK}
$t_{w(DRH)}$	Pulse duration, $\overline{DRDY}$ high	24			ns
$t_{p(GPIO)}$	Propagation delay time, last SCLK falling edge of WREG command to GPIOx output valid	3		100	ns
	SPI timeout per 8 bit (3)	2^{15}			ns

(1) Parameters are guaranteed by design.
(2) $t_{CLK} = 1 / f_{CLK}$.
(3) Only applicable when reading data without the RDATA command. All commands can be sent without any SCLK to $\overline{DRDY}$ signal timing restrictions.

Timing Diagrams

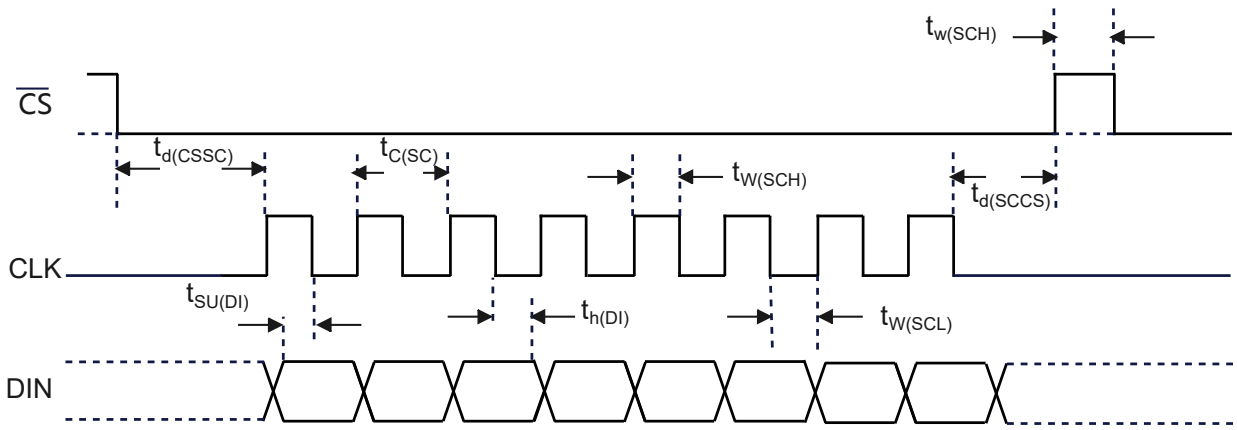


Figure 1. Serial Interface Timing Requirements

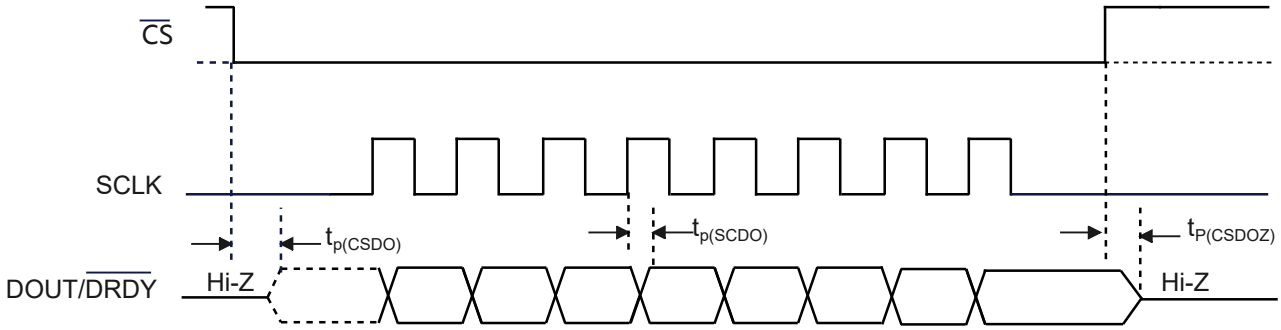


Figure 2. Serial Interface Switching Characteristics

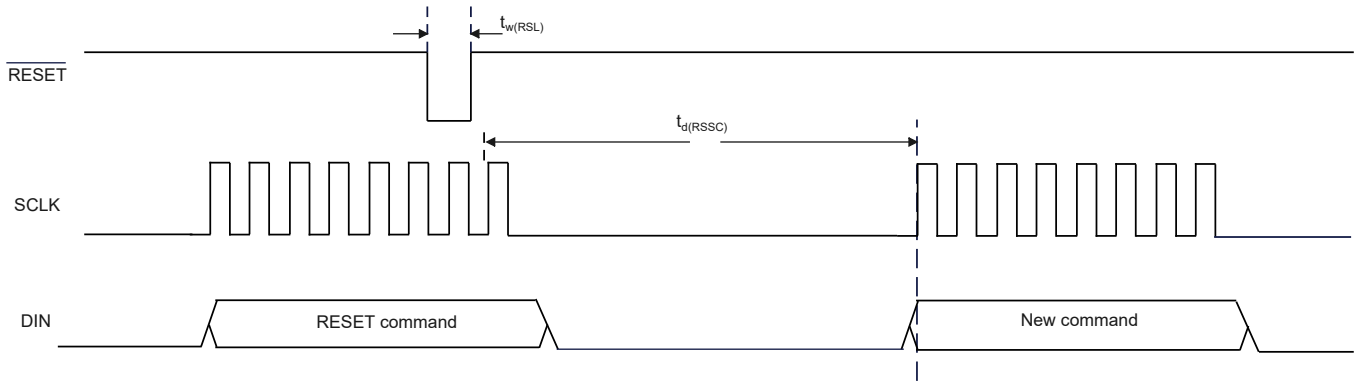


Figure 3. $\overline{\text{RESET}}$ Pin and RESET Command Timing Requirements

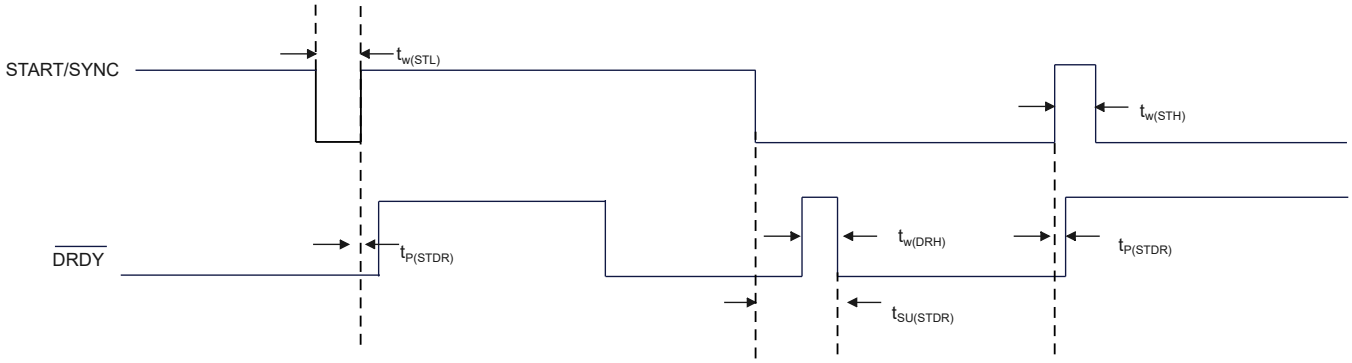


Figure 4. START/SYNC Pin Timing Requirements

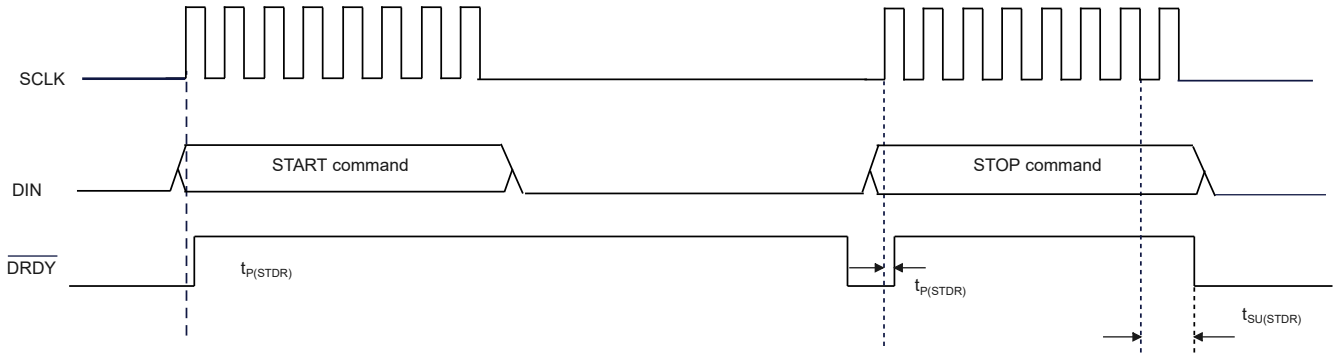


Figure 5. START Command Timing Requirements

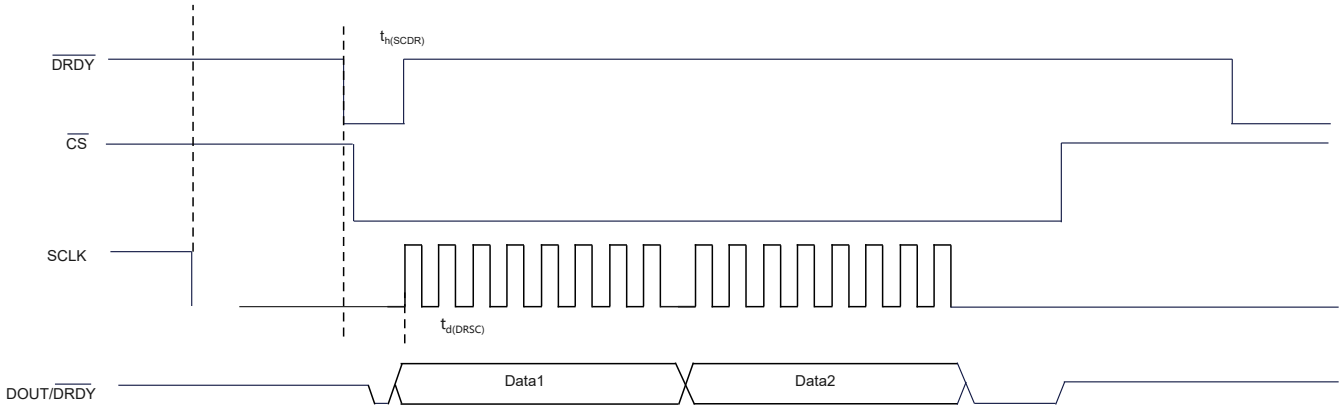


Figure 6. Read Data Direct (without an RDATA Command) Timing Requirements

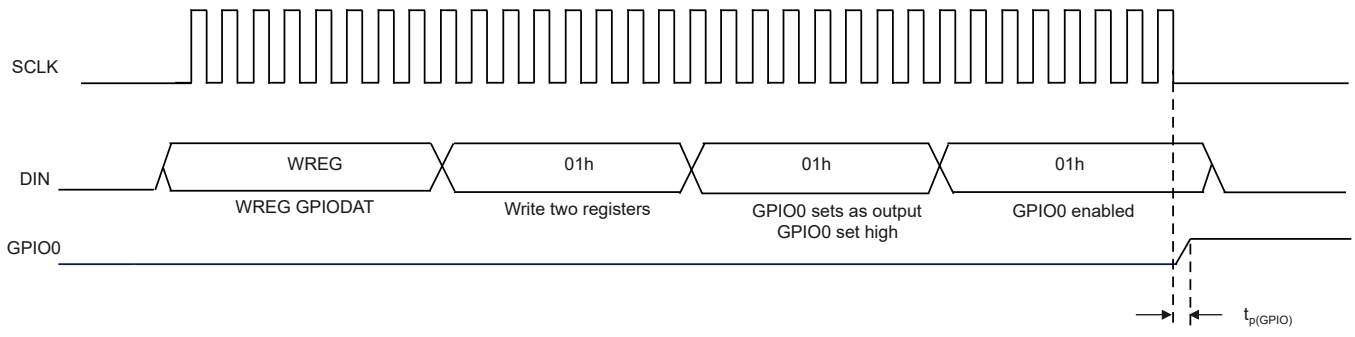


Figure 7. GPIO Switching Characteristics

Typical Performance Characteristics

All test conditions: V_{REF} = 2.5 V internal, AVDD = 5 V, IOVDD = 3.3 V, internal 4.096-MHz oscillator, and PGA enabled, T_A = 25°C, unless otherwise noted.

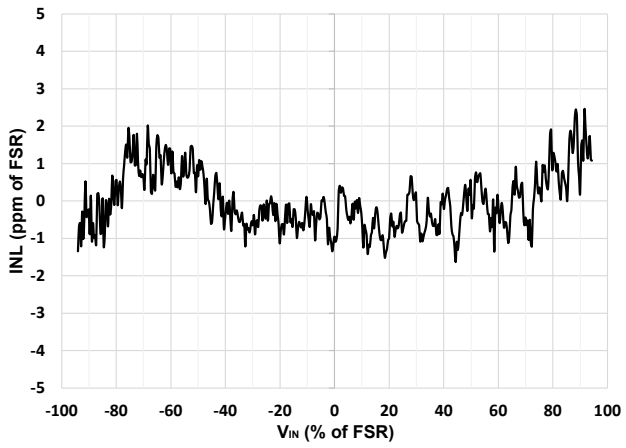


Figure 8. INL vs. Differential Input Voltage

PGA bypassed

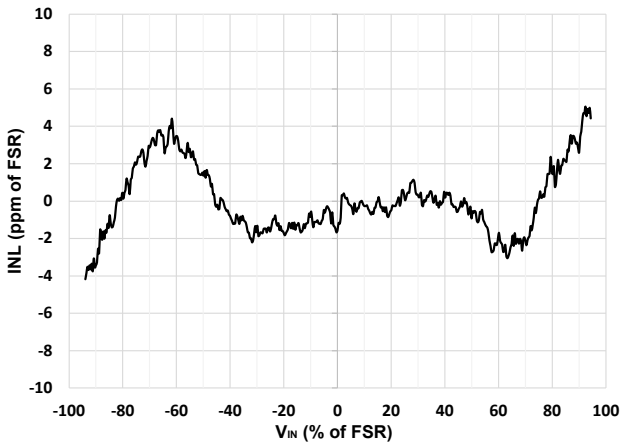


Figure 9. INL vs. Differential Input Voltage

PGA enabled, gain = 1

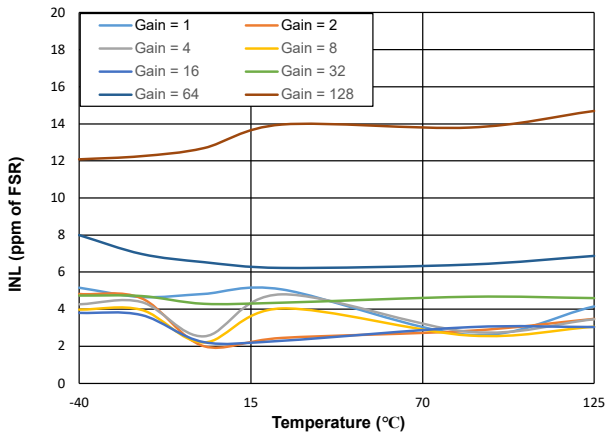


Figure 10. INL vs. Temperature

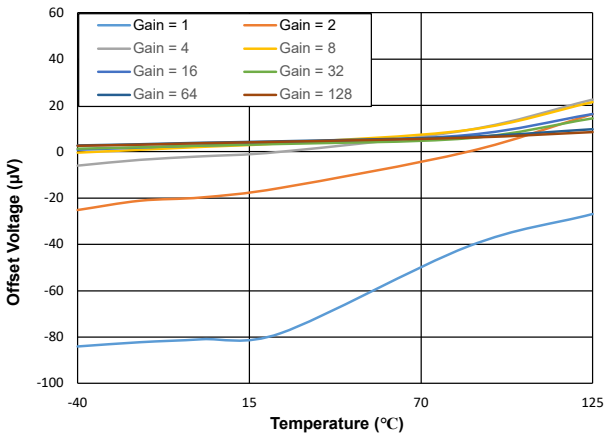


Figure 11. Offset Voltage vs. Temperature

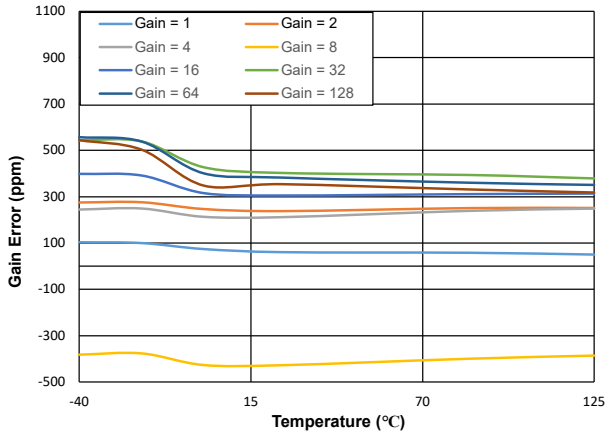


Figure 12. Gain Error vs. Temperature

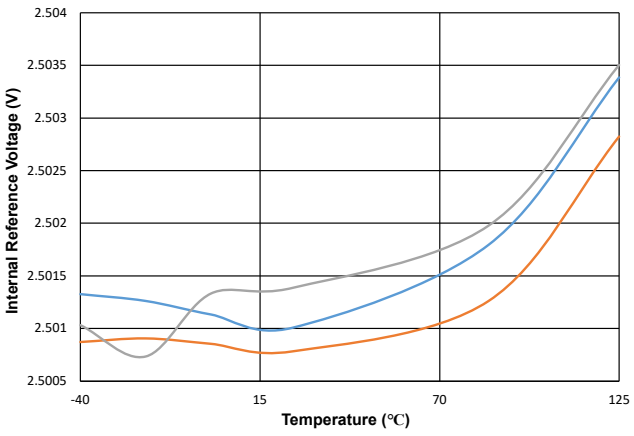


Figure 13. Internal Reference Voltage vs. Temperature

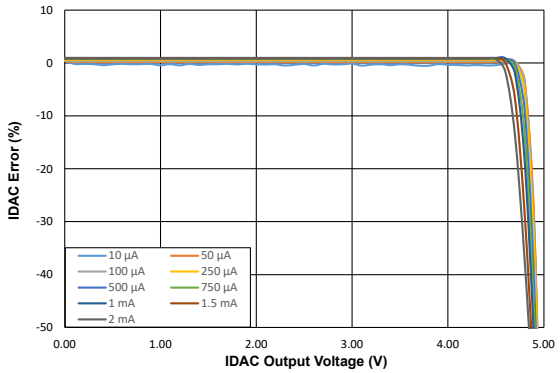


Figure 14. IDAC Accuracy vs. Compliance Voltage

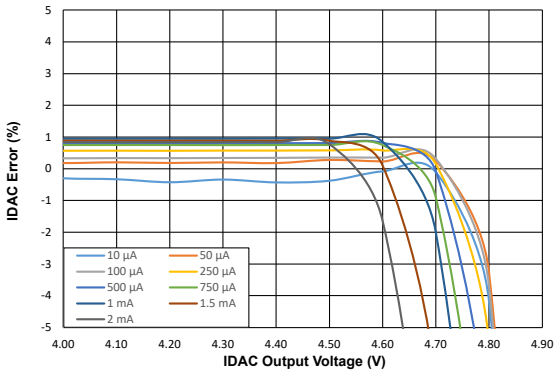


Figure 15. IDAC Accuracy vs. Compliance Voltage

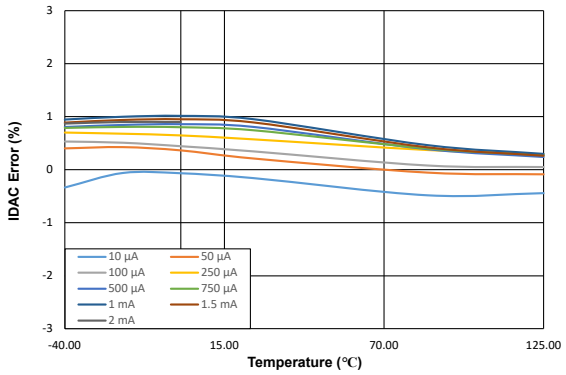


Figure 16. IDAC Accuracy vs. Temperature

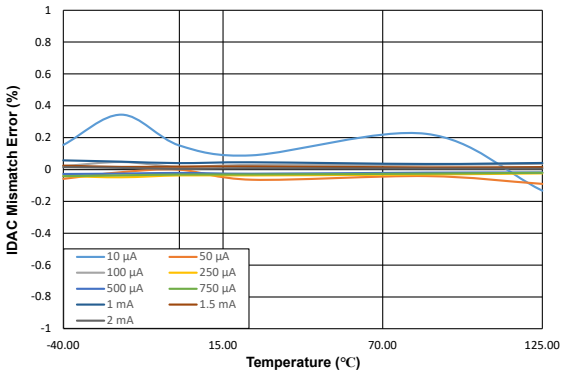


Figure 17. IDAC Matching vs. Temperature

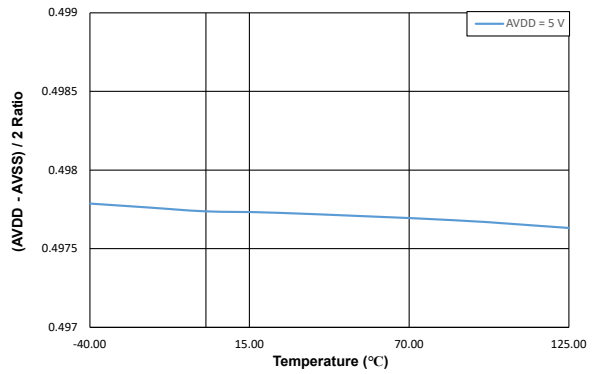


Figure 18. VBIAS Voltage [(AVDD – AVSS) / 2] vs. Temperature

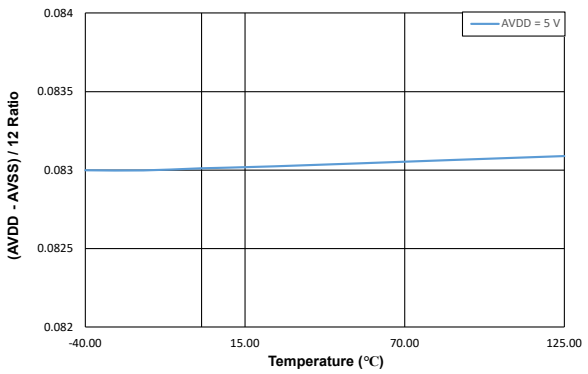


Figure 19. VBIAS Voltage [(AVDD – AVSS) / 12] vs. Temperature

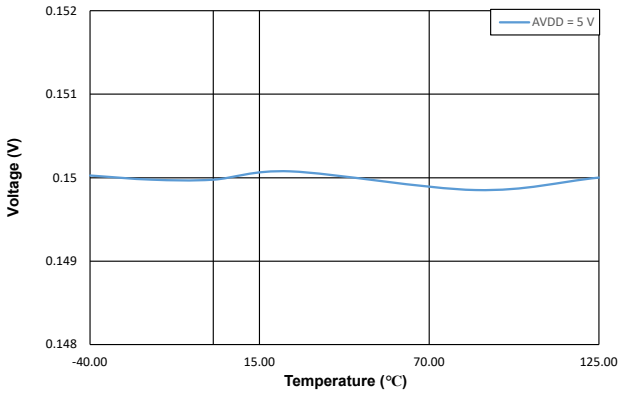


Figure 20. PGA Rail Detection, PGAN_RAILP, PGAP_RAILP Threshold from AVDD

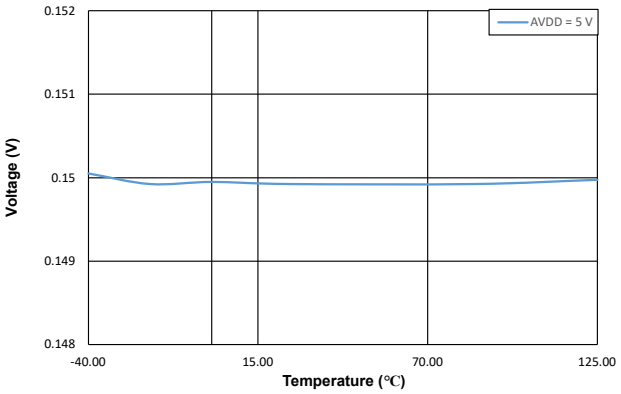


Figure 21. PGA Rail Detection, PGAN_RAILP, PGAP_RAILP Threshold from AVSS

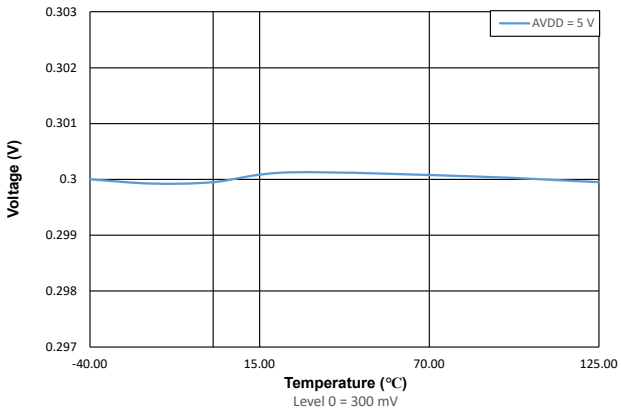


Figure 22. Reference Threshold Voltage, Level 0

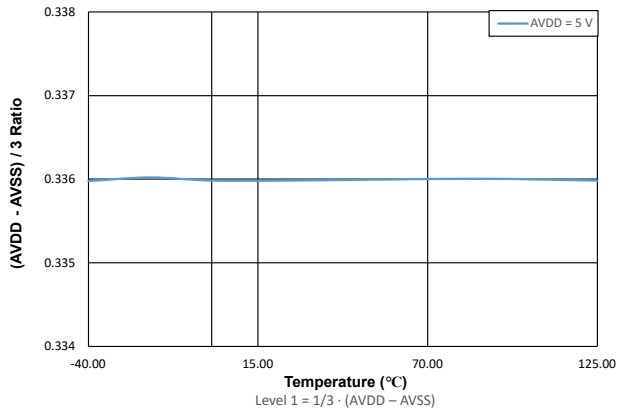


Figure 23. Reference Threshold Voltage, Level 1

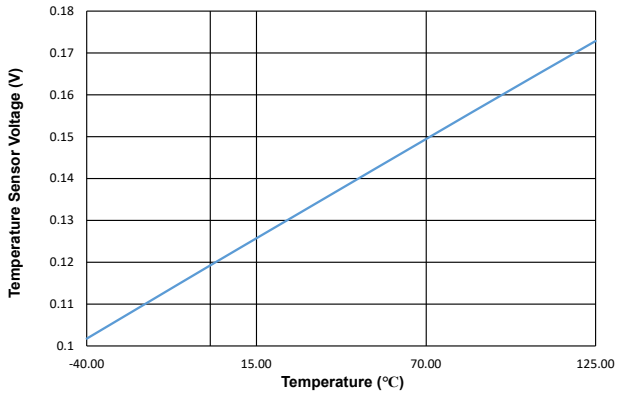


Figure 24. Temperature Sensor Voltage vs. Temperature

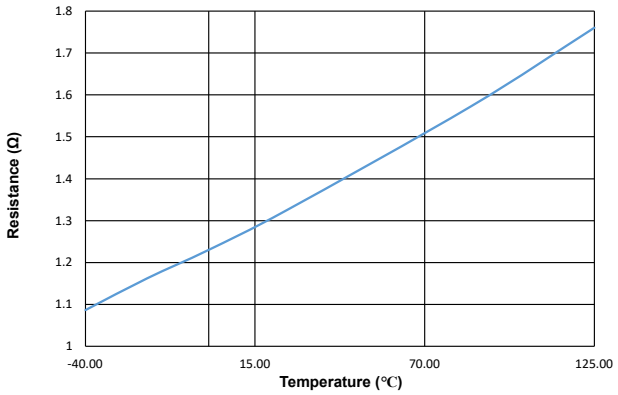


Figure 25. Low-Side Switch R_{ON} vs. Temperature

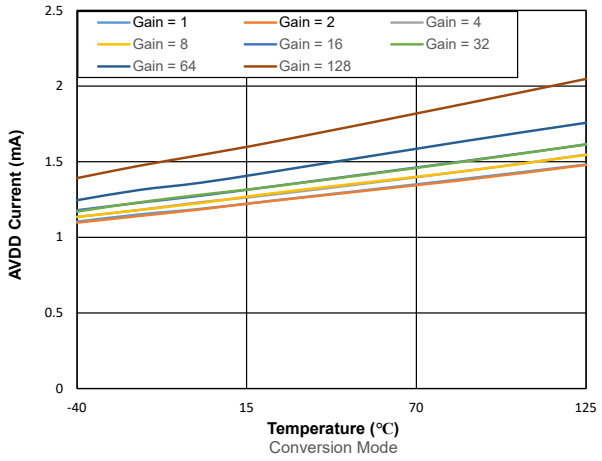


Figure 26. Analog Supply Current vs. Temperature

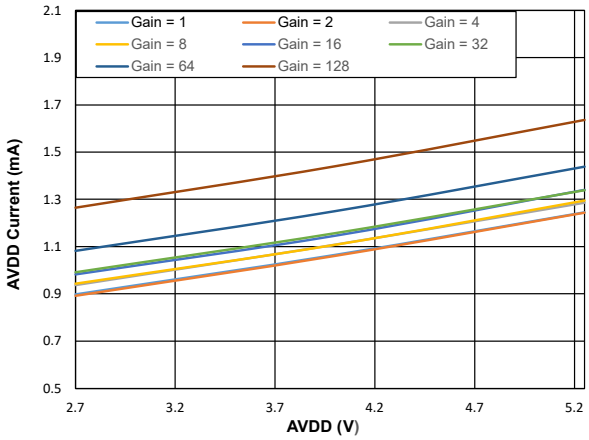


Figure 27. Analog Supply Current vs. AVDD

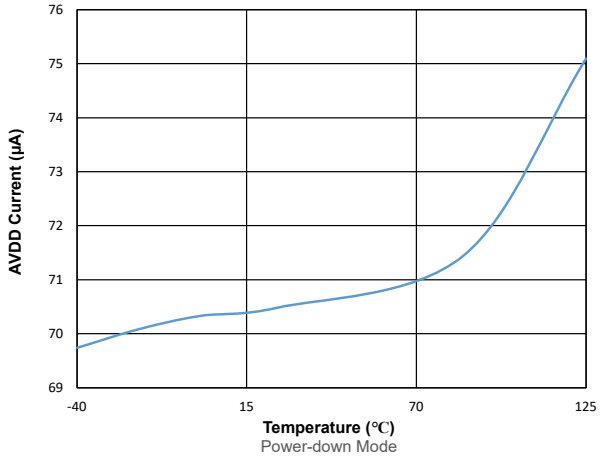


Figure 28. Analog Supply Current vs. Temperature

Power-down mode

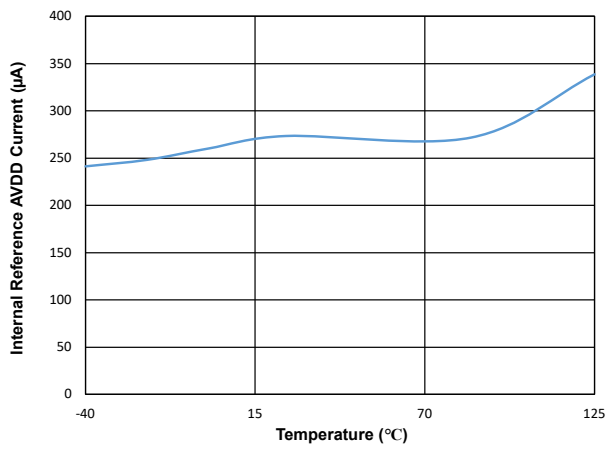


Figure 29. Internal Reference AVDD Current vs. Temperature

Noise Performance

Delta-sigma (ΔΣ) analog-to-digital converters (ADCs) are based on the principle of oversampling. The ratio between modulator frequency and output data rate is called the *oversampling ratio* (OSR). By increasing the OSR, and thus reducing the output data rate, the noise performance of the ADC can be optimized. In other words, the input-referred noise drops when reducing the output data rate because more samples of the internal modulator are averaged to yield one conversion result. Increasing the gain also reduces the input-referred noise, which is particularly useful when measuring low-level signals.

Use the following equations to calculate effective resolution and noise-free resolution when using a reference voltage other than 2.5 V.

$$\text{Effective Resolution} = \ln[(2 \cdot V_{REF}/\text{Gain})/V_{RMS-Noise}]/\ln(2) \quad (1)$$

$$\text{Noise} - \text{Free Resolution} = \ln[(2 \cdot V_{REF}/\text{Gain})/V_{PP-Noise}]/\ln(2) \quad (2)$$

Table 2. Noise in μV_{RMS} with Sinc Filter, at AVDD = 3.3 V, AVSS = 0 V, PGA Enabled, Global Chop Disabled, and Internal 2.5-V Reference

DATA RATE (SPS)	Sinc Filter							
	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128
2.5	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
5	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
10	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
16.6	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
20	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
50	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
60	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
100	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
200	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
400	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
800	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
1000	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
2000	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
4000	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.66
8000	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.89

Table 3. Noise in μV_{PP} with Sinc Filter, at AVDD = 3.3 V, AVSS = 0 V, PGA Enabled, Global Chop Disabled, and Internal 2.5-V Reference

DATA RATE (SPS)	Sinc Filter							
	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128
2.5	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
5	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
10	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
16.6	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
20	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
50	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
60	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
100	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.73
200	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.97
400	76.3	38.1	19.1	9.5	4.8	2.4	1.5	1.42
800	76.3	38.1	19.1	9.5	4.8	2.4	1.9	1.72
1000	76.3	38.1	19.1	9.5	4.8	2.4	2.0	2.04
2000	29.94	38.1	19.1	9.5	4.8	3.2	3.0	2.66
4000	45.80	38.1	19.1	9.5	5.5	4.6	4.3	3.98
8000	50.94	38.1	19.1	9.5	6.7	6.4	5.7	5.35

Table 4. Effective Resolution from RMS Noise with Sinc Filter at AVDD = 3.3 V, AVSS = 0 V, PGA Enabled, Global Chop Disabled, and Internal 2.5-V Reference

DATA RATE (SPS)	Sinc Filter							
	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128
2.5	16	16	16	16	16	16	16	16
5	16	16	16	16	16	16	16	16
10	16	16	16	16	16	16	16	16
16.6	16	16	16	16	16	16	16	16
20	16	16	16	16	16	16	16	16
50	16	16	16	16	16	16	16	16
60	16	16	16	16	16	16	16	16
100	16	16	16	16	16	16	16	16
200	16	16	16	16	16	16	16	16
400	16	16	16	16	16	16	16	16
800	16	16	16	16	16	16	16	16
1000	16	16	16	16	16	16	16	16
2000	16	16	16	16	16	16	16	16
4000	16	16	16	16	16	16	16	16
8000	16	16	16	16	16	16	16	15.4

Table 5. Noise-Free Resolution from Peak-to-Peak Noise with Sinc Filter at AVDD = 3.3 V, AVSS = 0 V, PGA Enabled, Global Chop Disabled, and Internal 2.5-V Reference

DATA RATE (SPS)	Sinc Filter							
	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128
2.5	16	16	16	16	16	16	16	16
5	16	16	16	16	16	16	16	16
10	16	16	16	16	16	16	16	16
16.6	16	16	16	16	16	16	16	16
20	16	16	16	16	16	16	16	16
50	16	16	16	16	16	16	16	16
60	16	16	16	16	16	16	16	16
100	16	16	16	16	16	16	16	15.7
200	16	16	16	16	16	16	16	15.3
400	16	16	16	16	16	16	15.7	14.7
800	16	16	16	16	16	16	15.3	14.5
1000	16	16	16	16	16	16	15.2	14.2
2000	16	16	16	16	16	15.6	14.7	13.8
4000	16	16	16	16	15.8	15.0	14.2	13.3
8000	16	16	16	16	15.5	14.6	13.7	12.8

Table 6. Noise in μV_{RMS} with Low-Latency Filter, at AVDD = 3.3 V, AVSS = 0 V, PGA Enabled, Global Chop Disabled, and Internal 2.5-V Reference

DATA RATE (SPS)	Low-Latency Filter							
	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128
2.5	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
5	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
10	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
16.6	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
20	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
50	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
60	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
100	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
200	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
400	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
800	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
1000	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
2000	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
4000	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.87
8000	76.3	38.1	19.1	9.5	4.8	2.4	1.2	1.14

Table 7. Noise in μV_{PP} with Low-Latency Filter, at AVDD = 3.3 V, AVSS = 0 V, PGA Enabled, Global Chop Disabled, and Internal 2.5-V Reference

DATA RATE (SPS)	Low-Latency Filter							
	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128
2.5	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
5	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
10	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
16.6	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
20	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
50	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.67
60	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.71
100	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.94
200	76.3	38.1	19.1	9.5	4.8	2.4	1.4	1.27
400	76.3	38.1	19.1	9.5	4.8	2.4	2.0	1.80
800	76.3	38.1	19.1	9.5	4.8	2.8	2.6	2.44
1000	76.3	38.1	19.1	9.5	4.8	3.2	2.9	2.84
2000	76.3	38.1	19.1	9.5	4.8	4.0	3.6	3.50
4000	76.3	62.2	21.8	13.4	7.3	6.1	5.7	5.21
8000	96.0	63.4	22.8	16.0	9.9	8.0	7.7	6.82

Table 8. Effective Resolution from RMS Noise with Low-Latency Filter at AVDD = 3.3 V, AVSS = 0 V, PGA Enabled, Global Chop Disabled, and Internal 2.5-V Reference

DATA RATE (SPS)	Low-Latency Filter							
	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128
2.5	16	16	16	16	16	16	16	16
5	16	16	16	16	16	16	16	16
10	16	16	16	16	16	16	16	16
16.6	16	16	16	16	16	16	16	16
20	16	16	16	16	16	16	16	16
50	16	16	16	16	16	16	16	16
60	16	16	16	16	16	16	16	16
100	16	16	16	16	16	16	16	16
200	16	16	16	16	16	16	16	16
400	16	16	16	16	16	16	16	16
800	16	16	16	16	16	16	16	16
1000	16	16	16	16	16	16	16	16
2000	16	16	16	16	16	16	16	16
4000	16	16	16	16	16	16	16	15.5
8000	16	16	16	16	16	16	16	15.1

Table 9. Noise-Free Resolution from Peak-to-Peak Noise with Low-Latency Filter at AVDD = 3.3 V, AVSS = 0 V, PGA Enabled, Global Chop Disabled, and Internal 2.5-V Reference

DATA RATE (SPS)	Low-Latency Filter							
	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128
2.5	16	16	16	16	16	16	16	16
5	16	16	16	16	16	16	16	16
10	16	16	16	16	16	16	16	16
16.6	16	16	16	16	16	16	16	16
20	16	16	16	16	16	16	16	16
50	16	16	16	16	16	16	16	15.8
60	16	16	16	16	16	16	16	15.7
100	16	16	16	16	16	16	16	15.3
200	16	16	16	16	16	16	16	14.9
400	16	16	16	16	16	16	15.3	14.4
800	16	16	16	16	16	15.8	14.9	14.0
1000	16	16	16	16	16	15.6	14.7	13.7
2000	16	16	16	16	16	15.3	14.4	13.4
4000	16	15.3	15.8	15.5	15.4	14.6	13.8	12.9
8000	15.7	15.3	15.7	15.3	14.9	14.3	13.3	12.5

Table 10. Noise in μV_{RMS} with Sinc Filter, at AVDD = 3.3 V, AVSS = 0 V, PGA Enabled, Global Chop Enabled, and Internal 2.5-V Reference

DATA RATE (SPS)	Sinc Filter							
	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128
2.5	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
5	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
10	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
16.6	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
20	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
50	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
60	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
100	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
200	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
400	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
800	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
1000	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
2000	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
4000	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
8000	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.66

Table 11. Noise in μV_{PP} with Sinc Filter, at AVDD = 3.3 V, AVSS = 0 V, PGA Enabled, Global Chop Enabled, and Internal 2.5-V Reference

DATA RATE (SPS)	Sinc Filter							
	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128
2.5	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
5	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
10	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
16.6	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
20	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
50	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
60	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
100	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
200	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.69
400	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.96
800	76.3	38.1	19.1	9.5	4.8	2.4	1.3	1.23
1000	76.3	38.1	19.1	9.5	4.8	2.4	1.4	1.42
2000	76.3	38.1	19.1	9.5	4.8	2.4	2.1	1.98
4000	165.3	52.0	40.5	12.3	4.3	3.5	3.2	3.04
8000	110.5	49.7	29.5	13.0	6.4	4.5	4.1	3.95

Table 12. Effective Resolution from RMS Noise with Sinc Filter at AVDD = 3.3 V, AVSS = 0 V, PGA Enabled, Global Chop Enabled, and Internal 2.5-V Reference

DATA RATE (SPS)	Sinc Filter							
	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128
2.5	16	16	16	16	16	16	16	16
5	16	16	16	16	16	16	16	16
10	16	16	16	16	16	16	16	16
16.6	16	16	16	16	16	16	16	16
20	16	16	16	16	16	16	16	16
50	16	16	16	16	16	16	16	16
60	16	16	16	16	16	16	16	16
100	16	16	16	16	16	16	16	16
200	16	16	16	16	16	16	16	16
400	16	16	16	16	16	16	16	16
800	16	16	16	16	16	16	16	16
1000	16	16	16	16	16	16	16	16
2000	16	16	16	16	16	16	16	16
4000	16	16	16	16	16	16	16	16
8000	16	16	16	16	16	16	16	15.9

Table 13. Noise-Free Resolution from Peak-to-Peak Noise with Sinc Filter at AVDD = 3.3 V, AVSS = 0 V, PGA Enabled, Global Chop Enabled, and Internal 2.5-V Reference

DATA RATE (SPS)	Sinc Filter							
	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128
2.5	16	16	16	16	16	16	16	16
5	16	16	16	16	16	16	16	16
10	16	16	16	16	16	16	16	16
16.6	16	16	16	16	16	16	16	16
20	16	16	16	16	16	16	16	16
50	16	16	16	16	16	16	16	16
60	16	16	16	16	16	16	16	15.7
100	16	16	16	16	16	16	16	15.3
200	16	16	16	16	16	16	16	15.8
400	16	16	16	16	16	16	16	15.3
800	16	16	16	16	16	16	15.8	15.0
1000	16	16	16	16	16	16	15.7	14.7
2000	16	16	16	16	16	16	15.2	14.3
4000	14.9	15.6	14.9	15.6	16	15.5	14.6	13.6
8000	15.5	15.6	15.4	15.6	15.6	15.1	14.2	13.3

Table 14. Noise in μV_{RMS} with Low-Latency Filter, at AVDD = 3.3 V, AVSS = 0 V, PGA Enabled, Global Chop Enabled, and Internal 2.5-V Reference

DATA RATE (SPS)	Low-Latency Filter							
	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128
2.5	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
5	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
10	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
16.6	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
20	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
50	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
60	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
100	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
200	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
400	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
800	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
1000	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
2000	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
4000	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.88
8000	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.89

Table 15. Noise in μV_{PP} with Low-Latency Filter, at AVDD = 3.3 V, AVSS = 0 V, PGA Enabled, Global Chop Enabled, and Internal 2.5-V Reference

DATA RATE (SPS)	Low-Latency Filter							
	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128
2.5	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
5	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
10	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
16.6	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
20	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
50	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
60	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.60
100	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.65
200	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.95
400	76.3	38.1	19.1	9.5	4.8	2.4	1.4	1.30
800	76.3	38.1	19.1	9.5	4.8	2.4	1.9	1.70
1000	76.3	38.1	19.1	9.5	4.8	2.4	2.0	1.85
2000	76.3	38.1	19.1	9.5	4.8	2.8	2.7	2.37
4000	158.4	142.1	43.4	13.3	6.2	5.6	5.3	5.27
8000	183.9	100.6	44.0	20.9	8.7	6.3	5.8	5.31

Table 16. Effective Resolution from RMS Noise with Low-Latency Filter at AVDD = 3.3 V, AVSS = 0 V, PGA Enabled, Global Chop Enabled, and Internal 2.5-V Reference

DATA RATE (SPS)	Low-Latency Filter							
	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128
2.5	16	16	16	16	16	16	16	16
5	16	16	16	16	16	16	16	16
10	16	16	16	16	16	16	16	16
16.6	16	16	16	16	16	16	16	16
20	16	16	16	16	16	16	16	16
50	16	16	16	16	16	16	16	16
60	16	16	16	16	16	16	16	16
100	16	16	16	16	16	16	16	16
200	16	16	16	16	16	16	16	16
400	16	16	16	16	16	16	16	16
800	16	16	16	16	16	16	16	16
1000	16	16	16	16	16	16	16	16
2000	16	16	16	16	16	16	16	16
4000	16	16	16	16	16	16	16	15.4
8000	16	16	16	16	16	16	16	15.4

Table 17. Noise-Free Resolution from Peak-to-Peak Noise with Low-Latency Filter at AVDD = 3.3 V, AVSS = 0 V, PGA Enabled, Global Chop Enabled, and Internal 2.5-V Reference

DATA RATE (SPS)	Low-Latency Filter							
	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128
2.5	16	16	16	16	16	16	16	16
5	16	16	16	16	16	16	16	16
10	16	16	16	16	16	16	16	16
16.6	16	16	16	16	16	16	16	16
20	16	16	16	16	16	16	16	16
50	16	16	16	16	16	16	16	16
60	16	16	16	16	16	16	16	16
100	16	16	16	16	16	16	16	15.9
200	16	16	16	16	16	16	16	15.3
400	16	16	16	16	16	16	15.8	14.9
800	16	16	16	16	16	16	15.4	14.5
1000	16	16	16	16	16	16	15.2	14.4
2000	16	16	16	16	16	15.8	14.8	14.0
4000	14.9	14.1	14.8	15.5	15.6	14.8	13.8	12.9
8000	14.7	14.6	14.8	14.9	15.1	14.6	13.7	12.8

Detailed Description

Overview

The TPC62412 is a precision 6-/12-channel, multiplexed ADC with integrated PGA and many other features, offering accurate measurement for low bandwidth input signals, and lower system cost and component count.

The device has a 16-bit delta-sigma converter, with configurable data rates. There is a sinc5 filter for optimized noise performance, and low latency filter for fast settling with 50-/60-Hz rejection for noisy industrial environments.

The TPC62412 incorporates several features that simplify precision sensor measurements. Key integrated features include:

- Low-noise PGA with integrated signal fault detection
- Low-drift 2.5-V voltage reference
- Dual, matched, sensor-excitation current sources (IDACs)
- Two sets of buffered external reference inputs with reference voltage level detection
- Internal oscillator
- Temperature sensor
- General-purpose input/output pins (GPIOs)
- A low-resistance switch connected to AVSS which can be used to disconnect bridge sensors to reduce current consumption

Analog inputs are configurable to be either single-ended inputs, differential inputs, or combination of the two. Many of the analog inputs have following features which can be programmed by the user. Please refer to register map for detail configuration information.

- Two sensor excitation current sources
- Sensor biasing voltage (VBIAS)
- Sensor burn-out current sources

The AVDD analog supply operates with bipolar supplies from ±1.5 V to ±2.625 V or a unipolar supply from 3.0 V to 5.25 V.

Functional Block Diagram

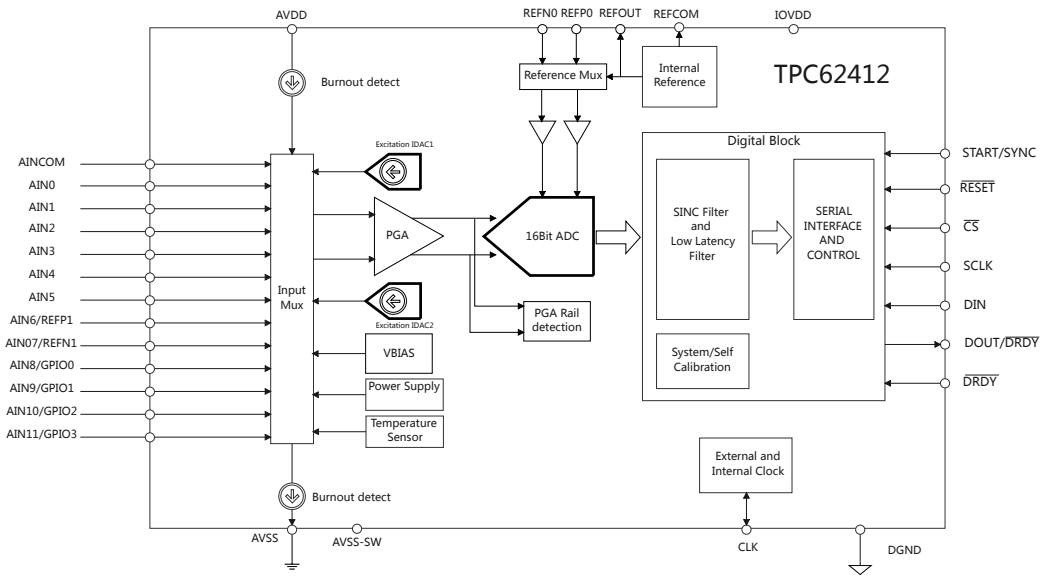


Figure 30. Functional Block Diagram

Feature Description

Multiplexer

The device contains a flexible input multiplexer; Any analog inputs can be selected as the positive or negative input for the PGA or ADC input. The AINCOM can be configured as either positive or negative input for the PGA. It functions as a standard analog input, similar to AINx. In single-ended measurement applications, AINCOM serves as the common input for the other analog inputs.

The multiplexer can also route the excitation current sources to drive external resistive sensors (bridges, RTDs, and thermistors).

The device can provide bias voltages for unbiased sensors (unbiased thermocouples for example) to analog input pins.

The device also has several system monitor functions which can be measured through the multiplexer:

- The inputs can be shorted together at mid-supply [(AVDD + AVSS) / 2] to measure and calibrate the input offset of the analog front-end and the ADC.
- The system monitor also includes a temperature sensor that provides a measurement of the device temperature.
- The system monitor can also measure the supply voltage, measuring [(AVDD – AVSS) / 4] for the analog supply.
- The system monitor contains a set of burn-out current sources that pull the inputs to either supply if the sensor has burned out and has a high impedance so that the ADC measures a full-scale reading.

Low-Noise Programmable Gain Amplifier

The device features a low-drift, low-noise, high-input impedance programmable gain amplifier (PGA). The PGA consists of two chopper-stabilized amplifiers and a resistor feedback network that sets the gain of the PGA.

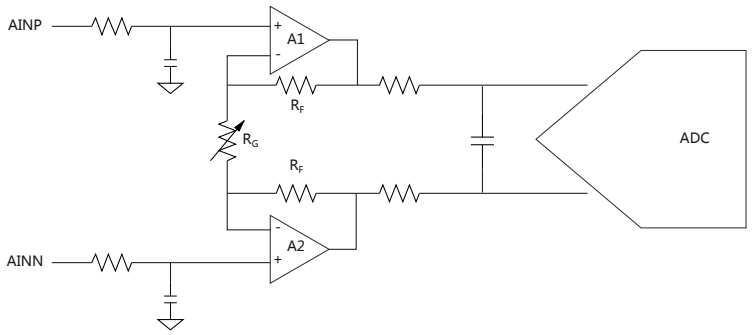


Figure 31. Simplified PGA Diagram

The PGA can be set to be 1, 2, 4, 8, 16, 32, 64, or 128 by using the GAIN[2:0] bits in the gain setting register. Gain is changed inside the device using a variable resistor, R_G. The differential full-scale input voltage range (FSR) of the PGA is defined by the gain setting and the reference voltage used, as shown in

$$FSR = \pm V_{REF}/Gain \quad (3)$$

The following is the full-scale ranges when using the internal 2.5-V reference. The PGA gains 64 and 128 are established in the digital domain. When the device is set to 64 or 128, the PGA is set to a gain of 32, and additional gain is established with digital scaling. The input-referred noise does still improve compared to the gain = 32 setting because the PGA is biased with a higher supply current to reduce noise.

Table 18. PGA Full-Scale Range

Gain Setting	FSR
1	±2.5 V
2	±1.25 V
4	±0.625 V
8	±0.313 V
16	±0.156 V
32	±0.078 V
64	±0.039 V
128	±0.020 V

The PGA can be enabled by setting corresponding values in the PGA_EN[1:0] bits of the gain setting register, and also can be disabled and bypassed.

PGA Input-Voltage Requirements

The PGA maximum and minimum absolute input voltages are limited by the voltage swing capability of the PGA output. The specified minimum and maximum absolute input voltages (V_{AINP} and V_{AINN}) depend on the PGA gain, the maximum differential input voltage (V_{INMAX}), and the tolerance of the analog power-supply voltages (AVDD and AVSS). Use the maximum voltage expected in the application for V_{INMAX}.

$$AVSS + 0.15\ V + \left|V_{INMAX}\right| \cdot (Gain - 1) / 2 < V_{AINP,}\ V_{AINN} < AVDD - 0.35\ V - \left|V_{INMAX}\right| \cdot (Gain - 1) / 2 \quad (4)$$

where V_{AINP}, V_{AINN} = absolute input voltage, $V_{INMAX} = V_{AINP} - V_{AINN}$ = maximum differential input voltage.

As mentioned in the previous section, PGA gain settings of 64 and 128 are scaled in the digital domain and are not implemented with the amplifier. When using the PGA in gains of 64 and 128, set the gain to 32 to calculate the absolute input voltage range.

PGA Rail Flags

The PGA output rail detection circuit can be enabled using the FL_RAIL_EN bit in the register. The PGA rail flags (FL_P_RAILP, FL_P_RAILN, FL_N_RAILP, and FL_N_RAILN) in the status register indicate if the positive or negative output of the PGA is closer to the analog supply rails than 150 mV. A flag going high indicates that the PGA is operating outside the linear operating or absolute input voltage range.

Bypassing the PGA

The device can be configured to disable and bypass the PGA by setting the PGA_EN[1:0] bits, and also removes the input range restrictions at a gain of 1. If the PGA is bypassed, the ADC absolute input voltage range extends beyond the AVDD and AVSS power supplies, allowing input voltages at or below ground.

In order to measure single-ended signals that are referenced to AVSS ($AIN_P = V_{IN}$, AIN_N = AVSS), the PGA must be bypassed.

Voltage Reference

The device offers an integrated low-drift 2.5-V reference, and for applications that require a different reference voltage value or a ratio metric measurement approach, the device offers two differential reference input pairs (REFP0, REFN0 and REFP1, REFN1).

For external reference, the reference voltage is:

$$V_{REF} = V_{(REFPx)} - V_{(REFNx)} \quad (5)$$

Where $V_{(REFPx)}$ and $V_{(REFNx)}$ are the absolute positive and absolute negative reference voltages.

The polarity of the reference voltage internal to the ADC must be positive. The magnitude of the reference voltage together with the PGA gain establishes the ADC full-scale differential input range as defined by FSR = $\pm V_{REF}$/ Gain.

The ADC also contains an integrated reference voltage monitor. This monitor provides continuous detection of a low or missing reference during the conversion cycle. The reference monitor flags (FL_REF_L0 and FL_REF_L1) are set in the STATUS byte.

Internal Reference

The ADC integrates a precision, low-drift, 2.5-V reference. By default, the internal voltage reference is powered down, and can be enabled with setting corresponding registers.

The REFOUT pin provides a buffered reference output voltage when the internal reference voltage is enabled. Suggest connecting a capacitor between REFOUT and AVSS. The larger capacitor can filter more noise at the expense of a longer reference start-up time.

The capacitor is not required if the internal reference is not used. The internal reference must be enabled when using the IDACs.

External Reference

The device provides two external reference inputs, which are differential with independent positive and negative inputs.

Internal or external reference buffers can be used to reduce the input current. Without buffering, the reference input current can lead to errors from either high reference source impedance or through reference input filtering.

Be careful that the specified absolute and differential reference voltage requirements should be followed when using internal or external references.

Reference Buffers

The device has two individually selectable reference input buffers to lower the reference input current. Use the $\overline{\text{REFP\_BUF}}$ and $\overline{\text{REFN\_BUF}}$ bits to enable or disable the positive and negative reference buffers respectively.

The reference buffers are recommended to be disabled when the internal reference is selected, or when the external reference input is at the supply voltage (REFPx at AVDD or REFNx at AVSS).

Clock Source

The clock of the device is either provided by the internal low-drift oscillator or an external clock source on the CLK input, which can be selected by the register. The internal oscillator is used by default after power up. If the device is reset, either via the $\overline{\text{RESET}}$ pin or the RESET command, the clock source defaults back to the internal oscillator, even if an external clock was previously selected.

Delta-Sigma Modulator

A high-order delta-sigma (ΔΣ) modulator is used to convert the analog input voltage into a data stream. The modulator runs at a clock frequency of $f_{MOD} = f_{CLK}/ 16$, where f_{CLK} is either provided by the internal oscillator or the external clock source.

Digital Filter

The device offers a sinc filter and a low-latency filter for both filtering and decimation of the digital data stream coming from the delta-sigma modulator. The implementation of the digital filter is determined by the data rate and filter mode.

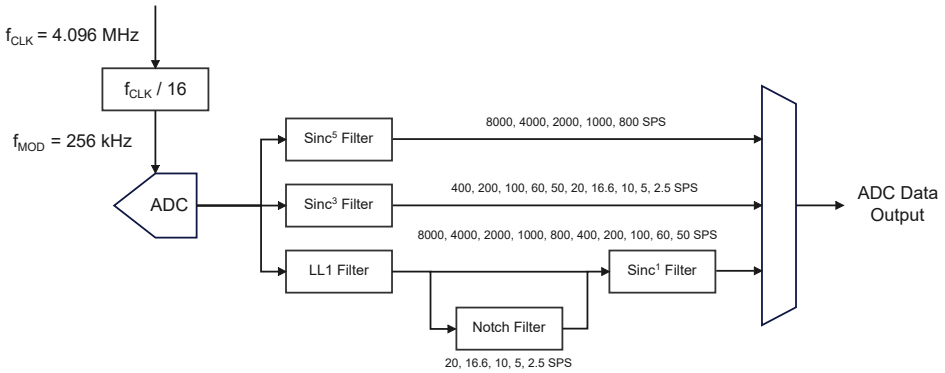


Figure 32. Digital Filter Architecture

Regardless of the FILTER type setting, the oversampling ratio is the same for each given data rate, meaning that the device requires a set number of modulator clocks to output a single ADC conversion data. The output data rate and corresponding oversampling ratio are shown below:

Table 19. ADC Data Rate and Digital Filter Oversampling Ratio

Nominal Data Rate (SPS) (1)	Data Rate Registers DR[3:0]	Oversampling Ratio (2)
2.5	0000	102400
5	0001	51200
10	0010	25600
16.6	0011	15360
20	0100	12800
50	0101	5120
60	0110	4264
100	0111	2560
200	1000	1280
400	1001	640
800	1010	320
1000	1011	256
2000	1100	128
4000	1101	64
8000	1110	32
8000	1111	32

(1) Applies to either the internal oscillator or an external 4.096 MHz clock.
(2) The oversampling ratio is f_{MOD} divided by the data rate; $f_{MOD} = f_{CLK} / 16$.

Low-Latency Filter

The low-latency filter can be selected by the FILTER bit. The filter is a finite impulse response (FIR) filter that provides settled data, given that the analog input signal has settled to the final value before the conversion is started. The low-latency filter is especially useful when multiple channels must be scanned in minimal time.

Low-Latency Filter Frequency Response

When the low-latency filter is selected, it provides both 50-Hz and 60-Hz line cycle noise rejection at data rate options at 2.5 SPS, 5 SPS, 10 SPS, and 20 SPS.

The following is the frequency response of the low-latency filter for different data rates.

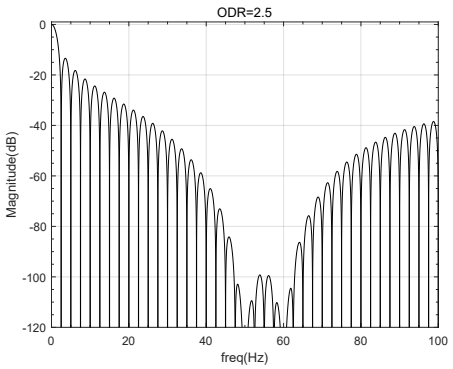


Figure 33. Low-Latency Filter Frequency Response, Data Rate = 2.5 SPS

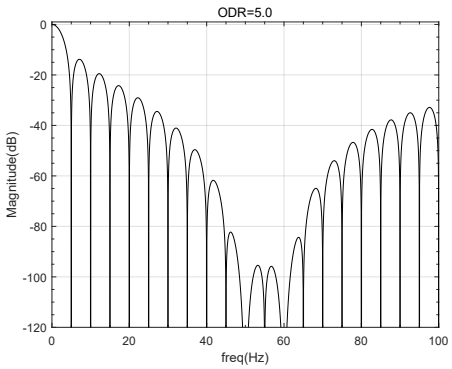


Figure 34. Low-Latency Filter Frequency Response, Data Rate = 5 SPS

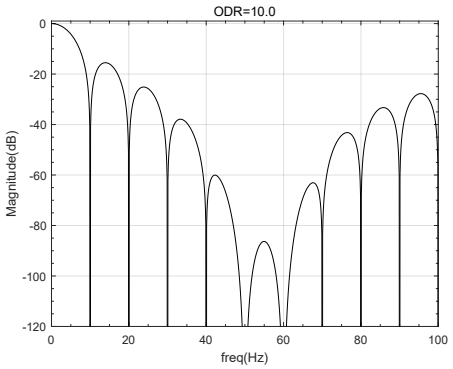


Figure 35. Low-Latency Filter Frequency Response, Data Rate = 10 SPS

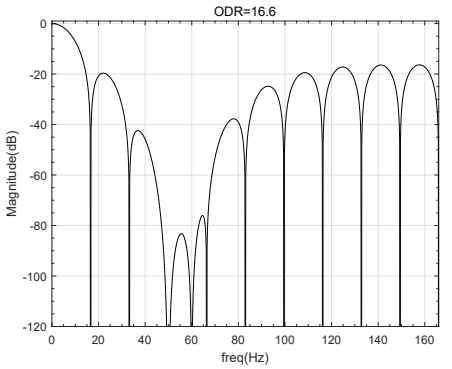


Figure 36. Low-Latency Filter Frequency Response, Data Rate = 16.6 SPS

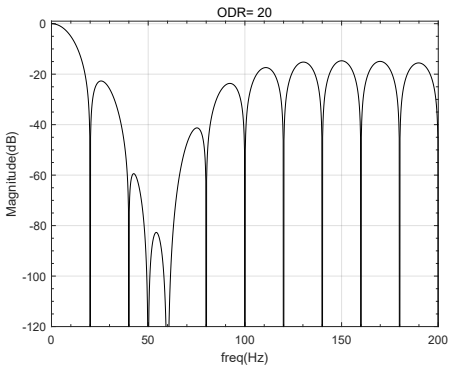


Figure 37. Low-Latency Filter Frequency Response, Data Rate = 20 SPS

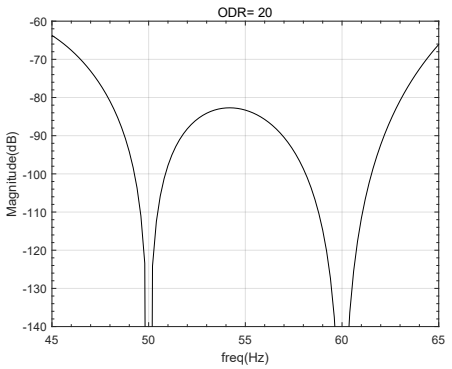


Figure 38. Low-Latency Filter Frequency Response, Data Rate = 20 SPS, Zoomed to 50 Hz and 60 Hz

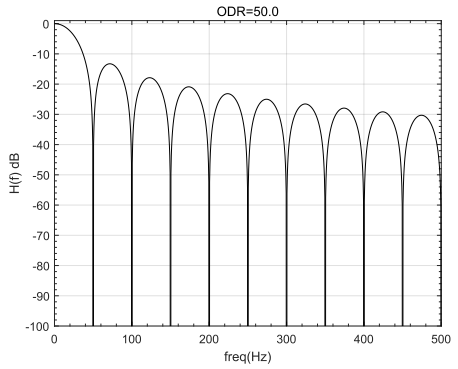


Figure 39. Low-Latency Filter Frequency Response, Data Rate = 50 SPS

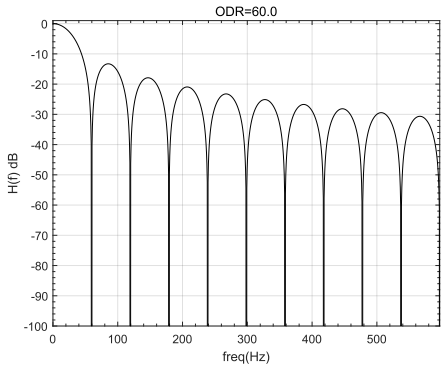


Figure 40. Low-Latency Filter Frequency Response, Data Rate = 60 SPS

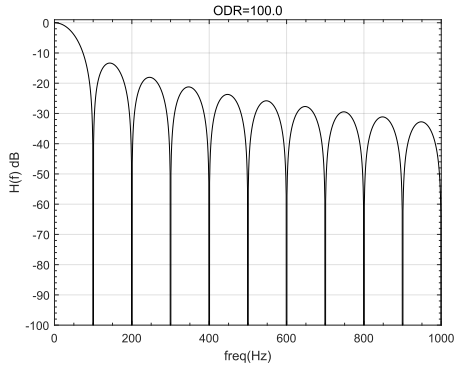


Figure 41. Low-Latency Filter Frequency Response, Data Rate = 100 SPS

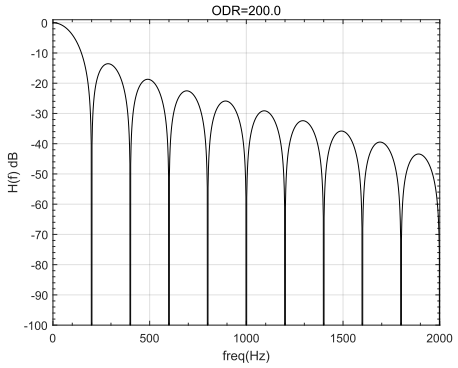


Figure 42. Low-Latency Filter Frequency Response, Data Rate = 200 SPS

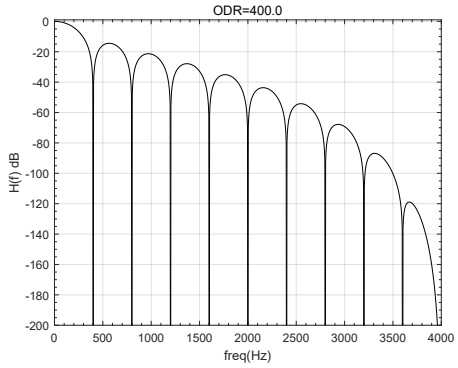


Figure 43. Low-Latency Filter Frequency Response, Data Rate = 400 SPS

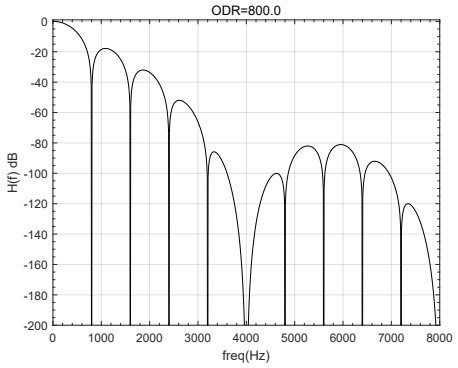


Figure 44. Low-Latency Filter Frequency Response, Data Rate = 800 SPS

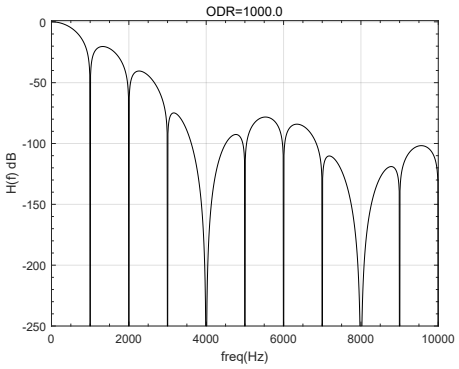


Figure 45. Low-Latency Filter Frequency Response, Data Rate = 1 kSPS

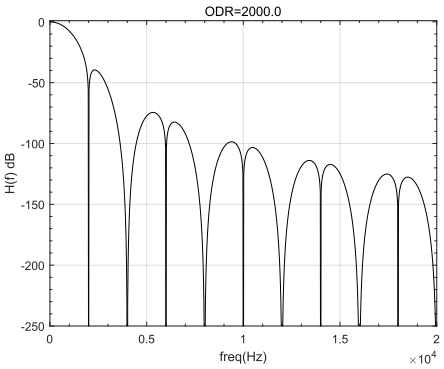


Figure 46. Low-Latency Filter Frequency Response, Data Rate = 2 kSPS

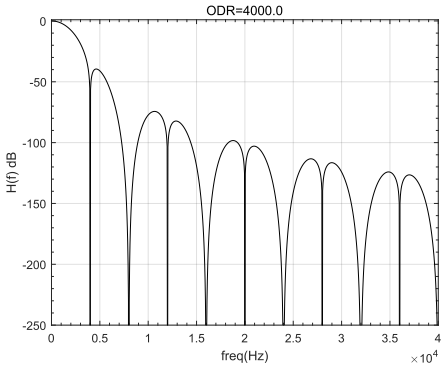


Figure 47. Low-Latency Filter Frequency Response, Data Rate = 4 kSPS

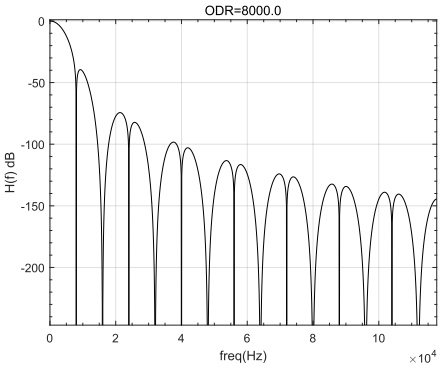


Figure 48. Low-Latency Filter Frequency Response, Data Rate = 8 kSPS

The following is the bandwidth of the low-latency filter for each data rate.

Nominal Data Rates (SPS) (1)	–3-dB Bandwidth (Hz) (1)
8000	2568.66
4000	1284.33
2000	642.02
1000	401.08
800	331.92
400	174.19
200	88.21
100	44.25
60	26.43
50	22.14
20	8.85
16.67	7.38
10	4.43
5	2.21

Nominal Data Rates (SPS) (1)	–3-dB Bandwidth (Hz) (1)
2.5	1.11

(1) Applies to the internal oscillator or an external 4.096-MHz clock. Scales proportional with f_{CLK}.

Please note that the low-latency filter notches and output data rate scale proportionally with the clock frequency. When external clock frequency is used, the data rate, conversion time, and filter notches will vary consequently.

Data Conversion Time for the Low-Latency Filter

The data settles in one data period when the low-latency filter is selected. However, a small amount of latency exists to calculate the conversion data from the modulator and do other operations. So the first conversion data takes a little bit longer than subsequent data conversions.

The following table shows the conversion times for the low-latency filter in each data rate and various conversion modes.

Table 20. Data Conversion Time for the Low-Latency Filter

Nominal Data Rate (1) (SPS)	First Data for Continuous Conversion Mode or Single-Shot Conversion Mode (ms) (2)	Second and Subsequent Conversions for Continuous Conversion Mode (ms) (2)
8000	0.4525	0.128
4000	0.8385	0.256
2000	1.6065	0.512
1000	2.1185	1.024
800	2.3745	1.28
400	3.6545	2.56
200	6.2145	5.12
100	11.3345	10.24
60	18.2465	17.152
50	21.5745	20.48
20	55.3665	51.2
16	65.6065	61.44
10	106.5665	102.4
5	208.9665	204.8
2.5	413.7665	409.6

(1) Applies to the internal oscillator or an external 4.096-MHz clock. Scales proportional with f_{CLK}.
(2) The time does not include the programmable delay configured by the DELAY[2:0] bits in the gain setting register. When using Global Chop Mode, two conversions are required, effectively doubling the additional time.

SincN Filter

The sincN digital filter is also available. Compared with low-latency filter, it has improved noise performance but has a N-cycle latency to get data out.

SincN Filter Frequency Response

The sincN digital filter's response scales with the data rate and has notches at multiples of the data rate. It has simultaneous 50-Hz and 60-Hz rejection at data rates of 2.5 SPS, 5 SPS, and 10 SPS. And it has only 50-Hz rejection at data rates of 16.6 SPS and 50 SPS, and only 60-Hz rejection at data rates of 20 SPS and 60 SPS.

The following is the frequency response of the low-latency filter for different data rates.

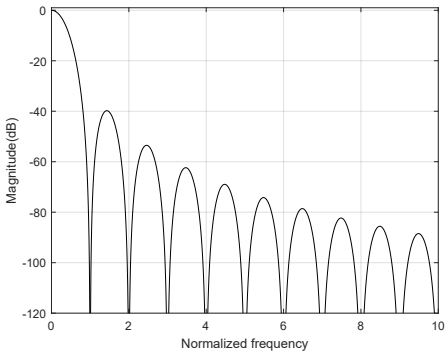


Figure 49. Sinc^3 Filter Frequency Response, Normalized to Data Rate

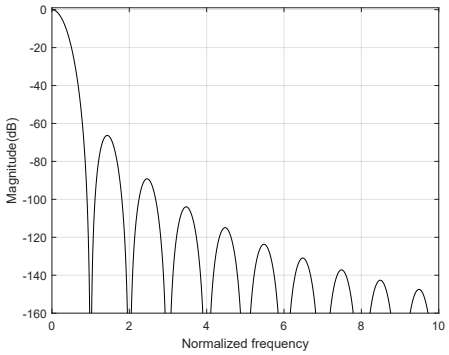


Figure 50. Sinc^5 Filter Frequency Response, Normalized to Data Rate

The following is the bandwidth of the sincN filter for each data rate.

Nominal Data Rate (SPS) (1)	–3-dB Bandwidth (Hz) (1)
8000	1630.80
4000	815.40
2000	407.70
1000	203.85
800	163.08
400	104.78
200	52.39
100	26.19
60	15.72
50	13.10
20	5.24
16.67	4.37
10	2.62
5	1.31
2.5	0.65

(1) Applies to the internal oscillator or an external 4.096-MHz clock. Scales proportional with f_{CLK}. Filter notches and output data rate scale proportionally with the clock frequency.

Data Conversion Time for the SincN Filter

The sincN filter normally takes 5 (for ODR ≥ 800 SPS) or 3 (for ODR ≤ 400 SPS) conversions to settle, and it needs different amounts of time to complete a conversion.

The following is the conversion times for the sincN filter for each ADC data rate and various conversion modes

Nominal Data Rate (1) (SPS)	First Data for Continuous Conversion Mode or Single-Shot Conversion Mode (2) (ms)	Second and Subsequent Conversions for Continuous Conversion Mode (3) (ms)
8000	0.708	0.128
4000	1.35	0.256
2000	2.63	0.512
1000	5.19	1.024
800	6.47	1.28
400	7.75	2.56
200	15.43	5.12
100	30.79	10.24
60	51.238	17.056
50	61.51	20.48
20	153.67	51.2
16	184.39	61.44
10	307.27	102.4
5	614.47	204.8
2.5	1228.87	409.6

(1) Applies to the internal oscillator or an external 4.096-MHz clock. Scales proportional with f_{CLK}.
(2) The time does not include the programmable delay configured by the DELAY[2:0] bits in the gain setting register. When using Global Chop Mode, two conversions are required, effectively doubling the additional time.
(3) Subsequent readings in continuous conversion mode do not have the programmable delay time.

Note on Conversion Time

There is a programmable conversion delay which can be added before the conversion starts. This delay allows for additional settling time for input filtering on the analog inputs and for the antialiasing filter after the PGA. Also, overhead time is needed to convert the modulator samples into an ADC conversion result. This overhead time includes any necessary offset or gain compensation after the digital filter to get the final data result.

The first conversion time when the device is in continuous conversion mode, or each conversion time in single-shot conversion mode, includes the programmable conversion delay, the modulator sampling time, and the overhead time. The second and subsequent conversions in continuous mode are the normal data period (period corresponding to the data rate).

50-Hz and 60-Hz Line Cycle Rejection

The digital filter provides enhanced rejection of coupled noise for data rates of 60 SPS and less. Please refer to the digital filter sections for frequency response. Configure the filter to tradeoff data rate and conversion latency against the required level of line cycle rejection. The tables below provide details on the ADC's 50 Hz and 60 Hz line-cycle rejection performance, considering ±1 Hz and ±2 Hz tolerances between the power-line and ADC clock frequencies. The best possible rejection ratio can be obtained by using an accurate ADC clock.

Table 21. Low-Latency Filter, 50-Hz and 60-Hz Line Cycle Rejection

Data Rate (SPS) (1)	Low-Latency Digital Filter Line Cycle Rejection (dB)			
	50 Hz ± 1 Hz	60 Hz ± 1 Hz	50 Hz ± 2 Hz	60 Hz ± 2 Hz
2.5	–112.4	–114.3	–103.4	–104.9
5	–110.9	–112.5	–93.2	–94.8
10	–110.2	–112.3	–91.4	–93.0
16.6	–109.7	–99.5	–91.0	–87.5
20	–94.3	–111.0	–81.1	–92.7
50	–34.0	–15.8	–27.8	–15.3
60	–15.0	–33.6	–13.9	–28.9

(1) f_{CLK} = 4.096 MHz.

Table 22. SincN Filter, 50-Hz and 60-Hz Line Cycle Rejection

Data Rate (SPS) (1)	Sincn Digital Filter Line Cycle Rejection (dB)			
	50 Hz ± 1 Hz	60 Hz ± 1 Hz	50 Hz ± 2 Hz	60 Hz ± 2 Hz
2.5	–108.9	–113.5	–121.5	–127.5
5	–103.2	–107.9	–90.3	–95.2
10	–102.0	–106.7	–84.7	–89.7
16.6	–101.8	–63.9	–83.6	–63.1
20	–53.7	–106.1	–54.1	–88.3
50	–101.8	–46.9	–83.0	–45.5
60	–41.0	–105.6	–38.5	–88.2

(1) f_{CLK} = 4.096 MHz.

Global Chop Mode

The device employs a very low-drift PGA and modulator to achieve minimal input voltage offset drift. However, a small offset drift may still be present during normal measurements. To further reduce offset voltage and drift, the ADC includes a global chop feature.

The global chop mode can be enabled using the G_CHOP bit. When the global chop is enabled, the ADC performs two internal conversions to cancel the input offset voltage. The first conversion is taken with normal input polarity. Then the ADC reverses the internal input polarity and does a second conversion. Finally, the average of the two conversions is given out as the final result, removing the offset voltage.

In global chop mode, sequences are similar to taking consecutive single-shot conversions and swapping the input on each conversion. In continuous conversion mode with the global chop mode enabled, the first conversion result is available after the ADC takes two separate conversions with settled data, and subsequent conversions completed in half the time as the first conversion is completed. Conversion times in global chop mode are specified below.

Table 23. Data Conversion Time for Global Chop Mode Using the Low-Latency Filter

Nominal Data Rate (1) (SPS)	First Data Conversion Period for Global Chop Mode (ms) (2)
8000	0.8945

Nominal Data Rate (1) (SPS)	First Data Conversion Period for Global Chop Mode (ms) (2)
4000	1.6665
2000	3.2025
1000	4.2265
800	4.7385
400	7.2985
200	12.4185
100	22.6585
60	36.4825
50	43.1385
20	110.7225
16	131.2025
10	213.1225
5	417.9225
2.5	827.5225

(1) Applies to the internal oscillator or an external 4.096-MHz clock. Scales proportional with f_{CLK}.
(2) The time does not include the programmable delay configured by the DELAY[2:0] bits in the gain setting register. When using Global Chop Mode, two conversions are required, effectively doubling the additional time.

Table 24. Data Conversion Time for Global Chop Mode Using the Sinc Filter

Nominal Data Rate (1) (SPS)	Conversion Period for Global Chop Mode (ms) (2)
8000	1.406
4000	2.69
2000	5.25
1000	10.37
800	12.93
400	15.49
200	30.85
100	61.57
60	102.466
50	123.01
20	307.33
16	368.77
10	614.53
5	1228.93
2.5	2457.73

(1) Applies to the internal oscillator or an external 4.096-MHz clock. Scales proportional with f_{CLK}.
(2) The time does not include the programmable delay configured by the DELAY[2:0] bits in the gain setting register. When using Global Chop Mode, two conversions are required, effectively doubling the additional time.

In global chop mode, if the data rate in use has 50-Hz and 60-Hz frequency response notches, the null frequencies remain unchanged.

The global chop mode also reduces the ADC noise by a factor of √2 because two conversions are averaged.

If necessary, the programmable conversion delay should be increased for settling of external components.

Excitation Current Sources (IDACs)

The device provides two matched current sources, which can be used as excitation current to resistive temperature devices (RTDs), thermistors, diodes, and other resistive sensors that require constant current biasing, to reduce system complexity. The current sources are programmable to output values between 10 μA to 2000 μA by IMAG registers. Each current source can be assigned to any of the analog inputs (AINx). Both current sources can also be connected to the same pin. The IDAC routing is controlled by the internal multiplexer and is configured in the excitation current register.

The internal reference should be enabled for IDAC operation. And the IDAC requires voltage headroom for the positive supply to operate. This voltage headroom is the compliance voltage.

Bias Voltage Generation

The device has an internal bias voltage generator which can be set to two different levels, (AVDD + AVSS) / 2 and (AVDD + AVSS) / 12 in the sensor biasing register. The bias voltage is internally buffered and can be applied to analog inputs AIN0 through AIN5 and AINCOM. The VBIAS can be used to bias thermocouples to within the common-mode voltage range of the PGA. The start-up time of the VBIAS voltage depends on the pin load capacitance.

System Monitor

The TPC62412 includes system monitor functions that can measure device temperature, monitor analog and digital power supplies, or use current sources to detect sensor malfunctions. These systems monitor functions are enabled in the system control register.

Internal Temperature Sensor

The internal temperature sensor can be selected by input multiplexer. The temperature sensor outputs a voltage proportional to the temperature as specified in the electrical characteristic table.

If enabled, PGA gain should be set to 4 for the temperature sensor measurement to remain within the allowed absolute input voltage range of the PGA.

Power Supply Monitors

The device provides monitor functions for the analog and digital interface power supply (AVDD and IOVDD), which can be selected by the the SYS_MON register.

The power-supply voltages are divided by a resistor network to reduce the voltages to within the ADC input range, (AVDD – AVSS) / 4 and IOVDD/4. When the supply voltage monitor is enabled, the analog inputs are disconnected from the ADC, and the PGA gain is fixed at 1, regardless of settings in the gain setting register. Supply voltage monitoring can be performed with the PGA, which can be either enabled or disabled. For accurate power supply measurements, the reference voltage must exceed the measured power supply levels in the above scaled power-supply readings.

Burn-Out Current Sources

The device provides Burn Out Current Source (BOCS) which can be enabled by SYS_MON registers. The current can be used to detect external sensor malfunctions. Current sources can be set to 0.2 μA, 1 μA, and 10 μA.

When enabled, one BOCS sources current is routed to the selected positive analog input (AIN_P) and the other BOCS sinks current from the selected negative analog input (AIN_N). If there is an open circuit in a burned-out sensor, these BOCSs pull the positive input towards AVDD and the negative input towards AVSS, resulting in a full-scale reading. A full-scale reading can also indicate that the sensor is overloaded, or the reference voltage is absent. A near-zero reading can indicate a shorted sensor.

When burn-out current sources are enabled, they can interfere with ADC readings of a functioning sensor. It's recommended to disable the burn-out current sources during precision measurements, enabling them only to check for sensor fault conditions. If global chop mode is active, it should be disabled before taking a measurement with the burn-out current sources.

Status Register

The TPC6241 includes a one-byte status register containing flags that indicate fault conditions. This status byte can be read directly from the status register or prepended to each ADC data read as the first byte by setting the SENDSTAT bit to 1 in the system control register.

The following sections explain the various fault conditions flagged within the STATUS byte. Flags for the PGA output voltage rail monitors and reference monitor are updated after each conversion, with the STATUS byte reflecting the flags from the most recent conversion cycle.

POR Flag

Once the power supplies are activated, the ADC stays in reset mode until the AVDD, IOVDD, and analog power supply (AVDD – AVSS) voltages surpass their respective power-on reset (POR) voltage thresholds. If a POR event occurs, the FL_POR flag is set to indicate that a POR event has taken place and has not yet been cleared. This flag can be cleared by writing to the user register to reset the bit to 0.

$\overline{\text{RDY}}$ Flag

The $\overline{\text{RDY}}$ flag indicates that the device has started up and is ready to receive a configuration change. During a reset or power-on reset (POR) event, the device resets the register map and may not be available for operation.

PGA Output Voltage Rail Monitors

The PGA includes an integrated output voltage monitor that triggers a flag if the PGA output voltage exceeds AVDD – 0.15 V or falls below AVSS + 0.15 V, indicating that the output has exceeded the output range of the PGA. Both V_{OUTN} and V_{OUTP} outputs can trigger overvoltage or undervoltage flags, resulting in a total of four flags. The PGA output voltage rail monitors are activated using the FL_REF_EN bit in the excitation current register. If the PGA is bypassed, the rail monitor remains operational and continues to sense the connection at the ADC input.

The PGA output voltage rail monitors are:

- FL_P_RAILP: V_{OUTP} has exceeded AVDD – 0.15 V
- FL_P_RAILN: V_{OUTP} dropped below AVSS + 0.15 V
- FL_N_RAILP: V_{OUTN} has exceeded AVDD – 0.15 V
- FL_N_RAILN: V_{OUTN} dropped below AVSS + 0.15 V

The flags are updated (set or cleared) only at the end of a conversion cycle. And a fault is latched during a conversion cycle.

Reference Monitor

The user has the option to continuously monitor the ADC reference inputs for conditions such as a shorted or missing reference voltage. The reference detection circuit features two thresholds: the first at 300 mV and the second at 1/3 of (AVDD – AVSS). This circuit measures the differential reference voltage and sets a flag in the STATUS byte, which is latched after each conversion, if the voltage falls below the specified thresholds. A reference voltage below 300 mV may indicate a potential short on the reference inputs or, in the case of a ratio metric RTD measurement, a broken connection between the RTD and the reference resistor.

Additionally, a resistor of 10 MΩ can be connected between the selected REFPx and REFNx inputs. The resistor can be used to detect a floating reference input. With a floating input, the resistor pulls both reference inputs to the same potential so that the reference detection circuit can detect this condition. The pull-together reference resistor is not recommended to be continuously connected to active reference inputs. This resistor lowers the input impedance of the reference inputs and can contribute the gain error to the measurement.

The reference detection circuits must be activated using the FL_REF_EN[1:0] bits in the reference control register. The FL_REF_L0 flag indicates whether the reference voltage is below 0.3 V, while the FL_REF_L1 flag indicates if the reference voltage is lower than 1/3 of (AVDD – AVSS). Reference monitor faults are latched during each conversion cycle, and the flags in the status register are updated at the falling edge of $\overline{DRDY}$.

General-Purpose Inputs and Outputs (GPIOs)

The TPC62412 features four pins (AIN8 to AIN11) that can function as either analog inputs or general-purpose input/output (GPIO) pins.

The functionality of the GPIO pins is managed by two registers. To configure a pin as a GPIO, use the CON[3:0] bits in the GPIO configuration register. The upper four bits (DIR[3:0]) of the GPIO data register determine whether the GPIO pin is set as an input or an output. The lower four bits (DAT[3:0]) of the GPIO data register hold the input or output data for the GPIO pins. When a GPIO pin is configured as an input, the corresponding DAT[x] bit reflects the status of the pin; if configured as an output, write the desired output status to the respective DAT[x] bit.

It's important to note that when a pin is configured as a GPIO, the corresponding logic is powered by AVDD and AVSS. If the device is operated with bipolar analog supplies, the GPIO outputs produce bipolar voltages. Care should be taken to avoid loading the GPIO pins when they are used as outputs, as excessive current can lead to droop or noise on the analog supplies.

Low-Side Power Switch

The device includes an integrated low-side power switch with low on-resistance that connects REFN0 to AVSS-SW. This power switch is designed to help reduce system power consumption in resistive bridge sensor applications by powering down the bridge circuit between conversions. When the PSW bit in excitation current register 1 is set to 1, the switch closes, powering the bridge. The switch automatically opens when the POWER DOWN command is issued or can be opened manually by setting the PSW bit to 0. By default, the switch remains open. It is important to connect AVSS-SW to AVSS.

Cyclic Redundancy Check (CRC)

The device has a checksum mode that can be used to improve interface robustness. The checksum mode ensures that only valid data is written to a register and data read is validated.

If an error occurs during a register write, the CRC_ERROR bit is set in the status register. To ensure that the register write was successful, it is important to read back the register and verify the checksum.

During a write operation, the checksum is calculated using the 8-bit command word and the 8- to 24-bit data, and the following polynomial is always used for CRC checksum calculations:

$$x^8 + x^2 + x + 1 \quad (6)$$

During read operations, the checksum is calculated using the command word and the 8- to 32-bit data output. Users can select between the above polynomial and a similar XOR function by CRC_EN bits. The XOR function requires less time for the host microcontroller to process than the polynomial-based checksum.

The 8-bit checksum is appended to the end of each read-and-write transaction. The following shows SPI write and read transactions, respectively.

Calibration

The ADC features offset and gain calibration commands, along with user-offset and full-scale (gain) calibration registers, each 24 bits wide, for ADC calibration. This calibration can correct internal ADC errors or system-level errors. You can initiate calibration either by sending calibration commands to the ADC or by direct user calibration, where calculated correction values are written directly to the calibration registers. The ADC supports self-calibration, system-offset calibration, and

system gain calibration; perform offset calibration before system gain calibration. After power-on, allow time for the power supplies and reference voltage to stabilize before beginning calibration.

The offset calibration register value is subtracted from the filter output and then multiplied by the full-scale register value divided by 400000h. The result is clipped to a 24-bit value to yield the final output. Calibration commands are unavailable when the device is in standby mode, which occurs when the START/SYNC pin is low or when the STOP command is issued.

Offset Calibration

The offset calibration word is a 24-bit, twos complement value distributed across three 8-bit registers, starting with offset calibration register 1. The maximum positive value is 7FFFFFh, and the maximum negative value is 800000h. This offset value is subtracted from each output reading for offset correction. A register value of 000000h indicates no offset correction. If global chop mode is enabled, the offset calibration register is bypassed. The table below provides example settings for the offset register.

Table 25. Offset Calibration Register Values

OFC[2:0] REGISTER VALUE	OFFSET CALIBRATED OUTPUT CODE(1)
000001h	FFFFFFh
000000h	000000h
FFFFFFh	000001h

(1) Ideal output code with shorted input, excluding ADC noise and offset voltage error.

The user can choose the number of samples to average for self or system offset calibration (1, 4, 8, or 16 samples) by setting the CAL_SAMP[1:0] bits in the system control register. Selecting fewer samples reduces calibration time but may compromise accuracy. Averaging more samples increases calibration time but improves accuracy by reducing noise.

Two commands are available for performing offset calibration. The SFOCAL command initiates a self-offset calibration, which internally sets the input to mid-scale by configuring SYS_MON[2:0] = 001 and measures the offset. The SYOCAL command performs a system offset calibration, where the user must apply a null voltage to measure and correct the system offset. Upon executing either command, the OFC register is updated with the new offset calibration value.

After an offset calibration is complete, the device automatically starts a new conversion, and the $\overline{\text{DRDY}}$ pin falls to signal that the conversion has finished.

Gain Calibration

The full-scale (gain) calibration word is a 24-bit straight binary value, spread across three 8-bit registers, starting with gain calibration register 1. This value is normalized to a unity-gain correction factor when the register value is set to 400000h. The table below provides register values for specific gain factors. When performing gain calibration, ensure that the input remains within the limits of the PGA input range to avoid errors.

Table 26. Offset Calibration Register Values

FSCAL[2:0] REGISTER VALUE	GAIN FACTOR
433333h	1.05
400000h	1.00
3CCCCCh	0.95

The SYGCAL command initiates a system gain calibration, requiring the user to apply a full-scale input to measure and correct gain error. Once SYGCAL is issued, the FSC register is updated with the new gain calibration value. The number of samples used for gain calibration is set by the CAL_SAMP[1:0] bits, similar to offset calibration.

The following a gain calibration, the device automatically begins a new conversion, with the $\overline{\text{DRDY}}$ pin falling to signal the completion of this conversion.

Device Functional Modes

The device has three operating modes: power-down, standby, and conversion mode. The figure below provides a flowchart that illustrates these operating modes and the transitions between them.

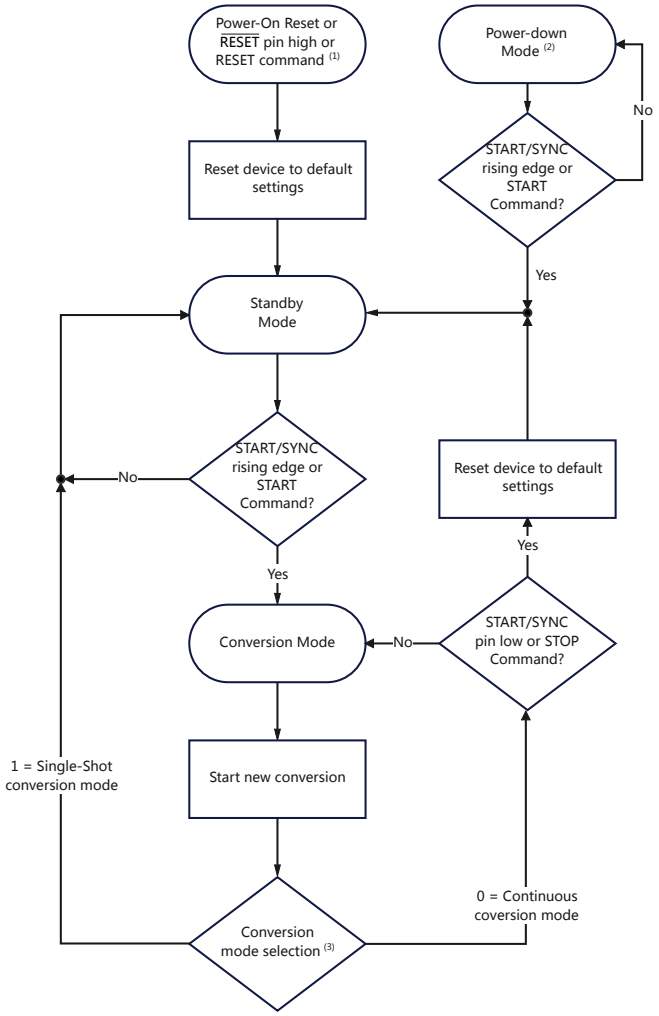


Figure 51. Operating Flow Chart

(1) Any reset (power-on, command, or pin), immediately resets the device.
(2) The POWERDOWN command halts any ongoing conversion and immediately places the device into power-down mode.
(3) Conversion mode is set by configuring the MODE bit in the data rate register.
(4) A rising edge on the START/SYNC pin or issuing the START command initiates a new conversion, interrupting any ongoing conversion.

Reset

The TPC62412 is reset in one of three ways:

- Power-on reset
- $\overline{\text{RESET}}$ pin
- $\overline{\text{RESET}}$ command

Upon a reset, all configuration registers return to their default values, and the device enters standby mode. It then awaits a rising edge on the START/SYNC pin or a START command to transition into conversion mode. If the device was previously using an external clock, the reset defaults it back to the internal oscillator.

Power-On Reset

The TPC62412 includes a power-on reset (POR) circuit that keeps the device in reset until all supply voltages reach approximately 1.65 V. This POR ensures the device starts in a known state, especially in cases of brown-out events where supply voltages dip below the minimum operating levels. After completing a POR sequence, the FL_POR flag in the status register is set high to indicate a POR event occurred.

Wait at least 2.2 ms after supply voltages stabilize before initiating communication with the device, except when polling the status register's $\overline{RDY}$ bit. If polling the $\overline{RDY}$ bit during this time, use an SCLK rate at half of the maximum specified rate to ensure correct readings as the device completes its internal configuration. This 2.2 ms delay is necessary for the internal oscillator to start up and finalize internal configurations. Once set, the $\overline{RDY}$ bit in the status register is cleared to 0, signaling that the device is ready for user configuration.

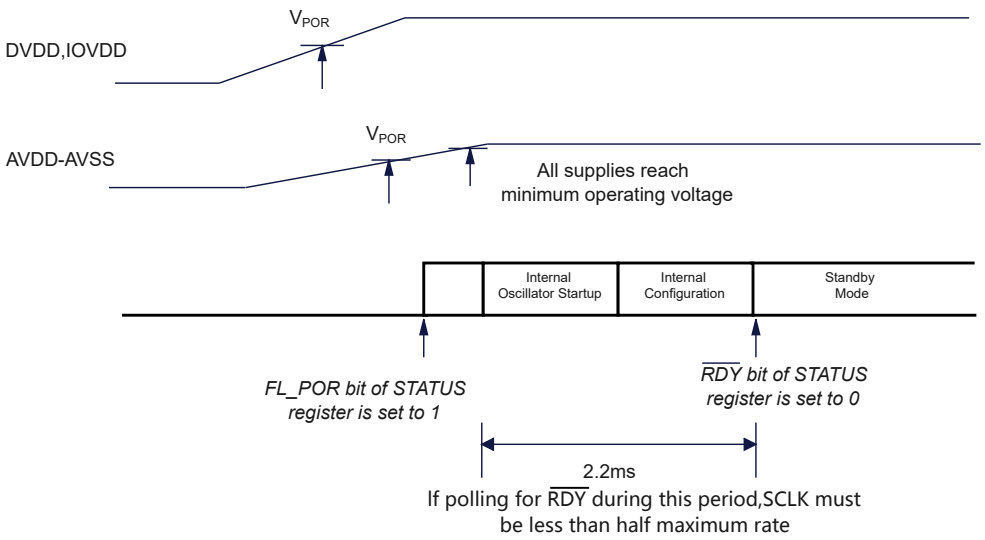


Figure 52. Power-On Reset Timing Sequence

Reset Pin

To reset the ADC, pull the $\overline{RESET}$ pin low for at least 4 clock cycles ($4 \cdot t_{CLK}$) and then return it to high. After the RESET pin's rising edge, allow a delay of $t_{d(RSSC)}$ before issuing the first serial interface command or initiating a conversion.

Reset by Command

To reset the ADC, you can also use the RESET command, which is decoded on the seventh falling edge of SCLK. After issuing the RESET command, wait for a delay of $t_{d(RSSC)}$ before sending any serial interface commands or starting a conversion.

Power-Down Mode

To enter power-down mode, issue the POWERDOWN command. In this mode, all analog and digital circuitry is turned off to minimize power consumption, independent of register settings. The internal voltage reference can optionally stay

active during power-down if a quicker start-up is needed. All configuration register values are preserved, and they remain accessible for read and write operations. To exit power-down mode, issue a WAKEUP command to transition to standby mode.

Upon issuing the POWER DOWN command, the device enters power-down mode $2 \cdot t_{CLK}$ after the seventh falling SCLK edge of the command. For optimal power saving on IOVDD, it is advisable to stop the external clock while in power-down mode, as the device does not automatically gate the external clock. Switching to the internal oscillator before entering power-down mode is recommended.

To exit POWERDOWN mode, issue the WAKEUP command, which transitions the device to standby mode. From there, the device waits for the rising edge of the START/SYNC pin or a START command to enter conversion mode.

While in power-down mode, the device still responds to the RREG, RDATA, and WAKEUP commands. However, the WREG and RESET commands is ignored until the WAKEUP command is issued, and the internal oscillator resumes operation. This ensures that the device can only be reconfigured or reset after it has exited power-down mode and is fully powered up.

Standby Mode

The TPC2410 device offers a variety of low-power modes, including power-down and standby modes, to optimize energy consumption. In standby mode, the device automatically enters this state when no conversion is ongoing. Several features can be powered down to reduce power consumption:

- The PGA can be disabled through the PGA_EN register.
- The internal reference can be turned off by adjusting the REFCON register.
- The digital filter is held in reset.
- The modulator and digital core clock are gated to reduce switching losses.

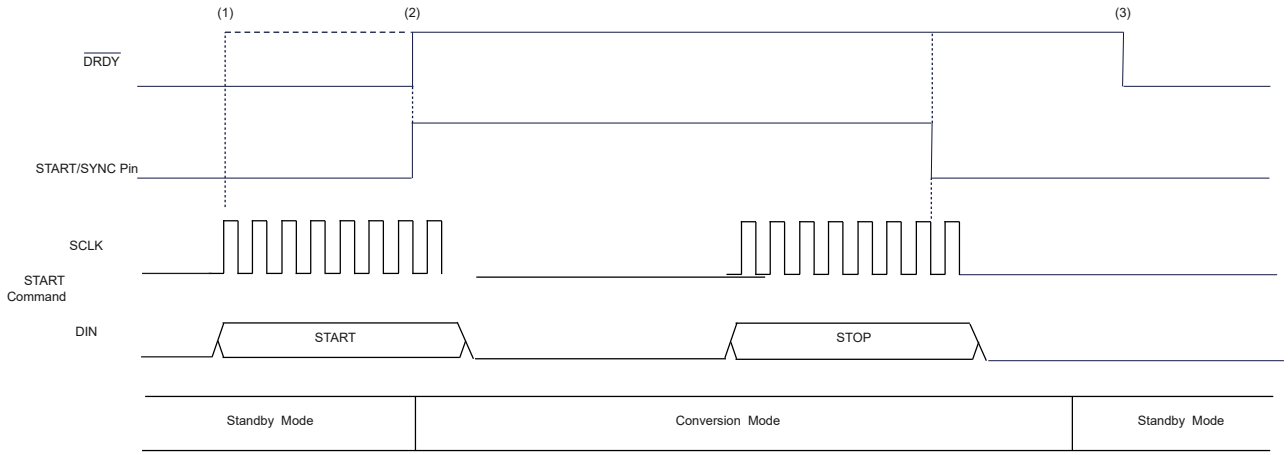
When the device is powered down in standby mode, certain components like the PGA and internal reference need additional time to power up before conversions can start. Additionally, calibration commands do not be processed in standby mode.

Conversion Mode

The TPC62412 provides two conversion modes: continuous conversion and single-shot conversion mode. In continuous-conversion mode, conversions occur continuously until the user intervenes to stop them. On the other hand, single-shot conversion mode executes a single conversion when triggered by a high signal on the START/SYNC pin or by sending the START command. The MODE bit in the data rate register is utilized to configure the desired conversion mode.

ADC conversions can be initiated either by manipulating the START/SYNC pin or by sending serial commands. To commence conversions in continuous or single-shot mode, it's necessary to send a START command or raise the START/SYNC pin to a high state. When employing commands to regulate conversions, it's advisable to maintain the START/SYNC pin low to prevent potential conflicts between the pin and commands. For synchronized conversions, align the conversion to occur at a specific time.

To synchronize with the START/SYNC pin, lower the pin. A rising edge on the START/SYNC pin initiates a new conversion. Similarly, synchronization can be achieved using the START command. If the device is in standby mode, issue a START command. If it's already in conversion mode, issue a STOP command followed by a START command. The STOP and START commands can be issued consecutively. A new conversion cycle commences on the seventh falling edge of the SCLK signal of the START command.



(1) The $\overline{DRDY}$ signal rises at the first SCLK rising edge or the rising edge of the START/SYNC pin.
(2) The START and STOP commands take effect 2 · t_{CLK} after the seventh SCLK falling edge in the command sequence. Similarly, if the START/SYNC pin is used to control conversions, a conversion begins 2 · t_{CLK} after the rising edge of this pin.
(3) To synchronize a conversion, issue the STOP command before the START command. No delay is needed between them.

Figure 53. Conversion Start and Stop Timing

Continuous Conversion Mode

Continuous conversion mode is activated by setting the MODE bit to 0 in the data rate register (04h). To initiate continuous conversions, either send a START command or raise the START/SYNC pin to a high state. When managing the device via commands, ensure the START/SYNC pin remains low. Lowering the START/SYNC pin or sending a STOP command halts ongoing conversions after the current cycle completes, as indicated by the falling edge of DRDY. Subsequently, the device transitions to standby mode.

Single-Shot Conversion Mode

To enable single-shot conversion mode, set the MODE bit to 1 in the data rate register (04h). To initiate a single conversion, either send a START command or raise the START/SYNC pin to a high state. Once the conversion is completed, the device returns to standby mode. For subsequent conversions, issue another START command or toggle the START/SYNC pin from low to high.

When employing the sincN filter, N conversion cycles are necessary for ADC data to stabilize. In single-shot mode with the sincN filter, the first N-1 ADC conversions are suppressed, and the third conversion provides the output data, ensuring settled data for the user. Consequently, the conversion time in single-shot mode is approximately three times the normal data period. Conversely, when using the low-latency filter, ADC data stabilizes within a single conversion. In single-shot mode with the low-latency filter, the data period closely aligns with the normal data period.

Programmable Conversion Delay

The ADC incorporates a delay before initiating a new conversion to allow for the settling of the integrated analog anti-alias filter. Additionally, extra delay may be necessary to accommodate external settling effects. This delay can be automatically configured to postpone the start of a conversion after a START command, the assertion of the START/SYNC pin, or the issuance of a WREG command to modify any configuration register from address 03h to 07h (as explained in the WREG section).

The programmable conversion delay feature is designed to account for analog settling time on the inputs, especially when switching multiplexer channels. By utilizing the DELAY[2:0] bits in the gain setting register (03h), users can set a delay ranging from 1 · t_{MOD} to 4096 · t_{MOD}, where t_{MOD} equals 16 · t_{CLK}. The default setting for programmable conversion delay is 14 · t_{MOD}.

Programming

Serial Interface

The ADC features an SPI-compatible, bidirectional serial interface that facilitates reading conversion data, as well as configuring and controlling the ADC. It exclusively supports SPI mode 1 (CPOL = 0, CPHA = 1). This serial interface comprises five control lines: $\overline{CS}$, SCLK, DIN, DOUT/$\overline{DRDY}$, and $\overline{DRDY}$. However, it can function with only four or even three control signals if necessary. If the ADC is the only device connected to the SPI bus, the $\overline{CS}$ input can be tied low, requiring only SCLK, DIN, and DOUT/$\overline{DRDY}$ for communication with the device.

Chip Select (CS)

The $\overline{CS}$ pin serves as an active low input that activates the ADC's serial interface for communication, particularly beneficial in scenarios where multiple devices share the same serial bus. Throughout the data transaction, $\overline{CS}$ must remain low. When CS is high, it resets the serial interface, disregards SCLK input activity (blocking input commands), and transitions the DOUT/$\overline{DRDY}$ output to a high-impedance state. Notably, the state of $\overline{CS}$ does not impact ADC conversions. In setups involving multiple devices on the bus, the dedicated $\overline{DRDY}$ pin offers continuous monitoring of conversion status unaffected by $\overline{CS}$. Alternatively, if the serial bus isn't shared with another peripheral, tying $\overline{CS}$ to DGND permanently enables the ADC interface, with DOUT/$\overline{DRDY}$ indicating conversion status. These adjustments streamline the serial interface from five I/Os to three I/Os.

Serial Clock (SCLK)

The serial interface clock serves as a noise-filtered, Schmidt-triggered input is crucial for clocking data into and out of the ADC. Input data is latched upon the falling edge of SCLK, while output data from the ADC is updated on the rising edge of SCLK. Once the data sequence concludes, return SCLK low. Despite the hysteresis present in the SCLK input, it's essential to maintain SCLK cleanliness to prevent inadvertent transitions. Mitigate ringing and voltage overshoot on the SCLK input by implementing measures such as placing a series termination resistor at the SCLK drive pin, which aids in reducing ringing.

Serial Data Input (DIN)

The serial data input pin (DIN) works in conjunction with SCLK to transmit data, including commands and register data, to the device. Data on DIN is captured by the device upon the falling edge of SCLK. It's important to note that the device never actively drives the DIN pin. When no command is being sent, it's recommended to keep DIN low, especially during data readback operations.

Serial Data Output and Data Ready (DOUT/DRDY)

The DOUT/$\overline{DRDY}$ pin serves a dual purpose, functioning both as a digital data output and as an indicator of ADC data readiness.

Firstly, when used in conjunction with SCLK, this pin facilitates the reading of conversion and register data from the device. Data, whether conversion or register information, is transmitted via DOUT/$\overline{DRDY}$ on the rising edge of SCLK. It's important to note that DOUT/$\overline{DRDY}$ transitions to a high-impedance state when $\overline{CS}$ is set high.

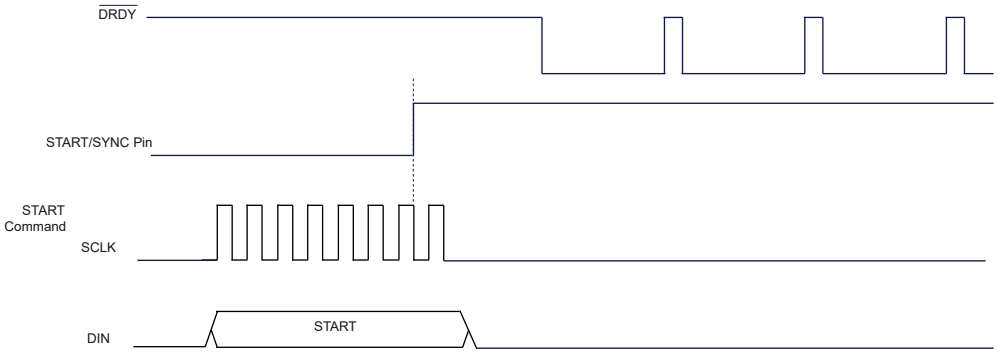
Secondly, DOUT/$\overline{DRDY}$ serves to signal the availability of new conversion data. When new conversion data becomes available, DOUT/$\overline{DRDY}$ transitions low simultaneously with the DRDY pin, indicating the readiness of new data. Both signals can be utilized to detect the availability of new data. However, in scenarios where multiple devices share the SPI bus and $\overline{CS}$ is high, it's advisable to use the dedicated $\overline{DRDY}$ pin for monitoring conversions.

Data Ready (DRDY)

The $\overline{DRDY}$ pin serves as an output indicator that transitions to a low state when conversion data are ready for retrieval. Upon power-on, $\overline{DRDY}$ is initially high. During conversion, the state of $\overline{DRDY}$ depends on whether the data has been retrieved or not.

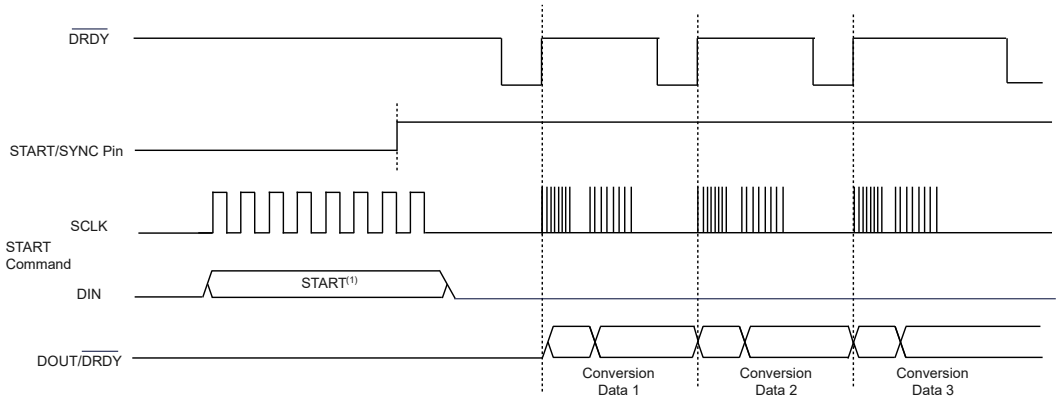
In continuous conversion mode, after $\overline{DRDY}$ transitions low to indicate data readiness, it returns high on the first rising edge of SCLK. If the data is not retrieved, $\overline{DRDY}$ remains low until it pulses high 24 times the clock period ($24 \cdot t_{CLK}$) before

the subsequent $\overline{\text{DRDY}}$ falling edge. It's crucial to retrieve the data before the next $\overline{\text{DRDY}}$ update to prevent data loss due to overwriting by new data. The figure below illustrates the $\overline{\text{DRDY}}$ operation without data retrieval, while another figure demonstrates the $\overline{\text{DRDY}}$ operation with data retrieval after each conversion cycle.



(1) After a data-ready indication, $\overline{\text{DRDY}}$ goes high on the rising edge of the first SCLK.

Figure 54. $\overline{\text{DRDY}}$ Operation without Data Retrieval



(1) After a data-ready indication, $\overline{\text{DRDY}}$ goes high on the rising edge of the first SCLK.

Figure 55. $\overline{\text{DRDY}}$ Operation with Data Retrieval

Timeout

The TPC62412 provides a serial interface timeout feature designed to restore communication integrity in case of interruptions. This functionality proves particularly beneficial in setups where the $\overline{\text{CS}}$ line remains perpetually low, not delineating communication sequences. Essentially, the SPI interface undergoes a reset if it fails to receive valid 8 bits within 215 times the clock period ($215 \cdot t_{CLK}$). Enabling this timeout mechanism involves setting the TIMEOUT bit to 1 in the system control register (09h).

Data Format

The devices provide 16 bits of data in binary twos complement format. The size of one code (LSB) is calculated by:

$1\ LSB = (2 \cdot V_{REF} / Gain) / 2^{16} = +FS / 2^{15}$

A positive full-scale input [V_{IN} ≥ (+FS – 1 LSB) = (V_{REF} / Gain – 1 LSB)] generates an output code of 7FFFh and a negative full-scale input (V_{IN} ≤ –FS = –V_{REF} / Gain) generates an output code of 8000h. The output saturates these codes for signals that exceed full scale.

Table 27. Ideal Output Code vs Input Signal

INPUT SIGNAL, VIN = V_{AINP} – V_{AINN}	IDEAL OUTPUT CODE(1)
≥ FS (2^{15} – 1) / 2^{15}	7FFFh
FS / 2^{15}	0001h
0	0000h
–FS / 2^{15}	FFFFh
≤ –FS	8000h

(1) Excludes the effects of noise, INL, offset, and gain errors.

The transfer function of analog input and ADC output code is shown below:

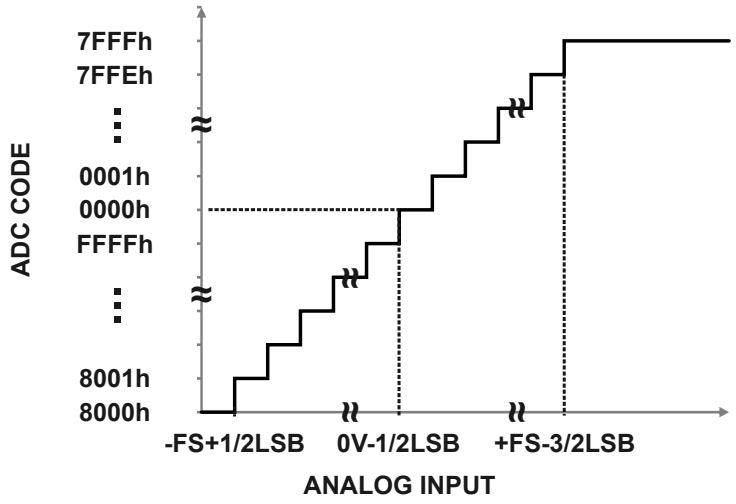


Figure 56. Code Transition Diagram

Commands

Commands play a key role in managing the ADC, configuring its settings, and fetching data. While numerous commands are standalone, meaning they consist of a single byte, the register write, and register read commands are multi-byte. These commands entail two command bytes followed by the register data byte or bytes.

Command	Description	First Command Byte	Second Command Byte
Control Commands			
NOP	No operation	0000 0000 (00h)	—
WAKEUP	Wake-up from power-down mode	0000 001x (02h, 03h) (1)	—
POWERDOWN	Enter power-down mode	0000 010x (04h, 05h) (1)	—
RESET	Reset the device	0000 011x (06h, 07h) (1)	—
START	Start conversions	0000 100x (08h, 09h) (1)	—
STOP	Stop conversions	0000 101x (0Ah, 0Bh) (1)	—
Calibration Commands			
SYOCAL	System offset calibration	0001 0110 (16h)	—
SYGCAL	System gain calibration	0001 0111 (17h)	—
SFOCAL	Self-offset calibration	0001 1001 (19h)	—
Data Read Command			
RDATA	Read data by command	0001 001x (12h / 13h) (1)	—
Register Read and Write Commands			
RREG	Read *nnnnn* registers starting at address *rrrrr*	001r rrrr (2)	000n nnnn(3)
WREG	Write *nnnnn* registers starting at address *rrrrr*	010r rrrr (2)	000n nnnn(3)

(1) x = don't care.
(2) r rrrr = starting register address.
(3) n nnnn = number of registers to read or write – 1.

Commands can be issued at any point, whether during a conversion or when conversions are halted. However, if register read or write commands are ongoing when conversion data becomes available, the ADC prevents the loading of conversion data into the output shift register. The $\overline{CS}$ input pin can transition high between commands or remain low between consecutive commands. However, it must remain low for the entire sequence of commands. To finish or abort a command before completion, transition $\overline{CS}$ high. Notice that only send commands are listed in the table.

NOP

The NOP (no-operation) command allows data to be clocked out without issuing a new command. It is useful for reading data from the ADC without changing its state or starting any additional operations.

WAKEUP

To exit power-down mode and transition the device into standby mode, issue the WAKEUP command. If the device is running on an external clock, ensure the external clock is active before sending the WAKEUP command, as the command does not be decoded if the external clock is not running.

POWERDOWN

Sending the POWERDOWN command aborts any ongoing conversion and places the device into power-down mode. The transition to power-down mode occurs 2 · t_{CLK} after the seventh falling edge of SCLK from the command.

For minimal power consumption on IOVDD, stop the external clock when in power-down mode, as the device does not automatically gate the external clock. If using an external clock, allow at least two additional t_{CLK}s after issuing the POWERDOWN command to ensure proper entry into power-down mode. It is recommended to select the internal oscillator before issuing the POWERDOWN command to conserve power. While in power-down mode, the available commands are RREG, RDATA, and WAKEUP.

POWERDOWN

Sending the POWERDOWN command aborts any ongoing conversion and places the device into power-down mode. The transition to power-down mode occurs 2 · t_{CLK} after the seventh falling edge of SCLK from the command.

For minimal power consumption on IOVDD, stop the external clock when in power-down mode, as the device does not automatically gate the external clock. If using an external clock, allow at least two additional t_{CLK}s after issuing the POWERDOWN command to ensure proper entry into power-down mode. It is recommended to select the internal oscillator before issuing the POWERDOWN command to conserve power. While in power-down mode, the available commands are RREG, RDATA, and WAKEUP.

RESET

The RESET command resets the digital filter and restores all configuration register values to their default settings. It also places the device into standby mode. In standby mode, the device waits for a rising edge on the START/SYNC pin or a START command to resume conversions. After issuing the RESET command, a delay time of $td_{(RSSC)}$ is required before sending the first serial interface command or starting a conversion.

If the device was previously using an external clock, the reset automatically switches the device to use the internal oscillator as its default configuration.

START

When the device is set to continuous conversion mode, issue the START command to begin conversions. After each conversion completes, the device automatically starts a new conversion until the STOP command is issued.

In single-shot conversion mode, the START command initiates a single conversion. Once the conversion completes, the device enters standby mode.

When controlling the device with the START and STOP commands, tie the START/SYNC pin low. The START command is ignored if the START/SYNC pin is high. If the device is already in conversion mode, issuing the START command has no effect.

STOP

The STOP command is used to halt continuous conversions. It allows the current conversion to complete, and after $\overline{DRDY}$ transitions low, the device enters standby mode. In single-shot conversion mode, the STOP command has no effect. When controlling the device using the START and STOP commands, ensure the START/SYNC pin is held low.

SYOCAL

The SYOCAL command starts a system offset calibration. For this calibration, the inputs should be externally shorted to a voltage within the input range, ideally close to the mid-supply voltage, which is (AVDD + AVSS) / 2. The OFC registers are updated once the calibration is completed. Calibration commands can only be issued when the device is in conversion mode.

SFOCAL

The SFOCAL command initiates a self-offset calibration. During this process, the device internally shorts the inputs to mid-supply and performs the calibration. The OFC registers are updated once the operation is complete. Calibration commands must be issued when the device is in conversion mode.

RDATA

The RDATA command is used to read conversion data from the device at any time, ensuring that data corruption does not occur, even when the $\overline{DRDY}$ or DOUT/$\overline{DRDY}$ signal cannot be monitored. The conversion result is read from a buffer, allowing a new data conversion to take place without corrupting the previously read conversion data.

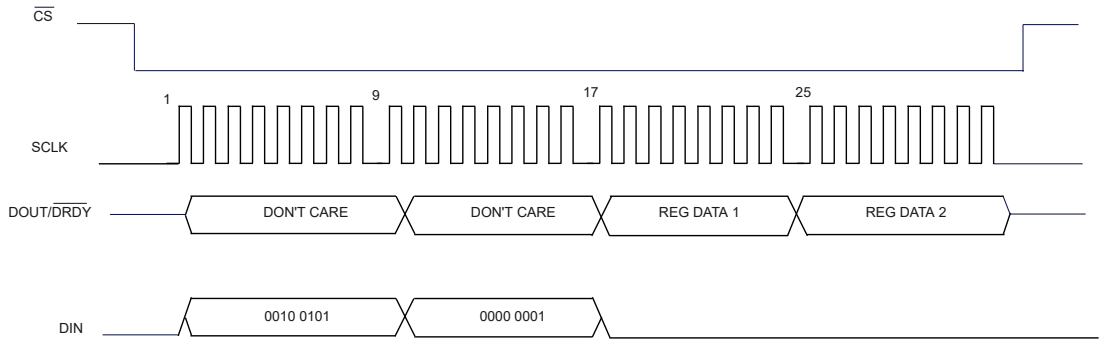
RREG

The RREG command is used to read device register data. It allows you to read either a single register or a block of registers, with the starting register address being any valid address in the register map. The command consists of two bytes: the first byte specifies the starting register address (001r rrrr, where `rrrr` is the address), and the second byte specifies the number of registers to read (minus 1), written as 000n nnnn (where `nnnn` represents the number of registers to read minus 1).

After the read command is issued, the ADC responds with one or more register data bytes, with the most significant bit transmitted first. If the byte count exceeds the last register address, the ADC outputs zero data. During the register read operation, any new conversion data does not be loaded into the output shift register to prevent data contention. However, the conversion data can be retrieved later using the RDATA command. Once the register read command has begun, further commands are blocked until one of the following conditions is met:

- The read operation completes.
- The read operation is terminated by taking the $\overline{CS}$ pin high.
- The read operation is terminated by a serial interface timeout.
- The ADC is reset by toggling the RESET pin.

The figure below shows an example of a two-register read operation. To read data from two registers starting at register REF (address = 05h), the commands required are: command byte 1 = 25h and command byte 2 = 01h. After sending these two command bytes, the DIN pin should remain low to complete the read operation correctly.



(1) $\overline{CS}$ can be set high or kept low between commands. If $\overline{CS}$ is kept low, the command must be completed before sending a new command.

Figure 57. Read Register Sequence

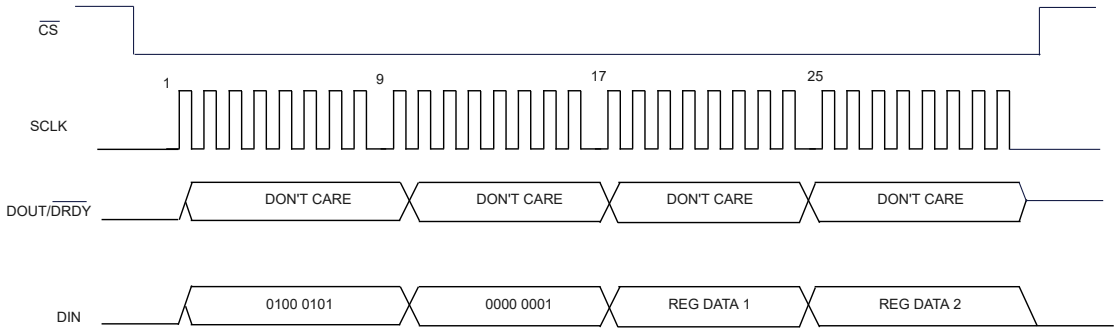
WREG

Use the WREG command to write data to the device registers. The data can be written one register at a time or as a block of registers. The starting register address can be any register within the register map.

The WREG command consists of two bytes. The first byte specifies the starting register address using the format 010r rrrr, where r rrrr is the starting register address. The second byte indicates the number of registers to write, minus one, using the format 000n nnnn, where n nnnn is the number of registers to write minus one. Following these command bytes, the register data is sent, with the most significant bit first. If the byte count exceeds the last register address, the ADC ignores the extra data. Once the WREG command has started, no further commands can be issued until one of the following occurs:

- The write operation is completed.
- The write operation is terminated by taking $\overline{CS}$ high.
- The write operation is terminated by a serial interface timeout.
- The ADC is reset by toggling the $\overline{RESET}$ pin.

The two-register write operation example is depicted in the figure below. The required commands to write data to two registers starting at register REF (address = 05h) are command byte 1 = 45h, which specifies the starting register address (05h), and command byte 2 = 01h, indicating that two registers being written to. The register data is then sent, starting with the most significant bit.



(1) $\overline{CS}$ can be set high or kept low between commands. If $\overline{CS}$ is kept low, the command must be completed before sending a new command.

Figure 58. Write Register Sequence

Writing new data to certain configuration registers resets the digital filter and starts a new conversion if a conversion is in progress. Registers that trigger a new conversion when written to are listed below:

- Channel configuration register (02h)
- Gain setting register (03h)
- Data rate register (04h)
- Reference control register (05h), bits [5:0]
- Excitation current register 1 (06h), bits [3:0]
- Excitation current register 2 (07h)
- System control register (09h), bits [7:5]

When the device is configured using the WREG command, the first data-ready indication occurs after the new conversion completes with the updated configuration settings. The data from the previous conversion is cleared upon restart, so it is important to read the previous data before performing the register write operation. A WREG to the relevant registers only initiates a new conversion if the new register data differs from the previous settings and if a conversion is currently in progress. If the device is in standby mode, the configuration is updated according to the WREG data, but the conversion does not begin until the START/SYNC pin is taken high or a START command is issued.

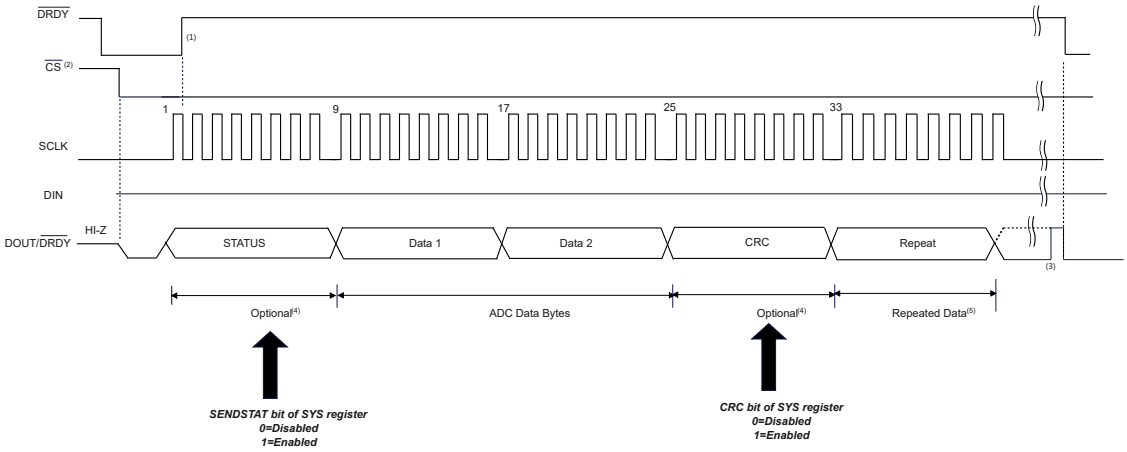
Reading Data

The ADC provides two methods for reading data: direct data read and command-based data read. In direct read mode, the ADC writes the new conversion data to the output shift register and the internal data-holding register. In this mode, the data can be read directly from the output shift register. In command mode, data is read from the data-holding register, which does not require synchronization with the $\overline{DRDY}$ signal for the start of data readback. This allows for data to be retrieved from the holding register without having to wait for $\overline{DRDY}$ to indicate that a new conversion completes.

Read Data Direct

In the read data direct method, ADC conversion data are shifted directly out from the output shift register, and no command is required. However, it is important to ensure that no serial activity occurs between the falling edge of $\overline{DRDY}$ and the readback, as this can make the data invalid. The serial interface operates in full duplex during direct data read, which means that commands are decoded while the data is being read. To prevent data corruption, keep the DIN line low during the readback if no command is intended. If an input command is issued during the readback, the ADC executes the command, potentially leading to data corruption. To avoid overwriting old data with new conversion results, synchronize the data readback with $\overline{DRDY}$ or DOUT/$\overline{DRDY}$, ensuring that the data is read before the next $\overline{DRDY}$ update.

The ADC data field can be 3, 4, or 5 bytes long, as shown below. This data field includes an optional STATUS byte, three bytes of conversion data, and an optional CRC byte. Once all bytes have been read, the data-byte sequence repeats with continued SCLKs. The sequence starts over with the first byte when new SCLKs are provided. To help ensure error-free communication, it is recommended to read the same data multiple times during each conversion interval. Alternatively, you can use the optional CRC byte for error checking, which provides an extra layer of verification.



(1) $\overline{DRDY}$ returns high on the first SCLK falling edge.
(2) If $\overline{CS}$ is tied low, the DOUT/$\overline{DRDY}$ pin asserts low simultaneously with the DRDY signal. This ensures that the device is in a continuous communication mode, where data can be read without the need for toggling the $\overline{CS}$ line.
(3) Complete the data retrieval process before new data becomes ready, ensuring that you finish reading the current data within 28 · t_{CLK} cycles before the next falling edge of the DOUT/$\overline{DRDY}$ and $\overline{DRDY}$ signals.
(4) The STATUS and CRC bytes are optional during data retrieval.
(5) The byte sequence, including any selected optional bytes, repeats with continued SCLK.

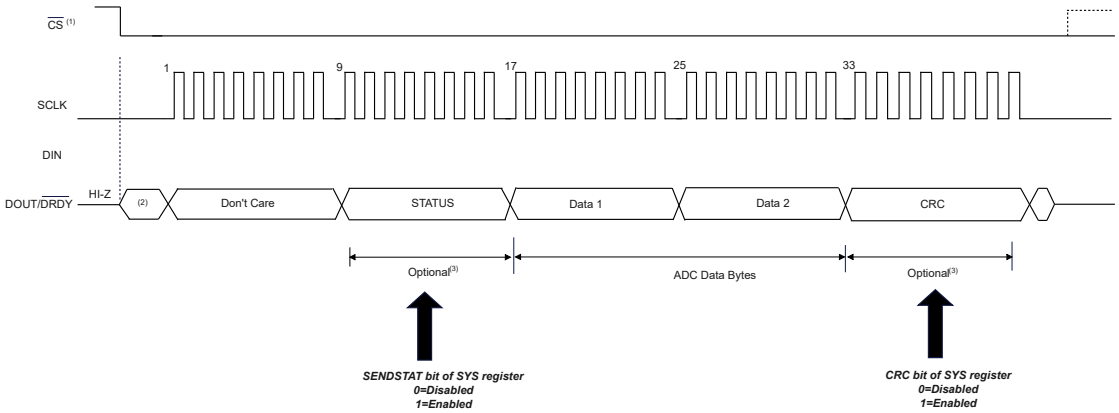
Figure 59. Read Data Direct

Read Data by RDATA Command

The RDATA command allows data retrieval from the data-holding register of the ADC, ensuring no risk of data corruption. This method does not require synchronization to DRDY, meaning data can be read at any time. However, polling $\overline{DRDY}$ for when data is ready is still an option.

In the RDATA command sequence, the most significant bit (MSB) of the output data begins on the first SCLK rising edge after the command is issued. The output data field can be 3, 4, or 5 bytes long, consisting of an optional STATUS byte, three bytes of conversion data, and an optional CRC byte. An RDATA command must be issued for each read operation, and the ADC does not respond to any other commands until the read operation is complete or terminated by taking $\overline{CS}$ high.

Once all bytes are read, the data-byte sequence (including the STATUS and CRC bytes, if enabled) repeats with the continuing SCLK.



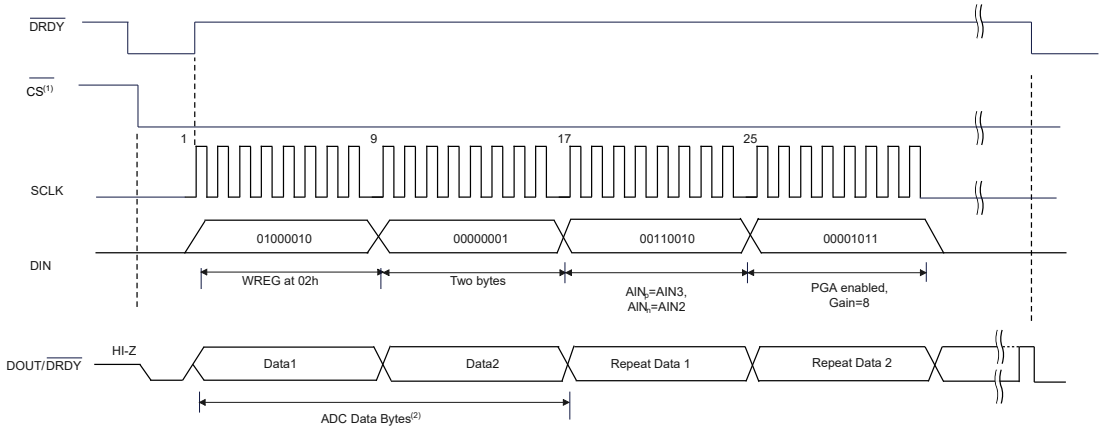
(1) $\overline{CS}$ can be tied low. When $\overline{CS}$ is low, the DOUT/$\overline{DRDY}$ pin asserts low simultaneously with $\overline{DRDY}$.
(2) DOUT/$\overline{DRDY}$ is driven low simultaneously with $\overline{DRDY}$. If a read operation occurs after the falling edge of DRDY, DOUT/$\overline{DRDY}$ can be either high or low.
(3) The STATUS and CRC bytes are optional during data retrieval.

Figure 60. Read Data by Command

Sending Commands When Reading Data

The serial interface of the device supports full-duplex operation during data retrieval, meaning that commands can be sent while simultaneously reading conversion data. However, if an RREG or RDATA command is issued during an ongoing data read, the current data read operation is aborted, leading to corrupted conversion data, unless the command is issued after the last byte of the conversion data has been retrieved. To avoid interruption during data read, keep DIN low while clocking out the data. The device begins outputting the requested data on DOUT/$\overline{DRDY}$ at the first rising edge of SCLK after the command byte.

A WREG command can be issued during a read operation without disrupting the ongoing data retrieval. This method allows for a seamless transition between reading data and configuring the device for the next conversion. For instance, in read data direct mode, a WREG command can be used to update two configuration registers while reading conversion data. After the command is clocked in, the device resets the digital filter and begins a new conversion based on the updated register settings, provided the device is in continuous conversion mode. The reset occurs after each byte is received, including when the first byte triggers a reset for the input multiplexer and another reset when the PGA is configured. The WREG command can be sent at any 8-bit boundary, and in this example, the STATUS and CRC bytes are disabled.



(1) $\overline{CS}$ can be tied low. When $\overline{CS}$ is low, the DOUT/$\overline{DRDY}$ pin asserts low simultaneously with $\overline{DRDY}$.
(2) The output data buffer operates in a cyclical manner, meaning that once the fourth byte of data is clocked in, the original data byte is re-issued. This ensures that the output data continues to repeat in a loop after the initial set of data has been transmitted.

Figure 61. Issuing a WREG Command When Reading Back ADC Data

Interfacing with Multiple Devices

When connecting multiple SPI devices to a single bus, each device should have a dedicated chip-select ($\overline{CS}$) line. This ensures that the SPI lines (SCLK, DIN, and DOUT/$\overline{DRDY}$) can be shared without interference. When a $\overline{CS}$ line of the device transitions high, the DOUT/$\overline{DRDY}$ pin goes into tri-state mode, meaning it is no longer actively driven. This makes DOUT/$\overline{DRDY}$ unreliable for indicating new data availability when $\overline{CS}$ is high. Instead, the $\overline{DRDY}$ pin can still signal when new data are available, as it remains actively driven even when $\overline{CS}$ is high.

If there is a limitation in the number of available GPIOs or if isolation is required between the microcontroller and the devices, the microcontroller can periodically drop the $\overline{CS}$ line for a device to check the state of DOUT/$\overline{DRDY}$. When $\overline{CS}$ is low, the DOUT/DRDY pin indicates whether new data are available. If DOUT/$\overline{DRDY}$ drives low, it means new data are ready. If it drives high, no new data is available. To ensure proper synchronization, DOUT/$\overline{DRDY}$ should be forced high after each data read and before taking $\overline{CS}$ high again. This can be done by issuing a RREG command to read a register where the least significant bit (LSB) is 1, which forces DOUT/$\overline{DRDY}$ to go high.

To avoid data corruption during retrieval, using the RDATA command is recommended. This command allows the microcontroller to retrieve valid data at any time, regardless of whether new data is ready, without the risk of corruption from an ongoing conversion.

Register Map

Configuration Registers

The TPC62412 register map comprises 18 8-bit registers utilized to configure and manage the device according to the desired mode of operation. Access these registers via the serial interface by employing the RREG and WREG register commands. Upon power-on or reset, the registers revert to their initial settings, as indicated in the Default column of the table.

Data can be written as a block to multiple registers using a single WREG command. When data are written as a block, the data of specific registers take effect immediately upon being shifted in. Writing new data to certain registers leads to a restart of conversions that are currently in progress. The registers that prompt a conversion restart are discussed in the WREG section.

Table 28. Configuration Register Map

ADDR	REGISTER	DEFAULT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	ID	xxh	RESERVED					DEV_ID[2:0]		
01h	STATUS	80h	FL_POR	$\overline{RDY}$	FL_P_RAILP	FL_P_RAILN	FL_N_RAILP	FL_N_RAILN	FL_REF_L1	FL_REF_L0
02h	INPMUX	01h	MUXP[3:0]				MUXN[3:0]			
03h	PGA	00h	DELAY[2:0]			PGA_EN[1:0]		GAIN[2:0]		
04h	DATARATE	14h	G_CHOP	CLK	MODE	FILTER	DR[3:0]			
05h	REF	10h	FL_REF_EN[1:0]		$\overline{REFP\_BUF}$	$\overline{REFN\_BUF}$	REFSEL[1:0]		REFCON[1:0]	
06h	IDACMAG	00h	FL_RAIL_EN	PSW	0	0	IMAG[3:0]			
07h	IDACMUX	FFh	I2MUX[3:0]				I1MUX[3:0]			
08h	VBIAS	00h	VB_LEVEL	VB_AINC	VB_AIN5	VB_AIN4	VB_AIN3	VB_AIN2	VB_AIN1	VB_AIN0
09h	SYS	10h	SYS_MON[2:0]			Reserved		TIMEOUT	CRC	SENDSTAT
0Ah	OFCAL0	00h	OFC[7:0]							
0Bh	OFCAL1	00h	OFC[15:8]							
0Ch	OFCAL2	00h	OFC[23:16]							
0Dh	FSCAL0	00h	FSC[7:0]							
0Eh	FSCAL1	00h	FSC[15:8]							
0Fh	FSCAL2	40h	FSC[23:16]							
10h	GPIODAT	00h	DIR[3:0]				DAT[3:0]			
11h	GPIOCON	00h	0	0	0	0	CON[3:0]			

Table 29. Device ID Register (address = 00h)

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	00h	**Reserved** Values are subject to change without notice
2:0	DEV_ID[2:0]	R	04h	**Device identifier** Identifies the model of the device. 000 : Reserved 001 : Reserved 010 : Reserved 011 : Reserved 100 : TPC62412 (12 channels, 16 bits) 101 : TPC62413 (6 channels, 16 bits) 110 : Reserved 111 : Reserved

Table 30. Device Status Register (address = 01h)

Bit	Field	Type	Reset	Description
7	FL_POR	R/W	1h	**POR flag** Indicates a power-on reset (POR) event has occurred. 0: Register has been cleared and no POR event has occurred. 1: POR event occurred and has not been cleared. Flag must be cleared by user register write (default).
6	$\overline{RDY}$	R	0h	**Device ready flag** Indicates the device has started up and is ready for communication. 0: ADC ready for communication (default) 1: ADC not ready
5	FL_P_RAILP	R	0h	**Positive PGA output at positive rail flag** (1) Indicates the positive PGA output is within 150 mV of AVDD. 0: No error (default) 1: PGA positive output within 150 mV of AVDD
4	FL_P_RAILN	R	0h	**Positive PGA output at negative rail flag** (1) Indicates the positive PGA output is within 150 mV of AVSS. 0: No error (default) 1: PGA positive output within 150 mV of AVSS
3	FL_N_RAILP	R	0h	**Negative PGA output at positive rail flag**(1) Indicates the negative PGA output is within 150 mV of AVDD. 0: No error (default) 1: PGA negative output within 150 mV of AVDD
2	FL_N_RAILN	R	0h	**Negative PGA output at negative rail flag** (1) Indicates the negative PGA output is within 150 mV of AVSS. 0: No error (default) 1: PGA negative output within 150 mV of AVSS
1	FL_REF_L1	R	0h	**Reference voltage monitor flag, level 1** (2) Indicates the external reference voltage is lower than 1/3 of the analog supply voltage. Can be used to detect an open-excitation lead in a 3-wire RTD application. 0: Differential reference voltage ≥ 1/3 · (AVDD – AVSS) (default) 1: Differential reference voltage < 1/3 · (AVDD – AVSS)
0	FL_REF_L0	R	0h	**Reference voltage monitor flag, level 0** (2) Indicates the external reference voltage is lower than 0.3 V. Can be used to indicate a missing or floating external reference voltage. 0: Differential reference voltage ≥ 0.3 V (default) 1: Differential reference voltage < 0.3 V

(1) The PGA rail monitors are enabled with the FL_RAIL_EN bit in excitation current register 1 (06h).
(2) The reference monitors are enabled with the FL_REF_EN[1:0] bits of the reference control register (05h)

Table 31. Input Multiplexer Register (address = 02h)

Bit	Field	Type	Reset	Description
7:4	MUXP[3:0]	R/W	0h	**Positive ADC input selection** Selects the ADC positive input channel. 0000 : AIN0 (default) 0001 : AIN1 0010 : AIN2 0011 : AIN3 0100 : AIN4 0101 : AIN5 0110 : AIN6 0111 : AIN7 1000 : AIN8 1001 : AIN9 1010 : AIN10 1011 : AIN11 1100 : AINCOM 1101 : Reserved 1110 : Reserved 1111 : Reserved
3:0	MUXN[3:0]	R/W	1h	**Negative ADC input selection** Selects the ADC negative input channel. 0000 : AIN0 0001 : AIN1 (default) 0010 : AIN2 0011 : AIN3 0100 : AIN4 0101 : AIN5 0110 : AIN6 0111 : AIN7 1000 : AIN8 1001 : AIN9 1010 : AIN10 1011 : AIN11 1100 : AINCOM 1101 : Reserved 1110 : Reserved 1111 : Reserved

Table 32. Gain Setting Register (address = 03h)

Bit	Field	Type	Reset	Description
7:5	DELAY[2:0]	R/W	0h	**Programmable conversion delay selection** Sets the programmable conversion delay time for the first conversion after a WREG when a configuration change resets of the digital filter and triggers a new conversion (1). 000 : 14 · t_{MOD} (default) 001 : 25 · t_{MOD} 010 : 64 · t_{MOD} 011 : 256 · t_{MOD} 100 : 1024 · t_{MOD} 101 : 2048 · t_{MOD} 110 : 4096 · t_{MOD} 111 : 1 · t_{MOD}
4:3	PGA_EN[1:0]	R/W	0h	**PGA enable** Enables or bypasses the PGA. 00 : PGA is powered down and bypassed. Enables single-ended measurements with unipolar supply (Set gain = 1 (2)) (default) 01 : PGA enabled (gain = 1 to 128) 10 : Reserved 11 : Reserved
2:0	GAIN[2:0]	R/W	0h	**PGA gain selection** Configures the PGA gain. 000 : 1 (default) 001 : 2 010 : 4 011 : 8 100 : 16 101 : 32 110 : 64 111 : 128

Table 33. Data Rate Register (address = 04h)

Bit	Field	Type	Reset	Description
7	G_CHOP	R/W	0h	**Global chop enable** Enables the global chop function. When enabled, the device automatically swaps the inputs and takes the average of two consecutive readings to cancel the offset voltage. 0 : Disabled (default) 1 : Enabled
6	CLK	R/W	0h	**Clock source selection** Configures the clock source to use either the internal oscillator or an external clock. 0 : Internal 4.096-MHz oscillator (default) 1 : External clock
5	MODE	R/W	0h	**Conversion mode selection** Configures the ADC for either continuous conversion or single-shot conversion mode. 0 : Continuous conversion mode (default) 1 : Single-shot conversion mode
4	FILTER	R/W	1h	**Digital filter selection** Configures the ADC to use either the sinc or the low-latency filter. 0 : Sinc filter 1 : Low-latency filter (default)
3:0	DR[3:0]	R/W	4h	**Data rate selection** Configures the output data rate (1). 0000 : 2.5 SPS 0001 : 5 SPS 0010 : 10 SPS 0011 : 16.6 SPS 0100 : 20 SPS (default) 0101 : 50SPS 0110 : 60 SPS 0111 : 100 SPS 1000 : 200 SPS 1001 : 400 SPS 1010 : 800 SPS 1011 : 1000 SPS 1100 : 2000 SPS 1101 : 4000 SPS 1110 : 8000 SPS 1111 : 8000 SPS

(1) Data rates of 60 Hz or less can offer line-cycle rejection; see the 50-Hz and 60-Hz Line Cycle Rejection section for more information.

Table 34. Reference Control Register (address = 05h)

Bit	Field	Type	Reset	Description
7:6	FL_REF_EN[1:0]	R/W	0h	**Reference monitor configuration** Enables and configures the reference monitor. 00 : Disabled (default) 01 : FL_REF_L0 monitor enabled, threshold 0.3 V 10 : FL_REF_L0 and FL_REF_L1 monitors enabled, thresholds 0.3 V and 1/3 · (AVDD – AVSS) 11 : FL_REF_L0 monitor and 10-MΩ pull-together enabled, threshold 0.3 V
5	$\overline{\text{REFP\_BUF}}$	R/W	0h	**Positive reference buffer bypass** Disables the positive reference buffer. Recommended when $V_{(REFPx)}$ is close to AVDD. 0 : Enabled (default) 1 : Disabled
4	$\overline{\text{REFN\_BUF}}$	R/W	1h	**Negative reference buffer bypass** Disables the negative reference buffer. Recommended when $V_{(REFNx)}$ is close to AVSS. 0 : Enabled 1 : Disabled (default)
3:2	REFSEL[1:0]	R/W	0h	**Reference input selection** Selects the reference input source for the ADC. 00 : REFP0, REFN0 (default) 01 : REFP1, REFN1 10 : Internal 2.5-V reference (1) 11 : Reserved
1:0	REFCON[1:0]	R/W	0h	**Internal voltage reference configuration** (2) Configures the behavior of the internal voltage reference. 00 : Internal reference off (default) 01 : Internal reference on, but powers down in power-down mode 10 : Reserved 11 : Reserved

(1) Disable the reference buffers when the internal reference is selected for measurements.
(2) The internal voltage reference must be turned on to use the IDACs.

Table 35. Excitation Current Register 1(address = 06h)

Bit	Field	Type	Reset	Description
7	FL_RAIL_EN	R/W	0h	**PGA output rail flag enable** Enables the PGA output voltage rail monitor circuit. 0 : Disabled (default) 1 : Enabled
6	PSW	R/W	0h	**Low-side power switch** Controls the low-side power switch. The low-side power switch opens automatically in power-down mode. 0 : Open (default) 1 : Closed
5:4	RESERVED	R	0h	**Reserved** Always write 0h
3:0	IMAG[3:0]	R/W	0h	**IDAC magnitude selection** Selects the value of the excitation current sources. Sets IDAC1 and IDAC2 to the same value. 0000 : Off (default) 0001 : 10 μA 0010 : 50 μA 0011 : 100 μA 0100 : 250 μA 0101 : 500 μA 0110 : 750 μA 0111 : 1000 μA 1000 : 1500 μA 1001 : 2000 μA 1010 - 1111 : Off

Table 36. Excitation Current Register 2 (address = 07h)

Bit	Field	Type	Reset	Description
7:4	I2MUX[3:0]	R/W	Fh	**IDAC2 output channel selection** Selects the output channel for IDAC2. 0000 : AIN0 0001 : AIN1 0010 : AIN2 0011 : AIN3 0100 : AIN4 0101 : AIN5 0110 : AIN6, REFP1 0111 : AIN7, REFN1 1000 : AIN8 1001 : AIN9 1010 : AIN10 1011 : AIN11 1100 : AINCOM 1101 - 1111 : Disconnected (default)
3:0	I1MUX[3:0]	R/W	Fh	**IDAC1 output channel selection** Selects the output channel for IDAC1. 0000 : AIN0 0001 : AIN1 0010 : AIN2 0011 : AIN3 0100 : AIN4 0101 : AIN5 0110 : AIN6, REFP1 0111 : AIN7, REFN1 1000 : AIN8 1001 : AIN9 1010 : AIN10 1011 : AIN11 1100 : AINCOM 1101 - 1111 : Disconnected (default)

Table 37. Sensor Biasing Register (address = 08h)

Bit	Field	Type	Reset	Description
7	VB_LEVEL	R/W	0h	**VBIAS level selection** Sets the VBIAS output voltage level. VBIAS is disabled when not connected to any input. 0 : (AVDD + AVSS) / 2 (default) 1 : (AVDD + AVSS) / 12
6	VB_AINC	R/W	0h	**AINCOM VBIAS selection (1)** Enables VBIAS on the AINCOM pin. 0 : VBIAS disconnected from AINCOM (default) 1 : VBIAS connected to AINCOM
5	VB_AIN5	R/W	0h	**AIN5 VBIAS selection (1)** Enables VBIAS on the AIN5 pin. 0 : VBIAS disconnected from AIN5 (default) 1 : VBIAS connected to AIN5
4	VB_AIN4	R/W	0h	**AIN4 VBIAS selection (1)** Enables VBIAS on the AIN4 pin. 0 : VBIAS disconnected from AIN4 (default) 1 : VBIAS connected to AIN4
3	VB_AIN3	R/W	0h	**AIN3 VBIAS selection (1)** Enables VBIAS on the AIN3 pin. 0 : VBIAS disconnected from AIN3 (default) 1 : VBIAS connected to AIN3
2	VB_AIN2	R/W	0h	**AIN2 VBIAS selection (1)** Enables VBIAS on the AIN2 pin. 0 : VBIAS disconnected from AIN2 (default) 1 : VBIAS connected to AIN2
1	VB_AIN1	R/W	0h	**AIN1 VBIAS selection (1)** Enables VBIAS on the AIN1 pin. 0 : VBIAS disconnected from AIN1 (default) 1 : VBIAS connected to AIN1
0	VB_AIN0	R/W	0h	**AIN0 VBIAS selection (1)** Enables VBIAS on the AIN0 pin. 0 : VBIAS disconnected from AIN0 (default) 1 : VBIAS connected to AIN0

(1) The bias voltage can be selected for multiple analog inputs at the same time.

Table 38. System Control Register (address = 09h)

Bit	Field	Type	Reset	Description
7:5	SYS_MON[2:0]	R/W	0h	**System monitor configuration** (1) Enables a set of system monitor measurements using the ADC. 000 : Disabled (default) 001 : PGA inputs shorted to (AVDD + AVSS) / 2 and disconnected from AINx and the multiplexer; gain set by the user 010 : Internal temperature sensor measurement; PGA must be enabled (PGA_EN[1:0] = 01); gain set by user(2) 011 : (AVDD – AVSS) / 4 measurement; gain set to 1 (3) 100 : DVDD / 4 measurement; gain set to 1 (3) 101 : Burn-out current sources enabled, 0.2-μA setting 110 : Burn-out current sources enabled, 1-μA setting 111 : Burn-out current sources enabled, 10-μA setting
4:3	Reserved	R/W	0h	Reserved
2	TIMEOUT	R/W	0h	**SPI timeout enable** Enables the SPI timeout function. 0 : Disabled (default) 1 : Enabled
1	CRC	R/W	0h	**CRC enable** Enables the CRC byte appended to the conversion result. When enabled, CRC is calculated across the 24-bit conversion result (plus the STATUS byte if enabled). 0 : Disabled (default) 1 : Enabled
0	SENDSTAT	R/W	0h	**STATUS byte enable** Enables the STATUS byte prepended to the conversion result. 0 : Disabled (default) 1 : Enabled

(1) With system monitor functions enabled, the AINx multiplexer switches are open for the (AVDD + AVSS) / 2 measurement, the temperature sensor, and the supply monitors.
(2) When using the internal temperature sensor, the gain must be 4 or less to keep the measurement within the PGA input voltage range.
(3) The PGA gain is automatically set to 1 when the supply monitors are enabled, regardless of the setting in GAIN[2:0].

Table 39. Offset Calibration Register 1 (address = 0Ah)

Bit	Field	Type	Reset	Description
7:0	OFC[7:0]	R/W	00h	Bits [7:0] of the offset calibration value.

Table 40. Offset Calibration Register 2 (address = 0Bh)

Bit	Field	Type	Reset	Description
7:0	OFC[15:8]	R/W	00h	Bits [15:8] of the offset calibration value.

Table 41. Offset Calibration Register 3 (address = 0Ch)

Bit	Field	Type	Reset	Description
7:0	OFC[23:16]	R/W	00h	Bits [23:16] of the offset calibration value.

Table 42. Gain Calibration Register 1 (address = 0Dh)

Bit	Field	Type	Reset	Description
7:0	FSC[7:0]	R/W	00h	Bits [7:0] of the gain calibration value.

Table 43. Gain Calibration Register 2 (address = 0Eh)

Bit	Field	Type	Reset	Description
7:0	FSC[15:8]	R/W	00h	Bits [15:8] of the gain calibration value.

Table 44. Gain Calibration Register 3 (address = 0Fh)

Bit	Field	Type	Reset	Description
7:0	FSC[23:16]	R/W	00h	Bits [23:16] of the gain calibration value.

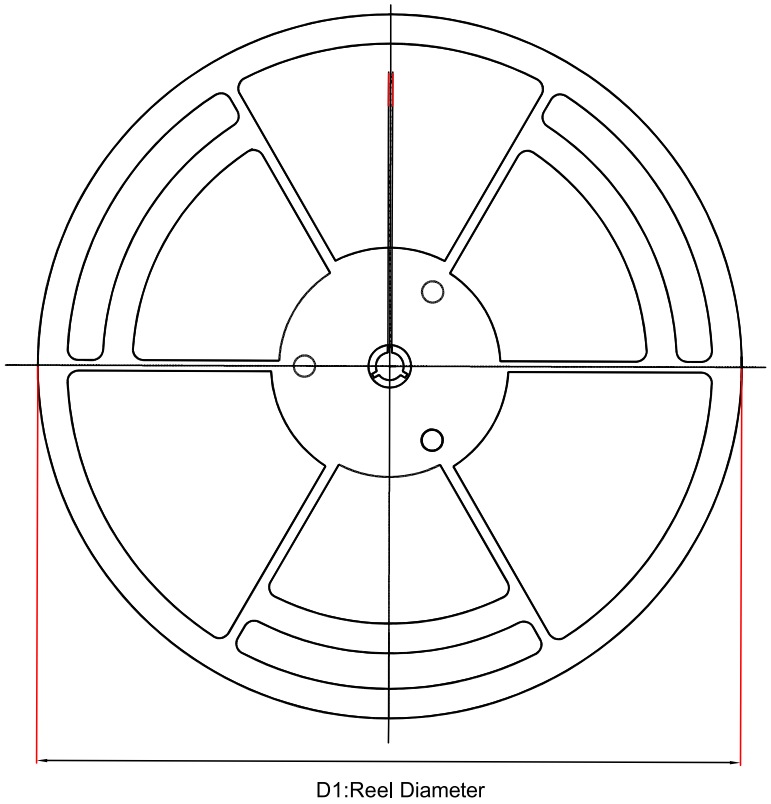
Table 45. GPIO Data Register (address = 10h)

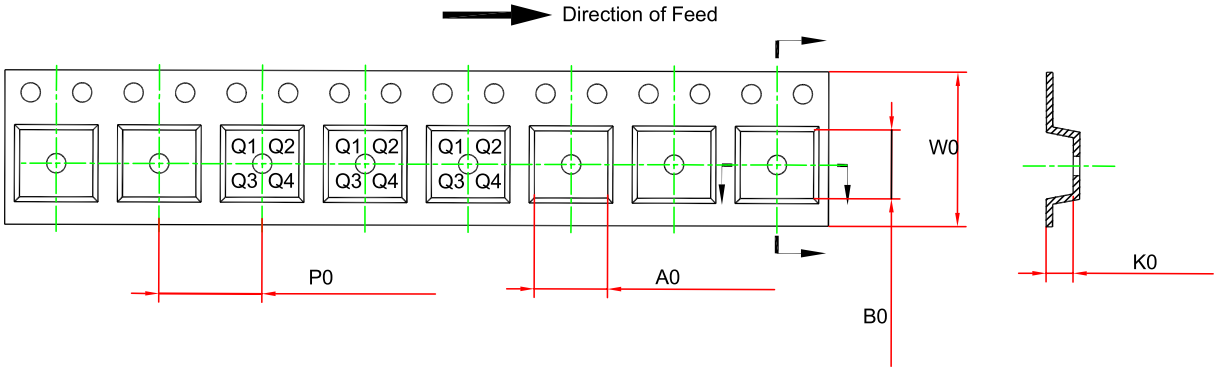
Bit	Field	Type	Reset	Description
7:4	DIR[3:0]	R/W	0h	**GPIO direction** Configures the selected GPIO as an input or output. 0 : GPIO[x] configured as output (default) 1 : GPIO[x] configured as input
3:0	DAT[3:0]	R/W	0h	**GPIO data** Contains the data of the GPIO inputs or outputs. 0 : GPIO[x] is low (default) 1 : GPIO[x] is high

Table 46. GPIO Data Register (address = 11h)

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	**Reserved** Always write 0h
3:0	CON[3:0]	R/W	0h	**GPIO pin configuration** Configures the GPIO[x] pin as an analog input or GPIO. CON[x] corresponds to the GPIO[x] pin. 0 : GPIO[x] configured as analog input (default) 1 : GPIO[x] configured as GPIO

Tape and Reel Information



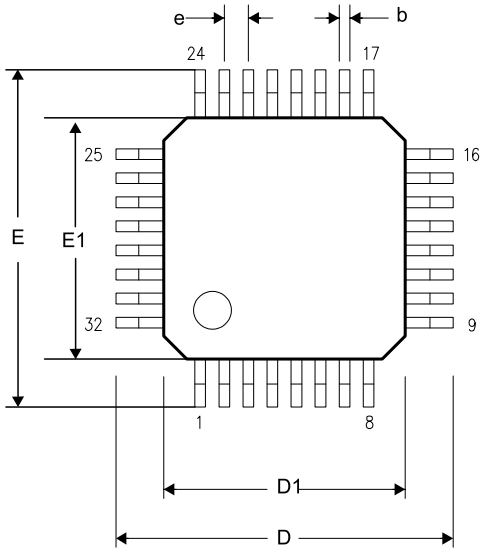


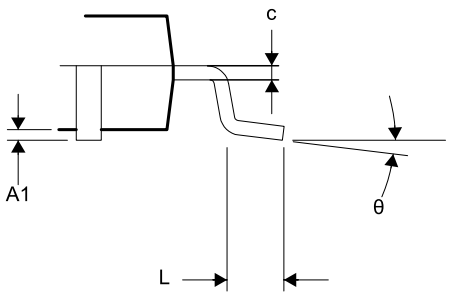
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPC62412-QPER	TQFP5X5-32	330	17.6	7.4	7.4	1.75	12	16	Q2

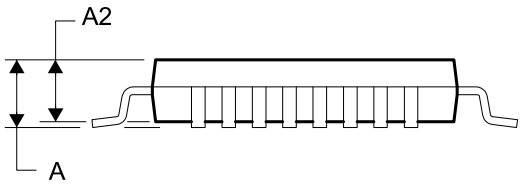
Package Outline Dimensions

TQFP5X5-32

Package Outline Dimensions QPE(TQFP5X5-32-A)







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	NA	1.200	NA	0.047
A1	0.050	0.150	0.002	0.006
A2	0.950	1.050	0.037	0.041
b	0.140	0.230	0.006	0.009
c	0.130	0.180	0.005	0.007
D	6.900	7.100	0.272	0.280
D1	4.950	5.050	0.195	0.199
E	6.900	7.100	0.272	0.280
E1	4.950	5.050	0.195	0.199
e	0.500 BSC		0.020 BSC	
L	0.400	0.700	0.016	0.028
θ	0	7°	0	7°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPC62412-QPER	−40 to 125℃	TQFP5X5-32	62412	MSL3	Tape and Reel, 1000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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