8-/16-Channel, 8-kSPS, 24-Bit, Highly Integrated Sigma-Delta ADC

Features

- ADC Performance:
  - Analog Multiplexer with 8-full Differential or 16-single Ended Inputs
  - Programmable Amplifier Programmable Gain: 1 to 128
  - Low Noise: nV_{RMS}
  - Programmable Data Rates: 2.5 SPS to 8 kSPS
  - Digital Filter: Simultaneous 50-Hz and 60-Hz Rejection at ≤ 20 SPS with Low-Latency Digital Filter
- Integrated Functions:
  - Dual-Matched Programmable Current Sources for Sensor Excitation: 10 μA to 2000 μA
  - Internal Reference: 2.5 V
  - Internal Oscillator
  - Internal Temperature Sensor
  - Extended Fault Detection Circuits
  - Self Offset and System Calibration
  - GPIO and GPO pins with external mux control
- Digital Interface
  - 3-/4- wire SPI-Compatible Interface with CRC Checking
- Digital Supply: 2.7 V to 5 V
- Package: 40-lead 6mm x 6 mm QFN
- Operating Temperature: –40°C to +125°C

Applications

- Process Control: PLC/DCS Modules
- Voltage, Current, Temperature, and Pressure Measurement Flow Meters
- Temperature Controllers
- Medical and Scientific Instrumentation

Description

TPC6240 is a precision 8-/16-channel, multiplexed ADC with integrated PGA and many other features, offering accurate measurement for low-bandwidth input signals, and lower-system cost and component count.

The device has a 24-bit delta-sigma converter, with configurable data rates. There are sinc5 filter for optimized nosie performance, and low-latency filter for fast settling with 50-/60-Hz rejection for noisy industrial environments.

A low-noise programmable gain amplifer provides 1~128 gain options to amplify low-level signals.

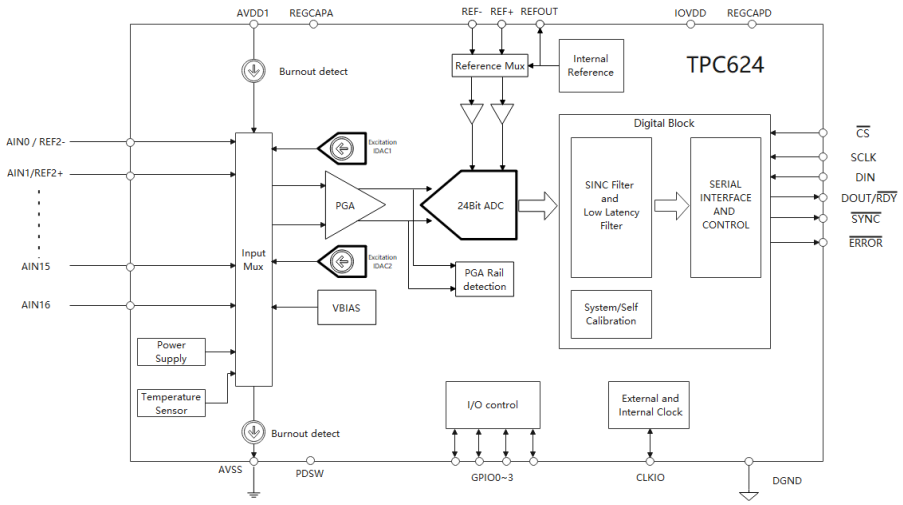
Additionaly, it integrates a precision 2.5-V band gap reference and integrated oscillator.

Two programmable exitation current souces are available for easy RTD biasing for temperature measurement.

Finally, more features such as burn out, CRC, voltage bias, system monitoring, and GPIOs are integrated.

The device is available in QFN6X6-40 package.

Typical Application Circuit



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Product Family Table

Order Number	ADC resolution	ADC channel	Temperature Range	Package
TPC6240-QFER-S	24	16	−40℃ to 125℃	QFN6X6-40

Revision History

Date	Revision	Notes
2023-07-18	Rev.A.0	Released Version.

Pin Configuration and Functions

TPC6240
QFN6X6-40
Top View

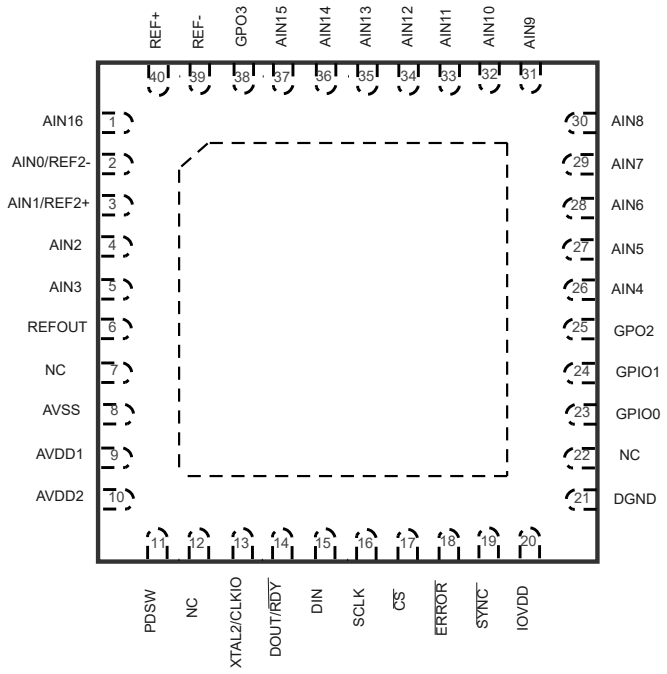


Table 1. Pin Functions: TPC6240

PIN No.	Mnemonic	Type	Description
1		AI	Analog Input. Selectable through cross point mux.
2	AIN0/REF2-	AI	Analog Input 0 (AIN0)/Reference 2, Negative Input (REF2-). An external reference can be applied between REF2+ and REF2-. REF2- can span from AVSS to AVDD1-1V. Analog Input 0 is selectable through cross point mux. Reference 2 can be selected through the REFSEL bits in the setup configuration register.
3	AIN1/REF2+	AI	Analog Input 1 (AIN0)/Reference 2, Positive Input (REF2+). An external reference can be applied between REF2+ and REF2-. REF2+ can span from AVDD1 to AVSS+1V. Analog Input 1 is selectable through cross point mux. Reference 2 can be selected through the REFSEL bits in the setup configuration register.
4	AIN2	AI	Analog Input. Selectable through cross point mux.
5	AIN3	AI	Analog Input. Selectable through cross point mux.
6	REFOUT	AO	Buffered Output of Internal Reference. The output is 2.5 V with respect to AVSS.
7	NC	NC	
8	AVSS	P	Negative Analog Supply. This supply ranges from 0 V to -2.75 V and is nominally set to 0 V.

PIN No.	Mnemonic	Type	Description
9	AVDD1	P	Analog Supply Voltage 1. This voltage ranges from 3.0 V minimum to 5.5 V maximum with respect to AVSS.
10	AVDD2	P	Analog Supply Voltage 2. This voltage should be connected with AVDD1 together.
11	PDSW	AO	Power-Down Switch Connected to AVSS. This pin is controlled by the PDSW bit in the GPIOCON register.
12	NC	NC	
13	CLKIO	DIO	Input 2 for Crystal (XTAL2)/Clock Input or Output (CLKIO). See the CLOCKSEL bit settings in the ADCMODE register (Table 25) for more information.
14	DOUT/$\overline{\text{RDY}}$	DO	Serial Data Output (DOUT)/Data Ready Output ($\overline{\text{RDY}}$). This pin serves a dual purpose. It functions as a serial data output pin to access the output shift register of the ADC. The output shift register can contain data from any of the on-chip data or control registers. The data-word/control word information is placed on the DOUT/$\overline{\text{RDY}}$ pin on the SCLK falling edge and is valid on the SCLK rising edge. When $\overline{\text{CS}}$ is high, the DOUT/$\overline{\text{RDY}}$ output is tristated. When $\overline{\text{CS}}$ is low, and a register is not being read, DOUT/$\overline{\text{RDY}}$ operates as a data ready pin, going low to indicate the completion of a conversion. If the data is not read after the conversion, the pin goes high before the next update occurs. The DOUT/$\overline{\text{RDY}}$ falling edge can be used as an interrupt to a processor, indicating that valid data is available.
15	DIN	DI	Serial Data Input to the Input Shift Register on the ADC. Data in this shift register is transferred to the control registers in the ADC, with the register address (RA) bits of the communications register identifying the appropriate register. Data is clocked in on the rising edge of SCLK.
16	SCLK	DI	Serial Clock Input. This serial clock input is for data transfers to and from the ADC. SCLK has a Schmitt trigger input, making the interface suitable for opto-isolated applications
17	$\overline{\text{CS}}$	DI	Chip Select Input. This is an active low logic input used to select the ADC. $\overline{\text{CS}}$ can be used to select the ADC in systems with more than one device on the serial bus. $\overline{\text{CS}}$ can be hardwired low, allowing the ADC to operate in 3-wire mode with SCLK, DIN, and DOUT used to interface with the device. When $\overline{\text{CS}}$ is high, the DOUT/$\overline{\text{RDY}}$ output is tristated.
18	$\overline{\text{ERROR}}$	DI/O	This pin can be used in one of the following three modes:
			Active low error input mode. This mode sets the ADC_ERROR bit in the STATUS register.
			Active low, open-drain error output mode. The STATUS register error bits are mapped to the $\overline{\text{ERROR}}$ pin. The $\overline{\text{ERROR}}$ pins of multiple devices can be wired together to a common pull-up resistor so that an error on any device can be observed.
			General-purpose output mode. The status of the pin is controlled by the ERR_DAT bit in the GPIOCON register. The pin is referenced between IOVDD and DGND, as opposed to the AVDD1 and AVSS levels used by the GPIO1 and GPIO2 pins. The $\overline{\text{ERROR}}$ pin has an active pull-up in this case.

PIN No.	Mnemonic	Type	Description
19	$\overline{\text{SYNC}}$	DI	Synchronization Input. Allows synchronization of the digital filters and analog modulators when using multiple devices.
20	IOVDD	P	Digital I/O Supply Voltage. IOVDD voltage ranges from 2 V to 5 V. IOVDD is independent of AVDD1 and AVDD2. For example, IOVDD can be operated at 3.3 V when AVDD1 or AVDD2 equals 5 V, or vice versa. If AVSS is set to -2.5 V, the voltage on IOVDD must not exceed 3.6 V.
21	DGND	P	Digital Ground.
22	NC	NC	
23	GPIO0	DI/O	General-Purpose Input/Output. Logic input/output on this this pin is referred to the AVDD1 and AVSS supplies.
24	GPIO1	DI/O	General-Purpose Input/Output. Logic input/output on this this pin is referred to the AVDD1 and AVSS supplies.
25	GPO2	DO	General-Purpose Output. Logic output on this this pin is referred to the AVDD1 and AVSS supplies.
26	AIN4	AI	Analog Input. Selectable through cross point mux.
27	AIN5	AI	
28	AIN6	AI	
29	AIN7	AI	
30	AIN8	AI	
31	AIN9	AI	
32	AIN10	AI	
33	AIN11	AI	
34	AIN12	AI	
35	AIN13	AI	
36	AIN14	AI	
37	AIN15	AI	
38	GPO3	DO	General-Purpose Output. Logic output on this this pin is referred to the AVDD1 and AVSS supplies.
39	REF-	AI	Reference 1 Input Negative Terminal. REF- can span from AVSS to AVDD1-1 V. Reference 1 can be selected through the REFSEL bits in the SETUP CONFIGURATION register.
40	REF+	AI	Reference 1 Input Positive Terminal. An external reference can be applied between REF+ and REF-. REF+ can span from AVDD1 to AVSS + 1 V. Reference 1 can be selected through the REFSEL bits in the SETUP CONFIGURATION register.
	EP	P	Exposed Pad. The exposed pad should be soldered to a similar pad on the PCB under the exposed paddle to confer mechanical strength to the package and for heat dissipation. The exposed pad must be connected to AVSS through this pad on the PCB.

Specifications

Absolute Maximum Ratings (1)

		Min	Max	Unit
Supply Voltage	AVDD1 to AVSS	–0.3	6.5	V
	AVDD1 to DGND	–0.3	6.5	V
	IOVDD to AVSS	–0.3	6.5	V
	IOVDD to DGND	–0.3	6.5	V
	AVSS to DGND	–3.25	0.3	V
Input/Output Pin	Analog Input to AVSS	–0.3	AVDD1 + 0.3	V
	Reference Input to AVSS	–0.3	AVDD1 + 0.3	V
	GPIO to AVSS	–0.3	AVDD1 + 0.3	V
	Digital Input to DGND	–0.3	IOVDD + 0.3	V
	Digital Output to DGND	–0.3	IOVDD + 0.3	V
	Analog and Digital Pin Input Current	–10	10	mA
Temperature	Operating Temperature Range	–40	125	°C
	Maximum Junction Temperature	–40	150	°C
	Storage Temperature Range	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Test Conditions	Min	Typ	Max	Units
Power Supply						
AVDD	Analog Power Supply	AVDD to AVSS	3		5.5	V
		AVSS to DGND	−2.5	0	0	V
		AVDD to DGND	1.5		5.5	V
DVDD	Digital Power Supply	IOVDD to DGND	2		5.5	V
		IOVDD to AVSS	2		8	V
VAIN	Absolute input voltage	PGA bypass	AVSS − 0.05		AVDD + 0.05	V

Parameter		Test Conditions	Min	Typ	Max	Units
		PGA enabled, Gain = 1-8	AVSS + 0.15		AVDD − 0.35	V
		PGA enabled, Gain =16 ~ 128				V
VIN	Differential input voltage	VIN = VAINP − VAINN	−VREF/Gain		VREF/Gain	V
Voltage Reference Input						
VREF	Absolute differential input Voltage		1		AVDD − AVSS	V
VREFN	Absolute negative reference Voltage	REF BUF Bypass	AVSS		VREFP − 1	V
		REF BUF Enable	AVSS + 0.5		VREFP − 1	V
VRFEFP	Absolute positive reference Voltage	REF BUF Bypass	VREFN + 1		AVDD + 0.05	V
		REF BUF Enable	VREFN + 1		AVDD − 0.5	V
External Clock Source						
	external clock frequency		2	4.096	4.5	MHz
	duty cycle		40	50	60	%
Internal Clock Source						
	Clock frequency			4.096		MHz
	Accuracy		−2		2	%
General Purpose Inputs						
	GPIO Input Voltage		AVSS − 0.05		AVDD + 0.05	V
Digital Inputs						
	Digital Input Voltage		DGND		IOVDD	V
Temperature Range						
TJ	Operating junction temperature		−40		125	℃

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
QFN6X6-40	114		°C/W

Electrical Characteristics

All minimum/maximum specifications at T_J = –40℃ to +125℃ and all typical specifications at T_J = 25℃, VDD = 3.0 V to 5.5 V, IOVDD = 1.65 V to 5.5 V, VSS = 0 V, unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Units
Analog Input					
Absolute Input Current	PGA bypassed		20		nA
	PGA enabled		0.1		nA
absolute Input Current Drift	PGA bypassed		2		pA/°C
	PGA enabled		2		pA/°C
Differential Input Current	VCM = AVDD/2, PGA bypassed		1		nA/V
	VCM = AVDD/2, PGA enabled		2		nA
Differential Input Current Drift	VCM = AVDD/2, PGA bypassed		20		pA/°C
	VCM = AVDD/2, PGA enabled		20		pA/°C
System Performance					
Resolution		24			bit
Data Rate		2.5		4k/8k	SPS
INL(best fit)	PGA bypassed		3		ppm_{FSR}
	PGA gain = 1~8		5		ppm_{FSR}
	PGA gain = 16~128		10		ppm_{FSR}
Input Offset Voltage	PGA bypassed	−180		180	μV
	PGA bypassed, after internal vos calibration	on the order of noisepp at the set DR			
	PGA bypassed, Global chop	−3.5	0.2	3.5	μV
	PGA gain = 1		±180		μV
	PGA gain = 2~8		±180/ GAIN		μV
	PGA gain = 16-128		15		μV
Offset Drift	PGA bypassed		200		nV/°C
	PGA Gain = 1~8		100		nV/°C
	PGA Gain = 16~128		20		nV/°C
	PGA bypassed or enable, Global chop		5		nV/°C
Gain Error (Exclude Voltage Reference Error)	PGA bypassed	−450		450	ppm
	PGA Gain = 1	−500		500	ppm
	PGA Gain = 2	−900		900	ppm
	PGA Gain = 4	−1300		1300	ppm
	PGA Gain = 8~128	−1700		1700	ppm
Gain Drift	PGA bypassed		0.5		ppm/°C

Parameter	Test Conditions	Min	Typ	Max	Units
(Exclude Voltage Reference Error)	PGA Gain = 1~128		1		ppm/°C
Noise (inout referred)	PGA Gain = 128, DR = 2.5SPS, sinc3		25		nV_{RMS}
CMRR	at dc ，PGA on		115		dB
PSRR	AVDD at dc，PGA on		90		dB
Voltage Reference inputs					
Absolute Input Current	Ref buffer disabled, ext VREF = 2.5 V		5		uA/V
	Ref buffer enabled, ext VREF = 2.5 V		2		uA/V
Internal Voltage Reference					
Output Voltage			2.5		V
Accuracy	TA = 25°C	±0.1%		±0.1%	%
Temperature Drift	−40~125°C		20		ppm/°C
Output Current	(AVDD = 3.0~3.3)	−5		5	mA
	(AVDD = 3.3~5.5)	−10		10	mA
Short-circuit Llimit Current	sink or source		50		mA
PSRR	AVDD at dc		85		dB
Load Regulation	AVDD = 2.7~3.3 (3.0~3.3), IL=−5~5 mA		60		µV/mA
	AVDD = 3.3~5.25 (3.3~5.5), IL=−10~10 mA		60		µV/mA
Startup Time	1 µF cap, 0.001% settling		5		ms
Capacitive Load Stability		1		47	µF
Reference Noise	0.1~10 Hz, 1 µF cap		12		μV_{PP}
Excitation Current Sources (IDACs)					
Current Setting			10, 50, 100, 250, 500, 750, 1000, 1500, 2000		µA
Compliance Voltage	10 µA~750 µA, 0.1% deviation	AVSS		AVDD-0.4	V
	1 mA~2 mA, 0.1% deviation	AVSS		AVDD-0.6	V
Accuracy (each IDAC) T_A = 25°C	10 µA to 100 µA	−5	0.7	5	%
	250 µA to 2 mA	−3	0.5	3	%
Current Mismatch betwewn IDACs T_A = 25°C	10 µA to 100 µA		0.15	0.8	%
	250 µA to 750 µA		0.1	0.6	%
	1 mA to 2 mA		0.07	0.4	%
Temperature Drift (each IDAC)	10 µA to 750 µA		20		ppm/°C

Parameter	Test Conditions	Min	Typ	Max	Units
	1 m to 2 mA		10		ppm/°C
Temperature Drift Matching between IDACs	10 µA to 100 µA		3		ppm/°C
	250 µA to 2 mA		2		ppm/°C
Startup Time			25		µs
BIAS Voltage					
Output Voltage Settings		(AVDD+AVSS)/2, (AVDD+AVSS)/12			V
Output Voltage Accuracy					%
Output Impedance			800		Ω
Startup Time	1 µF, 0.1% settling		2.8		ms
Burnout Current Sources(BOCS)					
Current Setting			0.2, 1, 10		µA
Accuracy	0.2 µA		±25		%
	1 µA		±4		%
	10 µA		±2		%
Reference Detection					
Threshold 1			0.3		V
Threshold 2					V
Threshold 2 accuracy，T_A = 25		-3	±1	3	%
Pull-together Resistance			10		MΩ
Temperature Sensor					
Output Voltage	T_A = 25°C		130		mV
Temperature Coefficient			436		µV/°C
Accuracy			±2		°C
Low-side Power Switch					
On Resistance			3	5	Ω
Current through Switch	200 mV to AVSS		50		mA
Digital Interface					
V_{IH}		0.7*IOVDD		IOVDD	V
V_{IL}		DGND		0.3*IOVDD	V
V_{OH}		0.8*IOVDD		IOVDD	V
V_{OL}		DGND		0.2*IOVDD	V
Input Current			±1		uA
Power disspation					

Parameter	Test Conditions	Min	Typ	Max	Units
AVDD, PD	AVDD = 3 V		8.5	20	uA
	ADD = 5.5 V		15	30	
AVDD, Standby	AVDD = 3 V		1.1	1.6	mA
	ADD = 5.5 V		1.5	2.1	
AVDD, Norm Run	AVDD = 3 V, GAIN = -2		1.1	1.7	mA
	AVDD = 3 V, GAIN = 8		1.15	1.8	
	AVDD = 3 V, GAIN = 32		1.25	1.9	
	AVDD = 3 V, GAIN = 128		1.5	2.3	
	AVDD = 5.5 V, GAIN = 2		1.6	2.2	
	AVDD = 5.5 V, GAIN = 8		1.65	2.3	
	AVDD = 5.5 V, GAIN = 32		1.7	2.4	
	AVDD = 5.5 V, GAIN = 128		2	2.8	
IODVDD, PD	IOVDD = 2 V		9	70	uA
	IOVDD = 5.5 V		20	110	
IOVDD, Standby,Norm Run	IOVDD = 2 V		15	70	uA
	IOVDD = 5.5 V		40	110	
AVDD UVLO			2.4		V
GPIO					
V_{IH}		0.7*VDD		VDD+0.05	V
V_{IL}		AVSS-0.05		0.3*VDD	V
V_{OH}	IOH = 1 mA	0.8*VDD		VDD	V
V_{OL}	IOL = 1 mA	VSS		0.2*VDD	V
I_O under I_{OVDD}					
V_{IH}	2 V < IOVDD < 2.3 V	0.65*IOVDD			V
	2.3 V < IOVDD < 5.5 V	0.7*IOVDD			V
V_{IL}	2 V < IOVDD < 2.3 V			0.35*IOVDD	V
	2.3 V < IOVDD < 5.5 V			0.7	V
V_{OH}	IOVDD > 4.5 V, Isource = 1 mA	0.8*IOVDD			V
	2.7 V < IOVDD < 4.5 V, Isource = 0.5 mA	0.8*IOVDD			V
	IOVDD < 2.7 V, Isource = 0.2 mA	0.8*IOVDD			V
V_{OL}	IOVDD > 4.5 V, Isink = 2 mA			0.4	V

Parameter	Test Conditions	Min	Typ	Max	Units
	2.7 V < IOVDD < 4.5 V, Isource = 1 mA			0.4	V
	IOVDD < 2.7 V, Isource=0.4mA			0.4	V
Leakage Current			±10		uA

Timing Requirements

All minimum/maximum specifications at T_J = –40℃ to +125℃ and all typical specifications at T_J = 25℃, IOVDD = 2 V to 5.5 V, DOUT = 20 pF to DGND, unless otherwise noted.

Parameter		Test Conditions/Comments	Min	Typ	Max	Unit
SCLK Pulse Width	t_3	SCLK high pulse width	25			ns
	t_4	SCLK low pulse width	25			ns
Read Operation	t_1	CS falling edge to DOUT/RDY active time	0			ns
		IOVDD = 4.5 V to 5.5 V			15	ns
		IOVDD = 2 V to 3.6 V			40	ns
	t_2	SCLK active edge to data valid delay	0			ns
		IOVDD = 4.5 V to 5.5 V			12	ns
		IOVDD = 2 V to 3.6 V			25	ns
	t_5	Bus relinquish time after CS inactive edge	2.5		20	ns
	t_6	SCLK inactive edge to CS inactive edge	0			ns
	t_7	SCLK inactive edge to DOUT/RDY high/low	10			ns
Write Operation	t_8	CS falling edge to SCLK active edge setup time4	0			ns
	t_9	Data valid to SCLK edge setup time	8			ns
	t_{10}	Data valid to SCLK edge hold time	8			ns
	t_{11}	CS rising edge to SCLK edge hold time	5			ns

Timing Diagrams

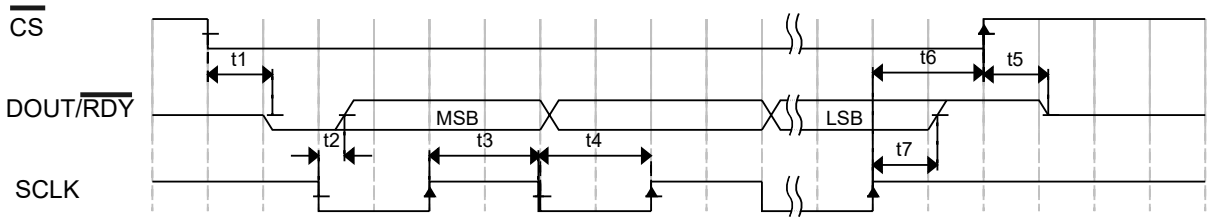


Figure 1. SPI Read Timing Diagram

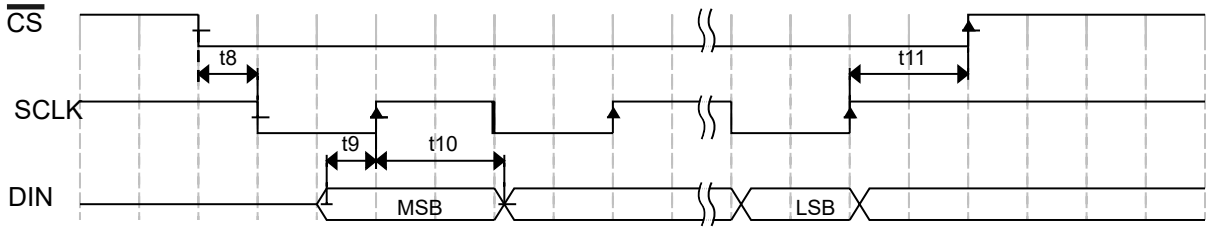


Figure 2. SPI Write Timing Diagram

Noise Performance

Delta-sigma (ΔΣ) analog-to-digital converters (ADCs) are based on the principle of oversampling. The ratio between modulator frequency and output data rate is called the*oversampling ratio*(OSR). By increasing the OSR, and thus reducing the output data rate, the noise performance of the ADC can be optimized. In other words, the input-referred noise drops when reducing the output data rate because more samples of the internal modulator are averaged to yield one conversion result. Increasing the gain also reduces the input-referred noise, which is particularly useful when measuring low-level signals.

Use following equations to calculate effective resolution and noise-free resolution when using a reference voltage other than 2.5 V.

$$\text{Effective Resolution} = \ln[(2 \cdot V_{REF} / \text{Gain}) / V_{RMS\text{-}Noise}] / \ln(2) \quad (1)$$

$$\text{Noise-Free Resolution} = \ln[(2 \cdot V_{REF} / \text{Gain}) / V_{PP\text{-}Noise}] / \ln(2) \quad (2)$$

Table 2. Noise in LSB_{RMS} with $Sinc^5$Filter, Global Chop Disabled, and Internal 2.5-V Reference

	SINC5								
ODR (Hz)	**GAIN=1**	**GAIN=2**	**GAIN=4**	**GAIN=8**	**GAIN=16**	**GAIN=32**	**GAIN=64**	**GAIN=128**	**PGA OFF**
8000	26.98	34.35	44.15	39.90	64.25	109.29	204.84	357.03	31.96
4000	28.12	42.06	40.74	36.17	50.23	83.39	149.16	260.17	32.33
2000	18.03	16.59	17.83	21.60	30.97	59.57	104.06	180.89	15.32
1000	12.21	12.11	12.40	17.81	24.00	40.89	72.42	135.30	11.37
800	9.89	9.32	10.57	14.70	19.92	34.30	64.85	124.29	10.03
400	8.55	8.34	8.82	11.04	16.57	29.17	47.49	90.97	7.88
200	6.60	5.64	6.40	7.66	11.52	20.69	37.88	62.15	5.92
100	5.03	4.22	5.15	5.78	8.27	15.11	26.15	48.55	4.16
60	4.18	3.22	4.06	4.97	6.25	11.35	20.89	37.68	3.47

	SINC5								
ODR (Hz)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128	PGA OFF
50	3.90	3.13	4.01	4.51	6.04	10.09	17.92	35.43	3.42
20	2.97	2.57	2.84	3.37	4.15	7.10	12.88	22.74	2.63
16	2.88	2.55	2.56	3.04	3.93	6.24	12.08	21.63	2.64
10	2.11	2.36	2.53	2.49	2.97	4.62	10.22	16.48	2.26
5	1.05	1.97	2.11	2.02	2.20	3.57	6.82	13.11	1.80
2.5	0.78	2.09	1.72	1.18	1.56	2.89	5.77	10.62	0.87

Table 3. Effective Resolution in RMS Noise with Sinc^{5}Filter, Global Chop Disabled, and Internal 2.5-V Reference

	SINC5								
ODR (Hz)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128	PGA OFF
8000	19.2	18.9	18.5	18.6	18.1	17.3	16.4	15.6	19.4
4000	19.2	19.0	18.9	18.9	18.5	17.8	16.9	16.0	19.2
2000	19.8	19.8	19.8	19.5	19.0	18.3	17.4	16.5	19.9
1000	20.4	20.4	20.3	20.0	19.6	18.7	18.0	17.1	20.5
800	20.7	20.5	20.4	20.2	19.7	18.9	18.0	17.2	20.7
400	20.9	20.8	20.8	20.6	20.1	19.3	18.3	17.4	20.9
200	21.3	21.3	21.2	20.9	20.5	19.8	18.9	18.0	21.3
100	21.7	21.7	21.6	21.4	21.0	20.2	19.4	18.4	21.7
60	21.9	21.9	21.8	21.7	21.4	20.6	19.7	18.9	21.9
50	22.0	22.0	21.9	21.9	21.5	20.7	19.9	18.9	22.0
20	22.4	22.3	22.3	22.3	22.2	21.4	20.5	19.6	22.4
16	22.5	22.3	22.4	22.5	22.3	21.4	20.6	19.8	22.5
10	22.9	22.5	22.5	22.9	22.7	21.9	20.9	20.1	23.0
5	23.9	22.7	22.9	23.5	23.1	22.3	21.6	20.6	24.0
2.5	24.4	23.4	23.7	24.0	23.6	22.9	22.0	21.0	24.4

Table 4. Noise in LSB_{pp} with Sinc^{5}Filter, Global Chop Disabled, and Internal 2.5-V Reference

	SINC5								
ODR (Hz)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128	PGA OFF
8000	189	254	317	265	395	682	1222	2034	172
4000	195	230	234	230	298	553	859	1416	215
2000	117	104	109	149	199	343	740	1298	91
1000	71	77	84	106	124	248	446	874	67
800	67	75	69	80	120	203	395	647	59
400	58	62	56	69	95	151	320	710	53

	SINC5								
ODR (Hz)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128	PGA OFF
200	45	41	41	56	77	120	219	398	42
100	29	31	28	39	56	94	150	311	30
60	26	30	25	31	38	69	125	217	25
50	22	22	26	27	36	69	116	231	22
20	17	19	17	21	23	39	66	137	19
16	17	18	18	17	21	36	67	111	15
10	11	16	15	12	15	32	52	98	10
5	6	11	10	9	12	22	36	69	7
2.5	4	7	6	6	9	14	25	45	4

Table 5. Noise Free Resolution from Peak to Peak Noise with Sinc^{5}Filter, Global Chop Disabled, and Internal 2.5-V Reference

	SINC5								
ODR (Hz)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128	PGA OFF
8000	16.4	16.0	15.7	16.0	15.4	14.6	13.7	13.0	16.6
4000	16.4	16.2	16.1	16.2	15.8	14.9	14.3	13.5	16.3
2000	17.1	17.3	17.2	16.8	16.4	15.6	14.5	13.7	17.5
1000	17.9	17.7	17.6	17.3	17.0	16.0	15.2	14.2	17.9
800	17.9	17.8	17.9	17.7	17.1	16.3	15.4	14.7	18.1
400	18.1	18.0	18.2	17.9	17.4	16.8	15.7	14.5	18.3
200	18.5	18.6	18.6	18.2	17.7	17.1	16.2	15.4	18.6
100	19.1	19.0	19.2	18.7	18.2	17.4	16.8	15.7	19.1
60	19.3	19.1	19.4	19.0	18.8	17.9	17.0	16.2	19.4
50	19.5	19.5	19.3	19.2	18.8	17.9	17.1	16.1	19.5
20	19.9	19.8	19.9	19.6	19.5	18.7	18.0	16.9	19.8
16	19.9	19.8	19.8	19.9	19.6	18.8	17.9	17.2	20.1
10	20.5	20.0	20.1	20.4	20.1	19.0	18.3	17.4	20.7
5	21.4	20.5	20.7	20.8	20.4	19.5	18.8	17.9	21.2
2.5	22.0	21.2	21.4	21.4	20.8	20.2	19.4	18.5	22.0

Table 6. Noise in $LSB_{RMS}$with Low Latency Filter, Global Chop Disabled, and Internal 2.5-V Reference

	LLF								
ODR (Hz)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128	PGA OFF
8000	78.8	105.92	87.27	75.45	97.03	131.3	231.3	457.6	57.17
4000	93.47	95.1	103.09	97.36	76.83	112.8	224.2	382.6	91.19
2000	20.64	21.09	24.73	27.24	42.18	69.88	127.5	242.1	18.47

	LLF								
ODR (Hz)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128	PGA OFF
1000	15.4	17.22	18.79	21.84	31.94	53.66	99.66	183.5	16.13
800	15.81	14.5	16.55	18.94	27.81	49.64	91.83	168.9	14.65
400	10.81	11.36	11.9	14.98	21.21	37.6	65.25	119.5	11
200	7.91	7.66	8.09	10.32	15.27	27.48	52.98	91.35	7.57
100	6.23	5.72	6.2	7.95	10.68	18.48	35.31	63.61	5.7
60	4.55	4.8	5.21	5.98	8.66	15.31	29.31	47.79	4.7
50	4.22	4.47	4.45	5.93	7.99	13.5	26.6	49.27	4.41
20	3.22	3.14	3.2	3.99	4.84	9.23	16.06	32.53	3.05
16	2.95	3.17	3.21	3.6	4.89	8.11	15.43	29.68	2.93
10	2.69	2.78	2.94	3.17	4.02	6.16	12.89	21.62	2.75
5	2.33	2.44	2.48	2.49	2.98	4.64	8.45	16.44	2.19
2.5	1.75	2.32	2.25	1.85	1.92	3.57	7.12	13.09	1.58

Table 7. Effective resolution in RMS noise with Low Latency Filter, Global Chop Disabled, and Internal 2.5-V Reference

	LLF								
ODR (Hz)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128	PGA OFF
8000	18.9	17.8	17.3	17.6	17.7	17.0	16.1	15.2	18.7
4000	18.2	17.6	17.6	18.1	17.8	17.3	16.5	15.7	18.3
2000	19.6	19.5	19.5	19.2	18.7	17.9	17.1	16.1	19.7
1000	20.0	19.9	19.8	19.5	19.1	18.3	17.4	16.5	20.0
800	20.1	20.0	19.9	19.7	19.2	18.4	17.5	16.7	20.1
400	20.5	20.4	20.4	20.1	19.7	18.9	18.0	17.1	20.6
200	20.9	21.0	20.9	20.5	20.1	19.3	18.5	17.5	20.9
100	21.4	21.4	21.3	21.0	20.6	19.8	19.0	18.0	21.3
60	21.7	21.6	21.5	21.4	21.0	20.2	19.3	18.5	21.6
50	21.7	21.7	21.7	21.5	21.1	20.3	19.4	18.6	21.7
20	22.1	22.1	22.1	22.0	21.7	20.9	20.1	19.2	22.1
16	22.2	22.2	22.2	22.1	21.9	21.1	20.2	19.4	22.2
10	22.4	22.4	22.3	22.4	22.3	21.5	20.6	19.6	22.5
5	23.2	22.5	22.6	23.1	22.7	22.0	21.1	20.2	23.2
2.5	23.9	22.8	23.0	23.6	23.1	22.4	21.5	20.7	23.8

Table 8. Noise in LSB_{pp} with Low Latency Filter, Global Chop Disabled, and Internal 2.5-V Reference

	LLF								
ODR (Hz)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128	PGA OFF
8000	223	578	793	642	473	829	1547	2774	397
4000	609	756	954	478	565	840	1335	2147	523
2000	138	151	153	209	241	398	708	1443	119
1000	115	110	115	127	213	291	638	1168	105
800	89	128	97	126	179	336	623	1069	97
400	67	74	72	103	120	220	484	799	68
200	57	55	58	67	92	169	274	647	60
100	32	37	45	48	62	108	214	438	36
60	31	38	40	38	55	87	166	287	34
50	31	29	29	39	51	81	142	267	28
20	19	23	21	26	35	54	97	189	22
16	21	19	19	24	29	55	107	174	20
10	16	16	17	18	20	36	67	128	17
5	9	15	13	13	17	24	42	79	10
2.5	7	12	10	8	12	18	38	65	8

Table 9. Noise Free Resolution from Peak to Peak noise with Low Latency Filter, Global Chop Disabled, and Internal 2.5-V Reference

	LLF								
ODR (Hz)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128	PGA OFF
8000	16.2	14.8	14.4	14.7	15.1	14.3	13.4	12.6	15.4
4000	14.7	14.4	14.1	15.1	14.9	14.3	13.6	12.9	15.0
2000	16.9	16.8	16.7	16.3	16.1	15.4	14.5	13.5	17.1
1000	17.2	17.2	17.2	17.0	16.3	15.8	14.7	13.8	17.3
800	17.5	17.0	17.4	17.0	16.5	15.6	14.7	13.9	17.4
400	17.9	17.8	17.8	17.3	17.1	16.2	15.1	14.4	17.9
200	18.2	18.2	18.1	17.9	17.5	16.6	15.9	14.7	18.1
100	19.0	18.8	18.5	18.4	18.0	17.2	16.3	15.2	18.8
60	19.0	18.8	18.7	18.8	18.2	17.6	16.6	15.8	18.9
50	19.0	19.1	19.1	18.7	18.3	17.7	16.9	15.9	19.2
20	19.8	19.5	19.6	19.3	18.9	18.2	17.4	16.4	19.5
16	19.6	19.8	19.8	19.4	19.1	18.2	17.3	16.6	19.7
10	20.0	20.0	19.9	19.8	19.7	18.8	17.9	17.0	19.9
5	20.8	20.1	20.3	20.3	19.9	19.4	18.6	17.7	20.7
2.5	21.2	20.4	20.7	21.0	20.4	19.8	18.8	18.0	21.0

Table 10. Noise in LSB_{RMS} with $Sinc^5$ Filter, Global Chop Enabled, and Internal 2.5-V Reference

	SINC5								
ODR (Hz)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128	PGA OFF
8000	25.00	42.49	43.10	60.40	48.27	81.85	149.72	281.31	45.47
4000	63.66	51.85	54.42	46.08	39.96	57.27	103.92	201.59	56.77
2000	12.33	12.85	14.71	15.64	23.20	40.35	77.98	133.62	12.16
1000	8.62	8.89	9.74	11.22	29.12	27.74	52.73	96.30	8.27
800	7.65	7.47	8.60	10.62	13.94	23.77	45.66	88.30	7.77
400	5.97	6.56	6.82	8.05	11.69	20.60	38.44	68.53	6.08
200	4.24	4.23	4.86	6.02	8.41	14.45	26.21	49.76	4.00
100	3.31	3.04	3.43	4.11	5.66	9.49	18.44	33.54	3.13
60	2.34	2.47	2.60	3.47	4.60	7.37	14.67	26.11	2.38
50	2.25	2.19	2.36	2.90	4.09	7.13	13.14	23.96	2.19
20	1.32	1.42	1.63	1.88	2.57	4.37	8.85	16.13	1.29
16	1.26	1.29	1.46	1.80	2.48	3.86	7.50	14.13	1.28
10	1.02	1.04	1.15	1.27	1.96	3.13	5.82	10.91	1.00
5	0.78	0.73	0.80	0.99	1.32	2.17	4.01	7.67	0.75
2.5	0.56	0.58	0.66	0.74	1.01	1.61	3.02	5.52	0.58

Table 11. Effective Resolution from RMS Noise with $Sinc^5$ Filter, Global Chop Enabled, and Internal 2.5-V Reference

	SINC5								
ODR (Hz)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128	PGA OFF
8000	19.4	18.6	18.6	18.1	18.4	17.6	16.8	15.9	18.5
4000	18.0	18.3	18.2	18.5	18.7	18.2	17.3	16.3	18.2
2000	20.4	20.3	20.1	20.0	19.5	18.7	17.7	16.9	20.4
1000	20.9	20.8	20.7	20.5	19.1	19.2	18.3	17.4	21.0
800	21.1	21.1	20.9	20.6	20.2	19.4	18.5	17.5	21.0
400	21.4	21.3	21.2	21.0	20.5	19.6	18.7	17.9	21.4
200	21.9	21.9	21.7	21.4	20.9	20.1	19.3	18.4	22.0
100	22.3	22.4	22.2	22.0	21.5	20.8	19.8	18.9	22.4
60	22.8	22.7	22.6	22.2	21.8	21.1	20.1	19.3	22.8
50	22.8	22.9	22.8	22.5	22.0	21.2	20.3	19.4	22.9
20	23.6	23.5	23.3	23.1	22.6	21.9	20.9	20.0	23.6
16	23.7	23.6	23.4	23.2	22.7	22.1	21.1	20.2	23.6
10	24.0	23.9	23.8	23.7	23.0	22.4	21.5	20.6	24.0
5	24.4	24.5	24.3	24.0	23.6	22.9	22.0	21.1	24.4
2.5	24.8	24.8	24.6	24.4	24.0	23.3	22.4	21.5	24.8

Table 12. Noise in LSB_{pp} with $Sinc^5$Filter, Global Chop Enabled, and Internal 2.5-V Reference

	SINC5								
ODR (Hz)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128	PGA OFF
8000	207	294	352	312	295	484	897	1799	290
4000	305	247	287	295	231	397	725	1410	284
2000	85	79	87	103	143	235	465	821	75
1000	49	47	64	65	573	159	303	477	47
800	43	42	49	71	84	131	279	492	45
400	41	34	45	51	68	125	207	384	38
200	27	32	26	33	53	81	147	299	23
100	18	18	20	24	40	56	113	195	18
60	14	14	14	20	25	40	88	169	15
50	14	13	16	18	25	43	82	144	12
20	7	8	10	11	16	25	52	97	8
16	7	8	8	12	14	25	45	82	7
10	6	6	7	8	11	20	33	64	5
5	5	4	4	5	8	13	24	46	4
2.5	2	2	4	4	5	9	17	29	3

Table 13. Noise Free Resolution from Peak to Peak noise with $Sinc^5$Filter, Global Chop Enabled, and Internal 2.5-V Reference

	SINC5								
ODR (Hz)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128	PGA OFF
8000	16.3	15.8	15.5	15.7	15.8	15.1	14.2	13.2	15.8
4000	15.7	16.1	15.8	15.8	16.1	15.4	14.5	13.5	15.9
2000	17.6	17.7	17.6	17.3	16.8	16.1	15.1	14.3	17.8
1000	18.4	18.4	18.0	18.0	14.8	16.7	15.8	15.1	18.4
800	18.6	18.6	18.4	17.9	17.6	17.0	15.9	15.1	18.5
400	18.6	18.9	18.5	18.3	17.9	17.0	16.3	15.4	18.8
200	19.2	19.0	19.3	19.0	18.3	17.7	16.8	15.8	19.5
100	19.8	19.8	19.7	19.4	18.7	18.2	17.2	16.4	19.8
60	20.2	20.2	20.2	19.7	19.4	18.7	17.5	16.6	20.1
50	20.2	20.3	20.0	19.8	19.4	18.6	17.6	16.8	20.4
20	21.2	21.0	20.7	20.5	20.0	19.4	18.3	17.4	21.0
16	21.2	21.0	21.0	20.4	20.2	19.4	18.5	17.6	21.2
10	21.4	21.4	21.2	21.0	20.5	19.7	19.0	18.0	21.7
5	21.7	22.0	22.0	21.7	21.0	20.3	19.4	18.5	22.0

	SINC5								
ODR (Hz)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128	PGA OFF
2.5	23.0	23.0	22.0	22.0	21.7	20.8	19.9	19.1	22.4

Table 14. Noise in LSB_{RMS} with Low Latency Filter, Global Chop Enabled, and Internal 2.5-V Reference

	LLF								
ODR (Hz)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128	PGA OFF
8000	49.13	85.38	33.97	95.63	69.61	99.45	179.22	323.61	54.93
4000	70.21	34.15	106.43	62.18	48.80	66.13	131.27	235.47	58.05
2000	16.15	16.67	16.74	21.61	28.71	49.58	96.51	166.91	17.01
1000	11.95	14.00	13.78	16.72	23.69	39.57	68.07	131.44	12.37
800	13.41	12.49	12.46	16.43	20.96	33.10	68.66	121.36	12.89
400	7.61	8.28	9.38	10.53	14.93	26.04	50.76	84.77	7.97
200	8.44	5.92	6.70	7.69	11.47	18.31	36.53	63.77	5.87
100	4.24	4.62	4.44	5.57	7.34	12.24	25.43	45.75	3.88
60	3.05	3.43	3.43	4.31	6.09	9.70	18.95	36.06	3.19
50	2.72	2.93	3.16	3.80	5.32	9.83	17.38	32.56	2.75
20	1.80	1.96	2.22	2.56	3.44	6.00	11.66	20.69	1.86
16	1.65	1.79	1.90	2.48	3.06	5.43	9.61	19.83	1.61
10	1.32	1.38	1.41	1.79	2.33	4.12	7.92	14.23	1.29
5	0.99	0.97	1.13	1.26	1.83	3.06	5.79	10.72	0.95
2.5	0.71	0.68	0.81	0.94	1.30	2.28	4.04	7.76	0.68

Table 15. Effective Resolution from RMS Noise with Low Latency Filter, Global Chop Enabled, and Internal 2.5-V Reference

	LLF								
ODR (Hz)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128	PGA OFF
8000	18.4	17.6	18.9	17.4	17.9	17.4	16.5	15.7	18.2
4000	17.9	18.9	17.3	18.0	18.4	18.0	17.0	16.1	18.1
2000	20.0	19.9	19.9	19.6	19.2	18.4	17.4	16.6	19.9
1000	20.4	20.2	20.2	19.9	19.4	18.7	17.9	17.0	20.4
800	20.3	20.4	20.4	20.0	19.6	19.0	17.9	17.1	20.3
400	21.1	21.0	20.8	20.6	20.1	19.3	18.3	17.6	21.0
200	20.9	21.4	21.3	21.1	20.5	19.8	18.8	18.0	21.4
100	21.9	21.8	21.8	21.5	21.1	20.4	19.3	18.5	22.0
60	22.4	22.2	22.2	21.9	21.4	20.7	19.8	18.8	22.3
50	22.6	22.4	22.3	22.1	21.6	20.7	19.9	19.0	22.5
20	23.2	23.0	22.8	22.6	22.2	21.4	20.5	19.6	23.1

	LLF								
ODR (Hz)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128	PGA OFF
16	23.3	23.2	23.1	22.7	22.4	21.6	20.7	19.7	23.3
10	23.6	23.5	23.5	23.2	22.8	22.0	21.0	20.2	23.6
5	24.0	24.0	23.8	23.7	23.1	22.4	21.5	20.6	24.1
2.5	24.5	24.5	24.3	24.1	23.6	22.8	22.0	21.0	24.6

Table 16. Noise in LSB_{pp} with Low Latency Filter, Global Chop Enabled, and Internal 2.5-V Reference

	LLF								
ODR (Hz)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128	PGA OFF
8000	265	424	387	417	384	638	1081	1900	349
4000	425	366	432	413	328	428	836	1274	442
2000	110	91	110	158	181	321	569	1081	93
1000	80	83	91	92	145	237	447	991	74
800	80	77	72	95	119	191	408	757	75
400	41	57	52	62	84	151	318	481	44
200	147	32	47	47	73	109	215	392	43
100	28	27	25	30	46	84	159	314	26
60	19	20	20	29	39	60	117	195	21
50	15	19	18	21	39	56	104	180	17
20	10	11	14	14	20	31	70	124	11
16	9	11	12	16	17	34	64	112	10
10	9	8	8	9	12	23	51	83	7
5	6	6	6	8	11	19	33	75	6
2.5	4	4	4	6	7	13	26	50	4

Table 17. Noise Free Resolution from Peak to Peak noise with Low Latency Filter, Global Chop Enabled, and Internal 2.5-V Reference

	LLF								
ODR (Hz)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128	PGA OFF
8000	16.0	15.3	15.4	15.3	15.4	14.7	13.9	13.1	15.6
4000	15.3	15.5	15.2	15.3	15.6	15.3	14.3	13.7	15.2
2000	17.2	17.5	17.2	16.7	16.5	15.7	14.8	13.9	17.5
1000	17.7	17.6	17.5	17.5	16.8	16.1	15.2	14.0	17.8
800	17.7	17.7	17.8	17.4	17.1	16.4	15.3	14.4	17.8
400	18.6	18.2	18.3	18.0	17.6	16.8	15.7	15.1	18.5
200	16.8	19.0	18.4	18.4	17.8	17.2	16.3	15.4	18.6
100	19.2	19.2	19.4	19.1	18.5	17.6	16.7	15.7	19.3

	LLF								
ODR (Hz)	GAIN=1	GAIN=2	GAIN=4	GAIN=8	GAIN=16	GAIN=32	GAIN=64	GAIN=128	PGA OFF
60	19.8	19.7	19.7	19.1	18.7	18.1	17.1	16.4	19.6
50	20.1	19.8	19.8	19.6	18.7	18.2	17.3	16.5	19.9
20	20.7	20.5	20.2	20.2	19.7	19.0	17.9	17.0	20.5
16	20.8	20.5	20.4	20.0	19.9	18.9	18.0	17.2	20.7
10	20.8	21.0	21.0	20.8	20.4	19.5	18.3	17.6	21.2
5	21.4	21.4	21.4	21.0	20.5	19.8	19.0	17.8	21.4
2.5	22.0	22.0	22.0	21.4	21.2	20.3	19.3	18.4	22.0

Detailed Description

Overview

TPC6240 is a precision 8-/16-channel, multiplexed ADC with integrated PGA and many other features, offering accurate measurement for low bandwidth input signals, and lower system cost and component count.

The device has a 24-bit delta-sigma converter, with configurable data rates. There are sinc5 filter for optimized nosie performance, and low latency filter for fast settling with 50-/60-Hz rejection for noisy industrial environments.

The TPC6240 incorporates several features that simplify precision sensor measurements. Key integrated features include:

- Low-noise PGA with integrated signal fault detection
- Low-drift 2.5-V voltage reference
- Dual, matched, sensor-excitation current sources (IDACs)
- Two sets of buffered external reference inputs with reference voltage level detection
- Internal oscillator
- Temperature sensor
- General-purpose input/output pins (GPIOs)
- A low-resistance switch connected to AVSS which can be used to disconnect bridge sensors to reduce current consumption

Analog inputs are configurable to be either single-ended inputs, differential inputs, or combination of the two. Many of the analog inputs have following features which can be programmed by the user. Please refer to register map for detail configuration information.

- Two sensor excitation current sources
- Sensor biasing voltage (VBIAS)
- Sensor burn-out current sources

The AVDD analog supply operates with bipolar supplies from ±1.5 V to ±2.625 V or with a unipolar supply from 3 V to 5.25 V.

Functional Block Diagram

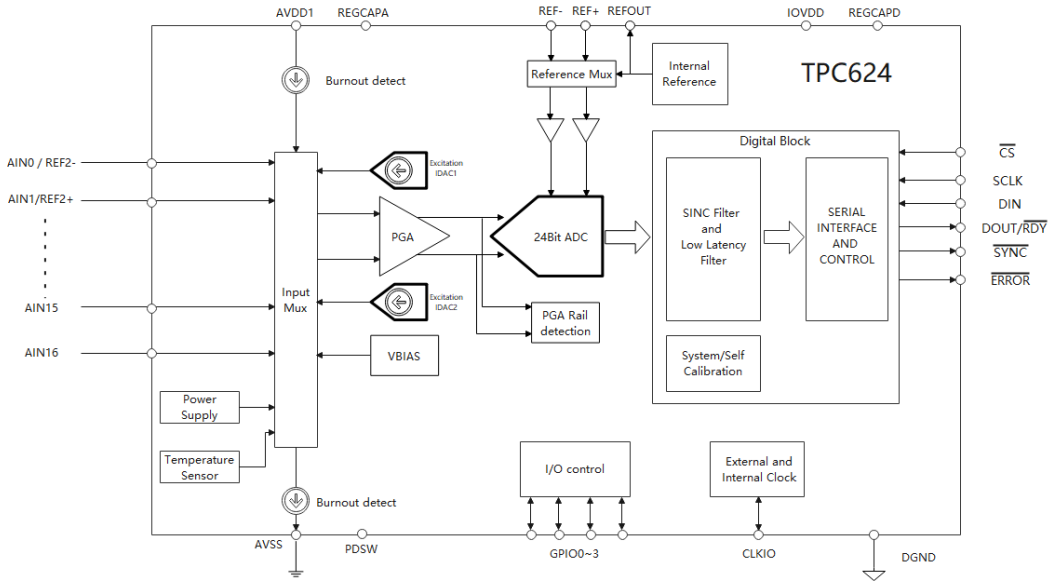


Figure 3. Functional Block Diagram

Feature Description

Multiplexer

The device contains a flexible input multiplexer; Any analog inputs can be selected as the positive or negative input for the PGA or ADC input.

The multiplexer can also route the excitation current sources to drive external resistive sensors (bridges, RTDs, and thermistors).

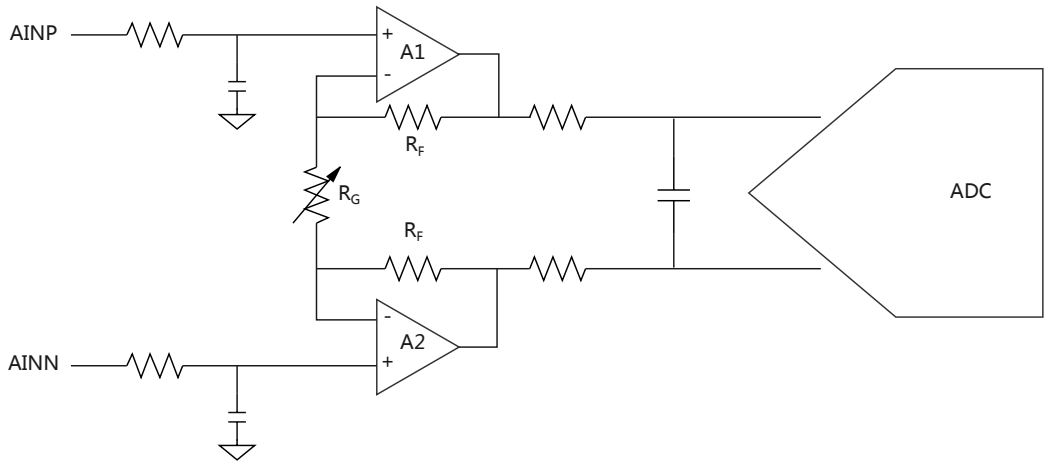
The device can provide bias voltages for unbiased sensors (unbiased thermocouples for example) to analog input pins.

The device also has several system monitor functions which can be measured through the multiplexer:

- The inputs can be shorted together at mid-supply [(AVDD + AVSS) / 2] to measure and calibrate the input offset of the analog front-end and the ADC.
- The system monitor also includes a temperature sensor that provides a measurement of the device temperature.
- The system monitor can also measure the supply voltage, measuring [(AVDD – AVSS) / 4] for the analog supply.
- The system monitor contains a set of burn-out current sources that pull the inputs to either supply if the sensor has burned out and has a high impedance so that the ADC measures a full-scale reading.

Low-Noise Programmable Gain Amplifier

The device features a low-drift, low-noise, high-input impedance programmable gain amplifier (PGA). The PGA consists of two chopper-stabilized amplifiers and a resistor feedback network that sets the gain of the PGA.



The PGA can be set to be 1, 2, 4, 8, 16, 32, 64, or 128 by using the GAIN[2:0] bits in the gain setting register. Gain is changed inside the device using a variable resistor, R_G. The differential full-scale input voltage range (FSR) of the PGA is defined by the gain setting and the reference voltage used, as shown in

$$FSR = \pm V_{REF} / \text{Gain} \quad (3)$$

Following is the full-scale ranges when using the internal 2.5-V reference. The PGA gains 64 and 128 are established in the digital domain. When the device is set to 64 or 128, the PGA is set to a gain of 32, and additional gain is established with digital scaling. The input-referred noise does still improve compared to the gain = 32 setting because the PGA is biased with a higher supply current to reduce noise.

Table 18. PGA Full Scale Range

GAIN SETTING	FSR
1	±2.5 V
2	±1.25 V
4	±0.625 V
8	±0.313 V
16	±0.156 V
32	±0.078 V
64	±0.039 V
128	±0.020 V

The PGA can be enabled by setting corresponding values in the AIN_PGA(N)[1:0] bits of the gain setting register, and also can be disabled and bypassed.

PGA Input-Voltage Requirements

The PGA maximum and minimum absolute input voltages are limited by the voltage swing capability of the PGA output. The specified minimum and maximum absolute input voltages (V_{AINP} and V_{AINN}) depend on the PGA gain, the maximum differential input voltage (V_{INMAX}), and the tolerance of the analog power-supply voltages (AVDD and AVSS). Use the maximum voltage expected in the application for V_{INMAX}.

$$AVSS + 0.15\ V + |V_{INMAX}| \cdot (Gain - 1) / 2 < V_{AINP}, V_{AINN} < AVDD - 0.35\ V - |V_{INMAX}| \cdot (Gain - 1) / 2 \quad (4)$$

where V_{AINP}, V_{AINN} = absolute input voltage, $V_{INMAX} = V_{AINP} - V_{AINN}$ = maximum differential input voltage.

As mentioned in the previous section, PGA gain settings of 64 and 128 are scaled in the digital domain and are not implemented with the amplifier. When using the PGA in gains of 64 and 128, set the gain to be 32 to calculate the absolute input voltage range.

PGA Rail Flags

The PGA output rail detection circuit can be enabled using the FL_RAIL_EN bit in the ADCMODE register. The PGA rail flags (FL_P_RAILP, FL_P_RAILN, FL_N_RAILP, and FL_N_RAILN) in the status register indicate if the positive or negative output of the PGA is closer to the analog supply rails than 150 mV. A flag going high indicates that the PGA is operating outside the linear operating or absolute input voltage range.

Bypassing the PGA

The device can be configured to disable and bypass the PGA by setting the PGA_EN[1:0] bits, and also removes the input range restrictions at a gain of 1. If the PGA is bypassed, the ADC absolute input voltage range extends beyond the AVDD and AVSS power supplies, allowing input voltages at or below ground.

In order to measure single-ended signals that are referenced to AVSS ($AIN_P = V_{IN}$, AIN_N = AVSS), the PGA must be bypassed.

Voltage Reference

The device offers an integrated low-drift 2.5-V reference, and for applications that require a different reference voltage value or a ratiometric measurement approach, the device offers two differential reference input pairs (REF+, REF- and REF1+, REF1-).

For external reference, the reference voltage is:

$$VREF = V(REFPx) - V(REFNx) \quad (5)$$

Where $V_{(REFPx)}$and $V_{(REFNx)}$are the absolute positive and absolute negative reference voltages

The polarity of the reference voltage internal to the ADC must be positive. The magnitude of the reference voltage together with the PGA gain establishes the ADC full-scale differential input range as defined by FSR = $\pm V_{REF}$/ Gain.

The ADC also contains an integrated reference voltage monitor. This monitor provides continuous detection of a low or missing reference during the conversion cycle. The reference monitor flags (FL_REF_L0 and FL_REF_L1) are set in the STATUS byte.

Internal Reference

The ADC integrates a precision, low-drift, 2.5-V reference. By default, the internal voltage reference is powered down, and can be enabled with setting corresoponding registers.

The REFOUT pin provides a buffered reference output voltage when the internal reference voltage is enabled. Suggest to connect a capacitor between REFOUT and AVSS. Larger capacitor can filter more noise at the expense of a longer reference start-up time.

The capacitor is not required if the internal reference is not used.

The internal reference must be powered on if using the IDACs.

External Reference

The device provides two external reference inputs, which are differential with independent positive and negative inputs.

Internal or external reference buffers can be used to reduce the input current. Without buffering, the reference input current can lead to errors from either high reference source impedance or through reference input filtering.

Be careful that the specified absolute and differential reference voltage requirements shoud be followed when using internal or external reference.

Reference Buffers

The device has two individually selectable reference input buffers to lower the reference input current. Use the REF_BUF_(N) [1:0] bits to enable or disable the positive and negative reference buffers respectively.

The reference buffers are recommended to be disabled when the internal reference is selected, or when the external reference input is at the supply voltage (REFPx at AVDD or REFNx at AVSS).

Clock Source

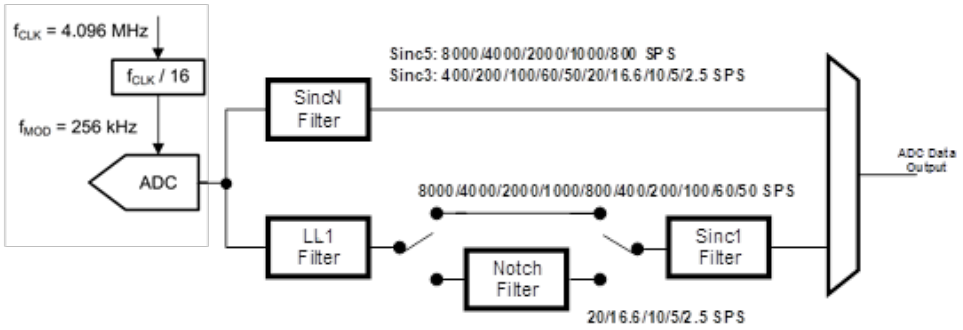
The device's clock is either provided by the internal low-drift oscillator or an external clock source on the CLK input, which can be selected by register. The internal oscillator is used by default after power up.

Delta-Sigma Modulator

A high order delta-sigma (ΔΣ) modulator is used ito convert the analog input voltage into a data stream. The modulator runs at a clock frequency of f_{MOD}= f_{CLK}/ 16, where f_{CLK} is either provided by the internal oscillator or the external clock source

Digital Filter

The device offers a sincN filter and a low- latency filter (low-latency filter) for both filtering and decimation of the digital data stream coming from the delta-sigma modulator. The implementation of the digital filter is determined by the data rate and filter mode.



Regardless of the FILTER type setting, the oversampling ratio is the same for each given data rate, meaning that the device requires a set number of modulator clocks to output a single ADC conversion data. The output data rate and corresponding oversampling ratio are shown below:

Table 19. ADC Data rate and digital filter oversampling ratio

NOMINAL DATA RATE (SPS) (1)	DATA RATE REGISTER DR[3:0]	OVERSAMPLING RATIO (2)
2.5	0000	102400
5	0001	51200
10	0010	25600
16.6	0011	15360
20	0100	12800
50	0101	5120
60	0110	4264
100	0111	2560
200	1000	1280
400	1001	640
800	1010	320
1000	1011	256
2000	1100	128
4000	1101	64
8000	1110	64
8000	1111	64

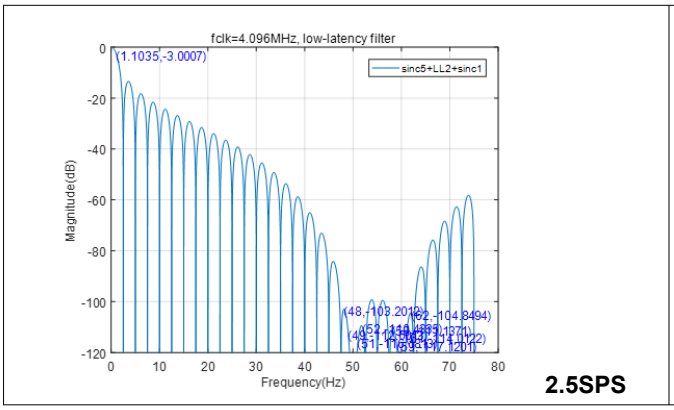
Low-Latency Filter

The low-latency filter can be selected by the FILTER bit. The filter is a finite impulse response (FIR) filter that provides settled data, given that the analog input signal has settled to the final value before the conversion is started. The low-latency filter is especially useful when multiple channels must be scanned in minimal time.

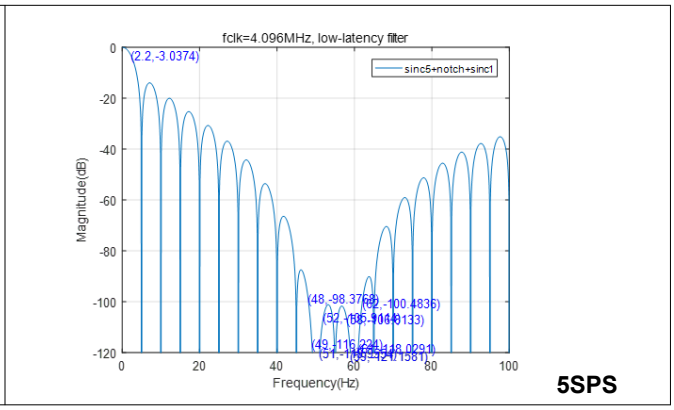
Low-Latency Filter Frequency Response

When The low-latency filter is selected, it provides both 50-Hz and 60-Hz line cycle noise rejection at data rate options at 2.5 SPS, 5 SPS, 10 SPS, and 20 SPS.

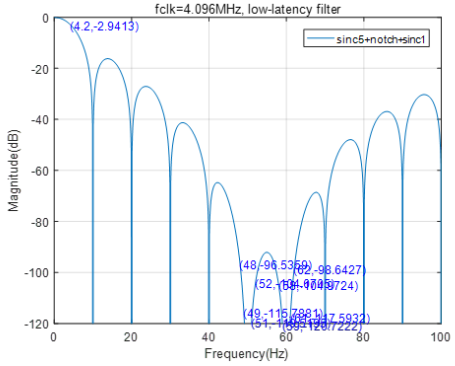
Following is the frequency response of the low-latency filter for different data rates.



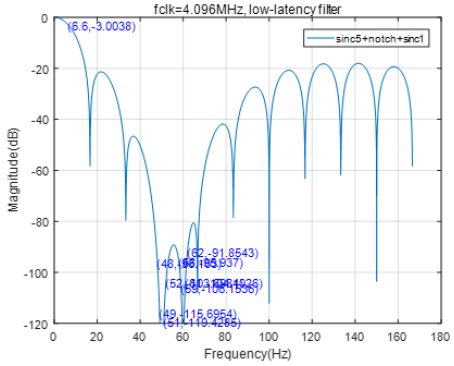
2.5SPS



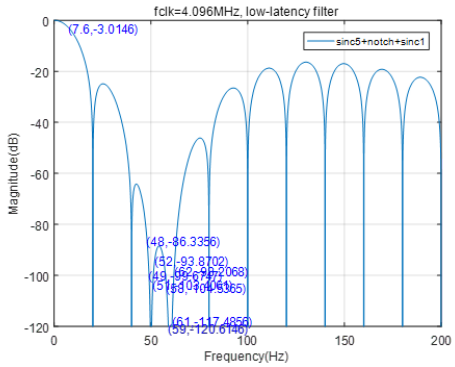
5SPS



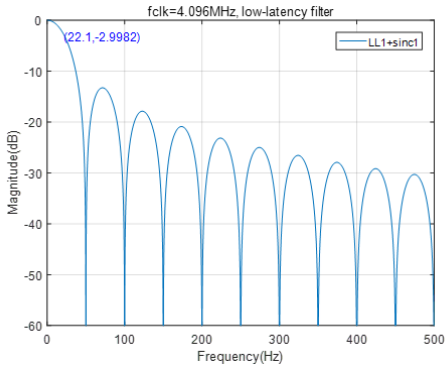
10SPS



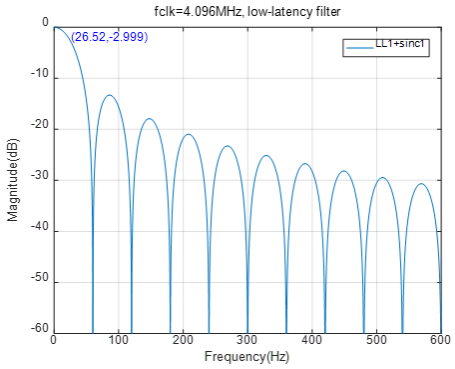
16.6SPS



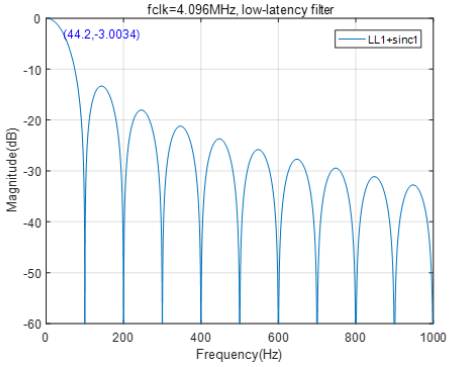
20SPS



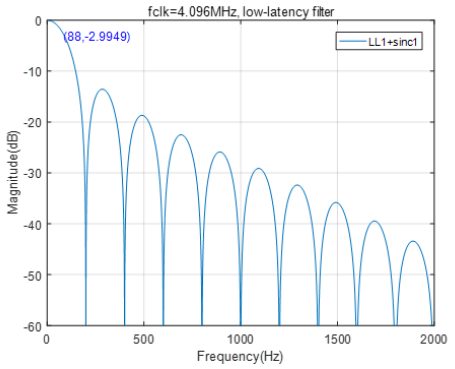
50SPS



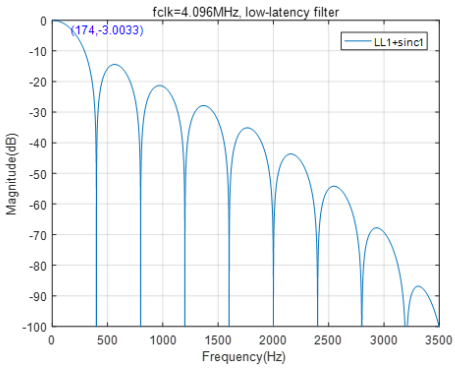
60SPS



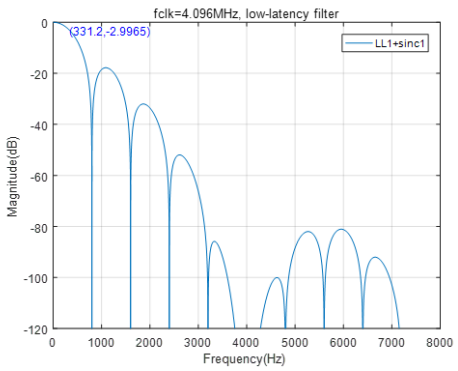
100SPS



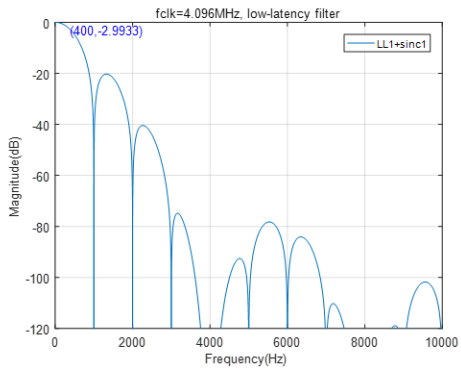
200SPS



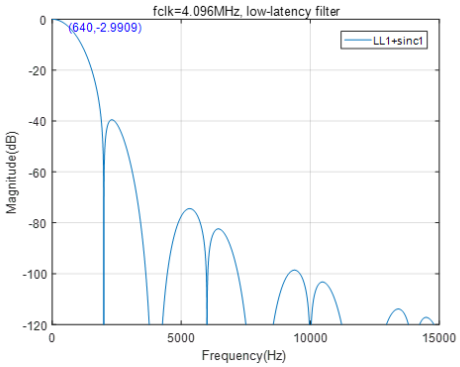
400SPS



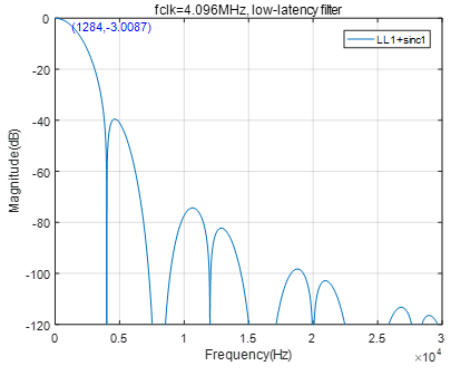
800SPS



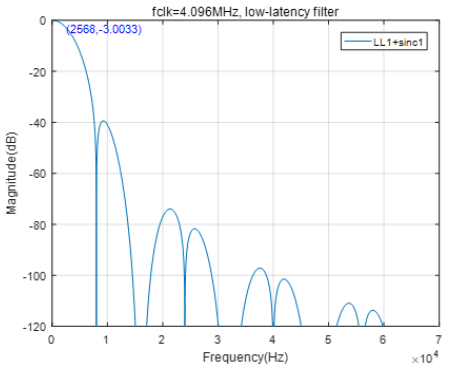
1000SPS



2000SPS



4000SPS



8000SPS

Following is the bandwidth of the low-latency filter for each data rate.

NOMINAL DATA RATE (SPS) (1)	–3-dB BANDWIDTH (Hz) (1)
8000	2568.66
4000	1284.33
2000	642.02
1000	401.08
800	331.92
400	174.19
200	88.21
100	44.25
60	26.43

NOMINAL DATA RATE (SPS) (1)	–3-dB BANDWIDTH (Hz) (1)
50	22.14
20	8.85
16.67	7.38
10	4.43
5	2.21
2.5	1.11

Note: Valid for the internal oscillator or an external 4.096-MHz clock. Scales proportional with f_{CLK}

Please be noted that the low-latency filter notches and output data rate scale proportionally with the clock frequency. When external clock frequency is used, the data rate, conversion time, and filter notches will vary consequently.

Data Conversion Time for the Low-Latency Filter

The data settles in one data period when the low-latency filter is selected. However, a small amount of latency exists to calculate the conversion data from the modulator and do other operations. So the first conversion data takes a little bit longer than subsequent data conversions.

Following table shows the conversion times for the low-latency filter in each data rate and various conversion modes.

NOMINAL DATA RATE (1)(SPS)	Global Chopper OFF		Global Chopper ON
	FIRST DATA FOR CONTINUOUS CONVERSION MODE OR SINGLE-SHOT CONVERSION MODE(2)(ms) (3)	SECOND AND SUBSEQUENT CONVERSIONS FOR CONTINUOUS CONVERSION MODE (ms) (3)	FIRST or SECOND DATA FOR CONTINUOUS CONVERSION MODE OR SINGLE-SHOT CONVERSION MODE (2) (ms) (3)
8000	0.4525	0.128	0.8945
4000	0.8385	0.256	1.6665
2000	1.6065	0.512	3.2025
1000	2.1185	1.024	4.2265
800	2.3745	1.28	4.7385
400	3.6545	2.56	7.2985
200	6.2145	5.12	12.4185
100	11.3345	10.24	22.6585
60	18.2465	17.152	36.4825
50	21.5745	20.48	43.1385
20	55.3665	51.2	110.7225
16	65.6065	61.44	131.2025
10	106.5665	102.4	213.1225
5	208.9665	204.8	417.9225
2.5	413.7665	409.6	827.5225

Note: Valid for the internal oscillator or an external 4.096-MHz clock. Scales proportional with f_{CLK}

Note: Conversions start at the rising edge of the START pin or on the final clock edge for a START command

Note: Time does not include the programmable delay set by the DELAY[2:0] bits in the gain setting register.

Note: Subsequent readings in continuous conversion mode do not have the programmable delay time.

SincN Filter

The sincN digital filter is also available. Compared with low-latecy filter, it has improved noise performance but has a N-cycle latency to get data out.

SincN Filter Frequency Response

The sincN digital filter's response scales with the data rate and has notches at multiples of the data rate. It has simultaneous 50-Hz and 60-Hz rejection at data rates of 2.5 SPS, 5 SPS, and 10 SPS. And it has only 50-Hz rejection at data rates of 16.6 SPS and 50 SPS, and only 60-Hz rejection at data rates of 20 SPS and 60 SPS.

Following is the bandwidth of the sincN filter for each data rate.

NOMINAL DATA RATE (SPS) (1)	–3-dB BANDWIDTH (Hz) (1)
8000	1630.80
4000	815.40
2000	407.70
1000	203.85
800	163.08
400	104.78
200	52.39
100	26.19
60	15.72
50	13.10
20	5.24
16.67	4.37
10	2.62
5	1.31
2.5	0.65

Note: Valid for the internal oscillator or an external 4.096-MHz clock. Scales proportional with f_{CLK}.

And filter notches and output data rate scale proportionally with the clock frequency.

Data Conversion Time for the SincN Filter

The sincN filter normally takes 5 (for ODR >=800Hz) or 3 (for ODR <=400Hz) conversions to settle, and it needs different amounts of time to complete a conversion.

Following is the conversion times for the sincN filter for each ADC data rate and various conversion modes

NOMINAL DATA RATE (1)(SPS)	Global Chopper OFF		Global Chopper ON
	FIRST DATA FOR CONTINUOUS CONVERSION MODE OR SINGLE-SHOT CONVERSION MODE (2) (ms) (3)	SECOND AND SUBSEQUENT CONVERSIONS FOR CONTINUOUS CONVERSION MODE (ms) (3)	FIRST or SECOND DATA FOR CONTINUOUS CONVERSION MODE OR SINGLE-SHOT CONVERSION MODE(2) (ms)(3)
8000	0.708	0.128	1.406
4000	1.35	0.256	2.69

NOMINAL DATA RATE (1)(SPS)	Global Chopper OFF		Global Chopper ON
	FIRST DATA FOR CONTINUOUS CONVERSION MODE OR SINGLE-SHOT CONVERSION MODE (2) (ms) (3)	SECOND AND SUBSEQUENT CONVERSIONS FOR CONTINUOUS CONVERSION MODE (ms) (3)	FIRST or SECOND DATA FOR CONTINUOUS CONVERSION MODE OR SINGLE-SHOT CONVERSION MODE(2) (ms)(3)
2000	2.63	0.512	5.25
1000	5.19	1.024	10.37
800	6.47	1.28	12.93
400	7.75	2.56	15.49
200	15.43	5.12	30.85
100	30.79	10.24	61.57
60	51.238	17.056	102.466
50	61.51	20.48	123.01
20	153.67	51.2	307.33
16	184.39	61.44	368.77
10	307.27	102.4	614.53
5	614.47	204.8	1228.93
2.5	1228.87	409.6	2457.73

Note: Test Valid for the internal oscillator or an external 4.096-MHz clock. Scales proportional with f_{CLK}.

Note: Conversions start at the rising edge of the START pin or on the final clock edge for a START command.

Note: Time does not include the programmable delay set by the DELAY bits in the gain setting register.

Note: Subsequent readings in continuous conversion mode do not have the programmable delay time.

Note on Conversion Time

There is a programmable conversion delay which can be added before the conversion starts. This delay allows for additional settling time for input filtering on the analog inputs and for the antialiasing filter after the PGA. Also, overhead time is needed to convert the modulator samples into an ADC conversion result. This overhead time includes any necessary offset or gain compensation after the digital filter to get final data result.

The first conversion time when the device is in continuous conversion mode, or each conversion time in single-shot conversion mode, includes the programmable conversion delay, the modulator sampling time, and the overhead time. And the second and subsequent conversions in continuous mode are the normal data period (period corresponding to the data rate).

50-Hz and 60-Hz Line Cycle Rejection

The digital filter provides enhanced rejection of coupled noise for data rates of 60 SPS and less. Please refer to digital filter sections for frequency response. The best possible rejection ratio can be get by using an accurate ADC clock.

Global Chop Mode

Although the device has a low-drift PGA and modulator to achieve very low input voltage offset drift, a small amount of offset voltage drift sometimes is left in normal measurement. The device has a global chop option to reduce the offset voltage and its drift to very low levels.

The global chop mode can be enabled using the G_CHOP bit. When the global chop is enabled, the ADC performs two internal conversions to cancel the input offset voltage. The first conversion is taken with normal input polarity. And then the

ADC reverses the internal input polarity and do a second conversion. Finally the average of the two conversions is given out as the final result, removing the offset voltage.

In global chop mode, sequences are similar to taking consecutive single-shot conversions and swapping the input on each conversion. In continuous conversion mode with the global chop mode enabled, the first conversion result is available after the ADC takes two separate conversions with settled data, and subsequent conversions complete in half the time as the first conversion completed.

In global chop mode, if the data rate in use has 50-Hz and 60-Hz frequency response notches, the null frequencies remain unchanged.

The global chop mode also reduces the ADC noise by a factor of √2 because two conversions are averaged.

If necessary, the programmable conversion delay should be increased for settling of external components.

Excitation Current Sources (IDACs)

The device provides two matched current sources, which can be used as excitation current to resistive temperature devices (RTDs), thermistors, diodes, and other resistive sensors that require constant current biasing, to reduce system complexity. The current sources are programmable to output values between 10 μA to 2000 μA by IMAG registers.

The internal reference should be enabled for IDAC operation. And the IDAC requires voltage headroom to the positive supply to operate. This voltage headroom is the compliance voltage.

Bias Voltage Generation

The device has an internal bias voltage generator which can be set to two different levels, (AVDD + AVSS) / 2 and (AVDD + AVSS) / 12, by VB_LEVEL register, . The VBIAS can be used to bias thermocouples to within the common-mode voltage range of the PGA.

System Monitor

The device provides a set of system monitor functions, to measure the on-chip temperature, analog power supply, digital power supply, or use current sources to detect sensor malfunction.

Internal Temperature Sensor

The internal temperature sensor can be selected by input multiplexer. The temperature sensor outputs a voltage proportional to the temperature as specified in the Electrical characteristic table

If enabled, PGA gain should be set to 4 for the temperature sensor measurement to remain within the allowed absolute input voltage range of the PGA.

Power Supply Monitors

The device provides monitor functions for the analog and digital interface power supply (AVDD and IOVDD), which can be selected by SYS_MON register.

The power-supply voltages are divided by a resistor network to reduce the voltages to within the ADC input range, (AVDD – AVSS) / 4 and IOVDD/4.

Burn-Out Current Sources

The device provides Burn Out Current Source (BOCS) which can be enabled by BURNOUT_EN registers. The current can be used to detect external sensor malfunctions. Current sources can be set to 0.2 μA, 1 μA, and 10 μA.

When enabled, one BOCS sources current is routed to selected positive analog input (AIN_P) and the other BOCS sinks current from the selected negative analog input (AIN_N). If there is an open-circuit in a burned out sensor, these BOCSs pull the positive input towards AVDD and the negative input towards AVSS, resulting in a full-scale reading. A full-scale reading can also indicate that the sensor is overloaded or the reference voltage is absent. A near-zero reading can indicate a shorted sensor.

Status Register
POR Flag

After the power supplies are turned on, the ADC remains in reset until AVDD and IOVDD voltage exceed the respective power-on reset (POR) voltage thresholds. If a POR event has occurred, the FL_POR bit is set. This flag indicates that a POR event has occurred and has not been cleared. This flag is cleared with a user register write to set the bit to 0.

UVLO Flag

When supply voltage falls below Under Voltage Lock Out (UVLO) thresholds, a FL_UVLO bit is set.

$\overline{\text{RDY}}$ Flag

The $\overline{\text{RDY}}$ flag indicates that the device has started up and is ready to receive a configuration change.

PGA Output Voltage Rail Monitors

The PGA contains an integrated output-voltage monitor. If the PGA output voltage exceeds AVDD – 0.15 V or drops below AVSS + 0.15 V, a flag is set to indicate that the output has gone beyond the output range of the PGA. Each PGA output V_{OUTN} and V_{OUTP} can trigger an overvoltage or undervoltage flag. So total four flags can be set by register bits FL_P_RAILP, FL_P_RAILP, FL_N_RAILP, FL_N_RAILP.

If the PGA is bypassed, then the rail monitor is still operational and is sensing the connection at the input of the ADC.

The flags are updated (set or cleared) only at the end of a conversion cycle. And a fault is latched during a conversion cycle.

Reference Monitor

A reference detection circuit can be selected to continuously monitor the differential ADC reference inputs, for a shorted or missing reference voltage. The reference detection circuit offers two thresholds, 300 mV and the second threshold is 1/3 · (AVDD – AVSS). The flag bit will be latched after each conversion in the STATUS register if the voltage is below the threshold.

A reference voltage less than 300 mV can indicate a potential short on the reference inputs or, in case of a ratiometric RTD measurement, a broken wire between the RTD and the reference resistor.

When the reference monitor is enabled, a 10 MΩ resistor is connected between the selected REFPx and REFNx inputs. The resistor can be used to detect a floating reference input. But it lowers the input reference input impedance and can lead to gain error.

ADC_ERROR

The ADC_ERROR bit in the status register is set when an over- range or underrange occurs at the output of the ADC during the conversion process. The ADC also outputs all 0s or all 1s respectively when an underrange or overrange occurs, . This flag is reset only when the underrange or overrange is removed.

REG_ERROR

The device has REG_CHECK function to be used to monitor any change in the value of the user registers. And the REG_ERROR bit is indicated if the content of one of the internal registers has changed from the value calculated when the register integrity check was activated.

General-Purpose Inputs and Outputs (GPIOs)

The device has two general-purpose digital input/output pins (GPIO0, GPIO1) and two general-purpose digital output pins (GPO2, GPO3). As the naming suggests, the GPIO0 and GPIO1 pins can be configured as inputs or outputs, but GPO2 and GPO3 are outputs only. The GPIO and GPO pins are enabled using the bits in the GPIOCON register.

The logic levels for these pins are referenced to AVDD and AVSS;

The $\overline{\text{ERROR}}$ pin can also be used as a general-purpose output by setting the ERR_EN bits in the GPIOCON register. The $\overline{\text{ERROR}}$ pin has an active pull-up, and the logic level for the pin is referenced to IOVDD and DGND.

Low-Side Power Switch

The device provides a low-side power switch between REFN0 and AVSS-SW by PDSW bit. The switch can be used to reduce system power consumption in resistive bridge sensor applications by powering down the bridge circuit between conversions.

Cyclic Redundancy Check (CRC)

The device has a checksum mode that can be used to improve interface robustness. The checksum mode ensures that only valid data is written to a register and data read is validated.

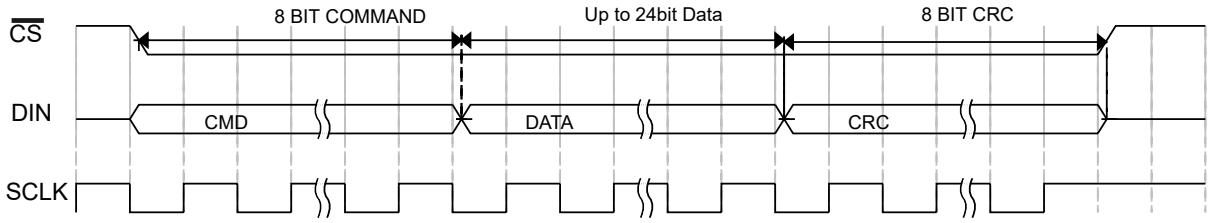
If an error occurs during a register write, the CRC_ERROR bit is set in the status register. And to ensure that the register write was successful, it is important to read back the register and verify the checksum.

During a write operation, the checksum is calculated using the 8-bit command word and the 8- to 24-bit data, and the following polynomial is always used for CRC checksum calculations:

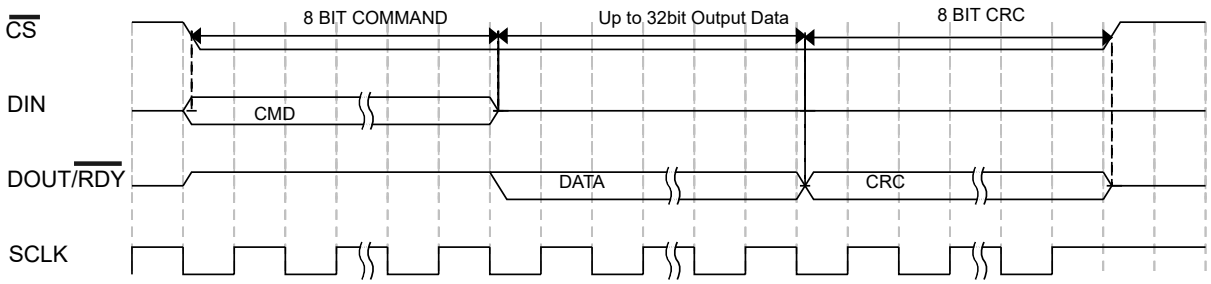
$$x^8 + x^2 + x + 1 \quad (6)$$

During read operations, the checksum is calculated using the command word and the 8- to 32-bit data output. User can select between above polynomial and a similar XOR function by CRC_EN bits. The XOR function requires less time for host microcontroller to process than the polynomial-based checksum.

The 8bit checksum is appended to the end of each read and write transaction. Following shows SPI write and read transactions, respectively.



SPI Write with CRC



SPI Read with CRC

Calibration

The device allows the user to read and write the calibration coefficients of the device for gain and offset. A read or write of the offset and gain registers can be performed at any time except during an internal or self calibration.

And the user can also trigger calibration mode for automotive gain and offset calibration, please refer to calibration mode section for detail.

Offset Calibration

The offset (zero-scale) registers are 24-bit registers that can be used to compensate for any offset error in the ADC or in the system. There are 4 offset registers, which are assigned to corresponding setup.

Gain Calibration

The gain (full-scale) registers are 24-bit registers that can be used to compensate for any gain error in the ADC or in the system. There are 4 gain registers, which are assigned to corresponding setup.

Configuration Overview

After power on-or reset, the default configuration is as follows:

- Channel configuration. CH0 is enabled, AIN0 is selected as the positive input, and AIN1 is selected as the negative input. Setup 0 is selected.
- Setup configuration. The input buffers are disabled, and the external reference is selected.
- ADC mode. Continuous conversion mode, the internal oscillator, and single cycle settling are enabled.
- Interface mode. CRC is disabled, and data + status output is disabled.

ADC Setups

The device has four independent setups. Each setup consists of the following four registers:

- Setup configuration register
- Filter configuration register
- Offset register
- Gain register

Each setup is a group of these registers, and the setup is selectable from the channel registers. This allows each channel to be assigned to one of 4 separate setups.

The motivation to have 4 setups is that user may need different speed/noise/offset/gain requirement on particular inputs versus other inputs. So the device provides flexibility for the configuration of each channel.

Device Functional Modes

The device operates in several different modes: Power Down Mode, Standby Mode, Single conversion Mode, Continous Convertion Mode and Calibration Mode.

Power Down Mode

All blocks are powered down in Power down mode. All registers lose their contents, and the GPIO outputs are placed in tristate. The ADC must be placed into standby mode at first, to prevent accidental entry to power-down mode.

Exiting power-down mode requires 64 SCLKs with $\overline{CS}$ = 0 and DIN = 1, that is, a serial interface reset. A 1ms delay is recommended before issuing subsequent serial interface command to allow internal circuit power up.

Standby Mode

In standby mode, most blocks are powered down, and the registers still maintain their contents. The internal reference, internal oscillator remains active, if they are selected or enabled be corresponding registers.

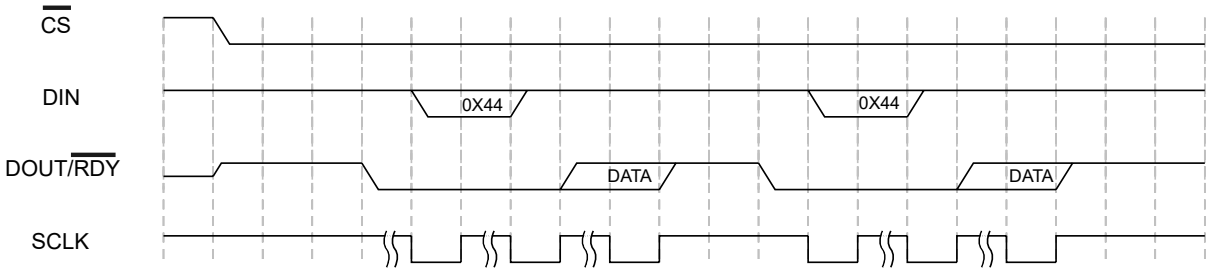
Continuous Conversion Mode

Continuous conversion is the default mode after power up. In this mode, the device converts continuously, and the $\overline{RDY}$ bit in the status register goes low each time when a conversion is complete. If CS is low, the DOUT/RDY line also goes low when a conversion is complete. And DOUT/RDY goes high when the data is read from the data register. To read a conversion, the user writes to the communications register, indicating that the next operation is a read. The user can read this register additional times if needed. However, the user must ensure that the data register is not being accessed at the completion of the next conversion.

When several channels are enabled, the ADC automatically sequences through each enabled channel from lowest enabled channel to highest, performing one conversion on each channel. When all channels are converted, the sequence starts again with the first channel.

The data register is updated as soon as latest conversion result is available. The DOUT/RDY pin pulses low each time a conversion is available. The user must read the conversion result before the ADC finishs conversion of the next channel; otherwise, the conversion result is lost.

If the DATA_STAT bit in the interface mode register is set to 1, the contents of the status register along with the conversion data, are output each time the data register is read. The status register indicates the channel to which the conversion corresponds.



Continuous Conversion Mode

Continous Read Mode

The device also provides a continuous read mode, in which it is not required to written the communications register before the ADC data is read. To enable continuous read mode, set the CONTREAD bit in the interface mode register.

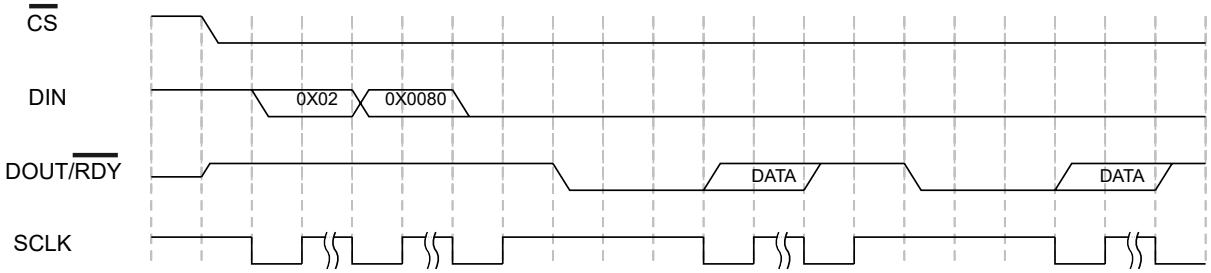
In this mode, the required number of SCLKs should be applied after DOUT/$\overline{RDY}$

goes low to read conversion result, and then DOUT/RDY returns high until the next conversion is available. In this mode, the data can be read only once.

If multiple ADC channels are enabled, each channel is output in turn, with the status bits being appended to the data if the DATA_STAT bit is set. The status register indicates the channel to which the conversion correspond

Hold DIN low in continuous read mode until an instruction is to be written to the device.

To exit continuous read mode, issue a dummy read of the ADC data register command (0x44) while $\overline{RDY}$ is low. The other method is to apply a software reset, that is 64 SCLKs with CS = 0 and DIN = 1. This resets the ADC and all register contents.



Continuous Read Mode

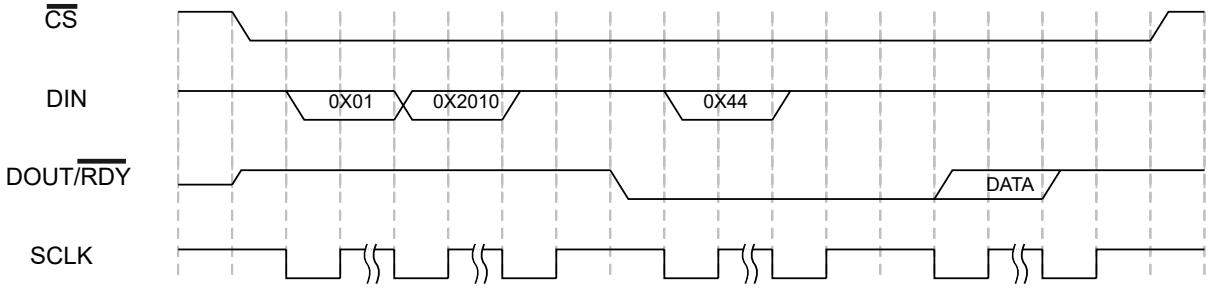
Single Conversion Mode

The device provides a single conversion mode, in which it performs a single conversion and then enter standby mode after complete. DOUT/$\overline{RDY}$ goes low to indicate the completion of a conversion. After the data-word is read from the data register, DOUT/$\overline{RDY}$ goes high. The data register can be read several times if needed, even when DOUT/$\overline{RDY}$ is high.

If several channels are enabled, the ADC automatically sequences through the enabled channels and performs a conversion on each channel. After the conversions are done, it returns to standby mode.

When a conversion is started, DOUT/$\overline{RDY}$ goes high , and goes low as soon as the conversion data is available. Then the ADC selects the next channel and begins a conversion. The user must read the present conversion while the next conversion is being performed.

If the DATA_STAT bit in the interface mode register is set to 1, the contents of the status register are output each time the data register is read along with the conversion data.



Single Conversion Mode

Calibration Mode

The device provides three calibration modes which can be used to eliminate the offset and gain errors automatically:

- Internal zero-scale calibration mode
- System zero-scale calibration mode
- System full-scale calibration mode

Only one channel can be active during calibration. To start a calibration, write the relative value to the MODE bits. When the calibration initiates, the DOUT/$\overline{RDY}$ pin and the $\overline{RDY}$ bit in the status register go high. After the calibration is complete, the contents of the corresponding offset or gain register are updated, and the $\overline{RDY}$ bit in the status register is set, the DOUT/$\overline{RDY}$ pin returns low (if CS is low). Then for the following conversions, the ADC conversion result is scaled using the calibration registers at first and then written to the data register.

During an internal offset calibration, the selected positive analog input pin is disconnected, and both modulator inputs are connected internally to the selected negative analog input pin.

System calibrations expect the system zero-scale (offset) and system full-scale (gain) voltages to be applied to the ADC pins before initiating the calibration modes. As a result, errors external to the ADC can be removed on system level.

If required, the offset calibration must always be performed before a full-scale calibration.

A calibration process is just like an ADC conversion. All calibrations require a time that is equal to the settling time of the selected filter and the output data rate to be completed.

The calibration registers can be read or written with user's own calibration coefficients at any time except during an internalor self calibration.

The following equations show the calibration calculations. In unipolar mode, the ideal relationship is as follows:

Data = [0.75*VIN]/VREF*2^23 - (Offset - 0X800000)] * (Gain/0X400000)*2 (7)

In bipolar mode, the ideal relationship is as follows:

Data = [0.75*VIN]/VREF*2^23 - (Offset - 0X800000)] * (Gain/0X400000)*2 + 0X800000 (8)

Serial Interface

The TPC6240 supports an SPI-compatible bus.

SPI Interface

In SPI mode, the device is controlled through a 3-wire or 4-wire serial interface. The interface operates in SPI Mode 3 and can be operated with CS tied low. In SPI Mode 3, SCLK idles high, the falling edge of SCLK is the drive edge, and the rising

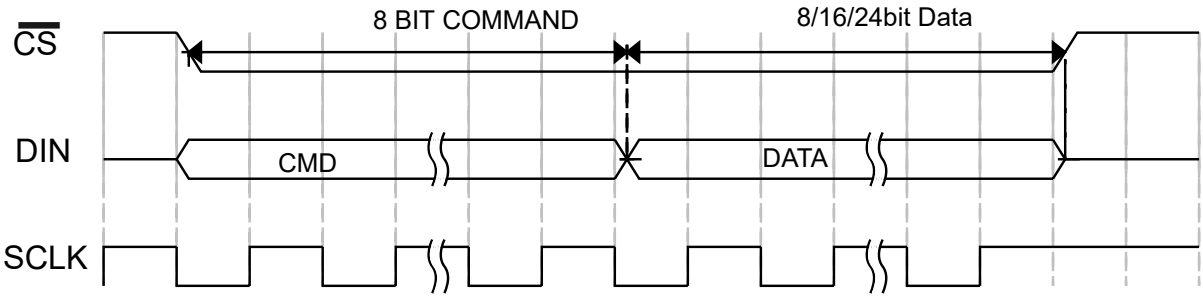
edge of SCLK is the sample edge. This means that data is clocked out on the falling/drive edge and data is clocked in on the rising/sample edge

Register Map Accessing

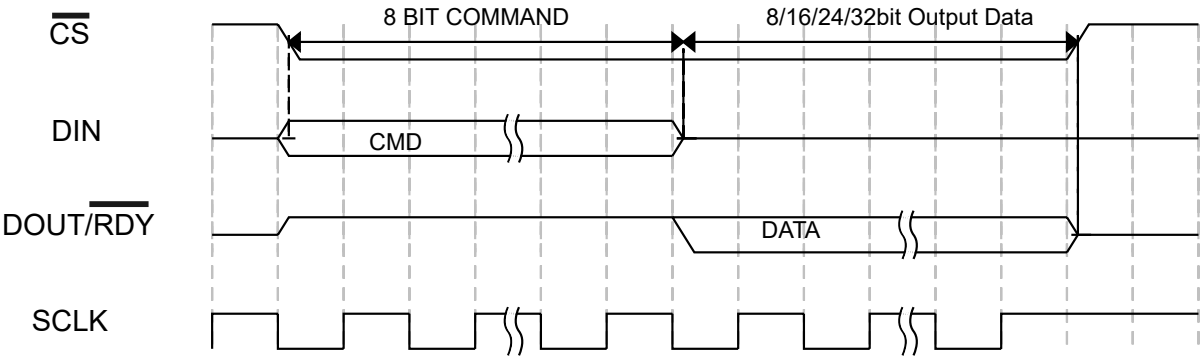
On power-up or after a reset, the digital interface default state expects a write to the communications register; therefore, all communication begins with writing to the communications register.

The data written to the communications register determines which register is being accessed and if the next operation is a read or write.

The writing and reading operations to a register are shown below:



Register Write



Register Read

Register Table

Table 20.

Reg	Name	Bits	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	Reset	RW
Reg	Name	Bits	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Reset	RW
Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	COMMS	[7:0]	WEN	R/W	RA						0x00	W
0x00	STATUS	[7:0]	RDY	ADC_ERROR	CRC_ERROR	REG_ERROR	CHANNEL				0x00	R
0x01	ADCMODE	[15:8]	REF_EN	FL_RAIL_EN	SING_CYC	RESERVED		DELAY			0x2020	RW
		[7:0]	RESERVED	MODE			CLOCKSEL		RESERVED	SOFTRST		
0x02	IFMODE	[15:8]	RESERVED			ALT_SYNC	RESERVED			DOUT_RESET	0x0000	RW
		[7:0]	CONTREAD	DATA_STAT	REG_CHECK	RESERVED	CRC_EN		RESERVED	WL16		
0x03	REGCHECK	[23:16]	REGISTER_CHECK[23:16]								0x000000	R
		[15:8]	REGISTER_CHECK[15:8]									
		[7:0]	REGISTER_CHECK[7:0]									
0x04	DATA	[23:0]	DATA[23:0]								0x000000	R
0x06	GPIOCON	[15:8]	RESERVED	PDSW	OP_EN2_3	RESERVED	SYNC_EN	ERR_EN		ERR_DAT	0x0800	RW
		[7:0]	GP_DATA3	GP_DATA2	IP_EN1	IP_EN0	OP_EN1	OP_EN0	GP_DATA1	GP_DATA0		
0x07	ID	[15:8]	ID[15:8]								0x6240	R
		[7:0]	ID[7:0]									
0x08	DIE ID		DIE ID [31:24]								0x00000000	
		[15:0]	DIE ID [23:16]									R
0x09			DIE ID[15:8]									
		[15:0]	DIE ID[7:0]									R
0x10	CH0	[15:8]	CH_EN0	SETUP_SEL0[1:0]		RESERVED			AINPOS0[4:3]		0x8001	RW
		[7:0]	AINPOS0[2:0]			AINNEG0						
0x11	CH1	[15:8]	CH_EN1	SETUP_SEL1[1:0]		RESERVED			AINPOS1[4:3]		0x0001	RW
		[7:0]	AINPOS1[2:0]			AINNEG1						

Reg	Name	Bits	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	Reset	RW
Reg	Name	Bits	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Reset	RW
Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x12	CH2	[15:8]	CH_EN 2	SETUP_SEL2[1:0]		RESERVED			AINPOS2[4:3]		0x0001	RW
		[7:0]	AINPOS2[2:0]			AINNEG2						
0x13	CH3	[15:8]	CH_EN 3	SETUP_SEL3[1:0]		RESERVED			AINPOS3[4:3]		0x0001	RW
		[7:0]	AINPOS3[2:0]			AINNEG3						
0x14	CH4	[15:8]	CH_EN 4	SETUP_SEL4[1:0]		RESERVED			AINPOS4[4:3]		0x0001	RW
		[7:0]	AINPOS4[2:0]			AINNEG4						
0x15	CH5	[15:8]	CH_EN 5	SETUP_SEL5[1:0]		RESERVED			AINPOS5[4:3]		0x0001	RW
		[7:0]	AINPOS5[2:0]			AINNEG5						
0x16	CH6	[15:8]	CH_EN 6	SETUP_SEL6[1:0]		RESERVED			AINPOS6[4:3]		0x0001	RW
		[7:0]	AINPOS6[2:0]			AINNEG6						
0x17	CH7	[15:8]	CH_EN 7	SETUP_SEL7[1:0]		RESERVED			AINPOS7[4:3]		0x0001	RW
		[7:0]	AINPOS7[2:0]			AINNEG7						
0x18	CH8	[15:8]	CH_EN 8	SETUP_SEL8[1:0]		RESERVED			AINPOS8[4:3]		0x0001	RW
		[7:0]	AINPOS8[2:0]			AINNEG8						
0x19	CH9	[15:8]	CH_EN 9	SETUP_SEL9[1:0]		RESERVED			AINPOS9[4:3]		0x0001	RW
		[7:0]	AINPOS9[2:0]			AINNEG9						
0x1A	CH10	[15:8]	CH_EN 10	SETUP_SEL10[1:0]		RESERVED			AINPOS10[4:3]		0x0001	RW
		[7:0]	AINPOS10[2:0]			AINNEG10						
0x1B	CH11	[15:8]	CH_EN 11	SETUP_SEL11[1:0]		RESERVED			AINPOS11[4:3]		0x0001	RW
		[7:0]	AINPOS11[2:0]			AINNEG11						
0x1C	CH12	[15:8]	CH_EN 12	SETUP_SEL12[1:0]		RESERVED			AINPOS12[4:3]		0x0001	RW
		[7:0]	AINPOS12[2:0]			AINNEG12						
0x1D	CH13	[15:8]	CH_EN 13	SETUP_SEL13[1:0]		RESERVED			AINPOS13[4:3]		0x0001	RW
		[7:0]	AINPOS13[2:0]			AINNEG13						
0x1E	CH14	[15:8]	CH_EN 14	SETUP_SEL14[1:0]		RESERVED			AINPOS14[4:3]		0x0001	RW

Reg	Name	Bits	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	Reset	RW
Reg	Name	Bits	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Reset	RW
Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[7:0]	AINPOS14[2:0]			AINNEG14						
0x1F	CH15	[15:8]	CH_EN15	SETUP_SEL15[1:0]		RESERVED			AINPOS15[4:3]		0x0001	RW
		[7:0]	AINPOS15[2:0]			AINNEG15						
0x20	SETUPCON0	[15:8]	RESERVED			BI_UNIPOLAR0	REF_BUF0[1:0]		AIN_PGA0[1:0]		0x1000	RW
		[7:0]	RESERVED		REF_SEL0		RESERVED		BURNOUT_EN0[1:0]			
0x21	SETUPCON1	[15:8]	RESERVED			BI_UNIPOLAR1	REF_BUF1[1:0]		AIN_PGA1[1:0]		0x1000	RW
		[7:0]	RESERVED		REF_SEL1		RESERVED		BURNOUT_EN1[1:0]			
0x22	SETUPCON2	[15:8]	RESERVED			BI_UNIPOLAR2	REF_BUF2[1:0]		AIN_PGA2[1:0]		0x1000	RW
		[7:0]	RESERVED		REF_SEL2		RESERVED		BURNOUT_EN2[1:0]			
0x23	SETUPCON3	[15:8]	RESERVED			BI_UNIPOLAR3	REF_BUF3[1:0]		AIN_PGA3[1:0]		0x1000	RW
		[7:0]	RESERVED		REF_SEL3		RESERVED		BURNOUT_EN3[1:0]			
0x24	FILTCON0	[15:8]	G_CHOP0	FILTER0	DR0[3:0]				ENNOTCH0	RESERVED	0x5000	RW
		[7:0]	RESERVED									RW
0x25	FILTCON1	[15:8]	G_CHOP1	FILTER1	DR1[3:0]				ENNOTCH1	RESERVED	0x5000	RW
		[7:0]	RESERVED									RW
0x26	FILTCON2	[15:8]	G_CHOP2	FILTER2	DR2[3:0]				ENNOTCH2	RESERVED	0x5000	RW
		[7:0]	RESERVED									RW
0x27	FILTCON3	[15:8]	G_CHOP3	FILTER3	DR3[3:0]				ENNOTCH3	RESERVED	0x5000	RW
		[7:0]	RESERVED									RW
0x28	OFFSET0	[23:0]	OFFSET0[23:0]								0x800000	RW

Reg	Name	Bits	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	Reset	RW
Reg	Name	Bits	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Reset	RW
Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x29	OFFSET1	[23:0]	OFFSET1[23:0]								0x800000	RW
0x2A	OFFSET2	[23:0]	OFFSET2[23:0]								0x800000	RW
0x2B	OFFSET3	[23:0]	OFFSET3[23:0]								0x800000	RW
0x2C	GAIN0	[23:0]	GAIN0[23:0]								0x400000	RW
0x2D	GAIN1	[23:0]	GAIN1[23:0]								0x400000	RW
0x2E	GAIN2	[23:0]	GAIN2[23:0]								0x400000	RW
0x2F	GAIN3	[23:0]	GAIN3[23:0]								0x400000	RW
0x30	CONTL1	[15:8]	PGAGAIN[2:0]			FL_REF_EN[1:0]		TS_EN	SYS_MON[1:0]		0x0000	RW
		[7:0]	VB_LEVEL	VB_AINC	VB_AIN5	VB_AIN4	VB_AIN3	VB_AIN2	VB_AIN1	VB_AIN0	0x0000	RW
0x31	CONTL2	[15:8]	IMAG[3:0]				I2MUX[3:0]				0x0000	RW
		[7:0]	I1MUX[3:0]				RESERVED				0x0000	RW
0x32	STATUS2	[15:8]					ADC_DET_OVRNG1	ADC_DET_OVRNG2	ADC_DET_OVRNG3	ADC_DET_OVRNG4	0x00	R
		[7:0]	FL_POR	FL_UVLO	FL_P_RAILP	FL_P_RAILN	FL_N_RAILP	FL_N_RAILN	FL_REF_L1	FL_REF_L0	0xC0	R

Table 21. Detailed Description

Communication Register (No address)							
Reg	**Name**	**Bits**	**Bit Name**	**Settings**	**Description**	**Reset**	**Access**
0x00	COMMS	7	WEN		This bit must be low to begin communications with the ADC.	0x0	W
		6	R/W		This bit determines if the command is a read or write operation.	0x0	W
				0	Write command		
				1	Read command		
		[5:0]	RA		The register address bits determine which register is to be	0x00	W

					read from or written to as part of the current communication.		
				000000	Status register		
				000001	ADC mode register		
				000010	Interface mode register		
				000011	Register checksum register		
				000100	Data register		
				000110	GPIO configuration register		
				000111	ID register		
				010000	Channel 0 register		
				010001	Channel 1 register		
				010010	Channel 2 register		
				010011	Channel 3 register		
				010100	Channel 4 register		
				010101	Channel 5 register		
				010110	Channel 6 register		
				010111	Channel 7 register		
				011000	Channel 8 register		
				011001	Channel 9 register		
				011010	Channel 10 register		
				011011	Channel 11 register		
				011100	Channel 12 register		
				011101	Channel 13 register		
				011110	Channel 14 register		
				011111	Channel 15 register		
				100000	Setup Configuration 0 register		
				100001	Filter Configuration 0 register		
				100010	Offset 0 register		
				100011	Gain 0 register		
				100100	RESERVED		
				100101	RESERVED		
				100110	RESERVED		

STATUS Register (0x00)

The status register is an 8-bit register that contains ADC and serial interface status information. It can optionally be appended to the data register by setting the DATA_STAT bit in the interface mode register (Bit 6, Register 0x02).

Reg	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x00	STATUS	7	RDY		The status of RDY is output to the DOUT/RDYpin whenever CS is low and a register is not being	0x0	R

					read. This bit goes low when the ADC has written a new result to the data register. In ADC calibration modes, this bit goes low when the ADC has written the calibration result. RDY is brought high automatically by a read of the data register.		
				0	Awaiting new data result		
				1	New data result available		
		6	ADC_ERROR		This bit, by default, indicates if an ADC over range or under range has occurred. The ADC result is clamped to ± full scale if an over range or under range occurs. This bit is updated when the ADC result is written and is cleared by removing the over range or under range condition on the analog inputs.	0x0	R
				0	No error		
				1	Error		
		5	CRC_ERROR		This bit indicates if a CRC error has occurred during a register write. For register reads, the host microcontroller determines if a CRC error has occurred. This bit is cleared by a read of this register.	0x0	R
				0	No error		
				1	CRC error		
		4	REG_ERROR		This bit indicates if the content of one of the internal registers has changed from the value calculated when the register integrity check was activated. The check is activated by setting the REG_CHECK bit in the interface mode register. This bit is cleared by clearing the REG_CHECK bit.	0x0	R
				0	No error		
				1	Error		
		[3:0]	CHANNEL		These bits indicate which channel was active for the	0x0	R

					ADC conversion whose result is currently in the data register. This may be different from the channel currently being converted. The bits are a direct mapping from the Channel x registers; therefore, Channel 0 results in 0x0 and Channel 15 results in 0x1F.		
				0	Channel 0		
				1	Channel 1		
				10	Channel 2		
				11	Channel 3		
				100	Channel 4		
				101	Channel 5		
				110	Channel 6		
				111	Channel 7		
				1000	Channel 8		
				1001	Channel 9		
				1010	Channel 10		
				1011	Channel 11		
				1100	Channel 12		
				1101	Channel 13		
				1110	Channel 14		
				1111	Channel 15		

ADC MODE Register (0x01)

The ADC mode register controls the operating mode of the ADC and the master clock selection. A write to the ADC mode register resets the filter and the RDY bits and starts a new conversion or calibration.

Reg	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x01	ADCMODE	15	REF_EN		Enables internal reference and outputs a buffered 2.5 V to the REFOUT pin.	0x0	RW
				0	Disabled		
				1	Enabled		
		14	FL_RAIL_EN		Enable PGA rail detector:	0x0	RW
				0	Disabled		
				1	Enabled		
		13	SING_CYC		This bit can be used when only a single channel is active to set the ADC to output only at the settled filter data rate.	0x1	RW

				0	Disabled		
				1	Enabled		
		[12:11]		RESERVED	These bits are reserved. Set to 0.	0x0	R
		[10:8]	DELAY		These bits allow a programmable delay to be added after a channel switch to allow settling of external circuitry before the ADC starts processing its input.	0x0	RW
				000	14*Tmod		
				001	25*Tmod		
				010	64*Tmod		
				011	256*Tmod		
				100	1024*Tmod		
				101	2048*Tmod		
				110	4096*Tmod		
				111	1*Tmod		
		7	RESERVED		When set to 1, the frequency of modulator and thus the output ODR is doubled.	0x0	RW
		[6:4]	MODE		These bits control the operating mode of the ADC. Details can be found in the Operating Modes section.	0x010	RW
				000	Continuous conversion mode		
				001	Single conversion mode		
				010	Standby mode		
				011	RESERVED.		
				100	Internal offset calibration		
				110	System offset calibration		
				111	System gain calibration		
		[3:2]	CLOCKSEL		This bit is used to select the ADC clock source. Selecting the internal	0x00	RW
					illator also enables the internal oscillator.		
				0	Internal oscillator		
				1	Internal oscillator output on XTAL2/CLKIO pin		

				10	External clock input on XTAL2/ CLKIO pin		
				11	RESERVED (internal oscillator)		
		[1]	RESERVED		These bits are reserved. Set to 0.	0x0	R
		[0]	SOFTRST		self clear after reset	0x0	W

Interface Mode Register(0x02)

The interface mode register configures various serial interface options.

Reg	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x02	IFMODE	[15:13]	RESERVED		These bits are reserved. Set to 0.	0x0	R
		12	ALT_SYNC		This bit enables a different behavior of the SYNC pin to allow the use of SYNC as a control for conversions when cycling channels. (For details, see the description of the SYNC_EN bit in the GPIO Configuration Register.)	0x0	RW
				0	Disabled		
				1	Enabled		
		[11:9]	RESERVED		These bits are reserved. Set to 0.	0x0	R
		8	DOUT_RESET		This bit prevents the DOUT/RDY pin from switching from outputting DOUT to outputting RDY soon after the last rising edge of SCLK during a read operation. Instead, the DOUT/RDY pin continues to output the LSB of the data until CS goes high, providing longer hold times for the SPI master to sample the LSB of the data. When this bit is set, CS must not be tied low.	0x0	RW
				0	Disabled		
				1	Enabled		
		7	CONTREAD		This bit enables continuous read of the ADC data register. To use continuous read, configure the ADC in continuous conversion	0x0	RW

					mode. For more details, see the Operating Modes section.		
				0	Disabled		
				1	Enabled		
		6	DATA_STAT		This bit enables the status register to be appended to the data register when read so that channel and status information is transmitted with the data. This is the only way to ensure that the channel bits read from the status register correspond to the data in the data register.	0x0	RW
				0	Disabled		
				1	Enabled		
		5	REG_CHECK		This bit enables a register integrity checker that can be used to monitor any change in the value of the user registers. To use this feature, configure all other registers as desired, with this bit cleared. Then write to this register to set the REG_CHECK bit to 1. If the contents of any of the registers change, the REG_ERROR bit is set in the status register. To clear the error, set the REG_CHECK bit to 0. Neither the interface mode register nor the ADC data or status register is included in the registers that are checked. If a register must have a new value written, clear this bit first; otherwise, an error is flagged when the new register contents are written.	0x0	RW
				0	Disabled		
				1	Enabled		
		4	RESERVED		This bit is reserved. Set to 0.	0x0	R
		[3:2]	CRC_EN		Enables CRC protection of register reads/writes. CRC increases the number of bytes in a serial interface transfer by one.	0x00	RW

					See the CRC Calculation section for more details.		
				0	Disabled.		
				1	XOR checksum enabled for register read transactions. Register writes still use CRC with these bits set.		
				10	CRC checksum enabled for read and write transactions.		
				11	Reserved		
		1	RESERVED		This bit is reserved. Set to 0.	0x0	R
		0	WL16		Changes the ADC data register to 16 bits. The ADC is not reset by a write to the interface mode register; therefore, the ADC result is not rounded to the correct word length immediately after writing to these bits. The first new ADC result is correct.	0x0	RW
				0	24-bit data		
				1	16-bit data		

Register Checksum Register (0x03)

The register check register is a 24-bit checksum calculated by XOR'ing the contents of the user registers and some non-accessible registers (Trim bits). The REG_CHECK bit in the interface mode register must be set for this to operate; otherwise, the register reads 0.

Reg	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x03	REGCHECK	[23:0]	REGISTER_CHECK		This register contains the 24-bit checksum of user registers when the REG_CHECK bit is set in the interface mode register.	0x000000	R

ADC Data Register (0x04)

The data register contains the ADC conversion result. The encoding is offset binary; however, it can be changed to unipolar by the BI_UNIPOLAR bit in the setup configuration register. Reading the data register brings the RDY bit and pin high if they are low. The ADC result can be read multiple times; however, because RDY has been brought high, it is not possible to know if another ADC result is imminent. The ADC does not write a new result into the data register if the register is currently being read.

Reg	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x04	DATA	[23:0]	DATA		This register contains the ADC conversion result. If the DATA_STAT bit is set in the interface mode register, the status register is appended to this register when read, making	0x000000	R

					this a 32-bit register. If WL16 is set in the interface mode register, this register is set to a length of 16 bits.		

GPIO Configure Register (0x06)

The GPIO configuration register controls the general-purpose I/O pins of the ADC.

Reg	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x06	GPIOCON	15	RESERVED		This bit is reserved. Set to 0.	0x0	R
		14	PDSW		This bit enables/disables the power-down switch function. Setting the bit allows the pin to sink current. This function can be used for bridge sensor applications where the switch controls the power-up/power-down of the bridge.	0x0	RW
		13	OP_EN2_3		This bit enables the GPO2 and GPO3 pins. Outputs are referenced between AVDD1 and AVSS.	0x0	RW
		12	RESERVED		RESERVED	0x0	RW
		11	SYNC_EN		This bit enables the SYNC pin as a sync input. When set low, the SYNC pin holds the ADC and filter in reset until SYNC goes high. An alternative operation of the SYNC pin is available when the ALT_SYNC bit in the interface mode register is set. This mode works only when multiple channels are enabled. In such cases, a low on the SYNC pin does not immediately reset the filter/ modulator. Instead, if the SYNC pin is low when the channel is due to be switched, the modulator and filter are prevented from starting a new conversion. Bringing SYNC high begins the next conversion. This alternative sync mode allows SYNC to be used while cycling through channels.	0x1	RW
				0	Disabled		

				1	Enabled		
		[10:9]	ERR_EN		These bits enable the ERROR pin as an error input/output.	0x0	RW
				0	Disabled		
				1	ERROR is an error input. The (inverted) readback state is OR'ed with other error sources and is available in the ADC_ERROR bit in the status register. The ERROR pin state can also be read from the ERR_DAT bit in this register.		
				10	ERROR is an open-drain error output. The status register error bits are OR'ed, inverted, and mapped to the ERROR pin. ERROR pins of multiple devices can be wired together to a common pull-up resistor so that an error on any device can be observed.		
				11	ERROR is a general-purpose output. The status of the pin is controlled by the ERR_DAT bit in this register. This is referenced between IOVDD and DGND, as opposed to the AVDD1 and AVSS levels used by the general- purpose I/O pins. It has an active pull-up in this case.		
		8	ERR_DAT		This bit determines the logic level at the ERROR pin if the pin is enabled as a general-purpose output. It reflects the readback status of the pin if the pin is enabled as an input.	0x0	RW
		7	GP_DATA3		This bit is the write data for GPO3.	0x0	W
		6	GP_DATA2		This bit is the write data for GPO2.	0x0	W
		5	IP_EN1		This bit turns GPIO1 into an input. Input should equal AVDD1 or AVSS.	0x0	RW

				0	Disabled		
				1	Enabled		
		4	IP_EN0		This bit turns GPIO0 into an input. Input should equal AVDD1 or AVSS.	0x0	RW
				0	Disabled		
				1	Enabled		
		3	OP_EN1		This bit turns GPIO1 into an output. Outputs are referenced between AVDD1 and AVSS.	0x0	RW
				0	Disabled		
				1	Enabled		
		2	OP_EN0		This bit turns GPIO0 into an output. Outputs are referenced between AVDD1 and AVSS.	0x0	RW
				0	Disabled		
				1	Enabled		
		1	GP_DATA1		This bit is the readback or write data for GPIO1.	0x0	RW
		0	GP_DATA0		This bit is the readback or write data for GPIO0.	0x0	RW

ID Register (0x07)

The ID register returns a 16-bit ID. For the TPC624, this is 0x6240.

Reg	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x07	ID	[15:0]	ID		The ID register returns a 16-bit ID code that is specific to the ADC.	0x6240	R

DIEID1 Register (0x08)

The ID register returns a 16-bit ID.

Reg	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x08	ID1	[15:0]	ID1		The ID register returns a 16-bit DIE ID code.		R

DIEID2 Register (0x09)

The ID register returns a 16-bit ID.

Reg	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x09	ID2	[15:0]	ID2		The ID register returns a 16-bit DIE ID code.		R

CH0 Register (0x10)

The channel registers are 16-bit registers that are used to select which channels are currently active, which inputs are selected for each channel.

Reg	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x10	CH0	15	CH_EN0		This bit enables Channel 0. If more than one channel is enabled, the ADC automatically sequences between them.	0x1	RW
				0	Disabled		
				1	Enabled (default)		
		[14:13]	SETUP_SEL0[1:0]		SETUP_SEL0	0x00	R
				00	SETUPCON0,FILTCON0,OFFSET0,GAIN0		
				01	SETUPCON1,FILTCON1,OFFSET1,GAIN1		
				10	SETUPCON2,FILTCON2,OFFSET2,GAIN2		
				11	SETUPCON3,FILTCON3,OFFSET3,GAIN3		
		[12:10]	RESERVED		These bits are reserved. Set to 0.	0x000	R
		[9:5]	AINPOS0		These bits select which of the analog inputs is connected to the positive input of the ADC for this channel. TEMP SENSOR ± is an internal temperature sensor.	0x0	RW
				0	AIN0 (default)		
				1	AIN1		
				10	AIN2		
				11	AIN3		
				100	AIN4		
				101	AIN5		
				110	AIN6		
				111	AIN7		
				1000	AIN8		
				1001	AIN9		
				1010	AIN10		
				1011	AIN11		
				1100	AIN12		
				1101	AIN13		
				1110	AIN14		

				1111	AIN15		
				10000	AIN16		
				10001	TEMP SENSOR +		
				10010	TEMP SENSOR −		
				10101	REF+		
				10110	REF−		
				Others	Disconnect		
		[4:0]	AINNEG0 (N)		These bits select which of the analog inputs is connected to the negative input of the ADC for this channel.	0x1	RW
				0	AIN0		
				1	AIN1 (default)		
				10	AIN2		
				11	AIN3		
				100	AIN4		
				101	AIN5		
				110	AIN6		
				111	AIN7		
				1000	AIN8		
				1001	AIN9		
				1010	AIN10		
				1011	AIN11		
				1100	AIN12		
				1101	AIN13		
				1110	AIN14		
				1111	AIN15		
				10000	AIN16		
				10001	TEMP SENSOR +		
				10010	TEMP SENSOR −		
				10101	REF+		
				10110	REF−		
				Others	Disconnect		

CH1~15 Register (0x11~0x1F)

Subsequent channel registers, CH1 to CH15, use the same structure as the CH0 register. They are disabled by default (MSB = 0). The sequencer progresses through each of the enabled channels in order. The following table shows the summary of these registers, their addresses, and their reset values.

Reg	Name	Bits	Bit Name	Settings	Description	Reset	Access

0x11~0x1F	CH1~CH15	15	CH_EN1 (N)		This bit enables Channel 1(N). If more than one channel is enabled, the ADC automatically sequences between them.	0x0	RW
				0	Disabled(default)		
				1	Enabled		
		[14:13]	SETUP_SEL(N)[1:0]		SETUP_SEL(N)	0x00	R
				00	SETUPCON0,FILTCON0,OFFSET0,GAIN0		
				01	SETUPCON1,FILTCON1,OFFSET1,GAIN1		
				10	SETUPCON2,FILTCON2,OFFSET2,GAIN2		
				11	SETUPCON3,FILTCON3,OFFSET3,GAIN3		
		[12:10]	RESERVED		These bits are reserved. Set to 0.	0x000	R
		[9:5]	AINPOS1 (N)		These bits select which of the analog inputs is connected to the positive input of the ADC for this channel. TEMP SENSOR ± is an internal temperature sensor.	0x0	RW
				0	AIN0 (default)		
				1	AIN1		
				10	AIN2		
				11	AIN3		
				100	AIN4		
				101	AIN5		
				110	AIN6		
				111	AIN7		
				1000	AIN8		
				1001	AIN9		
				1010	AIN10		
				1011	AIN11		
				1100	AIN12		
				1101	AIN13		
				1110	AIN14		
				1111	AIN15		
				10000	AIN16		
				10001	TEMP SENSOR +		

				10010	TEMP SENSOR −		
				10101	REF+		
				10110	REF−		
		[4:0]	AINNEG1 (N)		These bits select which of the analog inputs is connected to the negative input of the ADC for this channel.	0x1	RW
				0	AIN0		
				1	AIN1 (default)		
				10	AIN2		
				11	AIN3		
				100	AIN4		
				101	AIN5		
				110	AIN6		
				111	AIN7		
				1000	AIN8		
				1001	AIN9		
				1010	AIN10		
				1011	AIN11		
				1100	AIN12		
				1101	AIN13		
				1110	AIN14		
				1111	AIN15		
				10000	AIN16		
				10001	TEMP SENSOR +		
				10010	TEMP SENSOR −		
				10101	REF+		
				10110	REF−		

Setup Configuration 0 (0x20)

The setup configuration registers are 16-bit registers that configure the reference selection, input buffers, burnout currents, and output coding of the ADC.

Reg	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x20	SETUPCON0	[15:13]	RESERVED		These bits are reserved. Set to 0.	0x0	R
		12	BI_UNIPOLAR 0		This bit sets the output coding of the ADC for Setup 0.	0x1	RW
				0	Unipolar coded output		
				1	Offset binary coded output		
		[11:10]	REF_BUF_0[1:0]		Reference input buffer enable. These bits turn on the buffers	0x0	RW

					of the positive and negative reference inputs. This offers a high impedance input for an external reference source and isolates it from the switch capacitor reference sampling input of the ADC. Use both reference buffers together.		
				00	Reference input buffers disabled		
				01	REFP Buf En		
				10	REFN Buf En		
				11	Reference input buffers enabled		
		[9:8]	AIN_PGA_0[1:0]		Analog input PGA enable. These bits turn on the PGAs of the positive and negative analog inputs. This offers a high impedance input to the device and isolates the sensor/signal for measurement from the switch capacitor sampling input of the ADC. Use both analog input buffers together.	0x0	RW
				00	Analog input PGAs disabled		
				01/10	Analog input PGAs disabled		
				11	Analog input PGAs enabled		
		7	RESERVED		These bits are reserved. Set to 0.	0x0	RW
		6	RESERVED		These bits are reserved. Set to 0.	0x0	R
		[5:4]	REF_SEL0		These bits allow selection of the reference source for ADC conversion on Setup 0.	0x0	RW
				00	External reference supplied to REF+ and REF− pins		
				01	External Reference 2 supplied to AIN1/REF2+ and AIN0/REF2− pins		
				10	Internal 2.5 V reference; this reference must also be enabled in the ADC mode register		
				11	Reserved. Don't write.		
		[3:2]	RESERVED		These bits are reserved. Set to 0.	0x0	R

		[1:0]	BURNOUT_EN[1:0]		[BURNOUT_ EN1, BURNOUT_ EN0] The bits enable a current source on the positive analog input selected and a current sink on the negative analog input selected. The burnout currents are useful in diagnosis of an open wire, whereby the ADC result goes to full scale. Enabling the BURNOUT currents during measurement results in an offset voltage on the ADC reading of approximately 1 µV. This means the strategy for diagnosing an open wire operates best by turning on the BURNOUT currents at intervals, before or after precision measurements.	0x0	RW
				00	OFF		
				01	Burn-out current sources enabled, 10-µA setting		
				10	Burn-out current sources enabled, 0.2-µA setting		
				11	Burn-out current sources enabled, 1-µA setting		

Setup Configuration 1~3 (0x21~23)

The setup configuration registers are 16-bit registers that configure the reference selection, input buffers, burnout currents, and output coding of the ADC.

Reg	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x21~23	SETUPCON(N) N=1~3	[15:13]	RESERVED		These bits are reserved. Set to 0.	0x0	R
		12	BI_UNIPOLAR(N)		This bit sets the output coding of the ADC for Setup N (N=1~3).	0x1	RW
				0	Unipolar coded output		
				1	Offset binary coded output		
		[11:10]	REF_BUF_(N)[1:0]		Reference input buffer enable. These bits turn on the buffers of the positive and negative reference inputs. This offers a high impedance input for an external reference source and isolates it from the switch	0x0	RW

					capacitor reference sampling input of the ADC. Use both reference buffers together.		
				00	Reference input buffers disabled		
				11	Reference input buffers enabled		
		[9:8]	AIN_PGA_(N)[1:0]		Analog input PGA enable. These bits turn on the PGAs of the positive and negative analog inputs. This offers a high impedance input to the device and isolates the sensor/signal for measurement from the switch capacitor sampling input of the ADC. Use both analog input buffers together.	0x0	RW
				00	Analog input PGAs disabled		
				01/10	Analog input PGAs disabled		
				11	Analog input PGAs enabled		
		7	RESERVED		These bits are reserved. Set to 0.	0x0	RW
		6	RESERVED		These bits are reserved. Set to 0.	0x0	R
		[5:4]	REF_SEL(N)		These bits allow selection of the reference source for ADC conversion on Setup N.	0x0	RW
				00	External reference supplied to REF+ and REF− pins		
				01	External Reference 2 supplied to AIN1/REF2+ and AIN0/REF2− pins		
				10	Internal 2.5 V reference; this reference must also be enabled in the ADC mode register		
				11	Reserved. Don't write.		
		[3:2]	RESERVED		These bits are reserved. Set to 0.	0x0	R
		[1:0]	BURNOUT_EN(N)[1:0]		[BURNOUT_ EN(N)1, BURNOUT_ EN(N)0] The bits enable a current source on the positive analog input selected and a current sink on the negative analog input selected. The burnout currents are useful in diagnosis	0x0	RW

					of an open wire, whereby the ADC result goes to full scale. Enabling the BURNOUT currents during measurement results in an offset voltage on the ADC reading of approximately 1 µV. This means the strategy for diagnosing an open wire operates best by turning on the BURNOUT currents at intervals, before or after precision measurements.		
				00	OFF		
				01	Burn-out current sources enabled, 10-µA setting		
				10	Burn-out current sources enabled, 0.2-µA setting		
				11	Burn-out current sources enabled, 1-µA setting		

Filter Configuration 0 (0x24)

The filter configuration registers are 16-bit registers that configure the ADC data rate and filter options. Writing to any of these registers resets any active ADC conversion and restarts converting at the first channel in the sequence.

Reg	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x24	FILTCON0	[15]	G_CHOP0		Global chop enable	0x0	RW
					Enables the global chop function. When enabled, the device automatically swaps the inputs and takes the average of two consecutive readings to cancel the offset voltage.		
				0	Disabled (default)		
				1	Enabled		
		[14]	FILTER0		Configures the ADC to use either the sinc5 or the low-latency filter.	0x1	RW
				0	Sinc5 filter		
				1	Low-latency filter (default)		
		[13:10]	DR0[3:0]		Configures the output data rate(1).	0x0100	RW
				0000	2.5 SPS		
				0001	5 SPS		
				0010	10 SPS		
				0011	16.6 SPS		

				0100	20 SPS (default)		
				0101	50SPS		
				0110	60 SPS		
				0111	100 SPS		
				1000	200 SPS		
				1001	400 SPS		
				1010	800 SPS		
				1011	1000 SPS		
				1100	2000 SPS		
				1101	4000 SPS		
				1110	8000 SPS		
				1111	8000 SPS		
		[9]	ENNOTCH0		Notch filter Enable for channel 0.	0x0	RW
		[8:0]	RESERVED			0x0	RW

Filter Configuration N (0x25~27)

The filter configuration registers are 16-bit registers that configure the ADC data rate and filter options. Writing to any of these registers resets any active ADC conversion and restarts converting at the first channel in the sequence.

Reg	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x25~27	FILTCON(N)	[15]	G_CHOP(N)		Global chop enable	0x0	RW
					Enables the global chop function. When enabled, the device automatically swaps the inputs and takes the average of two consecutive readings to cancel the offset voltage.		
				0	Disabled (default)		
				1	Enabled		
		[14]	FILTER(N)		Configures the ADC to use either the sinc5 or the low-latency filter.	0x1	RW
				0	Sinc5 filter		
				1	Low-latency filter (default)		
		[13:10]	DR(N)[3:0]		Configures the output data rate(1).	0x0100	RW
				0	2.5 SPS		
				1	5 SPS		
				10	10 SPS		
				11	16.6 SPS		
				100	20 SPS (default)		
				101	50SPS		

				110	60 SPS		
				111	100 SPS		
				1000	200 SPS		
				1001	400 SPS		
				1010	800 SPS		
				1011	1000 SPS		
				1100	2000 SPS		
				1101	4000 SPS		
				1110	8000 SPS		
				1111	8000 SPS		
		[9]	ENNOTCH(N)		Notch filter Enable for channel N.	0x0	RW
		[8:0]	RESERVED				RW

Offset Register 0 (0x28)

The offset (zero-scale) registers are 24-bit registers that can be used to compensate for any offset error in the ADC or in the system.

Reg	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x28	OFFSET0	[23:0]	OFFSET[23:0]		Offset calibration coefficient	0x800000	RW

Offset Register N (0x29~2B)

The offset (zero-scale) registers are 24-bit registers that can be used to compensate for any offset error in the ADC or in the system.

Reg	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x29~2B	OFFSET(N)	[23:0]	OFFSET[23:0]		Offset calibration coefficient	0x800000	RW

Gain Register 0 (0x2C)

The gain (full-scale) registers are 24-bit registers that can be used to compensate for any gain error in the ADC or in the system.

Reg	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x23	GAIN0	[23:0]	GAIN[23:0]		Gain calibration coefficient	0x400000	RW

Gain Register N (0x2D~F)

The gain (full-scale) registers are 24-bit registers that can be used to compensate for any gain error in the ADC or in the system.

Reg	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2D~F	GAIN(N)	[23:0]	GAIN[23:0]		Gain calibration coefficient	0x400000	RW

CONTL1 Register (0x30)

Reg	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x30	CONTL1	[15:13]	PGAGAIN[2:0]		Configures the PGA gain.	0x0	RW
				0	1 (default)		

				1	2		
				10	4		
				11	8		
				100	16		
				101	32		
				110	64		
				111	128		
		[12:11]	FL_REF_EN[1:0]		Enables and configures the reference monitor.	0x0	RW
				0	Disabled (default)		
				1	FL_REF_L0 monitor enabled, threshold 0.3 V		
				10	FL_REF_L0 and FL_REF_L1 monitors enabled, thresholds 0.3 V and 1/3 · (AVDD – AVSS)		
				11	FL_REF_L0 monitor and 10-MΩ pull-together enabled, threshold 0.3 V		
		[10]	TS_EN		Enable Temperature sensor	0x0	RW
		[9:8]	SYS_MON[1:0]		Enables a set of system monitor measurements using the ADC. Don’t enable ADC input when using this register.	0x0	RW
				0	000 : Disabled (default)		
				1	PGA inputs shorted to (AVDD + AVSS) / 2 and disconnected from AINx and the multiplexer; gain set by user		
				10	IOVDD / 4 measurement; gain set to 1(3)		
				11	(AVDD – AVSS) / 4 measurement; gain set to 1(3)		
		7	VB_LEVEL		Sets the VBIAS output voltage level. VBIAS is disabled when not connected to any input.	0x0	RW
				0	(AVDD + AVSS) / 2 (default)		
				1	(AVDD + AVSS) / 12		
		6	VB_AINC		Enables VBIAS on the AINCOM pin.	0x0	RW
				0	VBIAS disconnected from AINCOM (default)		
				1	VBIAS connected to AINCOM		

		5	VB_AIN5		Enables VBIAS on the AIN5 pin.	0x0	RW
				0	VBIAS disconnected from AIN5 (default)		
				1	VBIAS connected to AIN5		
		4	VB_AIN4		Enables VBIAS on the AIN4 pin.	0x0	RW
				0	VBIAS disconnected from AIN4 (default)		
				1	VBIAS connected to AIN4		
		3	VB_AIN3		Enables VBIAS on the AIN3 pin.	0x0	RW
				0	VBIAS disconnected from AIN3 (default)		
				1	VBIAS connected to AIN3		
		2	VB_AIN2		Enables VBIAS on the AIN2 pin.	0x0	RW
				0	VBIAS disconnected from AIN2 (default)		
				1	VBIAS connected to AIN2		
		1	VB_AIN1		Enables VBIAS on the AIN1 pin.	0x0	RW
				0	VBIAS disconnected from AIN1 (default)		
				1	VBIAS connected to AIN1		
		0	VB_AIN0		Enables VBIAS on the AIN0 pin.	0x0	RW
				0	VBIAS disconnected from AIN0 (default)		
				1	VBIAS connected to AIN0		

CONTL2 Register (0x31)

Reg	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x31	CONTL2	[15:12]	IMAG[3:0]		Selects the value of the excitation current sources. Sets IDAC1 and IDAC2 to the same value.	0x0	RW
				0	Off (default)		
				1	10 μA		
				10	50 μA		
				11	100 μA		
				100	250 μA		
				101	500 μA		
				110	750 μA		
				111	1000 μA		
				1000	1500 μA		
				1001	2000 μA		

				1010-1111	Off		
		[11:8]	I2MUX[3:0]		Selects the output channel for IDAC2.	0xf	RW
				0	AIN0		
				1	AIN1		
				10	AIN2		
				11	AIN3		
				100	AIN4		
				101	AIN5		
				110	AIN6		
				111	AIN7		
				1000	AIN8		
				1001	AIN9		
				1010	AIN10		
				1011	AIN11		
				1100	AIN16		
				1101-1111	Disconnected (default)		
		[7:4]	I1MUX[3:0]		Selects the output channel for IDAC1.	0xf	RW
				0	AIN0		
				1	AIN1		
				10	AIN2		
				11	AIN3		
				100	AIN4		
				101	AIN5		
				110	AIN6		
				111	AIN7		
				1000	AIN8		
				1001	AIN9		
				1010	AIN10		
				1011	AIN11		
				1100	AIN16		
				1101-1111	Disconnected (default)		
		3	RESERVED		RESERVED	0x0	
		[2:0]	RESERVED		RESERVED		

STATUS2 Register (0x32)

Reg	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x32	STATUS2	[15:12]	RESERVED		RESERVED		

		[11]	ADC_DET_OVRNG4		INT4 over-range flag: when 1 indicates over-range occurs	0	
		[10]	ADC_DET_OVRNG3		INT3 over-range flag: when 1 indicates over-range occurs	0	
		[9]	ADC_DET_OVRNG2		INT2 over-range flag: when 1 indicates over-range occurs	0	
		[8]	ADC_DET_OVRNG1		INT1 over-range flag: when 1 indicates over-range occurs	0	
		[7]	FL_POR		POR flag Indicates a power-on reset (POR) event has occurred.	1	RW
				0	Register has been cleared and no POR event has occurred.		
				1	POR event occurred and has not been cleared. Flag must be cleared by user register write (default).		
		[6]	FL_UVLO		UVLO flag Indicates a UVLO event has occurred.	1	R
				0	Indicate UVLO is released.		
				1	Indicate UVLO has occurred.		
		[5]	FL_P_RAILP		Positive PGA output at positive rail flag(1) Indicates the positive PGA output is within 150 mV of AVDD.	0	
				0	No error (default)		
				1	PGA positive output within 150 mV of AVDD		
		[4]	FL_P_RAILN		Positive PGA output at negative rail flag(1) Indicates the positive PGA output is within 150 mV of AVSS.	0	
				0	No error (default)		
				1	PGA positive output within 150 mV of AVSS		
		[3]	FL_N_RAILP		Negative PGA output at positive rail flag(1) Indicates the negative PGA output is within 150 mV of AVDD.	0	
				0	No error (default)		

				1	PGA negative output within 150 mV of AVDD		
		[2]	FL_N_RAILN		Negative PGA output at negative rail flag(1) Indicates the negative PGA output is within 150 mV of AVSS.	0	
				0	No error (default)		
				1	PGA negative output within 150 mV of AVSS		
		[1]	FL_REF_L1		Reference voltage monitor flag, level 1(2) Indicates the external reference voltage is lower than 1/3 of the analog supply voltage. Can be used to detect an open-excitation lead in a 3-wire RTD application.	0	
				0	Differential reference voltage ≥ 1/3 · (AVDD – AVSS) (default)		
				1	Differential reference voltage < 1/3 · (AVDD – AVSS)		
		[0]	FL_REF_L0		Reference voltage monitor flag, level 0(2) Indicates the external reference voltage is lower than 0.3 V. Can be used to indicate a missing or floating external reference voltage.	0	
				0	Differential reference voltage ≥ 0.3 V (default)		
				1	Differential reference voltage < 0.3 V		

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPC6240 is supplied by several voltages.

Typical Configuration flow

The suggested flow to change the ADC configuration is as following:

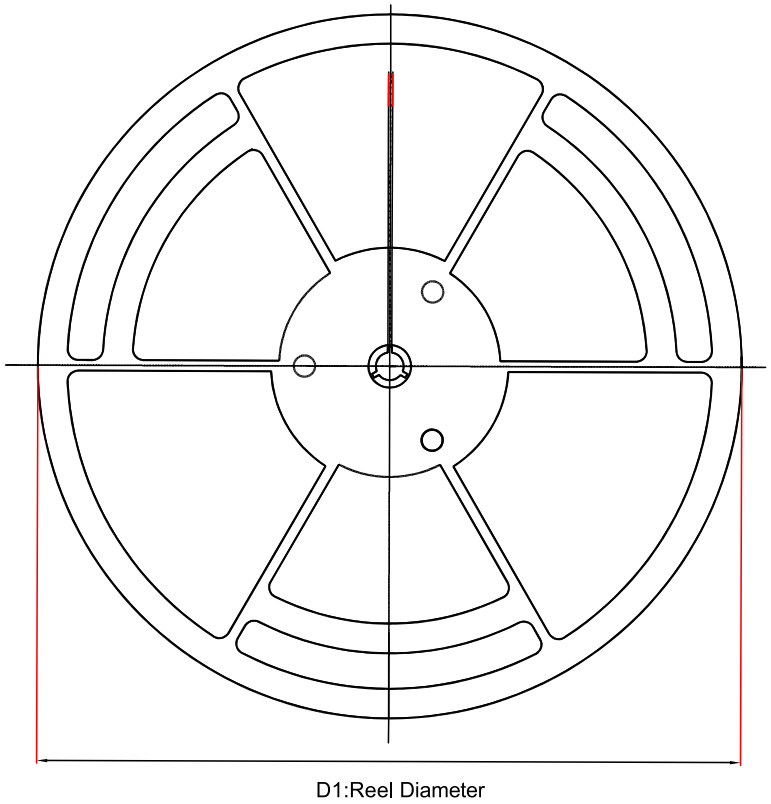
- Channel Configuration
- Setup Configuration
- ADC Mode and Interface Mode Configuration

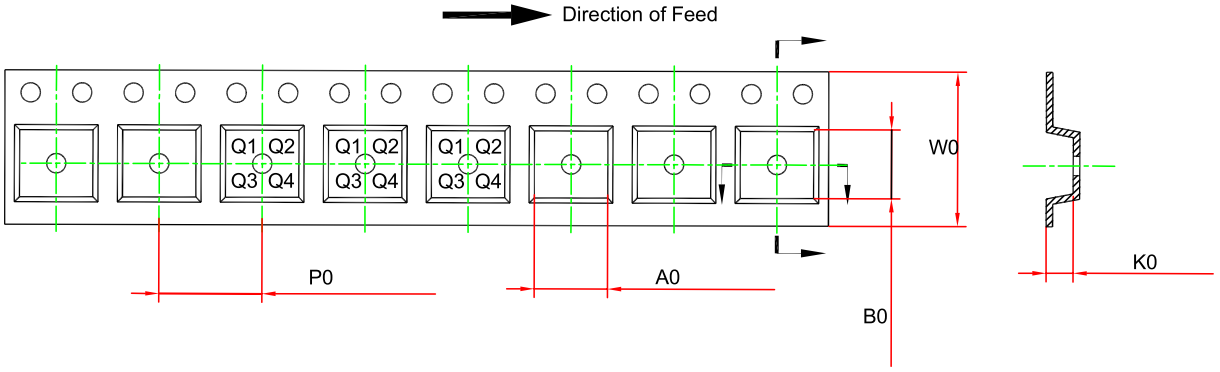
Layout

Layout Guideline

- Both input capacitors and output capacitors must be placed to the device pins as close as possible.
- It is recommended to bypass the input pin to ground with a 0.1-μF bypass capacitor.
- It is recommended to use wide and thick copper to minimize I×R drop and heat dissipation.
- Exposed pad must be connected to the PCB ground plane directly, the copper area must be as large as possible.

Tape and Reel Information



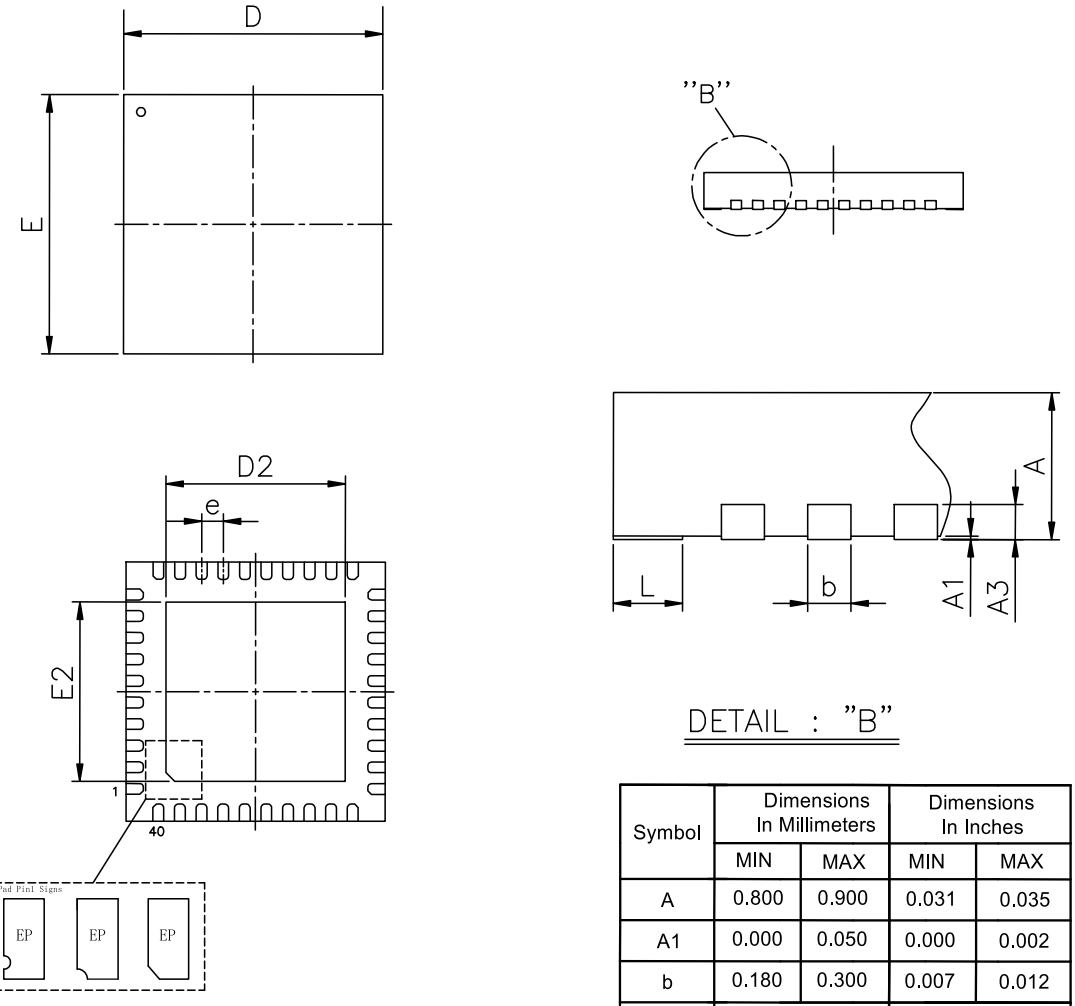


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPC6240-QFER-S	QFN6X6-40	330	21.6	6.3	6.3	1.1	12	16	Q1

Package Outline Dimensions

QFN6X6-40

Package Outline Dimensions QFE(QFN6X6-40-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.031	0.035
A1	0.000	0.050	0.000	0.002
b	0.180	0.300	0.007	0.012
A3	0.200 REF		0.008 REF	
D	5.900	6.100	0.232	0.240
E	5.900	6.100	0.232	0.240
e	0.500 BSC		0.020 BSC	
L	0.300	0.500	0.012	0.020
D2	4.000	4.300	0.157	0.169
E2	4.000	4.300	0.157	0.169

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPC6240-QFER-S	−40 to 125°C	QFN6X6-40	TPC6240	3	Tape and Reel, 3150	Green

(1) For future products, contact the 3PEAK factory for more information and sample.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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Performance Information. Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

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