I²C Interface, 24-Bit, 32 kSPS, 4-Channel Sigma-Delta ADC with Internal Reference

Features

- 24-Bit, 32 kSPS, 4-Channel ADC
- Wide Supply Range: 2.7 V to 5.5 V
- Programmable Data Rate:
  - 64 SPS to 32 kSPS
- Single-Cycle Settling
- Supporting Four Single-Ended or Two Differential Inputs
- Internal PGA
- Internal Oscillator
- Internal Low-Drift Voltage Reference
- Internal Programmable Comparator
- I²C-Compatible Interface
- Package: MSOP10
- Wide Operating Temperature Range: −40℃ to +125℃

Applications

- Current-shunt Measurements
- Voltage Measurements
- Industrial Automation
- Temperature Measurements

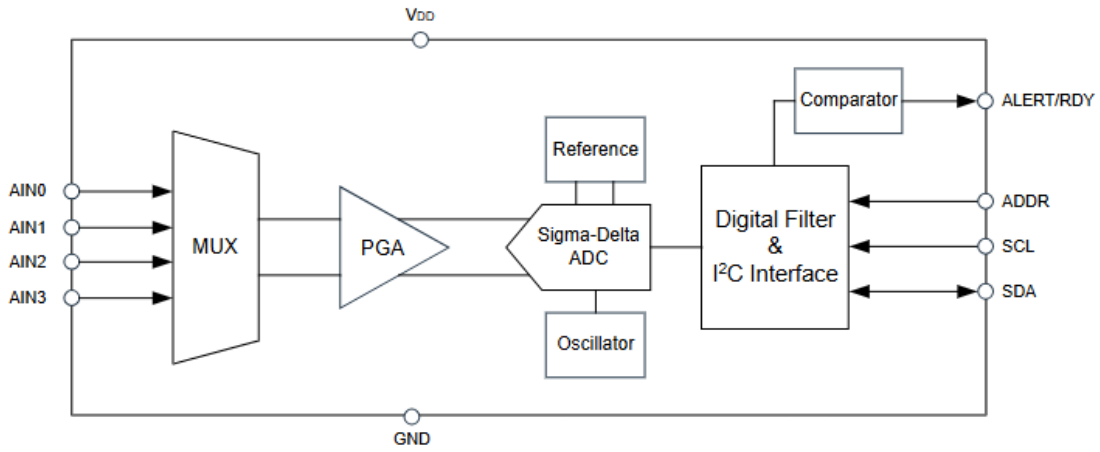
Description

The TPC6200I is a 24-bit Sigma-Delta ADC for high precision and low power measurement with I²C. The TPC6200I features an internal programmable gain amplifier (PGA), voltage reference, oscillator, digital filter and programmable comparator. The device supports a wide range of supply voltages from 2.7 V to 5.5 V.

The data rate of the TPC6200I is configurable from 64 SPS to 32 kSPS. The PGA provides input ranges spanning from ±256 mV to ±6.144 V, with the analog input negative voltage down to −128 mV, which allows both high precision positive and negative signal measurement. The integrated input mux supports two differential pairs or four independent single-ended inputs. The internal temperature sensor can be used for general temperature monitoring or thermal-couple cold-junction compensation.

The TPC6200I can be set in single-shot conversion mode or continuous conversion mode. The single-shot mode features power down after conversion, which is suitable for low-power applications. The digital interface supports communication with various host controllers with I²C-compatible serial interface. The TPC6200I is available in MSOP10 package and operates from −40°C to +125°C.

Functional Block Diagram



I²C Interface, 24-Bit, 32 kSPS, 4-Channel Sigma-Delta ADC with Internal Reference

Table of Contents

Product Family Table

Order Number	Channels	Resolution	Throughput	Package	Interface
TPC6200I-VS2R	4	24 Bits	32 kSPS	MSOP10	I²C

Revision History

Date	Revision	Notes
2026-03-26	Rev.A.0	Initial release.

Pin Configuration and Functions

TPC6200I
MSOP10 Package
Top View

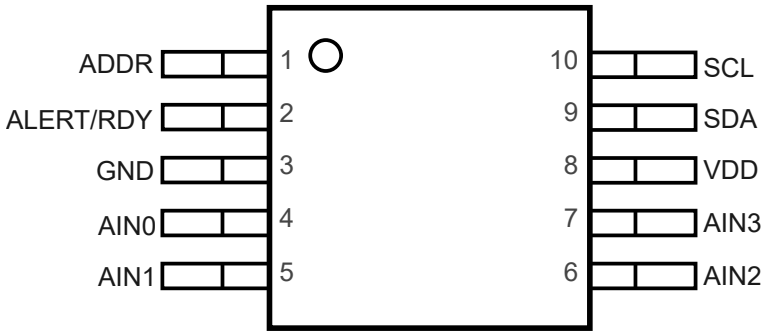


Table 1. Pin Functions: TPC6200I

Pin		Type (1)	Description
No.	Name		
1	ADDR	DI	I²C slave address select.
2	ALERT/RDY	DO	Comparator output or conversion ready.
3	GND	P	Ground.
4	AIN0	AI	Analog Input for Channel 0. If not used, float this pin or tie to VDD.
5	AIN1	AI	Analog Input for Channel 1. If not used, float this pin or tie to VDD.
6	AIN2	AI	Analog Input for Channel 2. If not used, float this pin or tie to VDD.
7	AIN3	AI	Analog Input for Channel 3. If not used, float this pin or tie to VDD.
8	VDD	P	Power supply. Connect a 0.1 µF power supply decoupling capacitor to GND.
9	SDA	DI/DO	Serial data input and output.
10	SCL	DI	Serial clock input.

(1) AI is analog input, GND is ground, P is power supply, DI is digital input and DO is digital output.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Analog Voltage	Analog Input Voltage to GND	GND − 0.3	VDD + 0.3	V
Digital Voltage	Digital Input Voltage to GND	GND − 0.3	VDD + 0.3	V
	Digital Output Voltage to GND	GND − 0.3	VDD + 0.3	V
Supply Voltage	VDD to GND	−0.3	5.5	V
Input current (continuous)	Any Pin except Power Supply Pins	−10	10	mA
T_J	Maximum Junction Temperature		150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
	Power Supply (VDD to GND)	2.7		5.5	V
FSR	Full-scale Input Voltage (1) (V_{IN} = $V_{(AINP)}$ - $V_{(AINN)}$)	±0.256		±6.144	V
$V_{(AINx)}$	Absolute Input Voltage	−0.128		VDD	V
Digital input Voltage	Absolute Input Voltage	GND		VDD	V
T_A	Operating Ambient Temperature	−40		125	℃

(1) This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3 V or 5.5 V (whichever is smaller) must be applied to this device.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
MSOP10	125	48	°C/W

Electrical Characteristics

All test conditions: VDD = 3.3 V, data rate = 1024 SPS, and FSR = ±2.048 V. T_A = −40 ℃ to 125 ℃, unless otherwise noted.

Parameter	Test Conditions		Min	Typ	Max	Unit
Analog Inputs						
Common-mode Input Impedance	FSR = ±6.144 V (1)			1.7		MΩ
	FSR = ±4.096 V (1)			0.87		MΩ
	FSR = ±2.048 V			0.51		MΩ
	FSR = ±1.024 V			0.54		MΩ
	FSR = ±0.512 V			0.26		MΩ
	FSR = ±0.256 V			0.26		MΩ
Differential Input Impedance	FSR = ±6.144 V (1)			0.74		MΩ
	FSR = ±4.096 V (1)			0.37		MΩ
	FSR = ±2.048 V			0.19		MΩ
	FSR = ±1.024 V			0.11		MΩ
	FSR = ±0.512 V			0.068		MΩ
	FSR = ±0.256 V			0.068		MΩ
System Performance						
Resolution	NO missing code		24			Bits
DR	Data rate		64, 128, 256, 512, 1024, 2000, 4000, 8000, 16000, 32000			SPS
	Data rate variation	All data rates	− 10%		10%	
INL	Integral nonlinearity	DR = 64 SPS, FSR = ±2.048 V	−35	±8	35	ppm
Offset Error	FSR = ±2.048 V, differential inputs		−0.2	0.056	0.2	mV
Offset Drift	FSR = ±2.048 V			0.6		μV/℃
Offset Power-supply Rejection	FSR = ±2.048 V, DC supply variation			1500		LSB/V
Offset Channel Match	Match between any two inputs			232		LSB
Gain Error	FSR = ±2.048 V, T_A = 25℃			0.05%	0.15%	
Gain Drift (2)	FSR = ±0.256 V			3.7		ppm/℃
	FSR = ±2.048 V			3.7	10	ppm/℃
	FSR = ±6.144 V (1)			3.7		ppm/℃
	Gain power-supply rejection			78		dB
Gain Match	Match between any two gains			0.05%	0.1%	
Gain Channel Match	Match between any two inputs			0.01%	0.1%	
CMRR	Common-mode Rejection Ratio	At DC, FSR = ±0.256 V		126		dB
		At DC,		115		dB

Parameter	Test Conditions		Min	Typ	Max	Unit
		FSR = ±2.048 V				
		At DC, FSR = ±6.144 V (1)		108		dB
		f_{CM} = 50 Hz, DR = 1 kSPS		114		dB
		f_{CM} = 60 Hz, DR = 1 kSPS		113		dB
Digital Input/Outputs						
V_{IH}	High-level input voltage		0.7 x VDD		VDD	V
V_{IL}	Low-level input voltage		GND		0.2 x VDD	V
V_{OH}	I_{SOURCE} = 1 mA		0.8 x VDD			V
V_{OL}	I_{SINK} = 1 mA		GND		0.2 x VDD	V
I_H	Input leakage, high	V_{IH} = 5.5 V	−10		10	µA
I_L	Input leakage, low	V_{IL} = GND	−10		10	µA
Power Supply						
I_{VDD}	Supply current	Power-down, T_A = 25℃		4.6	10	µA
		Operating, T_A = 25℃		4.6	7	mA
		Operating		4	5.5	mA
P_D	Power dissipation	VDD = 5 V		20		mW
Temperature Range	Specified performance		−40		+125	℃

(1) This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3 V or 5.5 V (whichever is smaller) must be applied to this device.

(2) Maximum value specified by characterization.

Timing Specifications (1)

All test conditions: VDD = 2.7 V to 5.5 V and T_A = −40 °C to 125 °C, unless otherwise noted.

Table 2. I²C Interface

Parameter	Description	Fast Mode		High-speed Mode		Unit
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0.01	0.4	0.01	3.4	MHz
t_{BUF}	Bus free time between START and STOP condition	600		160		ns
t_{HDSTA}	Hold time after repeated START condition. After this period, the first clock is generated.	600		160		ns
t_{SUSTA}	Setup time for a repeated START condition	600		160		ns
t_{SUSTO}	Setup time for STOP condition	600		160		ns
t_{HDDAT}	Data hold time	0		0		ns
t_{SUDAT}	Data setup time	100		10		ns
t_{LOW}	Low period of the SCL clock pin	1300		160		ns
t_{HIGH}	High period for the SCL clock pin	600		60		ns
t_F	Fall time for both SDA and SCL signals (2)		300		160	ns
t_R	Rise time for both SDA and SCL signals (2)		300		160	ns

(1) Parameters are provided by design simulation.
(2) For high-speed mode maximum values, the capacitive load on the bus line must not exceed 400 pF.

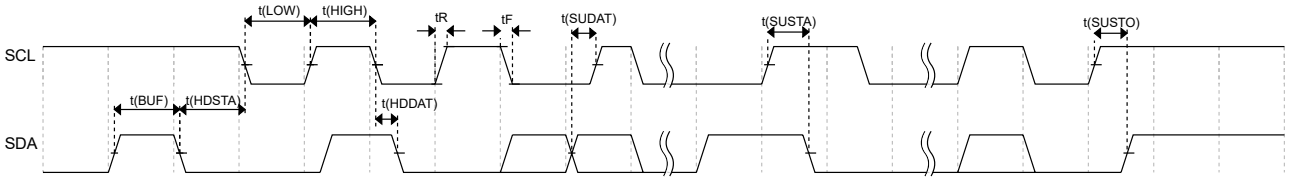


Figure 1. I²C Interface

Typical Performance Characteristics

All test conditions: T_A = 25°C, VDD = 3.3 V, FSR = ±2.048 V, DR = 64 SPS, unless otherwise noted.

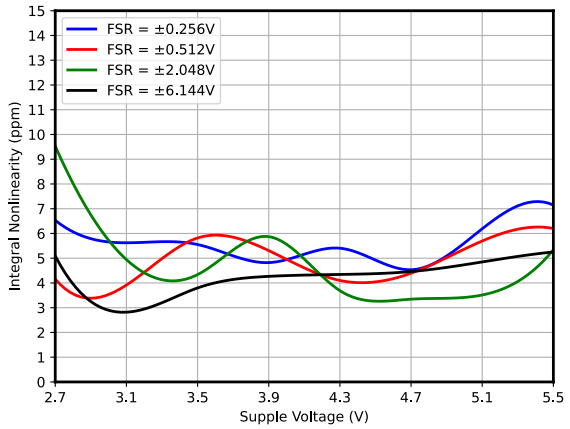
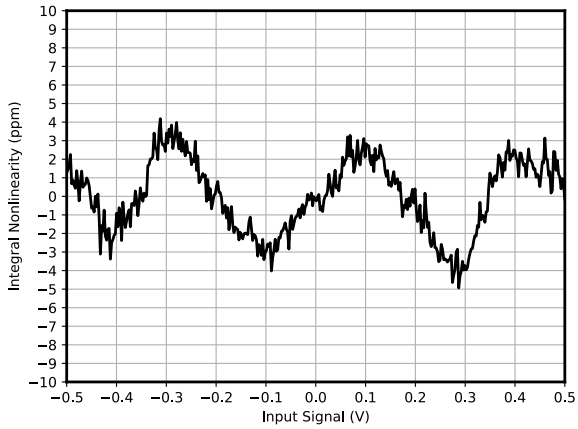
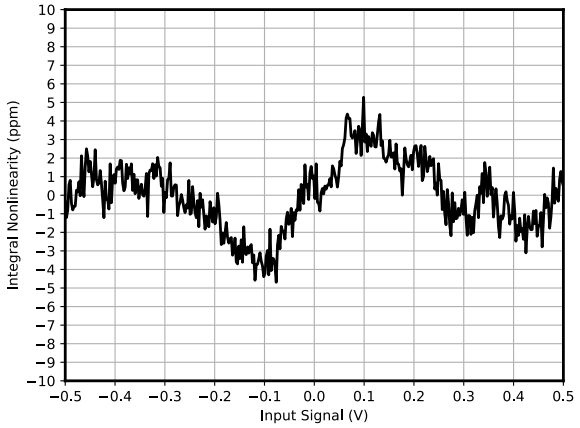


Figure 2. INL vs. Supply Voltage



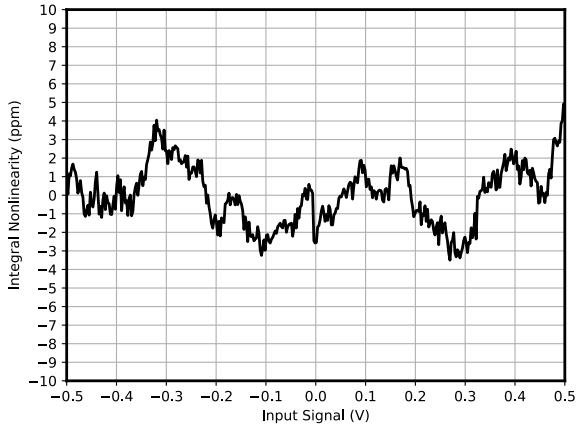
VDD = 3.3 V, FSR = ±0.512 V, DR = 64 SPS, best fit

Figure 3. INL vs. Input Signal



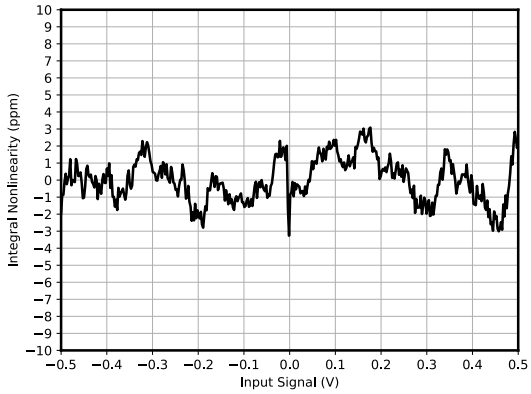
VDD = 5.0 V, FSR = ±0.512 V, DR = 64 SPS, best fit

Figure 4. INL vs. Input Signal



VDD = 3.3 V, FSR = ±2.048 V, DR = 64 SPS, best fit

Figure 5. INL vs. Input Signal



VDD = 5.0 V, FSR = ±2.048 V, DR = 64 SPS, best fit

Figure 6. INL vs. Input Signal

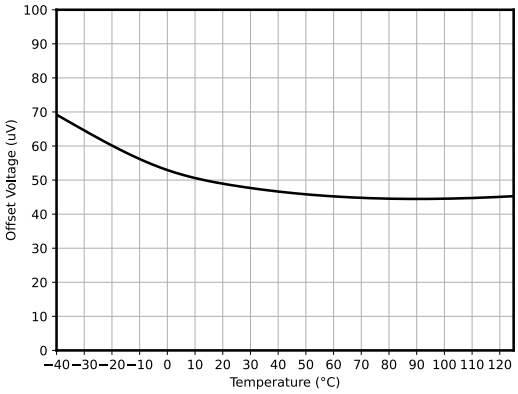


Figure 7. Differential Offset Voltage vs. Temperature

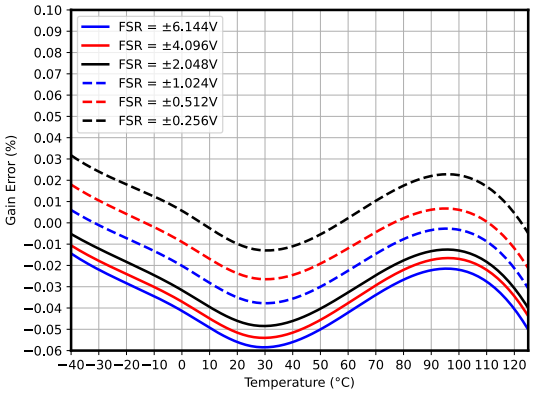
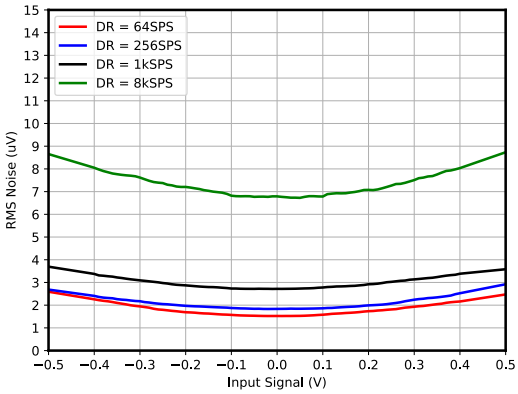
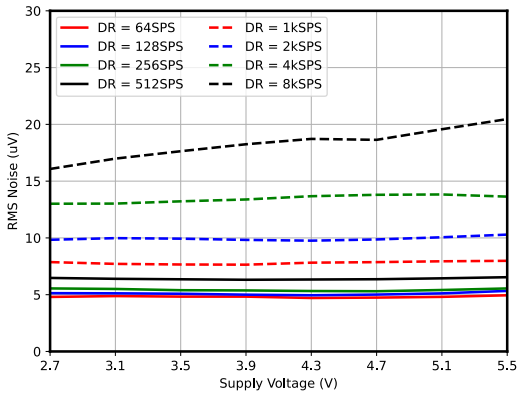


Figure 8. Gain Error vs. Temperature



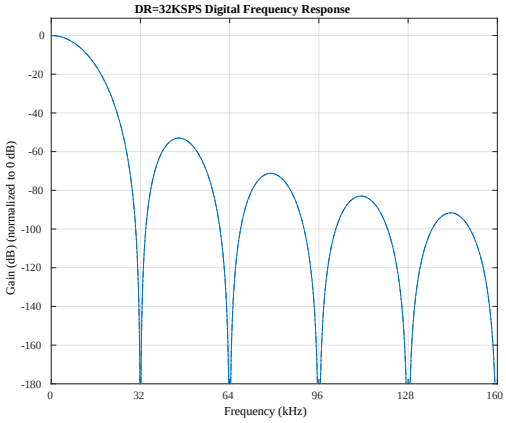
FSR = ±0.512 V

Figure 9. Noise vs. Input Signal



FSR = ±0.512 V

Figure 10. Noise vs. Supply Voltage



Provided by simulation results

Figure 11. Digital Filter Frequency Response

Noise Performance

The Sigma-Delta (ΣΔ) ADC architecture operates based on oversampling principles. In this approach, the input signal is sampled at a high frequency, known as the modulator frequency. The sampled signal is then processed through filtering and decimation in the digital domain, resulting in the final conversion output at a specified data rate. The oversampling ratio (OSR), which is the ratio between the modulator frequency and the output data rate, plays a crucial role. By increasing the OSR, and consequently lowering the output data rate, the noise performance of the ADC can be optimized. This is achieved by averaging more samples of the internal modulator, thereby reducing input-referred noise. Additionally, increasing the gain proves beneficial for measuring low-level signals as it further contributes to the reduction of input-referred noise.

The following tables provide an overview of the noise performance of the device, with data representative of typical noise characteristics at a temperature of 25°C and the inputs externally shorted together. Table 3 and Table 4 display the input-referred noise in units of microvolts root mean square (μVRMS), with microvolts peak-to-peak (μVPP) values shown in parentheses. Table 5 and Table 6 present the corresponding data in terms of effective number of bits (ENOB), calculated from μVRMS values using Equation 1. The noise-free bits, determined from peak-to-peak noise values using Equation 2, are enclosed in parentheses.

$$ENOB = \ln(FSR/V_{RMS-Noise})/\ln(2) \quad (1)$$

$$Noise-Free\ Bits = \ln(FSR/V_{PP-Noise})/\ln(2) \quad (2)$$

Table 3. Noise in μVRMS at VDD = 3.3 V (Global Chop on)

Data Rate (SPS)	FSR					
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V
64	13.02	8.83	4.52	2.31	1.36	1.04
128	13.98	9.5	4.75	2.49	1.5	1.11
256	16.38	10.57	5.34	2.94	1.71	1.3
512	18.94	12.03	6.48	3.42	2.07	1.51
1024	22.93	14.79	7.44	4.13	2.43	1.92
2k	29.28	18.25	9.57	5	3.14	2.33
4k	37.7	24.38	12.62	6.74	4.11	3.16
8k	49.34	34.42	16.72	8.76	5.65	4.46
16k	30.38	19.55	9.82	5.6	3.37	2.61
32k	48.29	26.57	15.77	6.87	4.49	3.39

Table 4. Noise in μVPP at VDD = 3.3 V (Global Chop on)

Data Rate (SPS)	FSR					
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V
64	78.11	52.97	27.13	13.85	8.13	6.22
128	83.9	56.98	28.5	14.92	9.03	6.63
256	98.25	63.43	32.01	17.65	10.28	7.8
512	113.65	72.21	38.86	20.5	12.42	9.08
1024	137.6	88.72	44.66	24.75	14.61	11.52
2k	175.68	109.48	57.41	29.97	18.85	13.95

Data Rate (SPS)	FSR					
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V
4k	226.19	146.29	75.74	40.42	24.64	18.98
8k	296.03	206.5	100.34	52.58	33.91	26.77
16k	182.29	117.3	58.92	33.63	20.21	15.65
32k	289.72	159.45	94.61	41.21	26.93	20.35

Table 5. ENOB from RMS Noise at VDD = 3.3 V (Global Chop on)

Data Rate (SPS)	FSR					
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V
64	19.85	19.82	19.79	19.76	19.53	18.91
128	19.75	19.72	19.72	19.65	19.38	18.82
256	19.52	19.56	19.55	19.41	19.19	18.59
512	19.31	19.38	19.27	19.19	18.92	18.37
1024	19.03	19.08	19.07	18.92	18.68	18.02
2k	18.68	18.78	18.71	18.65	18.31	17.75
4k	18.31	18.36	18.31	18.21	17.93	17.3
8k	17.93	17.86	17.9	17.83	17.47	16.81
16k	18.63	18.68	18.67	18.48	18.21	17.58
32k	17.96	18.23	17.99	18.19	17.8	17.2

Table 6. Noise-Free Bits from Peak-to-Peak Noise at VDD = 3.3 V (Global Chop on)

Data Rate (SPS)	FSR					
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V
64	17.26	17.24	17.2	17.17	16.94	16.33
128	17.16	17.13	17.13	17.07	16.79	16.24
256	16.93	16.98	16.97	16.82	16.6	16
512	16.72	16.79	16.69	16.61	16.33	15.78
1024	16.45	16.49	16.48	16.34	16.1	15.44
2k	16.09	16.19	16.12	16.06	15.73	15.16
4k	15.73	15.77	15.72	15.63	15.34	14.72
8k	15.34	15.28	15.32	15.25	14.88	14.22
16k	16.04	16.09	16.09	15.89	15.63	15
32k	15.37	15.65	15.4	15.6	15.21	14.62

Table 7. Noise in μVRMS at VDD = 3.3 V (Global Chop off)

Data Rate (SPS)	FSR					
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V
64	5.02	3.28	1.64	0.9	0.59	0.45
128	7.35	4.75	2.56	1.28	0.77	0.57
256	10.8	6.96	3.67	1.83	1.03	0.79
512	16.26	10.1	5.11	2.62	1.45	1.12
1024	22.83	13.92	7.44	3.82	2.08	1.66
2k	30.32	18.21	10.68	5.02	2.97	2.33
4k	38.96	22.82	13.64	6.76	3.83	3.16
8k	56.97	31.11	19.29	8.9	4.48	4.32
16k	55.33	34.1	18.39	8.97	5.65	3.65
32k	79.44	53.3	26.56	13.75	7.65	5.21

Table 8. Noise in μVPP at VDD = 3.3 V (Global Chop off)

Data Rate (SPS)	FSR					
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V
64	30.1	19.66	9.87	5.41	3.52	2.67
128	44.13	28.49	15.35	7.66	4.62	3.42
256	64.81	41.77	22	10.98	6.2	4.72
512	97.56	60.63	30.68	15.72	8.68	6.73
1024	136.99	83.51	44.63	22.9	12.49	9.99
2k	181.9	109.24	64.06	30.12	17.8	13.96
4k	233.78	136.9	81.85	40.59	23	18.94
8k	341.8	186.65	115.75	53.37	26.86	25.93
16k	331.98	204.62	110.33	53.81	33.91	21.9
32k	476.65	319.8	159.34	82.48	45.93	31.28

Table 9. ENOB from RMS Noise at VDD = 3.3 V (Global Chop off)

Data Rate (SPS)	FSR					
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V
64	21.22	21.25	21.25	21.11	20.73	20.13
128	20.67	20.72	20.61	20.61	20.34	19.78
256	20.12	20.17	20.09	20.09	19.92	19.31
512	19.53	19.63	19.61	19.58	19.43	18.8
1024	19.04	19.17	19.07	19.03	18.91	18.23
2k	18.63	18.78	18.55	18.64	18.4	17.75
4k	18.27	18.45	18.2	18.21	18.03	17.31

Data Rate (SPS)	FSR					
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V
8k	17.72	18.01	17.7	17.81	17.8	16.85
16k	17.76	17.87	17.77	17.8	17.47	17.1
32k	17.24	17.23	17.23	17.18	17.03	16.58

Table 10. Noise-Free Bits from Peak-to-Peak Noise at VDD = 3.3 V (Global Chop off)

Data Rate (SPS)	FSR					
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V
64	18.64	18.67	18.66	18.53	18.15	17.55
128	18.09	18.13	18.03	18.03	17.76	17.19
256	17.53	17.58	17.51	17.51	17.33	16.73
512	16.94	17.04	17.03	16.99	16.85	16.21
1024	16.45	16.58	16.49	16.45	16.32	15.65
2k	16.04	16.19	15.96	16.05	15.81	15.16
4k	15.68	15.87	15.61	15.62	15.44	14.72
8k	15.13	15.42	15.11	15.23	15.22	14.27
16k	15.18	15.29	15.18	15.22	14.88	14.51
32k	14.65	14.64	14.65	14.6	14.44	14

Detailed Description

Overview

The TPC6200I is a compact, low-power, 24-bit sigma-delta analog-to-digital converter (ADC) designed to minimize external circuitry and enhance performance. It incorporates a ΣΔ ADC core with adjustable gain, an internal voltage reference, a clock oscillator, and an I2C interface. Additionally, it integrates a comparator. The ADC core measures a differential signal, VIN, representing the difference between V(AINP) and V(AINN). The core features a differential, switched-capacitor ΣΔ modulator followed by a digital filter, providing strong common-mode signal attenuation.

The device operates in single-shot or continuous-conversion modes, with single-shot mode saving power by performing one conversion upon request and entering a power-down state. In continuous-conversion mode, the ADC automatically initiates conversions, and data can be read at any time, reflecting the most recent completed conversion.

Functional Block Diagram

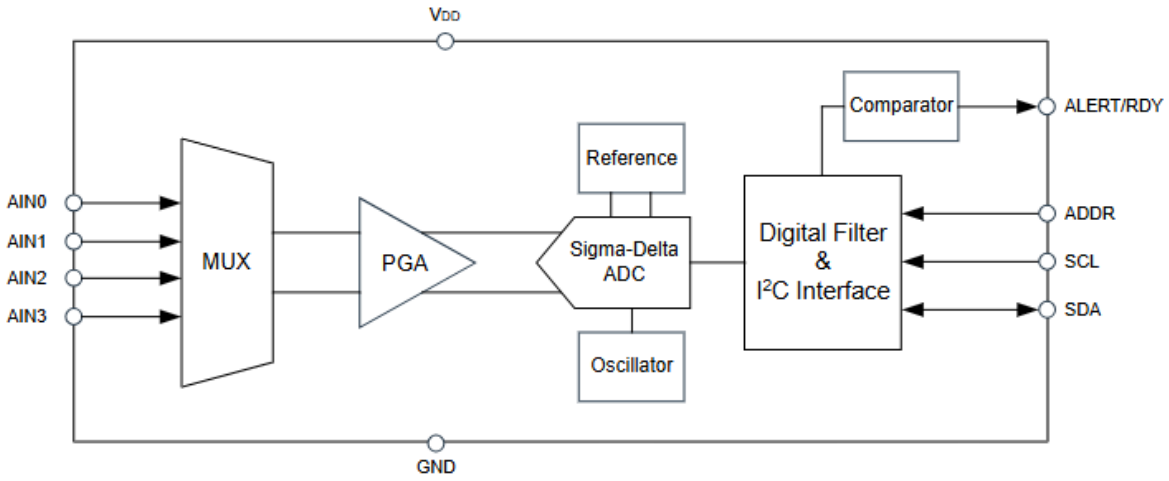


Figure 12. TPC6200I Block Diagram

Feature Description

Multiplexer

The TPC6200I is integrated with an input multiplexer (mux). It allows the measurement of either four single-ended signals or two differential signals. Also, the AIN0, AIN1, and AIN2 inputs can be differentially measured against AIN3. The configuration of the multiplexer is controlled by the MUX[2:0] bits in the Config register. In cases where single-ended signals are being measured, the negative input of the ADC is internally connected to GND through a switch within the multiplexer.

When single-ended inputs are being measured, the TPC6200I does not produce negative codes. Negative codes are indicative of negative differential signals, where $(V_{(AINP)} - V_{(AINN))} < 0$. Electrostatic discharge (ESD) diodes to VDD and GND serve to protect the ADC inputs. The TPC6200I is allowed to measure absolute negative input voltage down to −128 mV and still needs to prevent the ESD diodes from turning on; it is essential to maintain the absolute voltage on any input within the range specified in the following equation:

$$GND - 0.3\ V < V_{(AINx)} < VDD + 0.3\ V \quad (3)$$

If there is a possibility that the voltages on the input pins may violate these conditions, it is advisable to employ external Schottky diodes and series resistors. This helps to limit the input current to safe values. Additionally, overdriving one unused input on the TPC6200I may impact conversions occurring on other input pins at that time. In cases where overdriving unused inputs is a possibility, it is recommended to clamp the signal using external Schottky diodes.

Analog Inputs

The TPC6200I employs a switched-capacitor input stage, where capacitors undergo a continuous charging and discharging process to measure the voltage between AIN_P and AIN_N. The equivalent resistance is determined by the values of the capacitors and the frequency at which they are switched.

The common-mode input impedance is determined by applying a common-mode signal to the shorted AIN_P and AIN_N inputs and measuring the average current consumed by each pin. The common-mode input impedance may vary depending on the selected full-scale range. The common-mode input impedance is denoted as Z_{CM}.

The differential input impedance is measured by applying a differential signal to the AIN_P and AIN_N inputs. The average current flowing through the input pins represents the differential current and scales with the selected full-scale range. The symbol Z_{DIFF} represents the differential input impedance.

Note that this unbuffered input path provides a dynamic load to the driving source. Therefore, resistor/capacitor combinations on the input pins can cause DC gain errors, depending on the output impedance of the source that is driving the ADC input. The table below shows the allowable external resistance/capacitance values such that no gain error at the 20-bit level is introduced when the data rate is within 2 kSPS.

Table 11. External R-C Combination for No 20-Bit Gain Error

R (Ω)	C (pF)
16	1000
50	300
100	150

Full-Scale Range (FSR) and LSB Size

The gain setting of the PGA inside the TPC6200I ΣΔ ADC determines the input full-scale range (FSR). The full-scale range is configured by bits PGA[2:0] in the Config register, and can be set to ±6.144 V, ±4.096 V, ±2.048 V, ±1.024 V, ±0.512 V, or ±0.256 V.

The table below presents the Full-Scale Range (FSR) alongside the corresponding Least Significant Bit (LSB) size. The LSB size is calculated from the full-scale voltage using the formula in Equation 4. It is essential to ensure that the analog

input voltage never exceeds the specified analog input voltage range limit provided in the Electrical Characteristics. If a VDD greater than 4 V is utilized, the ±6.144-V full-scale range allows input voltages to extend up to the supply voltage. It is important to note that in such cases or whenever the supply voltage is less than the full-scale range (e.g., VDD = 3.3 V and full-scale range = ±4.096 V), a full-scale ADC output code cannot be achieved, resulting in a loss of dynamic range.

Equation (4): $LSB = FSR/2^{24}$

Table 12. Full-Scale Range and Corresponding LSB Size

FSR	LSB Size
±6.144 V (1)	732 nV
±4.096 V (1)	488 nV
±2.048 V	244 nV
±1.024 V	122 nV
±0.512 V	61 nV
±0.256 V	30.5 nV

(1) This parameter expresses the full-scale range of the ADC scaling. Do not apply more than VDD + 0.3 V to this device.

Voltage Reference

The TPC6200I integrates an internal voltage reference, and the use of an external reference is not supported with this device. Any errors associated with the initial voltage reference accuracy and its drift with temperature are accounted for in the gain error and gain drift specifications provided in the specifications.

Oscillator

The TPC6200I features an integrated oscillator, eliminating the need for an external clock to drive the device. It's important to note that the internal oscillator may exhibit drift over temperature and time. Additionally, the output data rate scales proportionally with the oscillator frequency.

Output Data Rate and Conversion Time

The TPC6200I provides programmable output data rates. Use the DR[2:0] bits in the Config register to set output data rates of 64 SPS, 128 SPS, 256 SPS, 512 SPS, 1024 SPS, 2 kSPS, 4 kSPS, 8 kSPS, 16 kSPS or 32 kSPS.

Conversions in the TPC6200I settle within a single cycle; thus, the conversion time is equal to 1/DR.

Digital Comparator

The TPC6200I integrates a digital comparator that can generate alerts through the ALERT/RDY pin. The COMP_MODE bit within the Config register determines whether the comparator functions as a traditional comparator or a window comparator. In traditional comparator mode, the ALERT/RDY pin is asserted (typically active low) when the conversion data surpasses the threshold defined in the high-threshold register (Hi_thresh). It remains asserted until the conversion data drops below the threshold specified in the low-threshold register (Lo_thresh). Conversely, in window comparator mode, the ALERT/RDY pin is asserted when the conversion data either exceeds the value set in the Hi_thresh register or falls below the value set in the Lo_thresh register.

In both window and traditional comparator modes, the comparator's behavior after assertion can be adjusted using the COMP_LAT bit within the Config register. When set, this feature causes the assertion to persist even if the input signal is within the threshold limits. Clearing this latched assertion is possible only through an SMBus alert response or by reading the Conversion register. Furthermore, the polarity of the ALERT/RDY pin can be configured as either active high or active low using the COMP_POL bit in the Config register.

The comparator functionality extends to activating the ALERT/RDY pin only after a specified number of consecutive readings surpass the threshold values defined in the threshold registers (Hi_thresh and Lo_thresh). The COMP_QUE[1:0] bits within

the Config register control this behavior, allowing configuration for one, two, or four readings beyond the thresholds before triggering the ALERT/RDY pin. Alternatively, these bits can disable the comparator function entirely, placing the ALERT/RDY pin into a high state.

Conversion Ready Pin

The ALERT/RDY pin can alternatively function as a conversion ready indicator. By setting MSB of the Hi_thresh register to 1 and that of the Lo_thresh register to 0, the pin can be configured for this purpose. The COMP_POL bit maintains its expected behavior in this mode. To keep the ALERT/RDY pin enabled and allow the conversion ready signal, any 2-bit value other than 11 should be set for the COMP_QUE[1:0] bits. The COMP_MODE and COMP_LAT bits become inactive in this configuration. When used as a conversion ready pin, ALERT/RDY still requires a pullup resistor. In continuous-conversion mode, the TPC6200I produces an approximately 8-µs conversion ready pulse on the ALERT/RDY pin at the end of each conversion. In single-shot mode with COMP_POL bit set to 0, the ALERT/RDY pin asserts high at the end of a conversion.

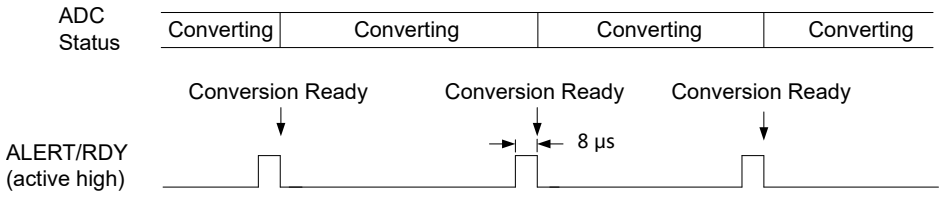


Figure 13. Conversion Ready Pulse in Continuous-Conversion Mode

SMBus Alert Response

In latching comparator mode (COMP_LAT = 1), the ALERT/RDY pin triggers when the comparator detects a conversion exceeding the upper or lower threshold value. This trigger is latched and can only be cleared by reading conversion data or by issuing a successful SMBus alert response and reading the asserting device's I²C address. If subsequent conversion data again exceeds the upper or lower threshold values, the pin reasserts. This reassertion does not impact conversions already in progress. The ALERT/RDY pin functions as an open-drain output, enabling multiple devices to share the same interface bus. When disabled, the pin maintains a high state to prevent interference with other devices on the bus line.

When the master detects that the ALERT/RDY pin has latched, it sends an SMBus alert command (00011001) to the I²C bus. All ADC data converters on the I²C bus with asserted ALERT/RDY pins respond to this command by transmitting their slave addresses. In cases where multiple devices on the I²C bus have latched ALERT/RDY pins, arbitration occurs during the address response phase of the SMBus alert to determine which device will clear its assertion. The device with the lowest I²C address wins arbitration and proceeds to clear its assertion. If a device loses arbitration, it does not clear the comparator output pin assertion. The master repeats the SMBus alert response process until all devices have cleared their respective assertions. In window comparator mode, the SMBus alert status bit indicates a logic 1 if signals exceed the high threshold and a logic 0 if signals exceed the low threshold.

Digital Interface

Device Functional Modes

Reset and Power-Up

When the TPC6200I powers up, the device undergoes a reset procedure that results in the configuration register (Config register) having all its bits set to their default values. In its default state, the device enters a power-down mode upon startup. During this mode, the device's interface and digital blocks remain active, but no data conversions take place. This initial power-down state is designed to prevent systems with stringent power-supply requirements from experiencing a surge during the power-up phase.

The TPC6200I devices are designed to respond to I²C general-call reset commands. Upon receiving a general call reset command (06h), the device initiates an internal reset procedure, like the actions taken during power-up.

Operating Modes

The TPC6200I operates in one of two modes: continuous-conversion or single-shot. The operating mode is determined by the state of the MODE bit in the Config register.

Single-Shot Mode and Power-Down

When the MODE bit in the Config register is set to 1, indicating single-shot mode, the TPC6200I enters a power-down state. This power-down state is the default state when power is first applied. While in this state, the device remains responsive to commands. The device will stay in the power-down state until a 1 is written to the single-shot (SS) bit in the Config register. When the SS bit is set, the device powers up, resets the SS bit to 0, and initiates a single conversion. Once the conversion is completed, and the conversion data are ready, the device returns to the power-down state. Attempting to write a 1 to the SS bit while a conversion is already in progress will have no effect. To switch to continuous-conversion mode, it is necessary to write a 0 to the MODE bit in the Config register.

Continuous-Conversion Mode

In continuous-conversion mode, where the MODE bit is set to 0, the TPC6200I consistently conducts conversions. Once a conversion is finished, the result is stored in the Conversion register, and the device promptly initiates another conversion. To transition to single-shot mode, one can write a 1 to the MODE bit in the Config register or perform a device reset.

Duty Cycling for Low Power

The noise performance of a ΣΔ ADC typically improves at lower output data rates, as more samples of the internal modulator are averaged to produce a single conversion result. In scenarios where power consumption is a critical consideration and the enhanced noise performance at low data rates is not essential, the TPC6200I provides support for duty cycling. This feature enables significant power savings by periodically requesting high data-rate readings at an effectively lower data rate.

Programming

I2C Interface

The I²C protocol is a serial communication protocol used for connecting multiple integrated circuits in a system. Both SDA and SCL lines are pulled high via pull-up resistors, and devices pull the lines low to signal data. It features a master-slave architecture, where one or more master devices communicate with one or more slave devices over a shared bus. However, TPC6200I can only be used as a slave device.

Connections to the I²C are established via the open-drain I/O lines, specifically SDA and SCL. The SDA line carries the actual data being transmitted between the master and slave devices, and the SCL line carries the clock signal generated by the master device to synchronize data transmission. Data transfer occurs in bytes (8 bits).

The bus protocol has been defined as follows:

- In the defined bus protocol, it's specified that data transfer can only be initiated when the bus is not currently engaged or "busy". This means that before starting any data transfer, it is essential to check and ensure that the bus is in an idle state, available for communication.
- The data line must maintain a stable state when the clock line is in a HIGH state. Any alterations or changes in the data line while the clock line is HIGH will be interpreted as control signals rather than data bits.
- Bus not busy: Both data and clock lines are HIGH.
- Start data transfer: During a start condition, the SDA (Serial Data) line transitions from high to low while the SCL (Serial Clock) line is high. This signals the beginning of a data transfer or communication session.
- Stop data transfer: During a stop condition, the SDA line transitions from low to high while the SCL line is high. This signals the end of the communication session, and the bus is released.
- Data valid: The data line (SDA) is considered to be in a state of valid data when, following a START condition, the data on the SDA line remains stable and can be reliably read for the entire duration of the HIGH period of the clock signal (SCL). There is one clock pulse per bit of data.
  Each data transfer begins with a START condition and ends with a STOP condition. The number of data bytes that can be transferred between the START and STOP conditions is not limited and it is determined by the master device. After each byte of data is transferred, the receiving device (the slave) acknowledges the receipt of the data by sending an acknowledgment bit (ACK) or a not-acknowledgment bit (NACK) as the ninth bit.
  The I²C bus specification defines three different modes of operation based on clock rates: standard mode (100 kHz clock rate), fast mode (400 kHz clock rate), and high-speed mode (3.4 MHz clock rate). The device supports all the modes.
- Acknowledgment: This is a signal sent by the receiving device (usually a slave device) to acknowledge the successful receipt of data from the transmitting device (usually the master device) for each byte. After the transmission of each byte, the sender releases the SDA (Serial Data) line and waits for the receiver's acknowledgment. The receiver (slave) acknowledges the successful reception of the data byte by pulling the SDA line low for a brief moment during the ACK bit time (usually the ninth clock cycle). This brief low pulse of the SDA line serves as an acknowledgment, indicating that the data was received without error and that the receiver is ready to accept the next byte of data.

The address byte represents the initial byte received immediately after the master device initiates the START condition. The last bit within the address byte, known as the R/$\overline{W}$ (Read/Write) bit, specifies the type of operation to be executed. When the bit is set to 1, it signifies that a read operation is selected. Conversely, when the R/W bit is set to 0, it signifies a write operation. Following the initiation of the START condition, the device observes the state of the SDA bus. The slave device promptly responds by transmitting an acknowledge signal along the SDA line. This acknowledgment signal serves as confirmation that the ADC has identified the master's request and is prepared to proceed with the requested read or write operation.

I2C Address Selection

The address pin ADDR of the TPC6200I is used for configuring the I²C address of the device. This pin offers flexibility by allowing connection to different voltage levels or I²C bus lines, enabling the selection of four distinct addresses, which are GND, VDD, SDA, and SCL. When using the SDA pin as the device address, it's important to ensure proper communication. To do so, hold the SDA line low for at least 100 ns after the SCL line goes low. This ensures accurate decoding of the address during I²C communication. The table below illustrates the address configurations:

Table 13. ADDR Pin Connection and Corresponding Slave Address

ADDR Pin Connection	Slave Address
GND	1001000
VDD	1001001
SCL	1001010
SDA	1001011

I2C General Call

The TPC6200I can respond to the I²C general call address (0000000) when the eighth bit is 0. Upon receiving the general call address, the devices acknowledge it and await commands in the second byte of the I²C frame. If the second byte is 00000110 (06h), the TPC6200I resets internal registers and enters a power-down state.

I2C Speed Modes

The TPC6200I can be used as a slave receiver or slave transmitter. As a slave device, the TPC6200I is not able to drive the SCL line.

Receive Mode

In slave receive mode, the initial byte sent from the master to the slave comprises the 7-bit device address, followed by a low R/$\overline{W}$ bit. Subsequently, the master transmits the Address Pointer register byte. The TPC6200I acknowledges the reception of the Address Pointer register byte. Following this, the next two bytes are written to the address specified by the register address pointer bits, P[1:0]. Each byte sent is acknowledged by the TPC6200I. Register bytes are transmitted with the most significant byte first, followed by the least significant byte.

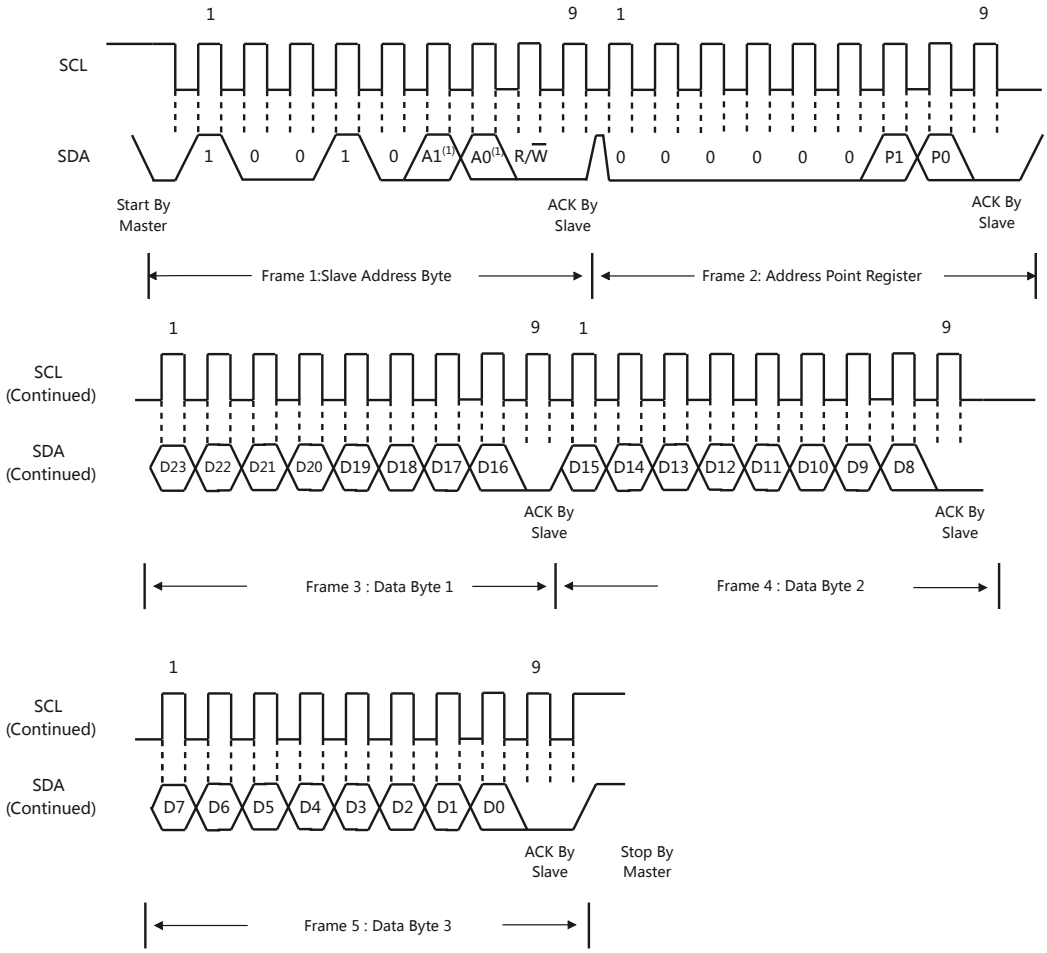
Transmit Mode

In slave transmit mode, the master initiates communication by sending the 7-bit slave address followed by the high R/$\overline{W}$ bit. This signals the slave to transmit data, indicating that the TPC6200I is being read from. Next, the slave sends the most significant byte of the register specified by the register address pointer bits, P[1:0]. The master acknowledges this byte. Subsequently, the slave sends the least significant byte, followed by another acknowledgment from the master. The master can terminate transmission after any byte by either not acknowledging or issuing a START or STOP condition.

Writing To and Reading from the Registers

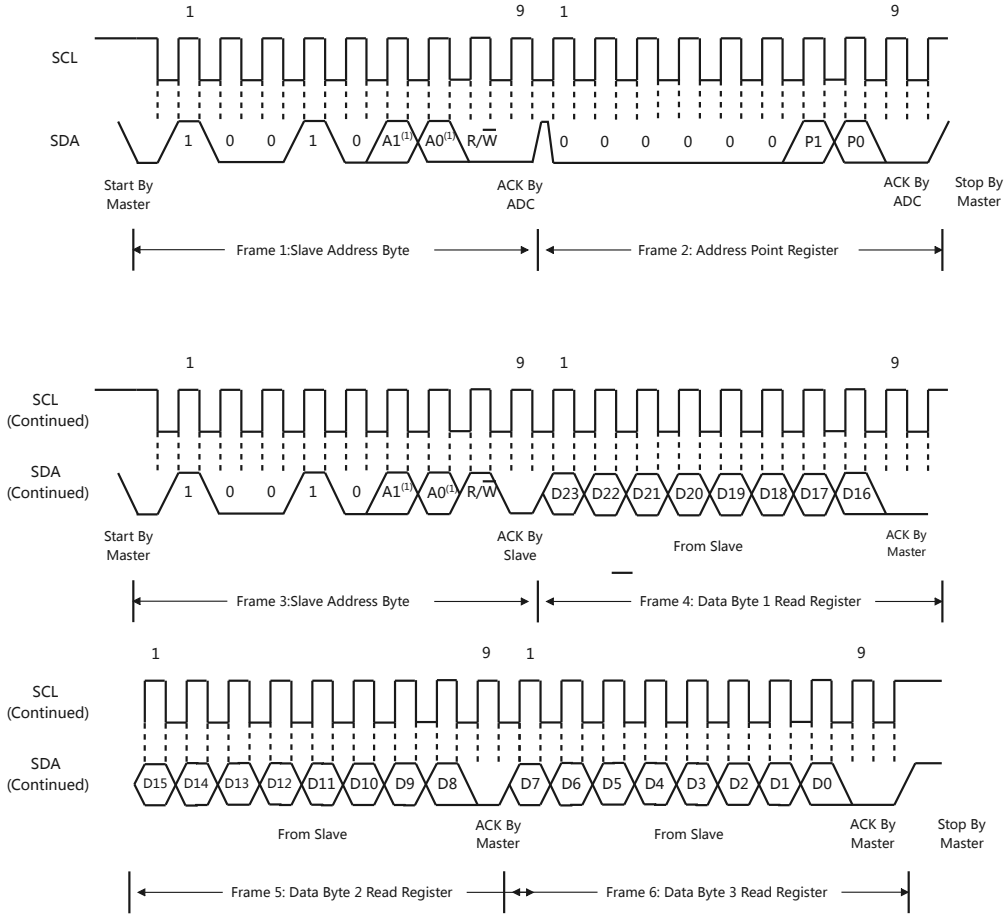
To access a specific register within the TPC6200I, the master initiates the process by writing the appropriate value to the register address pointer bits P[1:0] in the Address Pointer register. This action takes place immediately after transmitting the slave address byte, followed by the low R/$\overline{W}$ bit, and upon receiving a successful acknowledgment from the slave. Once the Address Pointer register is written with the desired value, the slave acknowledges this action, after which the master concludes the process by issuing either a STOP or a repeated START condition on the bus.

When reading from the ADC, the register to be read is determined by the previous value written to bits P[1:0]. To switch to a different register for reading, a new value must be written to P[1:0]. This is achieved by the master issuing a slave address byte with the R/$\overline{W}$ bit low, followed by the Address Pointer register byte. No additional data transmission is required, and the master can then conclude the operation by issuing a STOP condition. Subsequently, the master can initiate a new read operation by issuing a START condition followed by the slave address byte with the R/$\overline{W}$ bit high. If repeated reads from the same register are required, there's no need to resend the Address Pointer register each time, as the TPC6200I retains the value of P[1:0] until it's altered by a subsequent write operation. However, for every write operation targeting a different register, the Address Pointer register must be updated accordingly.



(1) The values of A0 and A1 are determined by the ADDR pin.

Figure 14. Timing Diagram for Writing to TPC6200I



(1) The values of A0 and A1 are determined by the ADDR pin.
(2) Master can leave SDA high to terminate a single-byte read operation.
(3) Master can leave SDA high to terminate a two-byte read operation.

Figure 15. Timing Diagram for Reading from TPC6200I

Data Format

The TPC6200I outputs data in a 24-bit binary two's complement format. For a positive full-scale (+FS) input, the output code is 7FFFFFh, while a negative full-scale (−FS) input results in an output code of 800000h. The output codes clip at these values for signals that exceed the full-scale range. The table below provides a summary of the ideal output codes corresponding to different input signals.

Table 14. Input Signal versus Ideal Output Code

INPUT SIGNAL, VIN (AIN_P – AIN_N)	IDEAL OUTPUT CODE (1)
≥ FS (2^{23} – 1) / 2^{23}	7FFFFFh
FS / 2^{23}	000001h
0	000000h
−FS / 2^{23}	FFFFFFh
≤ −FS	800000h

(1) Excludes the effects of noise, INL, offset, and gain errors.

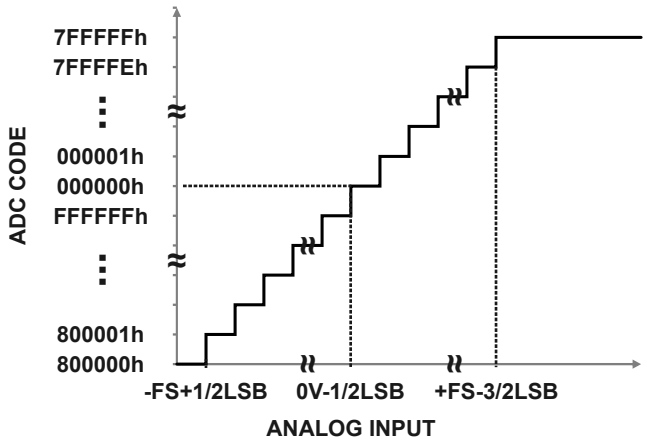


Figure 16. Code Transition Diagram

Register Summary

The TPC6200I features four accessible registers via I²C in the address pointer register. The Conversion register is the result of the most recent conversion, while the Config register sets operating modes and inquiries about the device's status. The other registers Lo_thresh and Hi_thresh are configurable for the comparator threshold voltage.

Address Pointer Register [reset = N/A]

All four registers are accessed by writing to the Address Pointer register.

Table 15. Address Pointer Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	P[1:0]	
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. Address Point Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	Reserved	W	0h	Always write 0h
1:0	P[1:0]	W	0h	Register address pointer 00 : Conversion register 01 : Config register 10 : Lo_thresh register 11 : Hi_thresh register

Conversion Register (P[1:0] = 0h) [reset = 0000h]

The 24-bit Conversion register stores the results of the latest conversion in binary twos complement format. After power-up, the register is reset to 0 and retains this value until the initial conversion is finished. Refer to the table below for the register format.

Table 17. Conversion Register

23	22	21	20	19	18	17	16
D23	D22	D21	D20	D19	D18	D17	D16
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
D15	D14	D13	D12	D11	D10	D9	D8
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
D7	D6	D5	D4	D3	D2	D1	D0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. Conversion Register Field Descriptions

Bit	Field	Type	Reset	Description
23:0	D[23:0]	R	000000h	24-bit conversion result

Config Register (P[1:0] = 1h) [reset = 858320h]

The 24-bit Config register can be configured to set the TPC6200I operating mode, input selection, data rate, full-scale range, and comparator mode. The register format is shown in the table below.

Table 19. Config Register

23	22	21	20	19	18	17	16
OS	MUX[2:0]			PGA[2:0]			MODE
R/W-1h	R/W-0h			R/W-2h			R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DR[2:0]			COMP_MODE	COMP_POL	COMP_LAT	COMP_QUE[1:0]	
R/W-4h			R/W-0h	R/W-0h	R/W-0h	R/W-3h	
7	**6**	**5**	**4**	**3**	**2**	**9**	**8**
DR_Boost[1:0]		Global Chop	Reserved				
R/W-0h		R/W-1h	R/W-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. Config Register Field Descriptions

Bit	Field	Type	Reset	Description
23	OS	R/W	1h	**Operation status or Single-shot conversion start** This bit is used to configure the device operation status or start a single conversion. OS can only be written when in power-down state and has no effect when a conversion is ongoing. When writing: 0 = No effect 1 = Start a single conversion (when in power-down state) When reading: 0 = Device is currently performing a conversion 1 = Device is not currently performing a conversion
22:20	MUX[2:0]	R/W	0h	**Input multiplexer configuration** These bits configure the input multiplexer. 000 = AIN_P is AIN0 and AIN_N is AIN1 (default) 001 = AIN_P is AIN0 and AIN_N is AIN3 010 = AIN_P is AIN1 and AIN_N is AIN3 011 = AIN_P is AIN2 and AIN_N is AIN3 100 = AIN_P is AIN0 and AIN_N is GND 101 = AIN_P is AIN1 and AIN_N is GND 110 = AIN_P is AIN2 and AIN_N is GND 111 = AIN_P is AIN3 and AIN_N is GND
19:17	PGA[2:0]	R/W	2h	**Programmable gain amplifier configuration** These bits configure the programmable gain amplifier. 000 = FSR is ±6.144 V (1) 001 = FSR is ±4.096 V (1) 010 = FSR is ±2.048 V (default)

Bit	Field	Type	Reset	Description
				011 = FSR is ±1.024 V 100 = FSR is ±0.512 V 101 = FSR is ±0.256 V 110 = FSR is ±0.256 V 111 = FSR is ±0.256 V
16	MODE	R/W	1h	**Device operating mode** This bit controls the TPC6200I operating mode. 0 = Continuous-conversion mode 1 = Power-down and single-shot mode (default)
15:13	DR[2:0]	R/W	4h	**Data rate** These bits control the data-rate setting. 000 = 64 SPS 001 = 128 SPS 010 = 256 SPS 011 = 512 SPS 100 = 1024 SPS (default) 101 = 2 kSPS 110 = 4 kSPS 111 = 8 kSPS
12	COMP_MODE	R/W	0h	**Comparator mode** This bit configures the ADC comparator operation mode. 0 = Traditional comparator (default) 1 = Window comparator
11	COMP_POL	R/W	0h	**Alert polarity** This bit sets the alert polarity of the ALERT/RDY pin 0 = Active low (default) 1 = Active high **Ready polarity** This bit sets the ready polarity of the ALERT/RDY pin in continuous-conversion mode 0 = Active low (default) 1 = Active high This bit sets the ready polarity of the ALERT/RDY pin in single-shot mode 0 = Active high (default) 1 = Active low
10	COMP_LAT	R/W	0h	**Latching comparator** This bit sets whether the ALERT/RDY pin latches after being asserted or clears after conversions are within the margin of the upper and lower threshold values. 0 = Nonlatching comparator. The ALERT/RDY pin does not latch when asserted (default). 1 = Latching comparator function ensures that the ALERT/RDY pin remains latched until either the conversion data is read by the master or the master sends an appropriate

Bit	Field	Type	Reset	Description
				SMBus alert response. In response, the device asserts its address, becoming the lowest address currently asserting the ALERT/RDY bus line
9:8	COMP_QUE[1:0]	R/W	3h	**Comparator queue and disable** These bits serve dual functions. When configured as 11, the comparator is deactivated, and the ALERT/RDY pin enters a high-impedance state. In any other configuration, the ALERT/RDY pin and the comparator function are enabled. The specific value set determines the number of consecutive conversions surpassing either the upper or lower threshold required to trigger the assertion of the ALERT/RDY pin. 00 = Assert after one conversion 01 = Assert after two conversions 10 = Assert after four conversions 11 = Disable comparator and set ALERT/RDY pin to high-impedance (default)
7:6	DR_Boost[1:0]	R/W	0h	**Data rate boost** These bits control the data-rate boost setting. 01 = 16 kSPS 10 = 32 kSPS 11 = 32 kSPS
5	Global Chop Mode	R/W	1h	**Global chop mode** These bits set the global chop mode. 1 = Enable global chop (default) 0 = Disable global chop
4:0	Reserved	R/W	0h	**Reserved** Writing either 0 or 1 to this bit has no effect. Always reads back 0.

(1) This parameter expresses the full-scale range of the ADC scaling. Do not apply more than VDD + 0.3 V to this device.

Lo_thresh (P[1:0] = 2h) [reset = 8000h]

The lower threshold values utilized by the comparator are stored in two 16-bit registers in two's complement format. As the comparator functions as a digital comparator, it necessitates updating the values in these registers whenever there is a modification in the PGA (Programmable Gain Amplifier) settings.

Enabling the conversion-ready function of the ALERT/RDY pin involves setting the MSB of the Hi_thresh register to 1 and the MSB of the Lo_thresh register to 0. To utilize the comparator function of the ALERT/RDY pin effectively, it's imperative that the value in the Hi_thresh register always surpasses that in the Lo_thresh register. When configured in RDY mode, the ALERT/RDY pin outputs the OS bit in single-shot mode and delivers a continuous-conversion ready pulse in continuous-conversion mode.

Table 21. Lo_thresh Register

15	14	13	12	11	10	9	8
Lo_thresh15	Lo_thresh14	Lo_thresh13	Lo_thresh12	Lo_thresh11	Lo_thresh10	Lo_thresh9	Lo_thresh8
R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Lo_thresh7	Lo_thresh6	Lo_thresh5	Lo_thresh4	Lo_thresh3	Lo_thresh2	Lo_thresh1	Lo_thresh0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Hi_thresh (P[1:0] = 2h) [reset = 8000h]

The higher threshold values utilized by the comparator are stored in two 16-bit registers in two's complement format. As the comparator functions as a digital comparator, it necessitates updating the values in these registers whenever there is a modification in the PGA (Programmable Gain Amplifier) settings.

Enabling the conversion-ready function of the ALERT/RDY pin involves setting the MSB of the Hi_thresh register to 1 and the MSB of the Lo_thresh register to 0. To utilize the comparator function of the ALERT/RDY pin effectively, it's imperative that the value in the Hi_thresh register always surpasses that in the Lo_thresh register. When configured in RDY mode, the ALERT/RDY pin outputs the OS bit in single-shot mode and delivers a continuous-conversion ready pulse in continuous-conversion mode.

Table 22. Hi_thresh Register

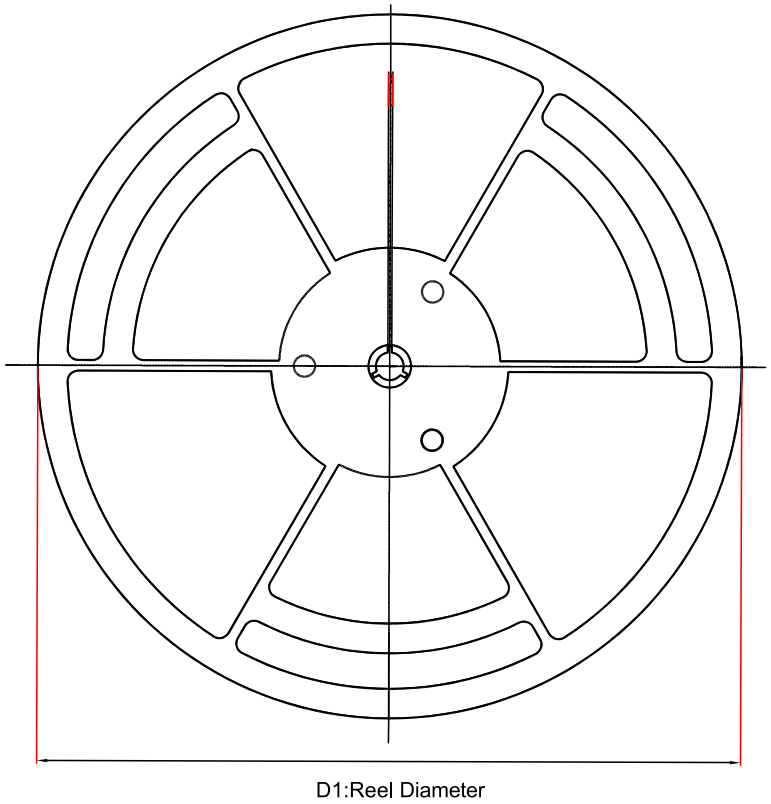
15	14	13	12	11	10	9	8
Hi_thresh15	Hi_thresh14	Hi_thresh13	Hi_thresh12	Hi_thresh11	Hi_thresh10	Hi_thresh9	Hi_thresh8
R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Hi_thresh7	Hi_thresh6	Hi_thresh5	Hi_thresh4	Hi_thresh3	Hi_thresh2	Hi_thresh1	Hi_thresh0
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

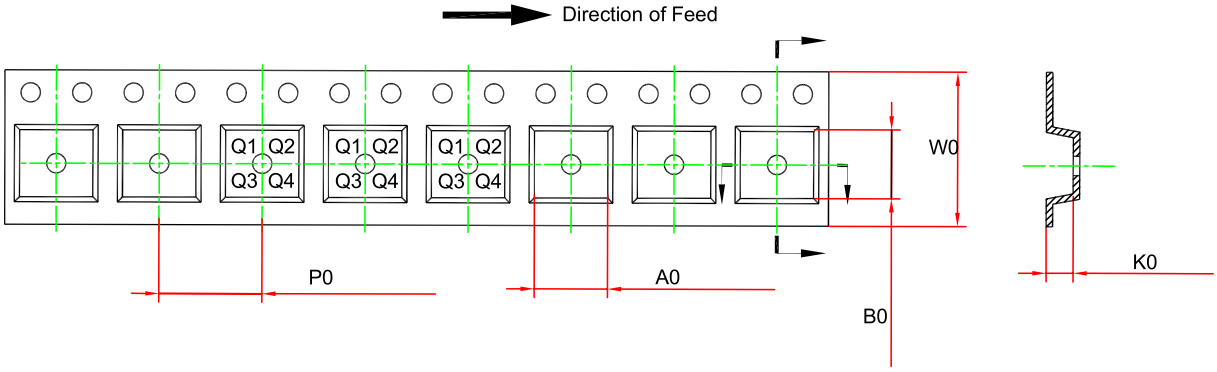
LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. Lo_thresh and Hi_thresh Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	Lo_thresh[15:0]	R/W	8000h	Low threshold value
15:0	Hi_thresh[15:0]	R/W	7FFFh	Hi threshold value

Tape and Reel Information



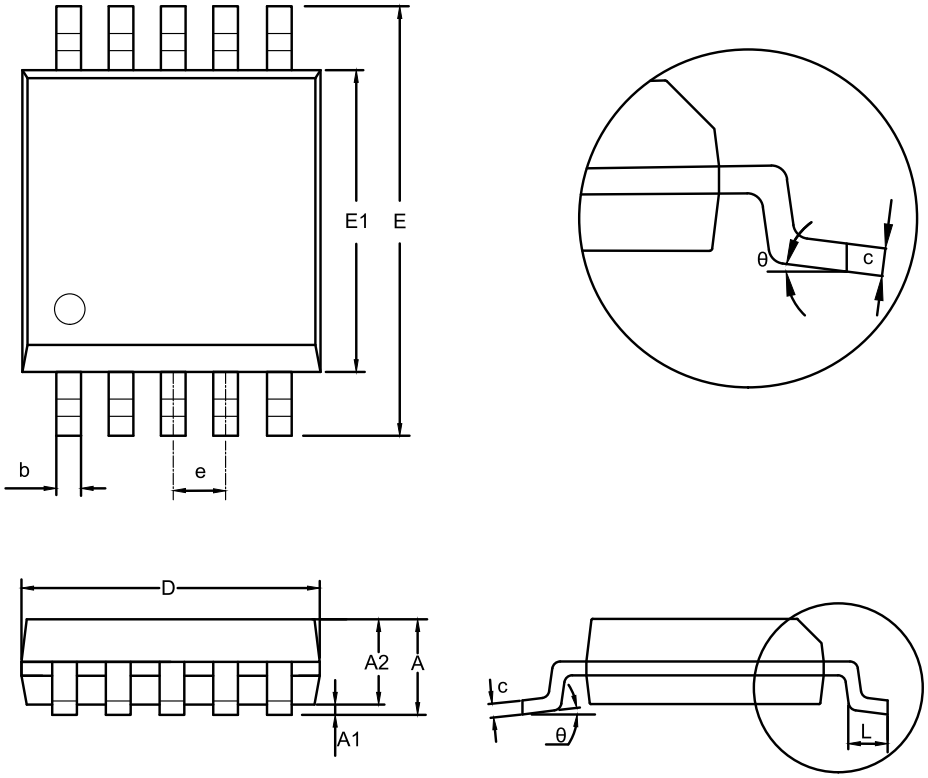


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPC6200I-VS2R	MSOP10	330	17.6	5.3	3.4	1.4	8	12	Q1

Package Outline Dimensions

MSOP10

Package Outline Dimensions VS2(MSOP-10-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	1.100	0.031	0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	4.700	5.100	0.185	0.201
E1	2.900	3.100	0.114	0.122
e	0.500 BSC		0.020 BSC	
L	0.400	0.800	0.016	0.031
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPC6200I-VS2R	−40 to 125°C	MSOP10	6200I	2	T&R, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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