18-Bit SAR ADC with Fully Differential Inputs

Features

- 18-bit SAR ADC without Zero Latency
  - Throughput Speed: 300 KSPS
- Unipolar, Differential Analog Input
  - -VREF to VREF
- External VREF
  - 2.5 V to VDD
- High Linearity
  - DNL: ±0.6 LSB Typical
  - INL: ±2 LSB Typical
  - THD: -110 dB Typical at 1 kHz
- High Dynamic Range and Noise Performance
  - SNR: 96 dB Typical at 1 kHz
  - Dynamic Range: 96 dB Typical at 1 kHz
- Serial Interface:
  - SPI Compatible
- Daisy-Chain is Supported
- Wide Operating Temperature Range:
  - −40°C to +125°C
- Package: MSOP10

Applications

- Data Acquisitions
- Instruments
- Industry Measurement and Control
- Medical Equipment
- Automatic Test Equipment

Description

The TPC5180 is an 18-bit analog-to-digital converter (ADC). The device supports unipolar, differential input, and the input range -VREF ~VREF with a common mode voltage of VREF/2.

The device operates with a 2.5 V to VDD external reference.

The device offers an SPI-compatible interface and supports daisy-chain operation for multiple device applications.

The devices also offer an optional busy indicator bit, which can be used to synchronize with the host.

Typical Application Circuit

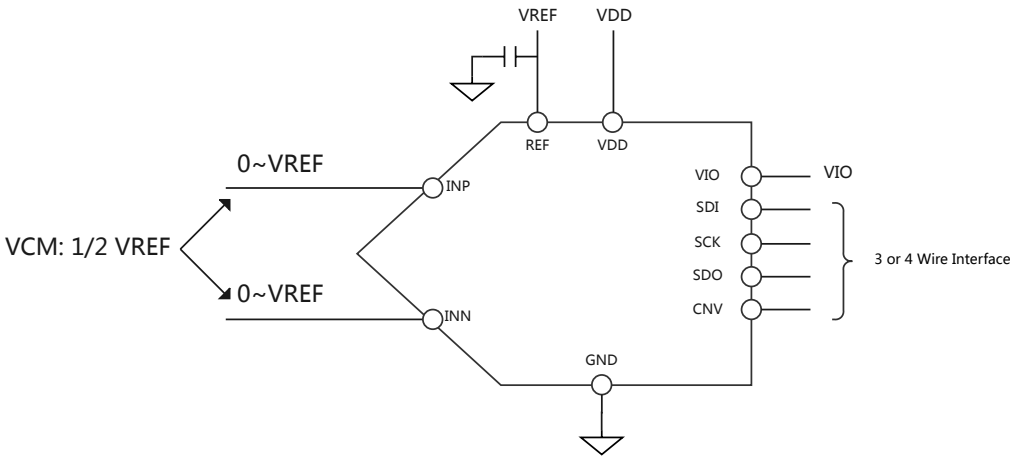


Table of Contents

Product Family Table

Order Number	Resolution	Input Range	Throughput Speed	Package
TPC5180-VS2R	18	-VREF~VREF Fully Differential	300K SPS	MSOP10
TPC5160-VS2R	16	-VREF~VREF Fully Differential	600K SPS	MSOP10
TPC5161-VS2R	16	0~VREF Pseudo Differential	600K SPS	MSOP10

Revision History

Date	Revision	Notes
2023-09-26	Rev.A.0	Initial release.

Pin Configuration and Functions

TPC5180
MSOP10 Package
Top View

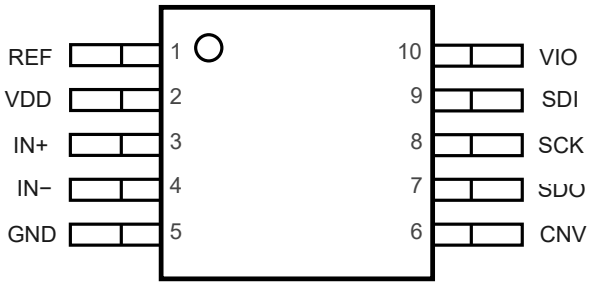


Table 1. Pin Functions: TPC5180

Pin		I/O	Description
No.	Name		
1	REF	I	Reference voltage.
2	VDD	O	Power supply.
3	IN+	O	Positive analog Input.
4	IN-	I	Negative analog Input.
5	GND	–	Power Ground.
6	CNV		Conversion input. It initiates the conversions of the device and selects the interface mode together with SDI. 1. Chain mode: SDI is low during CNV rising edge. 2. $\overline{CS}$ mode: SDI is high during CNV rising edge.
7	SDO		Serial Data output.
8	SCK		Serial Data clock.
9	SDI		Serial Data input. It selects the serial mode together with CNV.
10	VIO		Digital interface power.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Analog Voltage	IN+, IN- to GND	−0.3	VDD + 0.3	V
	VREF to GND	−0.3	VDD + 0.3	V
Digital Voltage	Digital Inputs to GND	−0.3	VIO + 0.3	V
	Digital Outputs to GND	−0.3	VIO + 0.3	V
Supply Voltage	VDD to GND	−0.3	6	V
	VIO to GND	-0.3	VDD+0.3	V
T_J	Maximum Junction Temperature	−40	150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
VDD	4.5	5	5.5	V
V_{REF}	3	5	VDD	V
VIO	1.71	3.3	VDD	V

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
MSOP10	125	48	°C/W

Electrical Characteristics

All test conditions: VDD = 5 V, VIO = 1.71 V to 5 V, T_A = −40°C to +125°C, unless otherwise noted.

Parameter	Test conditions		Min	Typ	Max	Unit
AC Accuracy(1)						
SNR	fin = 1 kHz	REF = 5 V	93	96		dB
		REF = 3 V		92		dB
SINAD	fin = 1 kHz	REF = 5 V		95		dB
		REF = 3 V		91.5		dB
Dynamic Range	fin = 1 kHz	REF = 5 V		96		dB
		REF = 3 V		92		dB
THD	fin = 1 kHz	REF = 5 V		-110		dB
SFDR	fin = 1 kHz	REF = 5 V		-108		dB
DC Accuracy						
Resolution	NO missing code		18			Bits
DNL	REF = 5 V		-0.99	±0.6	1.1	LSB
	REF = 3 V			±0.6		
INL	REF = 5 V		-8	±2	8	LSB
	REF = 3 V			±2		
Gain Error	REF = 5 V		-36	±16	36	LSB
Gain Error Drift				±0.35		ppm/°C
Zero Code Error	REF = 5 V		-18	±1.5	18	LSB
Zero Code Error Drift				±0.35		ppm/°C
Power Supply Sensitivity	AVDD +/-5%			70		dB
Analog Input						
Voltage Range	IN+ - IN-		-VREF		VREF	V
Common Mode Input Range (1)			VREF/2 – 0.1		VREF/2 + 0.1	
Operating Input Voltage	IN+		-0.1		VREF+0.1	V
	IN-		-0.1		VREF+0.1	V
Analog Input CMRR	fin = 10 kHz			84		dB
Leakage Current at 25℃				1		nA
Input Capacitance				33		pF
Throughput						
Conversion Rate	VIO ≥ 2.3 V up to 85°C, VIO ≥3.3 V above 85°C up to 125°C		0	0.3		MHz
	VIO ≥ 1.71 V, VIO ≤ 3.3 V up to 125°C			0.3		MHz
Acquisition Time				1.7		us

Parameter	Test conditions		Min	Typ	Max	Unit
Conversion time				1.63		us
Transient Response				1.7		us
Reference						
REFERENCE Voltage Range			2.5		VDD	V
REFERENCE Load Current	300 KSPS, REF = 5 V			130		uA
Sampling Dynamics						
-3dB BW				20		MHz
Aperture Delay				4		ns
Digital Input						
V_{IH}	VIO > 3 V		0.7*VIO			V
V_{IL}	VIO > 3 V				0.3*VIO	V
V_{IH}	VIO <= 3 V		0.7*VIO			V
V_{IL}	VIO <= 3 V				0.3*VIO	V
I_{IH}	input current		-1		1	uA
I_{IL}	input current		-1		1	uA
Digital Output						
Data Format			Serial 18bit straight binary			
Pipeline Delay			Conversion results available immediately after completed conversion			
V_{OH}	output logic high voltage	current source = 500 uA	VIO-0.2			V
V_{OL}	output logic low voltage	current sink = 500 uA			0.2	V
Power Supply						
V_{DD}			4.5		5.5	V
V_{IO}			1.8		VDD	V
Standby Current				3200		uA
V_{DD} Current (I_{VDD})	operating	fs = 1 kHz		3		mA
	operating	fs = 300 kHz		3.5		mA

(1) Parameters are provided by lab bench test and design simulation.

Timing Requirements (1)

All test conditions: at V_{DD} = 5 V, V_{IO} = 1.71 V to 5 V, T_A= −40°C to +125°C, C_{load} = 20 pF, unless otherwise noted.

Parameter		Min	Typ	Max	Unit
t_{CONV}	Conversion Time: CNV Rising Edge to Data Available	1540	1620	1700	ns
t_{ACQ}	Acquisition Time	1630			ns
t_{CYC}	Time between Conversions	3330			ns
t_{CNVH}	CNV Pulse Width (CS Mode)	9			ns
t_{SCK}	SCK Period (CS Mode)				ns
	VIO above 4.5 V	16			ns
	VIO above 3.3 V	17			ns
	VIO above 1.7 V	25			ns
t_{SCK}	SCK Period (Chain Mode)				ns
	VIO above 4.5 V	16			ns
	VIO above 3.3 V	17			ns
	VIO above 1.7 V	25			ns
t_{SCKL}	SCK Low Time	5			ns
t_{SCKH}	SCK High Time	5			ns
t_{HSDO}	SCK Falling Edge to Data Remains Valid	3.5			ns
t_{DSDO}	SCK Falling Edge to Data Valid Delay				
	VIO above 4.5 V			14	ns
	VIO above 3.3 V			15	ns
	VIO above 1.7 V			23	ns
t_{EN}	CNV or SDI Low to SDO D15 MSB Valid (CS Mode)				
	VIO above 4.5 V			12	
	VIO above 3.3 V			13	ns
	VIO above 1.7 V			21	ns
t_{DIS}	CNV or SDI High or Last SCK Falling Edge to SDO High Impedance (CS Mode)			10	ns
$t_{SSDICNV}$	SDI Valid Setup Time from CNV Rising Edge	8			ns
$t_{HSDICNV}$	SDI Valid Hold Time from CNV Rising Edge (CS Mode)	0			
$t_{HSDICNV}$	SDI Valid Hold Time from CNV Rising Edge (Chain Mode)	0			ns
$t_{SSCKCNV}$	SDI Valid Hold Time from CNV Rising Edge (Chain Mode)	8			ns
$t_{HSCKCNV}$	SCK Valid Setup Time from CNV Rising Edge (Chain Mode)	0.5			ns
$t_{SSDISCK}$	SCK Valid Hold Time from CNV Rising Edge (Chain Mode)	0			ns
$t_{HSDISCK}$	SDI Valid Setup Time from SCK Falling Edge (Chain Mode)	0.5			ns
$t_{DSDOSDI}$	SDI Valid Hold Time from SCK Falling Edge (Chain Mode)			9	ns

(1) Parameters are provided by design simulation.

Typical Performance Characteristics

All test condition: VDD = 5.0 V, VREF = 5.0 V，VIO= 3.3 V，T_A = +25°C, unless otherwise noted.

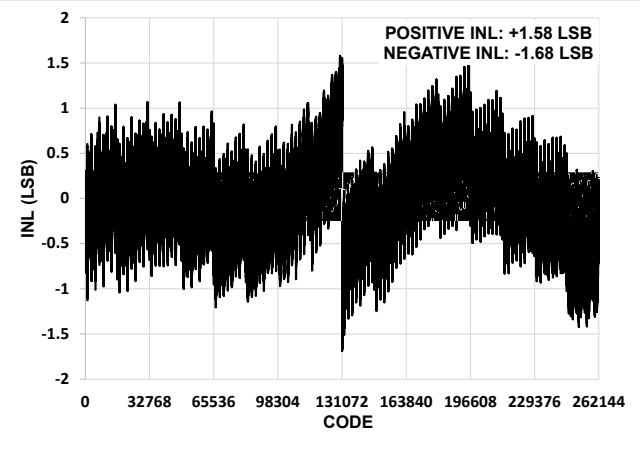


Figure 1. Integral Nonlinearity vs. Code

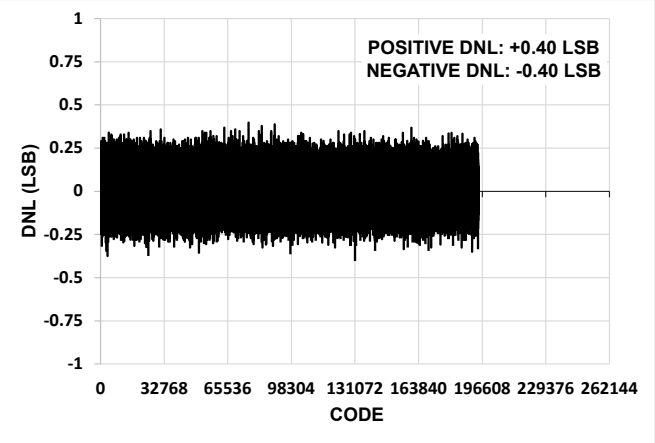


Figure 2. Differential Nonlinearity vs. Code

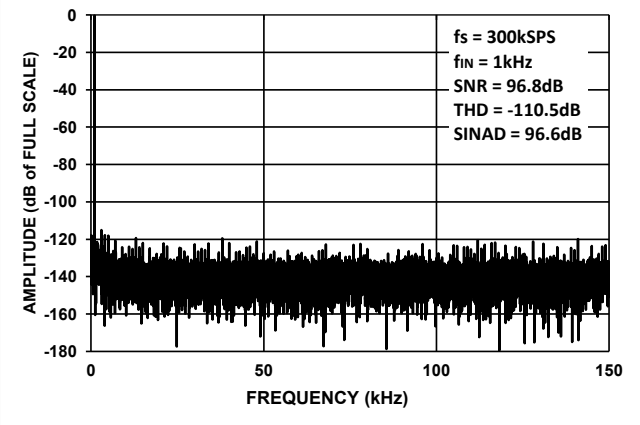


Figure 3. FFT Plot

Detailed Description

Overview

TPC5180 is an 18-bit successive approximation register (SAR) ADC. The device is capable to convert analog input into digital output without latency or pipeline delay, so it is ideal for multiple channel applications.

When a conversion is initiated, the analog input is sampled on internal capacitor, and then converted based on charge redistribution with the internal clock. During conversion, the input is disconnected from the internal capacitor.

After conversion, the device reconnects the sampling capacitors to input pins, and enters acquisition phase.

Functional Block Diagram

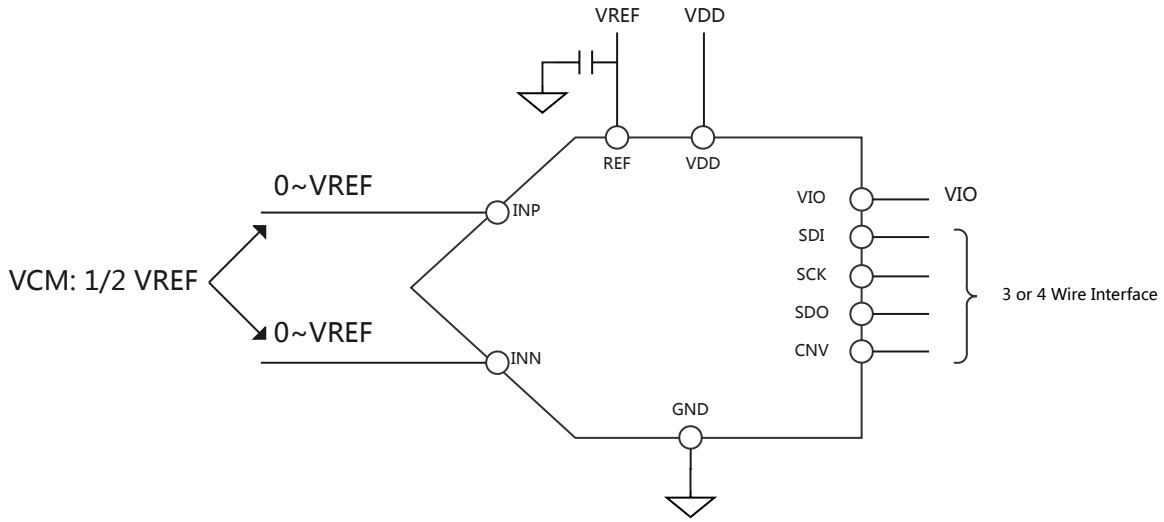


Figure 4. TPC5180 Block Diagram

Feature Description

Analog Input

The following is the equivalent input sampling circuit. The sampling switch is represented by a resistance in series with the ideal switch. The electrostatic discharge (ESD) protection diodes from both analog inputs are also shown in the figure.

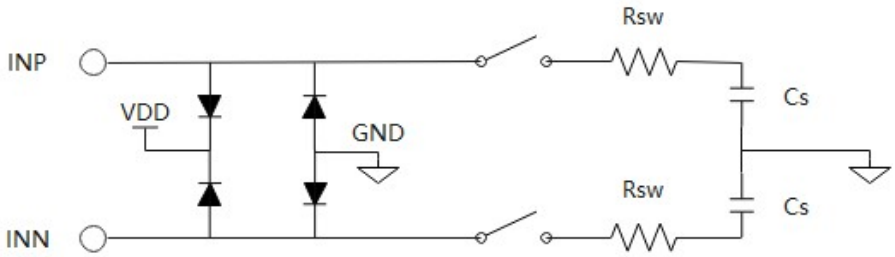


Figure 5. Equivalent Input Sampling Circuit

Reference

The device operates with an external reference voltage. During the conversion process, internal capacitors are switched onto the reference terminal, and a dynamic charge is required. The switching frequency is proportional to the internal conversion clock frequency. A reference driver circuit is required to support the dynamic charge so that the noise and linearity performance of the device is not degraded.

ADC Transfer Function

The device is a unipolar, differential input device, and the output is in twos complement format.The transfer equation is shown in the following table:

Description	Analog Input	Digital output Code (Hex)
Full scale range	2*VREF	-
Least Significant Bit (LSB)	2*VREF/262144	-
Positive full scale	VREF – 1 LSB	7FFF
Midscale	0 V	0000
Midscale – 1 LSB	0 – 1LSB	FFFF
Negative full scale	-VREF	8000

Device Function Modes

The device offers $\overline{CS}$ mode and Daisy-chain mode for interfacing with the host.

The mode in which the device operates depends on the SDI level when the CNV rising edge occurs. The device operates in $\overline{CS}$ mode if SDI is high at the CNV rising edge. If SDI is low at the CNV rising edge, or if SDI and CNV are connected, the device operates in daisy-chain mode.

In $\overline{CS}$ mode, the device is compatible with SPI hosts. This interface can use a 3-wire or 4-wire interface. The 3-wire interface, using the CNV, SCK, and SDO signals, minimizes the wiring connections and is useful for isolation applications. The 4-wire interface, using the SDI, CNV, SCK, and SDO signals, allows the user to sample the analog input independent of the serial interface timing, and is useful to control an individual device while having multiple similar devices on board.

In daisy-chain mode, multiple devices can be cascaded on a single data line similar to a shift register. This mode is useful to reduce component count and signal traces on the board.

In both modes, the device can either operate with or without a busy indicator, where the busy indicator is a bit preceding the output data bits that can be used to interrupt the digital host and trigger the data transfer.

$\overline{CS}$ Mode

The device operates in $\overline{CS}$ mode if SDI is high at the CNV rising edge. There are four different interface options available in this mode: 3-wire $\overline{CS}$ mode without a busy indicator, 3-wire $\overline{CS}$ mode with a busy indicator, 4-wire $\overline{CS}$ mode without a busy indicator, and 4-wire $\overline{CS}$ mode with a busy indicator.

3-wire $\overline{CS}$ Mode without Busy Indicator

This mode is useful when a single ADC is connected to an SPI-compatible digital host.

In this mode, SDI can be connected to VIO. A CNV rising edge samples the input signal, causes the device to enter a conversion phase, and SDO is forced to 3-state. Conversion is done with an internal clock and continues regardless of the state of CNV. So CNV can be pulled low then to select other devices on the board.

However, CNV must return and hold high before the conversion time elapses. A high level on CNV at the end of the conversion ensures the device does not generate a busy indicator.

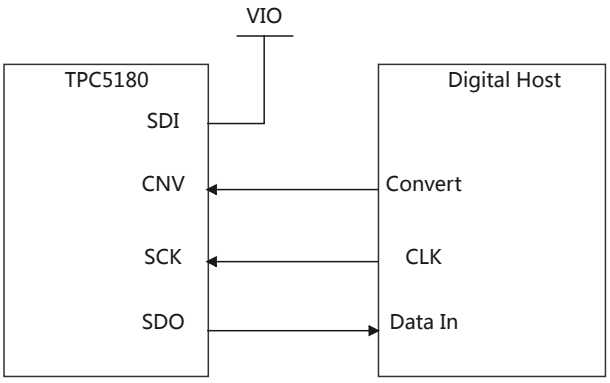


Figure 6. Connection Diagram: 3-Wire $\overline{CS}$ Mode without Busy Indicator

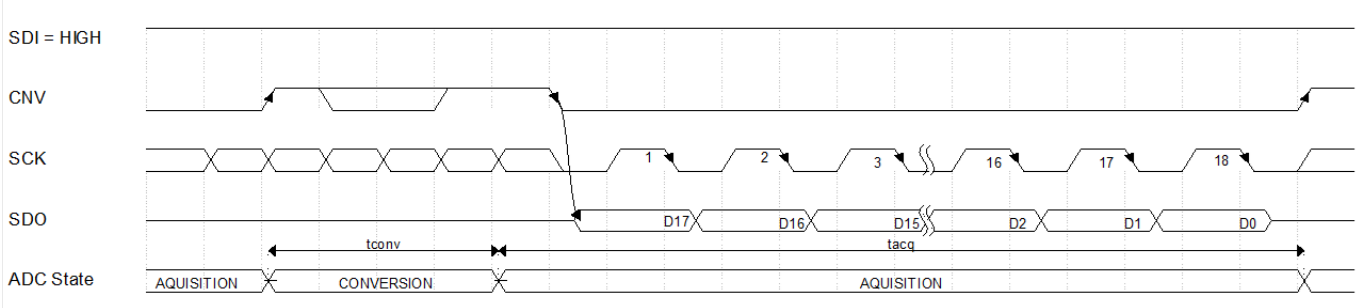


Figure 7. Timing Diagram: 3-Wire $\overline{CS}$ Mode without Busy Indicator

On the CNV falling edge, SDO comes out of 3-state and the device outputs the MSB of the data at first, and then low data bits on subsequent SCK falling edges.

The data is valid on both SCK edges. The rising edge can be used to capture the data, and the SCK falling edge allows a faster reading rate if there is an acceptable hold time.

SDO goes to 3-state after the 18th SCK falling edge or when CNV goes high, whichever occurs first.

3-wire $\overline{CS}$ Mode with a Busy Indicator

This mode is useful when a single ADC is connected to an SPI-compatible digital host and an interrupt-driven data transfer is required.

In this mode, SDI can be connected to VIO. A CNV rising edge samples the input signal, causes the device to enter a conversion phase, and SDO is forced to 3-state.

Conversion is done with an internal clock and continues regardless of the state of CNV. So CNV can be pulled low then to select other devices on the board.

A pull-up resistor on the SDO pin ensures that $\overline{CS}$ pin of digital host is held high when SDO is in 3-state.

However, CNV must be pulled low before conversion time elapses. A low level of CNV at the end of conversion ensures the device generates a busy indicator.

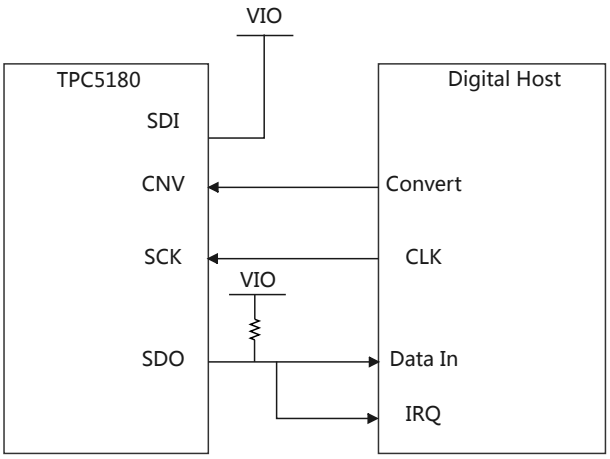


Figure 8. Connection Diagram: 3-Wire $\overline{CS}$ Mode with a Busy Indicator

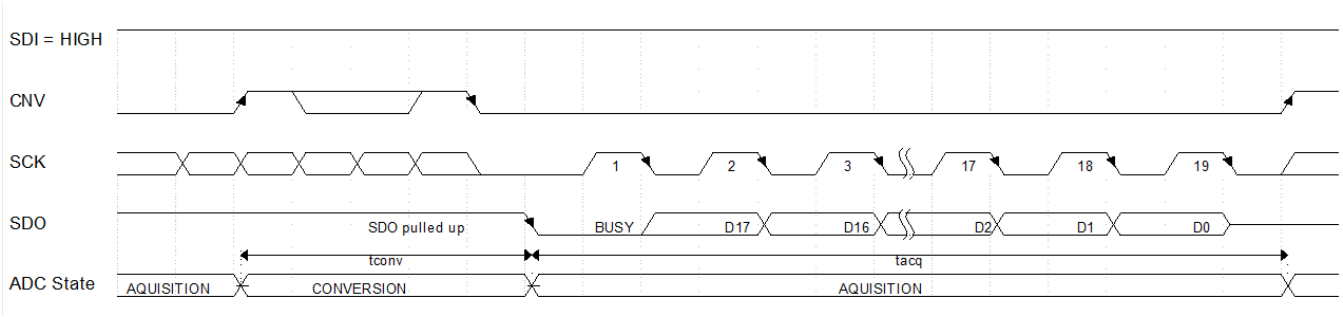


Figure 9. Timing Diagram: 3-Wire $\overline{CS}$ Mode with a Busy Indicator

When the conversion completes, the device enters an acquisition state. SDO comes out of 3-state, and outputs a busy indicator bit (low level). This feature provides a high-to-low transition on the $\overline{CS}$ pin of the digital host.

Then the data bits are clocked out on the subsequent SCLK falling edges, MSB first.

The data is valid on both SCK edges. The rising edge can be used to capture the data, and SCK falling edge allows a faster reading rate if there is an acceptable hold time.

SDO goes to 3-state after the 17th SCK falling edge or when CNV goes high, whichever occurs first.

4-wire $\overline{CS}$ Mode without Busy Indicator

This mode is useful when one or more ADCs are connected to an SPI-compatible digital host. The following is the connection diagram of the two ADCs.

In this mode, SDI is controlled by the digital host and functions as $\overline{CS}$.

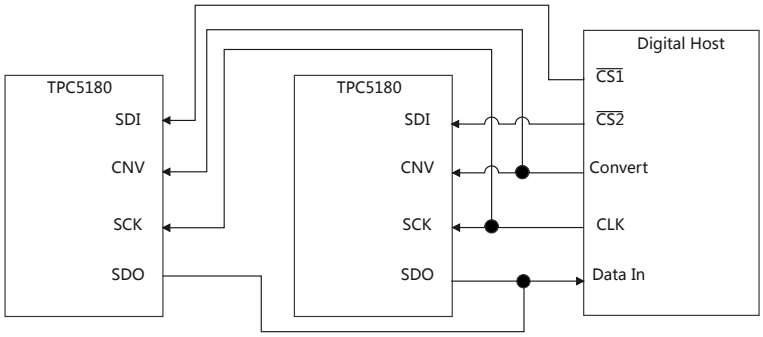


Figure 10. Connection Diagram: Two ADCs with 4-Wire $\overline{CS}$ Mode without Busy Indicator

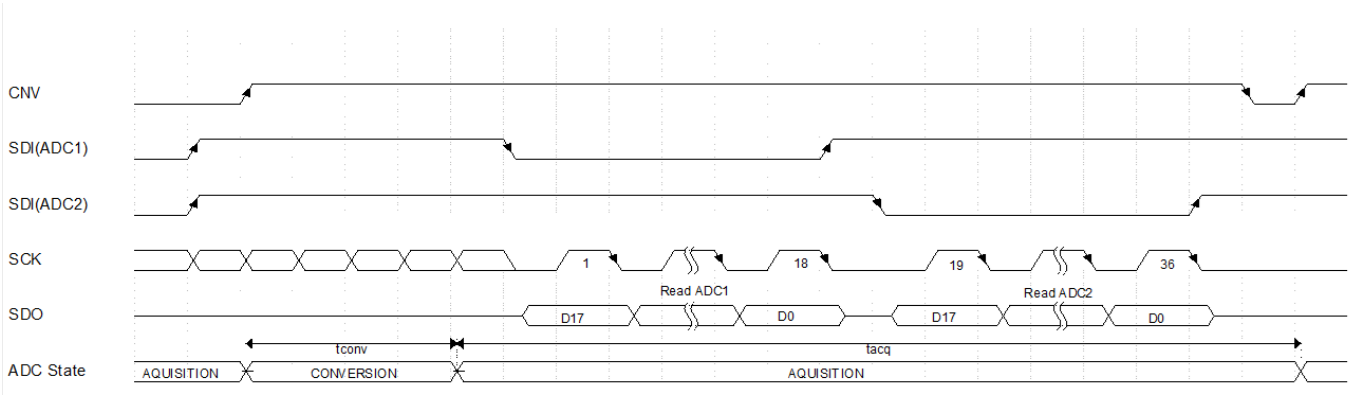


Figure 11. Timing Diagram: Two ADCs with 4-Wire $\overline{CS}$ Mode without Busy Indicator

When SDI is high, a CNV rising edge samples the input signal, causes the device to enter a conversion phase, and forces SDO to 3-state.

In this mode, CNV must be held high from the start of the conversion until all data bits are read.

Conversion is done with the internal clock regardless of the state of SDI. So SDI (functioning as $\overline{CS}$) can be pulled low to select other devices on the board.

However, SDI must return and hold high before the conversion time elapses. A high level on SDI at the end of the conversion ensures the device does not generate a busy indicator.

On the SDI falling edge, SDO comes out of 3-state and the device outputs the MSB of the data at first, and then low data bits on subsequent SCK falling edges.

The data is valid on both SCK edges. The rising edge can be used to capture the data, and the SCK falling edge allows a faster reading rate if there is an acceptable hold time.

SDO goes to 3-state after the 18th SCK falling edge or when SDI goes high, whichever occurs first.

When multiple devices are connected together on the same data bus, the SDI of the second device (functioning as $\overline{CS}$ for the second device) can go low after the first device data are read, and the SDO of the first device is in 3-state.

Care must be taken so that CNV and SDO of the devices are not low together during the read cycle.

4-Wire $\overline{CS}$ Mode with Busy Indicator

This mode is most useful when a single ADC is connected to a digital host and an interrupt-driven data transfer is desired.

In this mode, SDI is controlled by the digital host and functions as $\overline{CS}$.

A pull-up resistor on SDO pin ensures that $\overline{CS}$ pin of digital host is held high when SDO is in 3-state.

When SDI is high, a CNV rising edge samples the input signal, causes the device to enter a conversion phase, and forces SDO to 3-state.

In this mode, CNV must be held high from the start of the conversion until all data bits are read.

Conversion is done with the internal clock regardless of the state of SDI. So SDI (functioning as $\overline{CS}$) can be pulled low to select other devices on the board.

However, CNV must be pulled low before conversion time elapses. A low level of CNV at the end of conversion ensures the device generates a busy indicator.

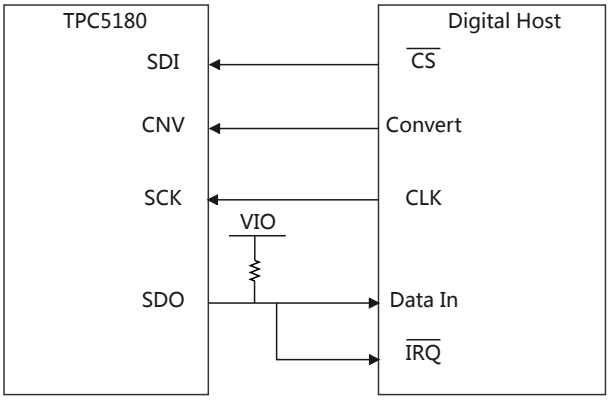


Figure 12. Connection Diagram: 4-wire $\overline{CS}$ Mode with a Busy Indicator

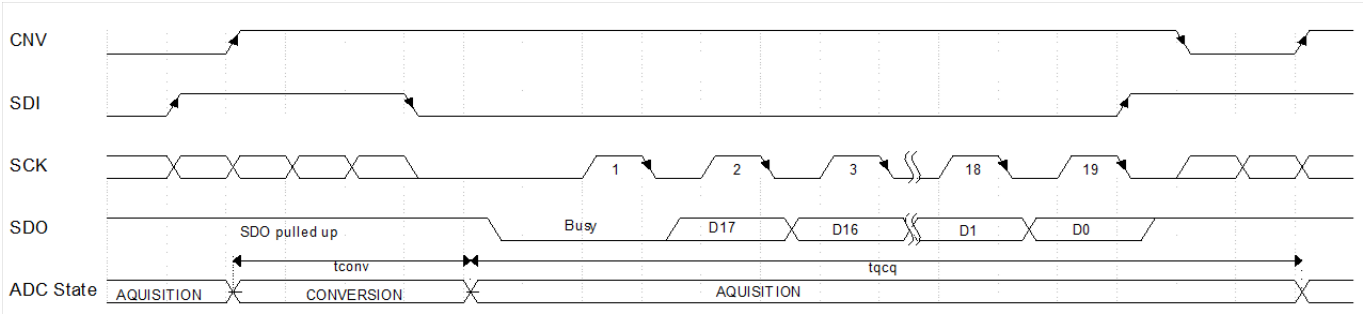


Figure 13. Timing Diagram: 4-Wire $\overline{CS}$ Mode with a Busy Indicator

When the conversion completed, the device enters an acquisition state. SDO comes out of 3-state, and outputs a busy indicator bit (low level). This feature provides a high-to-low transition on the $\overline{CS}$ pin of the digital host.

Then the data bits are clocked out on the subsequent SCLK falling edges, MSB first.

The data is valid on both SCK edges. The rising edge can be used to capture the data, and the SCK falling edge allows a faster reading rate if there is an acceptable hold time.

SDO goes to 3-state after the 17th SCK falling edge or when SDI goes high, whichever occurs first.

Care must be taken so that CNV and SDO of the devices are not low together during the read cycle.

Daisy-Chain Mode

Daisy-chain mode is selected if SDI is low at CNV rising edge or if SDI and CNV are connected.

Daisy-Chain Mode without Busy Indicator

This mode is useful in applications where the digital host has limited interfacing capability with multiple ADCs.In this mode, the CNV pins of all ADCs in the chain are connected and are controlled by a single pin of the digital host. The SCK pins are also connected and controlled by a single pin of the digital host.

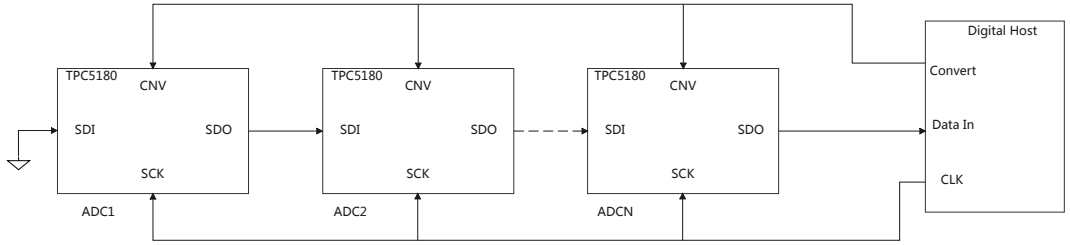


Figure 14. Connection Diagram: Daisy-Chain Mode without Busy Indicator

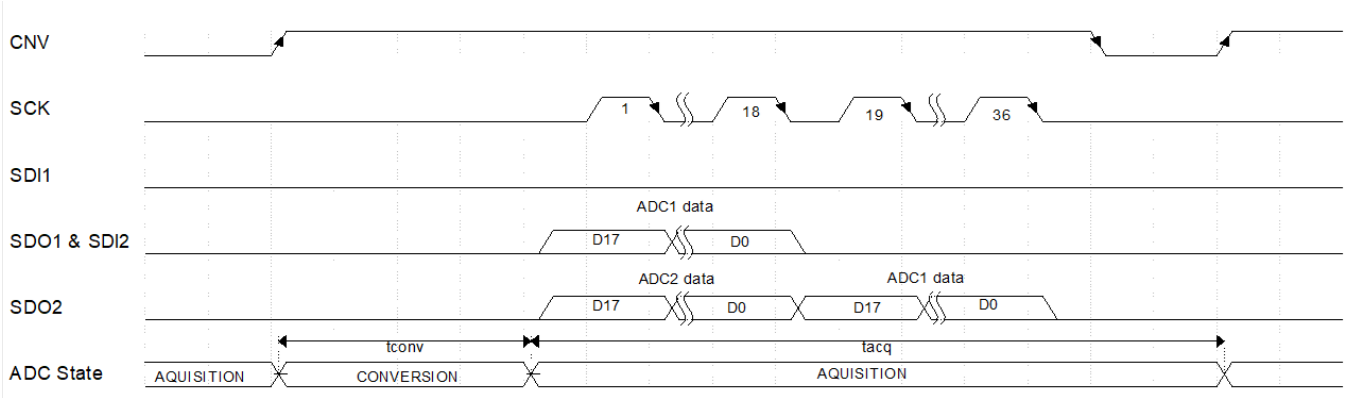


Figure 15. Timing Diagram: Daisy-Chain Mode without Busy Indicator

The SDO pin is driven low when SDI and CNV are both low.

A CNV rising edge with SDI low selects daisy-chain mode, samples the analog input, and causes the device to enter a conversion phase.

In this mode, CNV must remain high from the start of the conversion until all data bits are read. When started, the conversion continues with the internal clock, regardless of the state of SCK.

However, SCK must be low at the CNV rising edge so that the device does not generate a busy indicator at the end of the conversion.

At the end of conversion, every ADC in the chain outputs the MSB bit of the conversion result on its own SDO pin. The internal shift register of each ADC latches the data available on its SDI pin and shifts out the next bit of data on its SDO pin on every subsequent SCK falling edge.

Therefore, the digital host receives the data of ADC N at first (MSB first), followed by the data of ADC N–1, and so on. A total of 18 x N SCK falling edges are required to capture the outputs of all N devices in the chain.

The data is valid on both SCK edges. The rising edge can be used to capture the data, and SCK falling edge allows a faster reading rate if there is an acceptable hold time.

Daisy-Chain Mode with a Busy Indicator

This mode is useful in applications where the digital host has limited interfacing capability with multiple ADCs, and an interrupt-driven data transfer is desired.

In this mode, the CNV pins of all ADCs in the chain are connected and are controlled by a single pin of the digital host. The SCK pins are also connected and controlled by a single pin of the digital host.

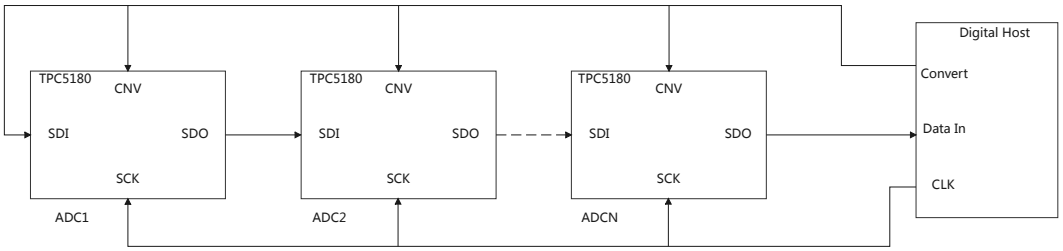


Figure 16. Connection Diagram: Daisy-Chain Mode with Busy Indicator

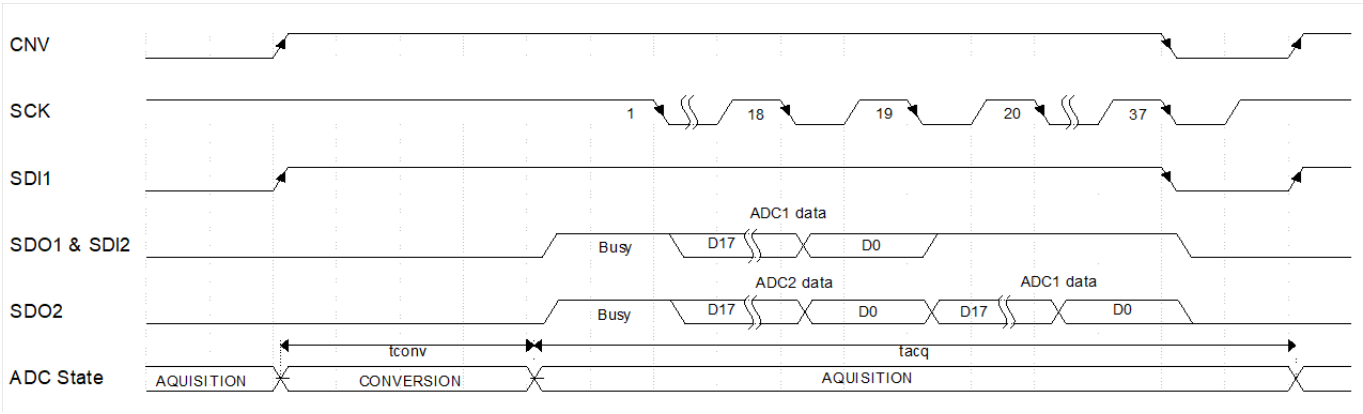


Figure 17. Timing Diagram: Daisy-Chain Mode with Busy Indicator

The SDO pin is driven low when SDI and CNV are both low.

A CNV rising edge with SDI low selects daisy-chain mode, samples the analog input, and causes the device to enter a conversion phase.

In this mode, CNV must remain high from the start of the conversion until all data bits are read. When started, the conversion continues with internal clock, regardless of the state of SCK.

However, SCK must be high at the CNV rising edge so that the device generates a busy indicator at the end of the conversion.

At the end of conversion, every ADC in the chain forces its SDO pin high, providing a low-to-high transition on the $\overline{IRQ}$ pin of the digital host. The internal shift register of each ADC latches the data available on its SDI pin and shifts out the next bit of data on its SDO pin on every subsequent SCK falling edge. Therefore, the digital host receives the interrupt signal followed by the data of ADC N (MSB first), and then the data of

ADC N–1, and so on. A total of (18 × N) + 1 SCK falling edges are required to capture the outputs of all N devices in the chain. The busy indicator bits of ADC 1 to ADC N–1 do not propagate to the next device in the chain.

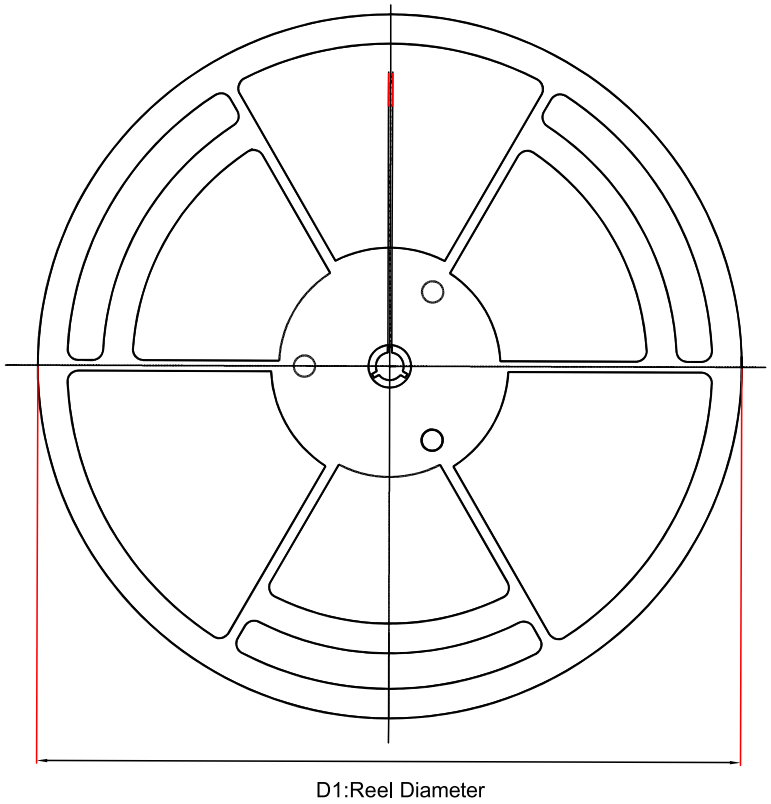
The data is valid on both SCK edges. The rising edge can be used to capture the data, and SCK falling edge allows a faster reading rate if there is an acceptable hold time.

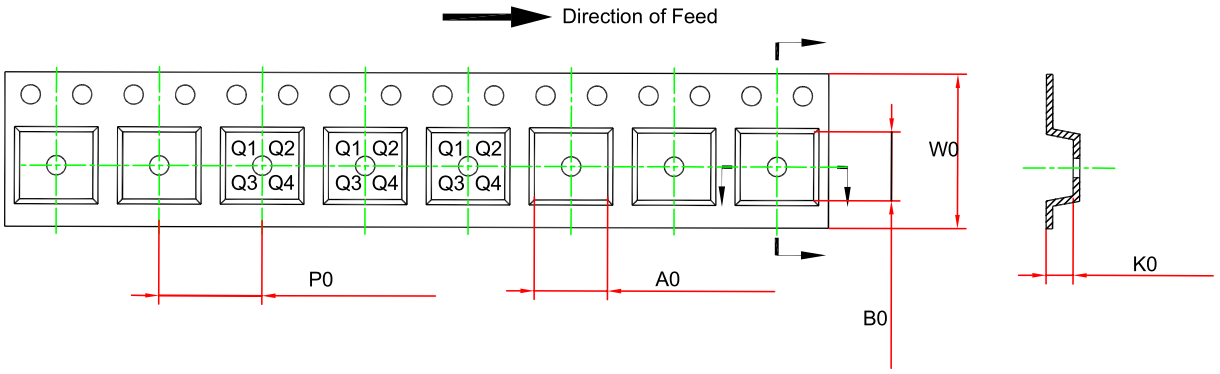
Power Supply Sequence

The recommended power supply sequence is listed below:

1. Power-up: VDD → VIO → REF → Analog Input. It should be noticed that REF and analog input must be applied after VDD. However, the device is insensitive to VDD and VIO sequence, which means VIO could be applied before VDD. Besides, it's high-Z status for digital input pins without VDD and VIO applied and digital signal on these pins even would not cause issue even if VDD and VIO are gone.
2. Power-down: Analog Input → REF → VIO → VDD.

Tape and Reel Information



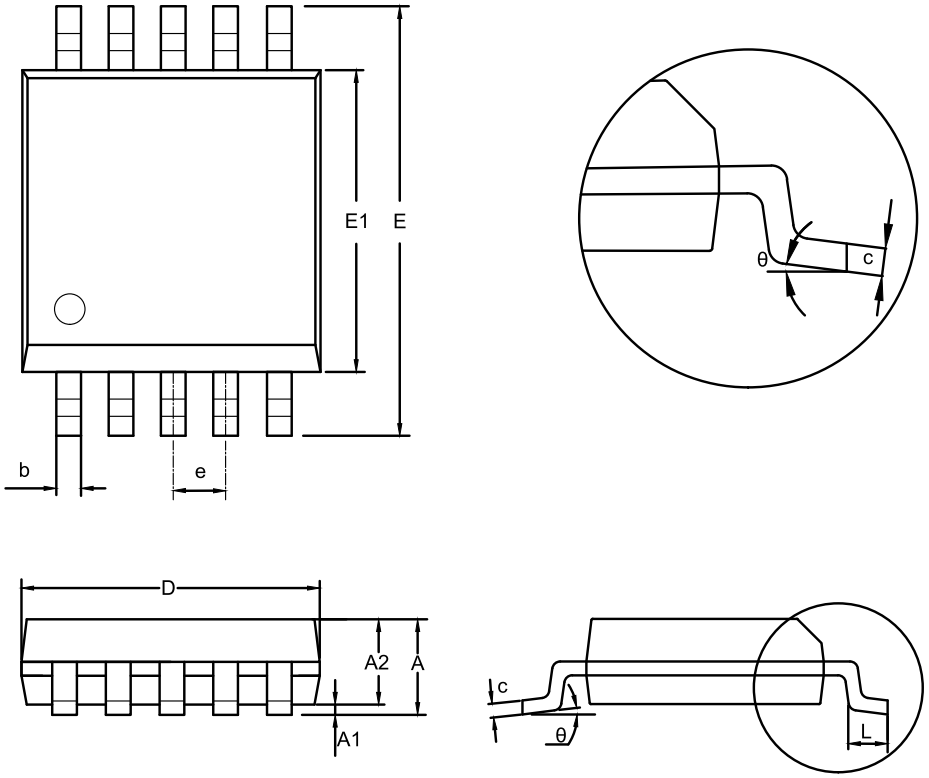


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPC5180-VS2R	MSOP10	330	17.6	5.2	3.3	1.5	8	12	Q1

Package Outline Dimensions

MSOP10

Package Outline Dimensions VS2(MSOP-10-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	1.100	0.031	0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	4.700	5.100	0.185	0.201
E1	2.900	3.100	0.114	0.122
e	0.500 BSC		0.020 BSC	
L	0.400	0.800	0.016	0.031
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPC5180-VS2R	−40 to 125°C	MSOP10	5180	MSL1	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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