16-Bit 8-Channel 1-MSPS SAR ADC

Features

- Multi-channel SAR ADC Product Family
- 16-bit Resolution with No Missing Code
- 8-channel Multiplexed Inputs
- Flexible Input Types
  - Unipolar Single-ended
  - Unipolar Differential Pairs
  - Unipolar Differential (GND sense)
  - Bipolar Differential Pairs
  - Bipolar Differential (COM = V_{REF}/2)
- Throuput: 1 MSPS
- High Linearity
  - DNL: ±0.55 LSB typical
  - INL: ±1.5 LSB typical
- High Dynamic Performance
  - SNR: 89.4 dB typical
  - SINAD: 89.2 dB typical
  - THD: −103 dB typical
- Analog Input Range: 0 V to V_{REF} with V_{REF} up to VDD
- Multiple Reference Types
  - Internal 4.096 V
  - External Buffered (up to 4.096 V)
  - External (up to VDD)
- Integrated Function
  - Internal Temperature Sensor
  - Channel Senquencer
  - Configurable One-pole Filter
  - Busy Indicator
- Single 5 V Supply Operation
- 1.8-V to 5-V Logic Interface
- Serial Interface Compatible with SPI
- Package: QFN 20-pin 4 mm x 4 mm
- Wide Operating Temperature Range
  - −40°C to +125°C

Applications

- Data Acquisitions
- Industry Automation
- Instrumentation
- Medical Equipment
- Power Line Monitoring

Description

The TPC51701 is a 8-channel, 16-bit analog-to-digital converter (ADC) operating with a single power supply VDD.

The TPC51701 is high intergrated with 16-bit SAR ADC, 8-channel multiplexer with a flexible sequencer, configurable one-pole filter, low drift internal buffered reference and a temperature sensor. Multiple input types is supported including unipolar and bipolar single-ended or differential.

The TPC51701 offers a serial port interface (SPI) for resigter and conversion results writing or reading. The interface is supplied with VIO that ranged from 1.8 V to 5 V.

The TPC51701 is available in compact 20-lead QFN 4 mm x 4 mm pacakge and operating from −40°C to +125°C.

TPC517xx is a product family covering different resultion, throughput and number of channels.

Block Diagram

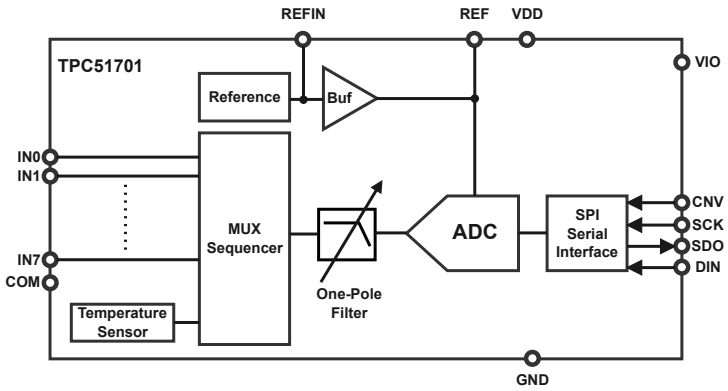


Table of Contents

Product Family Table

Order Number	Channels	Resolution	Throughput	Package
TPC51701-QFOR	8	16 bit	1MSPS	QFN4X4-20
TPC51707-QFOR	8	18 bit	800kSPS	QFN4X4-20

Revision History

Date	Revision	Notes
2023-12-01	Rev.A.0	Initial release.

Pin Configuration and Functions

TPC51701
QFN4X4-20 Package
Top View

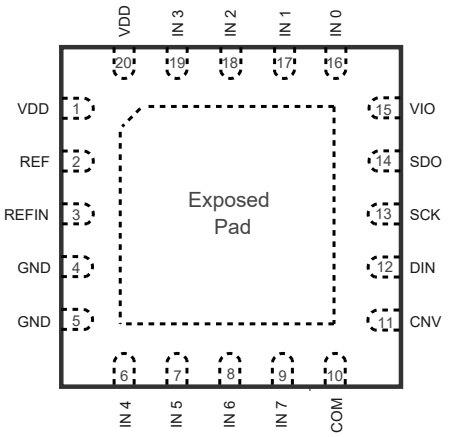


Table 1. Pin Functions: TPC51701

Pin		Type	Description
No.	Name		
1, 20	VDD	P	Power supply. Typically 4.5 V to 5.5 V and decoupled with 10 μF and 100 nF capacitors.
2	REF	AI/O	Reference Input/Output.
3	REFIN	AI/O	Internal Reference Output/Reference Buffer Input.
4, 5	GND	P	Power Supply Ground.
6, 7 8, 9	IN4, IN5 IN6, IN7	AI	Analog Input Channel 4, Analog Input Channel 5, Analog Input Channel 6, and Analog Input Channel 7.
10	COM	AI	Common Channel Input. All input channels, IN[7:0], can be referenced to a common-mode point of 0 V or V_{REF}/2 V.
11	CNV	DI	Conversion Input. On the rising edge, CNV initiates the conversion. During conversion, if CNV is held high, the busy indictor is enabled.
12	DIN	DI	Data input for writing the 14-bit configuration register. The configuration register can be written to during and after conversion.
13	SCK	DI	Serial Data Clock Input. This input clocks out the data on SDO and clock in data on DIN with MSB first.
14	SDO	DO	Serial Data Output. The conversion result is output on this pin and synchronized to SCK. In unipolar modes, conversion results are straight binary; in bipolar modes, conversion results are twos complement.
15	VIO	P	Input/Output Interface Digital Power.
16, 17 18, 19	IN0, IN1 IN2, IN3	AI	Analog Input Channel 0, Analog Input Channel 1, Analog Input Channel 2, and Analog Input Channel 3.

Pin		Type	Description
No.	Name		
21 (EPAD)	Exposed Pad	P	The exposed paddle is not connected internally. Recommended that the pad be connected to the GND.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Analog Voltage	INx, COM	GND − 0.3	VDD + 0.3	V
	REF, REFIN	GND − 0.3	VDD + 0.3	V
Digital Voltage	DIN, CNV, SCK to GND	GND − 0.3	VIO + 0.3	V
	SDO to GND	GND − 0.3	VIO + 0.3	V
Supply Voltage	VDD, VIO to GND	− 0.3	7	V
	VDD to VIO	− 7	7	V
T_J	Maximum Junction Temperature		150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
VDD	4.5	5	5.5	V
V_{REF}	2	5	VDD	V
VIO	1.8		VDD	V

Thermal Information

Package Type	θ_{JA}	θ_{JC}	θ_{JB}	Unit
QFN4X4-20	51.0	25.1	21.6	°C/W

Electrical Characteristics

All test conditions is at VDD = 5 V, V_{REF} = 5 V, VIO = 5 V, T_A = −40 °C to +125 °C, unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Unit
AC Accuracy					
SNR	f_{in} = 1 kHz, V_{REF} = 5 V external REF	84.7	89.4		dB
	f_{in} = 1 kHz, V_{REF} = 4.096 V internal REF	83.5	88.2		dB
SINAD	f_{in} = 1 kHz, V_{REF} = 5 V external REF	84.1	89.2		dB
	f_{in} = 1 kHz, V_{REF} = 4.096 V internal REF	83	88.1		dB
Dynamic Range	f_{in} = 1 kHz		90.2		dB
THD	f_{in} = 1 kHz		−103		dB
SFDR	f_{in} = 1 kHz		−105		dB
DC Accuracy					
Resolution	NO MISSING CODE	16			Bits
DNL	V_{REF} = 5 V external REF	−0.99	±0.55	1.1	LSB
INL	V_{REF} = 5 V external REF	−3.3	±1.5	2.3	LSB
Gain Error		−14	±3	29	LSB
Gain Error Match			±3.8		LSB
Gain Error Temperature Drift			±0.8		ppm/℃
Offset Error		−14	±9	14	LSB
Offset Error Match			±2.6		
Offset Error Temperature Drift			±0.3		ppm/℃
Power Supply Sensitivity	AVDD +/-5%		0.8		LSB
Analog Input					
Voltage Range	Unipolar Mode	0		$+V_{REF}$	V
	Bipolar Mode	$-V_{REF}/2$		$+V_{REF}/2$	V
Absolute Input Voltage	Positive input, unipolar and bipolar modes	– 0.1		V_{REF} + 0.1	V
	Negative or COM input, unipolar mode	– 0.1		+ 0.1	V
	Negative or COM input, bipolar mode	$V_{REF}/2$ − 0.1	$V_{REF}/2$	$V_{REF}/2$ + 0.1	V
Analog Input CMRR	f_{in} = 1 kHz		75		dB
Leakage Current at 25℃ Input Impedance	Acquisition phase		1		nA
Input Capacitance	ADC sampling capacitor		35		pF
Throughput					
Conversion Rate	Full Bandwidth			1000	kSPS
	¼ Bandwidth			250	kSPS
Internal Reference					

Parameter	Test Conditions	Min	Typ	Max	Unit
REF Output Voltage		4.086	4.096	4.106	V
REFIN Output Voltage			4.096		V
REF Output Current			±300		μA
Temperature Drift			±10		ppm/℃
Line Regulation	VDD = 5 V ± 5%		±10		ppm/V
Turn-On Settling Time	CREF = 10 μF		2		ms
External Reference(1)					
Voltage Range	REF input	2		VDD	V
	REFIN input (buffered)	2		VDD−0.3	V
Current Drain	1 MSPS, REF = 5 V		300		μA
Temperature Sensor					
Output Voltage	At 25℃		755		mV
Temperature Sensitivity			−1.67		mV/℃
Sampling Dynamics					
–3 dB Input Bandwidth	Full bandwidth		14		MHz
	¼ bandwidth		3.6		MHz
Aperture Delay	VDD = 5 V		6		ns
Digital Input					
V_{IH}		0.7 × VIO		VIO + 0.3	V
V_{IL}		−0.3		0.3 × VIO	V
I_{IH}	Input Current		±2		uA
I_{IL}	Input Current		±2		uA
Digital Output					
Data Format	Unipolar mode	Serial 16bit straight binary			
	Bipolar mode	Serial 16-bit twos complement			
Pipeline Delay		Conversion results available immediately after completed conversion			
V_{OH}	I_{SOURCE} = −500 μA	VIO − 0.2			V
V_{OL}	I_{SINK} = +500 μA			0.2	V
Power Supply					
VDD	Specified performance	4.5		5.5	V
VIO	Specified performance	1.8		VDD + 0.3	V
Power Dissipation	VDD = 5 V, 1 MSPS throughput with internal reference		38		mW
Temperature Range	Specified performance	−40		+125	℃

(1) Parameters are provided by lab bench test and design simulation.

Timing Requirements (1)

All test conditions is at VDD= 5.0 V, VIO = 1.8 V to 5 V, T_A = −40°C to +125°C, unless otherwise noted.

Parameter		Min	Typ	Max	Unit
t_{CONV}	Conversion Time: CNV Rising Edge to Data Available			668	ns
t_{ACQ}	Acquisition Time	332			ns
t_{CYC}	Time Between Conversions	1			µs
t_{CNVH}	CNV Pulse Width	10			ns
t_{DATA}	Data Write/Read During Conversion			263	ns
t_{SCK}	SCK Period	t_{DSDO} + 2			ns
t_{SCKL}	SCK Low Time	8			ns
t_{SCKH}	SCK High Time	8			ns
t_{HSDO}	SCK Falling Edge to Data Remains Valid	5			ns
t_{DSDO}	SCK Falling Edge to Data Valid Delay				
	VIO Above 4.5 V			15	ns
	VIO Above 3 V			15	ns
	VIO Above 2.7 V			15	ns
	VIO Above 2.3 V			15	ns
	VIO Above 1.8 V			16	ns
t_{EN}	CNV Low to SDO D15 MSB Valid				
	VIO Above 4.5 V			19	ns
	VIO Above 3 V			20	ns
	VIO Above 2.7 V			21	ns
	VIO Above 2.3 V			21	ns
	VIO Above 1.8 V			23	ns
t_{DIS}	CNV High or Last SCK Falling Edge to SDO High Impedance			32	ns
t_{CLSCK}	CNV Low to SCK Rising Edge	10			ns
t_{QUIET}	Last SCK Falling Edge to CNV Rising Edge Delay	40			ns
t_{SDIN}	DIN Valid Setup Time from SCK Rising Edge	5			ns
t_{HDIN}	DIN Valid Hold Time from SCK Rising Edge	5			ns

(1) Parameters are provided by design simulation.

Typical Performance Characteristics

All test conditions is at VDD = 5 V, V_{REF} = 5 V, VIO = 5 V, unless otherwise noted.

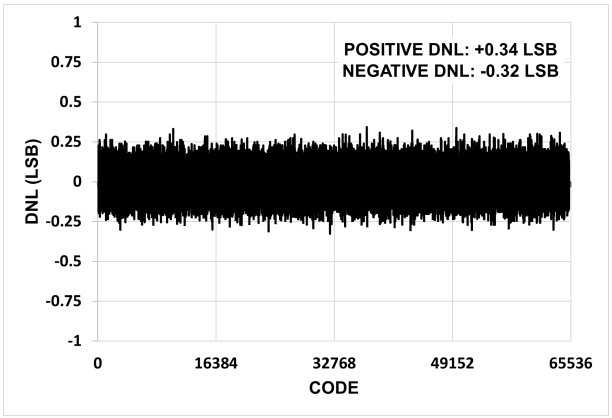


Figure 1. DNL vs. Code

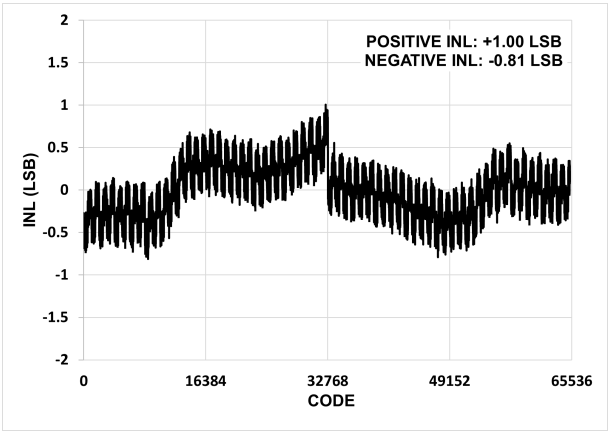


Figure 2. INL vs. Code

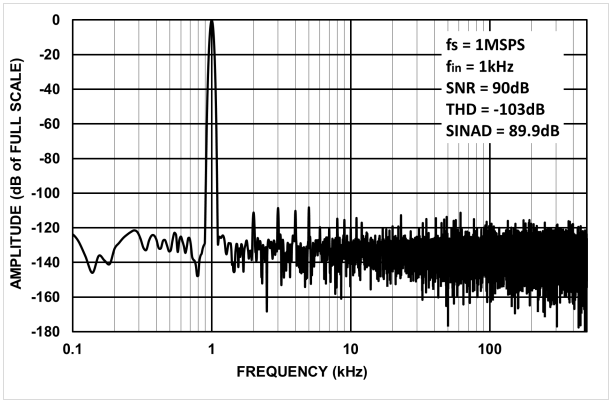


Figure 3. FFT, VREF = 5 V, External Ref

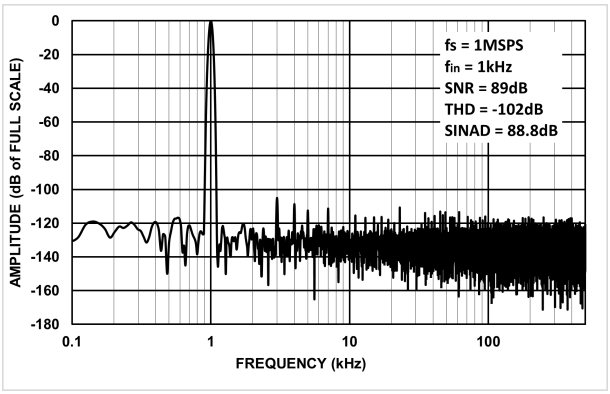


Figure 4. FFT, VREF = 4.096 V, Internal Ref

Detailed Description

Overview

The TPC51701 is a 8-channel, 16-bit, 1-MSPS successive approximation register (SAR) ADC. It is a compact solution for multi-channel data acquisition with high resolution ADC, 8-channel high isolation multiplexer including flexible channel sequencer, internal reference and buffer, internal temperature sensor for monitoring and configurable analog low-pass filter. ADC communicates with host through simple SPI serial interface. There are several options to read/wirte ADC data, which are during conversion, after conversion and spanning conversion.

The TPC51701 is specified from 4.5 V to 5.5 V VDD supply and interface digital logic supply offers wide range from 1.8 V to 5 V to compatible with host. The device is in compact 20-lead, 4 mm x 4 mm QFN package and is also pin compitable with other TPC517xx family products.

Functional Block Diagram

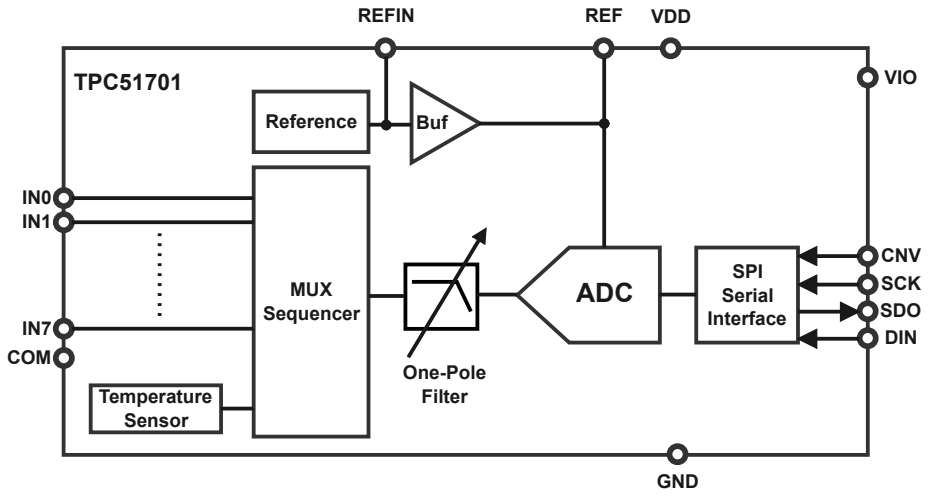


Figure 5. TPC51701 Block Diagram

Feature Description

Analog Input Configurations

TPC51701 input is configurable through register (CFG[12:10]). Generally, the positive input range is 0 V to V_{REF} V. Negative input or COM input should be referenced to ground for unipolar input case, and be referenced to $V_{REF}/2$ for bipolar input case. The following is detailed description of available input type configurations:

1. INx is single-ended input referenced to system ground; CFG[12:10] = 'b111.
2. Bipolar differential with a common reference COM = $V_{REF}/2$. INx is differential positive input and COM is common negative input; CFG[12:10] = 'b010.
3. Unipolar differential with a common reference COM connected to ground. INx is differential positive input and COM is common negative input; CFG[12:10] = 'b110.
4. Bipolar differential pairs INx+ and INx- with INx- referenced to $V_{REF}/2$; CFG[12:10] = 'b00X. INx+ is defined in channel configuration CFG[9:7].
5. Unipolar differential pairs INx+ and INx- with INx- referenced to ground; CFG[12:10] = 'b10X. INx+ is defined in channel configuration CFG[9:7].
6. Combinations of any above input types.

Sequencer

The TPC51701 incorpertes a highly flexible sequencer. The sequencer changes the input channel automatically configured in the register. Channels could be scanned as following modes, singles or pairs, with or without the temperature sensor (after the last channel is coverted).

The sequencer always starts with channel IN0 and ends up with the channel set in register CFG[9:7]. In input channel pairs mode, the last channel pair is set inCFG[9:7]. The channel pairs are paired as following way, IN (even) is the IN+ and IN (odd) is the IN-.

In order to enable the sequencer, the CFG[2:1] register is set to initializethe sequencer. After CFG[13:0] are updated, DIN must be held low while reading data out (at least for Bit 13), or the CFG register begins updating again.

While in a sequence operation, the CFG register can be changed by writing 01 to CFG[2:1]. If changing CFG11 (paired or single channel) or CFG[9:7], the sequence will reinitialize and convert IN0 (or IN1) after CFG is updated.

Voltage Reference Input/Output

The TPC51701 intergrates a high precision internal reference with buffer, and also supports external reference input.

The internal reference is 4.096 V output. If internal reference is enabled, the reference voltage is present on the REFIN pin.

The internal temperature sensor is active only when internal reference is enabled (internal reference buffer can be disabled). The internal temperature sensor output voltage is single-ended conversion, straight binary refers to the ADC GND pin

The external reference is optional only if high performance reference voltage is needed. The external reference is input through REFIN and internal reference buffer could be used.

ADC Transfer Function

For unipolar input configuration, that is single ended, differential with COM connected to ground, and diffrential pairs with INx- referenced to ground, the output data is in straight binary format.

For bipolar input configuration, that is differential with COM connected to $V_{REF}/2$, and diffrential pairs with INx- referenced to $V_{REF}/2$, the output data is in twos complement format.

Description	Unipolar Analog Input V_{REF} = 4.096 V	Digital Output Code (Straight Binary Hex)	Bipolar Analog Input V_{REF} = 4.096 V	Digital Output Code (Twos Complement Hex)
FSR − 1 LSB	4.095938 V	0xFFFF	2.047938 V	0x7FFF
Midscale + 1 LSB	2.048063 V	0x8001	62.5 µV	0x0001
Midscale	2.048 V	0x8000	0 V	0x0000
Midscale − 1 LSB	2.047938 V	0x7FFF	−62.5 µV	0xFFFF
−FSR + 1 LSB	62.5 µV	0x0001	−2.047938 V	0x8001
−FSR	0 V	0x0000	−2.048 V	0x8000

Digital Interface

The TPC51701 offers a simple 4-wire serial interface that is compatible with SPI. The digital interface uses CNV, DIN, SCK and SDO for serial interface communication

Reading/Writing during Conversion

Data reading and writing operation is completed within conversion phase. When reading/writing during conversion N, conversion results are for the previous N-1 conversion, and writing the CFG is for the next N+1 acquisition and conversion.

Reading/Writing during Conversion

Data reading and writing operation is completed within conversion phase. When reading/writing during conversion N, conversion results are for the previous N-1 conversion, and writing the CFG is for the next N+1 acquisition and conversion.

Initially, CNV is brought high to start conversion, and CNV must be brought low to enable reading/writing during conversion. It should be noticed that reading/writing must be finished within t_{DATA}, thus the SCK frequency is limited by:

$$f_{SCK} \geq \frac{\text{Number of SCK edges}}{t_{DATA}} \quad (1)$$

Reading/Writing after Conversion (During Acquisition)

Data reading and writing operation is completed within acquisition phase. When reading/writing during acquisition N, conversion results are for the previous N-1 conversion, and writing the CFG is for the next N+1 acquisition and conversion.

Maximum throughput is limited by finishing reading/writing within min t_{ACQ}. There is no limit for slow throughput rate which is required by user. Further more, reading/writing still must be within acquisition phase.

Reading/Writing Spanning Conversion

Data reading and writing operation is across acquisition and conversion phase. The data access starts at the current acquisition N and spans into the conversion N. Conversion results are for the previous N-1 conversion, and writing the CFG register is for the next N+1 acquisition and conversion.

Similarly, reading/writing must be within t_{DATA} in converstion phase and maximum throughput is limited by min t_{ACQ}time in acquisition phase. On the whole, the total time limit for maximum throughput is min t_{ACQ} time + t_{DATA} time.

The host can run at any low throughput rateand reading/writing should be taken place druing acquisition phase with additional time into the conversion.

Spanning conversion requires CNV pulled high to start conversion, and data access is not allowed when CNV is high.

Reigister Configuration, CFG

There is a 14-bit configuration register CFG[13:0] in the device. The CFG register is latched (MSB first) on DIN with 14 SCK rising edges. CFG update is edge dependent, allowing for asynchronous or synchronous hosts. The register can be written to during conversion, during acquisition, or spanning acquisition/conversion and is updated at the end of conversion, tCONV (maximum). It should be noticed that at power-up, the CFG register is undefined and two dummy conversions are required

to update the register. The CFG word is updated on the first 14 SCK rising edges. If the CFG readback is enabled, an additional 14 SCK falling edges are required to output the CFG word associated with the conversion results, with the CFG MSB following the LSB of the conversion result.

Table 2. Register Description

<table>
<tr><th>Bit(s)</th><th>Name</th><th colspan="4">Description</th></tr>
<tr><td>[13]</td><td>CFG</td><td colspan="4">Configuration update.
0 = Keep current configuration settings.
1 = Overwrite contents of register.</td></tr>
<tr><td rowspan="8">[12:10]</td><td rowspan="8">INCC</td><td colspan="4">Input channel configuration. Selection of pseudobipolar, pseudodifferential, pairs, single-ended, or temperature sensor.</td></tr>
<tr><td>Bit 12</td><td>Bit 11</td><td>Bit 10</td><td>Function</td></tr>
<tr><td>0</td><td>0</td><td>X</td><td>Bipolar differential pairs; INx− referenced to VREF/2 ± 0.1 V.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Bipolar; INx referenced to COM = VREF/2 ± 0.1 V.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Temperature sensor.</td></tr>
<tr><td>1</td><td>0</td><td>X</td><td>Unipolar differential pairs; INx− referenced to GND ± 0.1 V.</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Unipolar, IN0 to IN7 referenced to COM = GND ± 0.1 V (GND sense).</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Unipolar, IN0 to IN7 referenced to GND.</td></tr>
<tr><td rowspan="5">[9:7]</td><td rowspan="5">INx</td><td colspan="4">Input channel selection in binary fashion.</td></tr>
<tr><td>Bit 9</td><td>Bit 8</td><td>Bit 7</td><td>Channel</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>IN0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>IN1</td></tr>
<tr><td>...</td><td>...</td><td>...</td><td>...</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>IN7</td></tr>
<tr><td>[6]</td><td>BW</td><td colspan="4">Select bandwidth for low-pass filter. Refer to the Selectable Low-Pass Filter section.
0 = ¼ of BW, uses an additional series resistor to further bandwidth limit the noise. Maximum throughput must also be reduced to ¼.
1 = Full BW.</td></tr>
<tr><td rowspan="9">[5:3]</td><td rowspan="9">REF</td><td colspan="4">Reference/buffer selection. Selection of internal, external, and external buffered references, and enabling of the on-chip temperature sensor. Refer to the Voltage Reference Output/Input section.</td></tr>
<tr><td>Bit 5</td><td>Bit 4</td><td>Bit 3</td><td>Function</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Do not use.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Internal reference and temperature sensor enabled. REF = 4.096 V buffered output.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Use external reference. Temperature sensor enabled. Internal buffer disabled.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Use external reference. Internal buffer and temperature sensor enabled.</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Do not use.</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Do not use.</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Use external reference. Internal reference, internal buffer and temperature sensor disabled.</td></tr>
</table>

Bit(s)	Name	Description			
		1	1	1	Use external reference. Internal buffer enabled. Internal reference and temperature sensor disabled.
[2:1]	SEQ	Channel sequencer. Allows scanning channels in an IN0 to IN[7:0] fashion. Refer to the Sequencersection.			
		Bit 2	Bit 1	Function	
		0	0	Disable sequencer.	
		0	1	Update configuration during sequence.	
		1	0	Scan IN0 to IN[7:0] (set in CFG[9:7]), then temperature.	
		1	1	Scan IN0 to IN[7:0] (set in CFG[9:7]).	
0	RB	Read back the CFG register.			
		0 = Read back current configuration at end of data.			
		1 = Do not read back contents of configuration.			

General Timing without a Busy Indicator

Following figures illustrate the general timing without a busy indicatior for reading/writing during conversion, after conversion and spanning conversion mode. The busy indicator is disabled if CNV is high at the end of conversions.

A CNV rising edge starts a conversion, forces SDO to high impedance and ignores SDI data input. Once conversion is initiated, it it continues until completion irrespective of the state of CNV. However, CNV should be returned to high before safe data time t_{DATA} and hold high until conversion period is completed, in oder to disable busy indicator.

After the conversion phase, the ADC starts acquisition. Once CNV is brought low after EOC (End of Conversion), SDO is driven from high impedance to the MSB. The MSB of CFG should be also be presented on SDI if necessary for CFG update. When CNV is low, both CFG configuration and data readback operation is available. The first 14 SCK rising edges update the CFG, and the first 15 SCK falling edges trigger out the conversion results starting with MSB − 1. Data access is limited within safe data reading/writing time, t_{DATA}. If the full configuration 14 bits of CFG[13:0] word was not written to before EOC, it is discarded and the current configuration remains. If the 16 btis conversion result is not read out fully within t_{DATA}prior to end of conversions, it is lost as the ADC updates SDO with the MSB of the current conversion and falling SCK edges clock out bits starting with MSB−1.

The SDO data is available for both SCK edges. After the 16th or 30th (plus 14 bits CFG readback) SCK falling edge, or when CNV goes high (whichever occurs first), SDO returns to high impedance.

If CFG readback is enabled, the CFG is read back MSB first following the LSB of the conversion result. A total of 30 SCK falling edges is required to return SDO to high impedance if this is enabled.

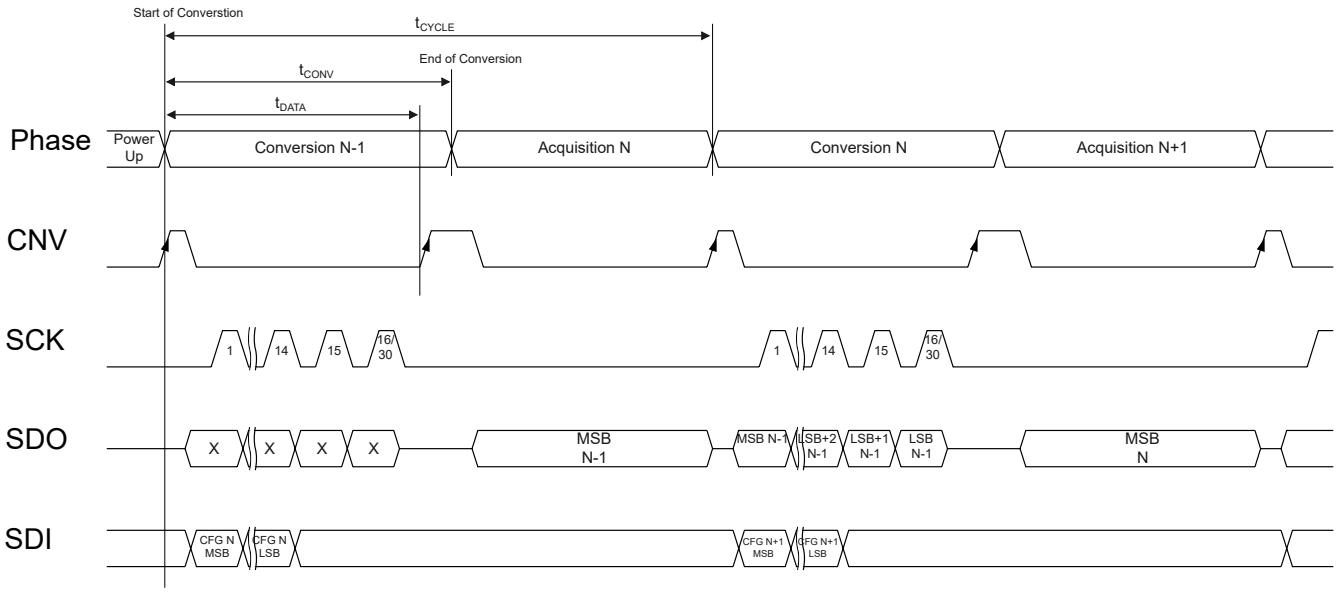


Figure 6. General Interface Timing for Read/Write during Conversion without a Busy Indicator

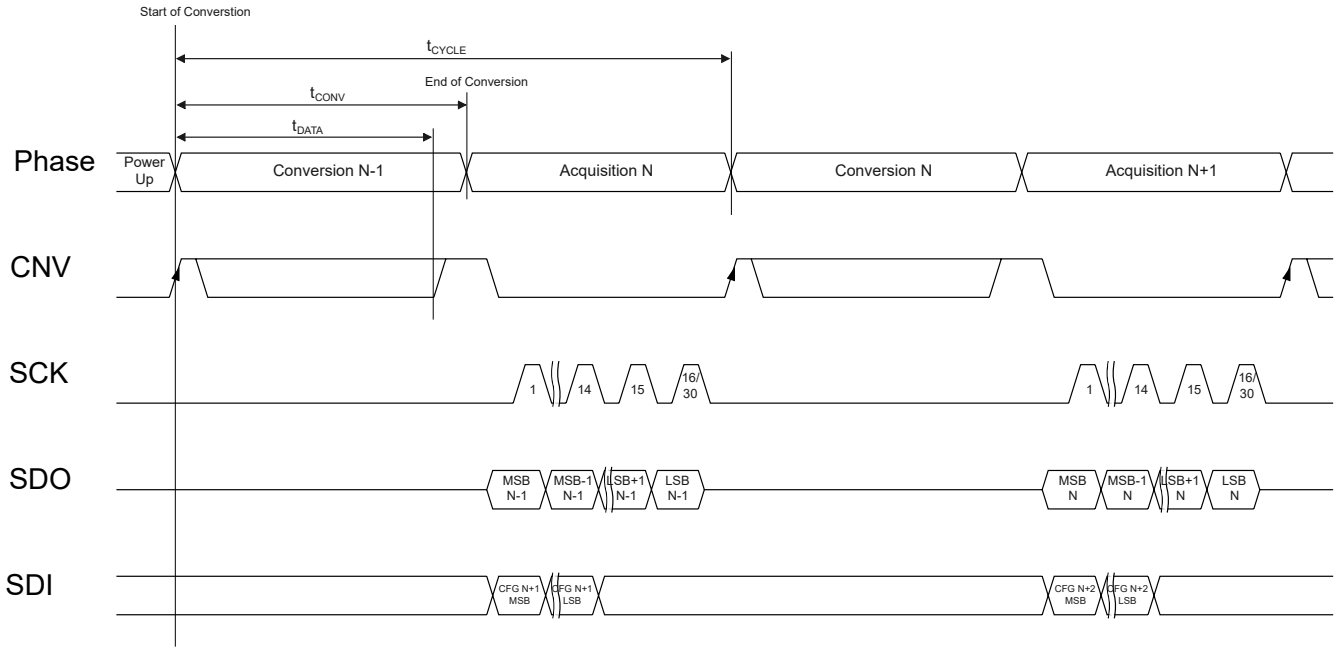


Figure 7. General Interface Timing for Read/Write after Conversion without a Busy Indicator

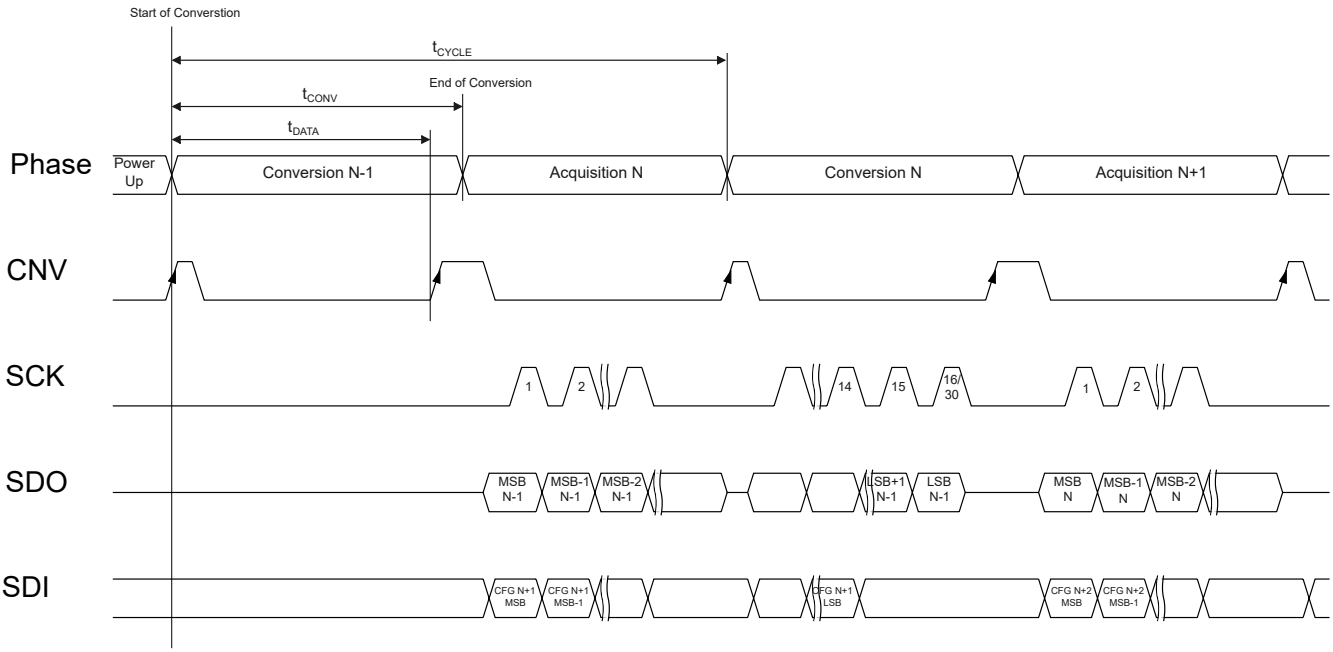


Figure 8. General Interface Timing for Read/Write Spanning Conversion without a Busy Indicator

General Timing with a Busy Indicator

Following figures illustrate the general timing with a busy indicatior for reading/writing during conversion, after conversion and spanning conversion mode. The busy indicator is enabled if CNV is low at the end of conversions. SDO should be returned to high impedance to generate busy indicator properly.

A CNV rising edge starts a conversion, forces SDO to high impedance and ignores SDI data input. Once conversion is initiated, it it continues until completion irrespective of the state of CNV. However, CNV should be returned to low before safe data time t_{DATA} and hold low until conversion period is completed, in oder to enable busy indicator. When the conversion is finished, SDO changes from high impedance to low, if SDO is pulled-up to VIO, a falling edge on SDO acting as a busy indicator interrupt host to start data transfer.

After the conversion phase, the ADC starts acquisition. Once CNV is low after EOC (End of Conversion), the MSB of CFG should be also be presented on SDI if necessary for CFG update. When CNV is low, both CFG configuration and data readback operation is available. The first 14 SCK rising edges update the CFG, and the first 16 SCK falling edges trigger out the conversion results starting with MSB. Data access is limited within safe data reading/writing time, t_{DATA}. If the full configuration 14 bits of CFG[13:0] word was not written to before EOC, it is discarded and the current configuration remains. If the 16 bits conversion result is not read out fully within t_{DATA} prior to end of conversions, it is lost.

The SDO data is available for both SCK edges. Only after the 17th SCK falling edge, SDO returns to high impedance. It should be noted that if optional 17th (or 31th) SCK falling edge is not used, the busy feature cannot be detected if the LSB for the conversion is just low.

If CFG readback is enabled, the CFG is read back MSB first following the LSB of the conversion result. A total of 31 SCK falling edges is required to return SDO to high impedance if this is enabled.

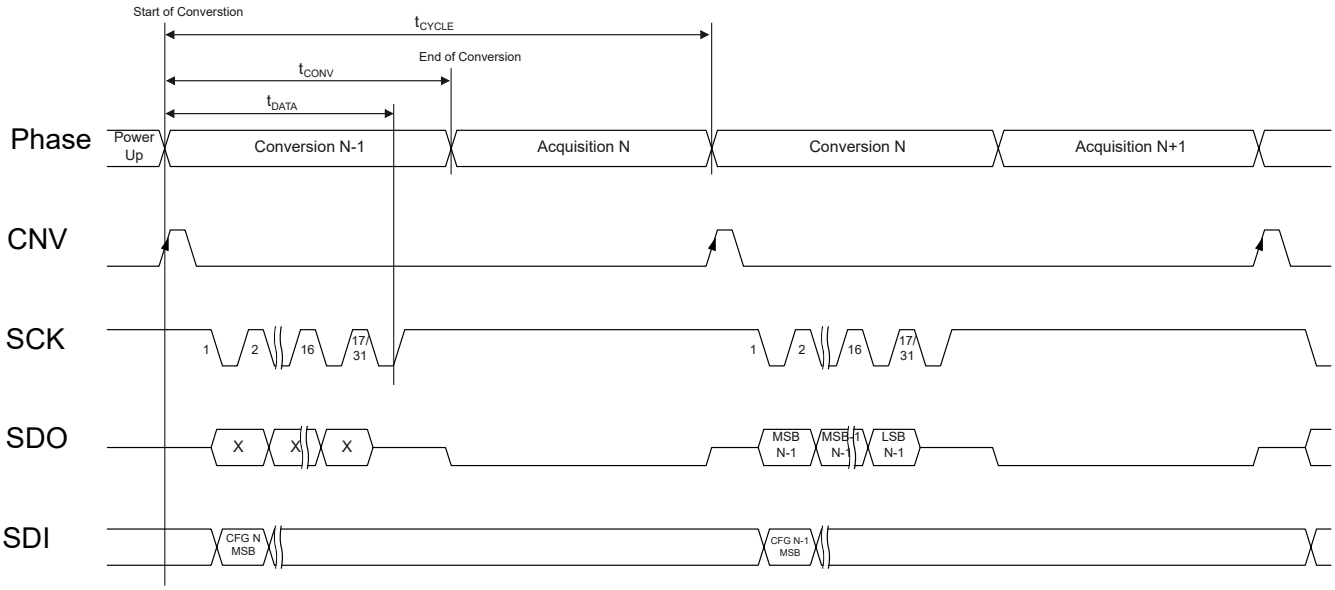


Figure 9. General Interface Timing for Read/Write during Conversion with a Busy Indicator

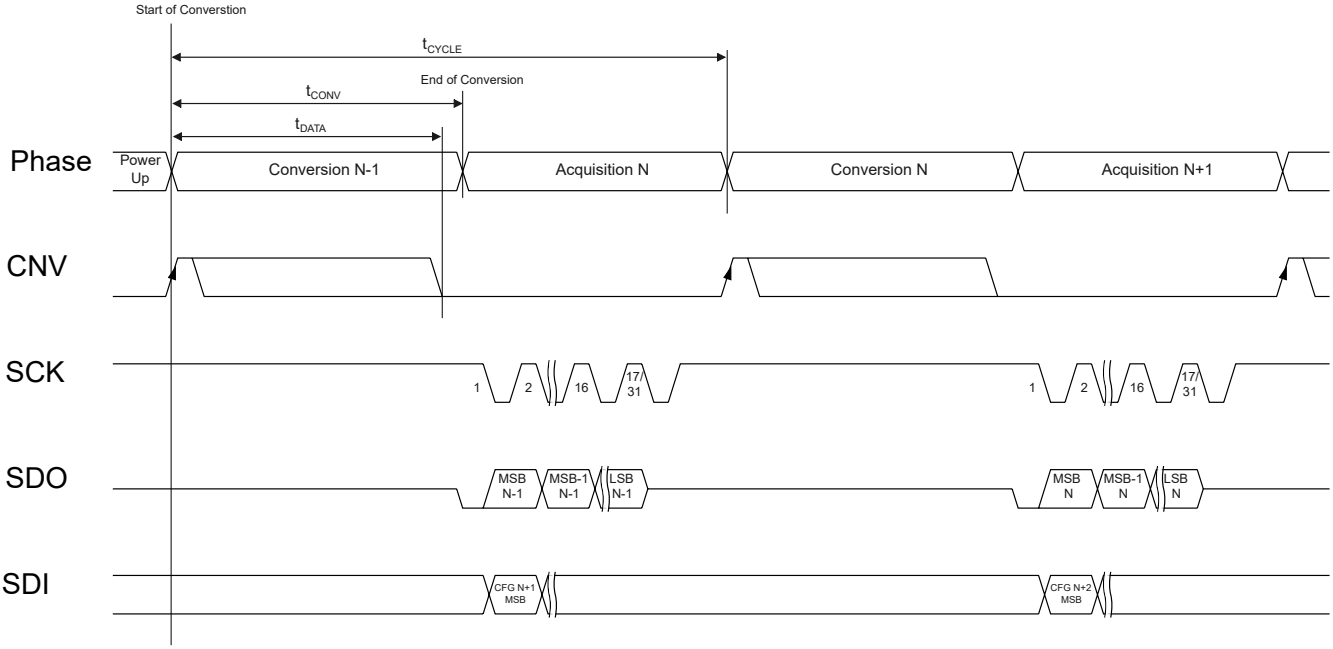


Figure 10. General Interface Timing for Read/Write after Conversion with a Busy Indicator

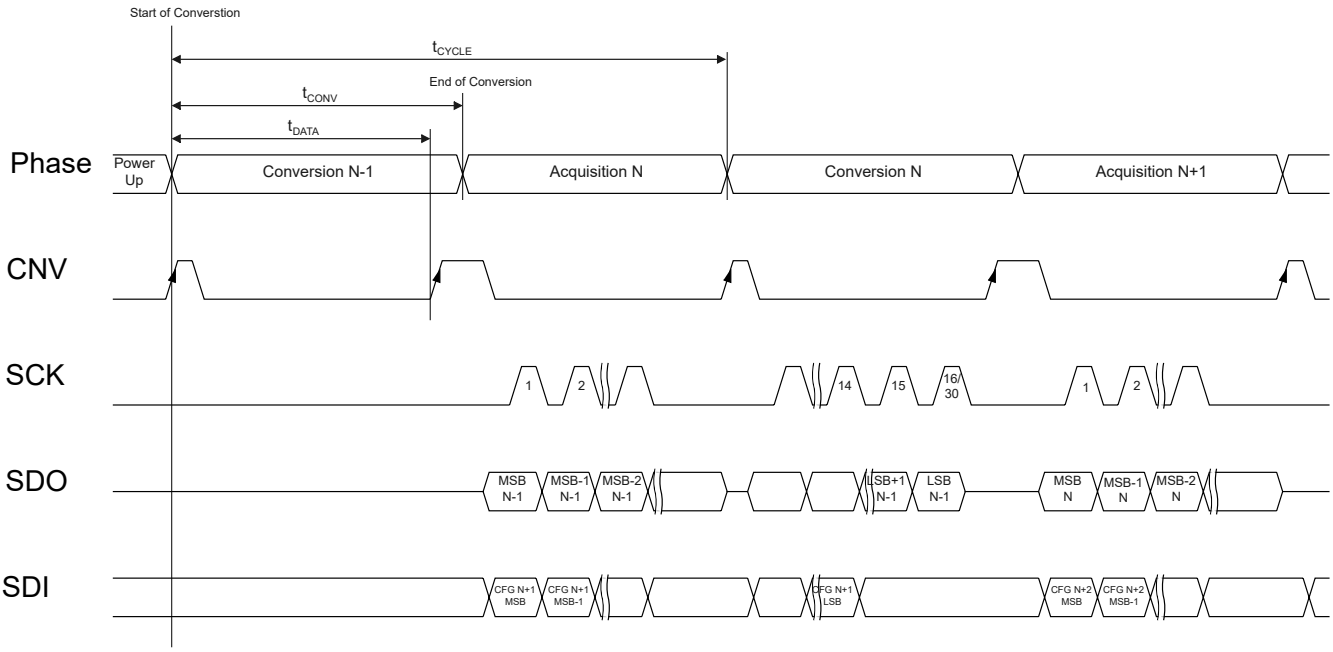


Figure 11. General Interface Timing for Read/Write Spanning Conversion with a Busy Indicator

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Typical Application

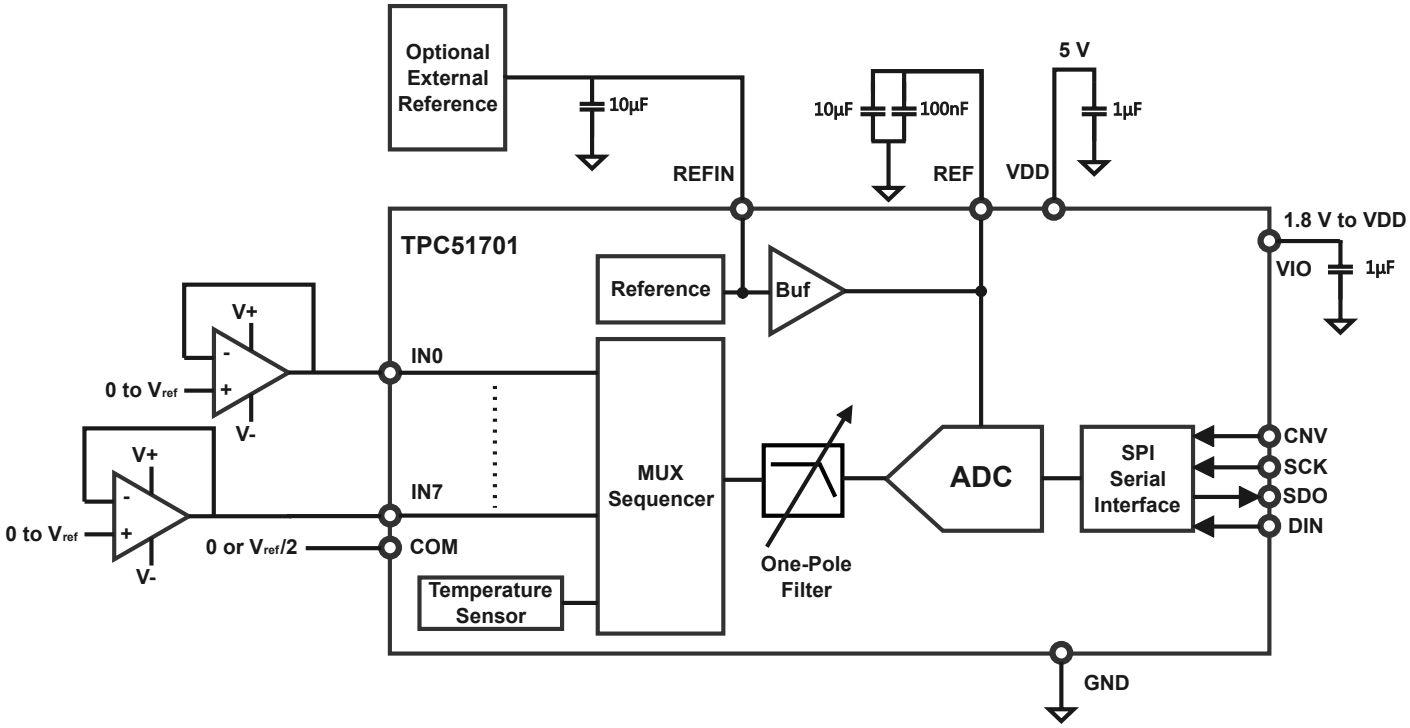


Figure 12. Typical Application Diagram

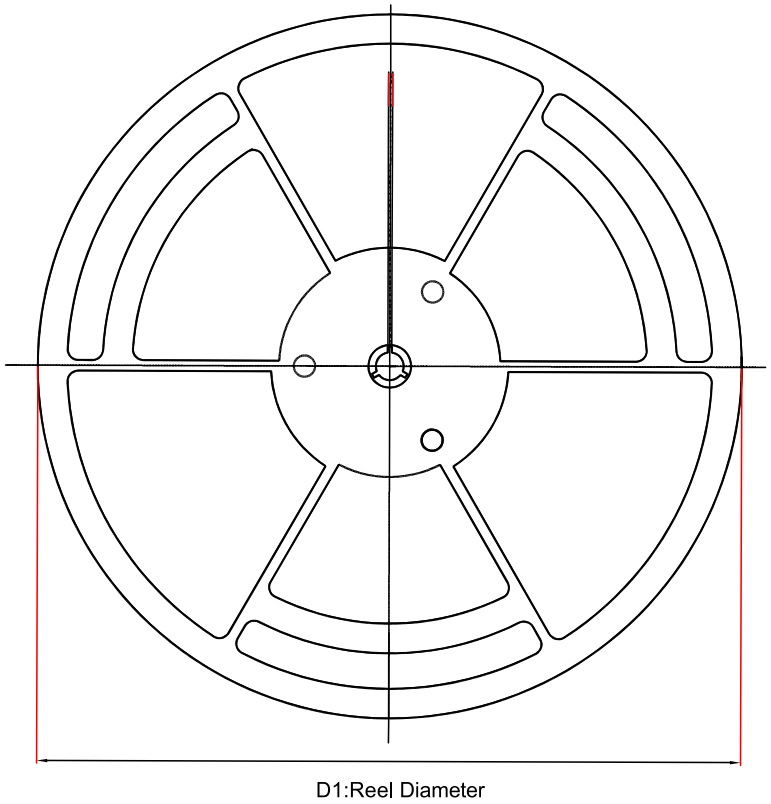
Table 3. Recommended 3PEAK ADC Driver Amplifiers

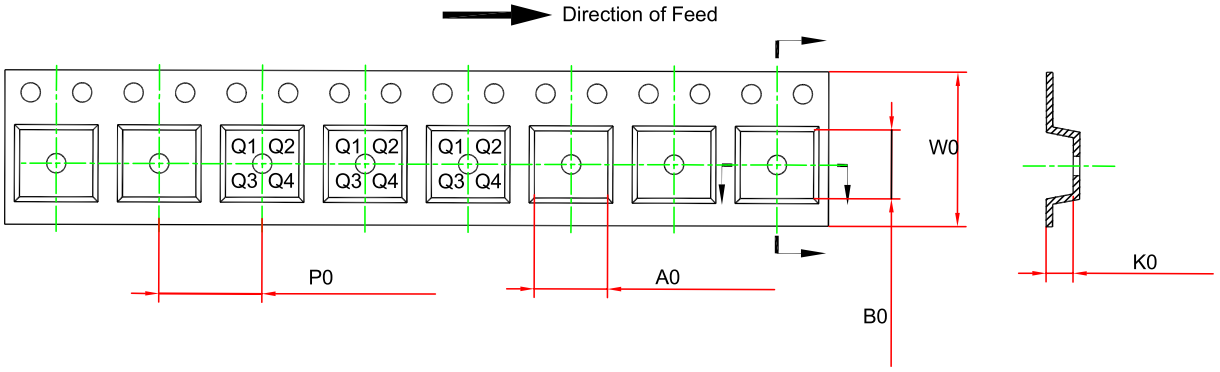
Part Number	CH	VDD (V)	GBWP (MHz)	Slew Rate (V/µs)	eN@1kHz (nV/√Hz)	IBIAS (pA)	VOS (max) (mV)	VOS TC (µV/°C)	Package
TPA2681	1	8~36	20	10	10	100000	3	2	SOT23-5
TPA2682	2	8~36	20	10	10	100000	3	2	SOP8,MSOP8
TPA1881	1	4.5~36	12	10	6	500	0.02	0.05	SOT23-5,SOP8
TPA1882	2	4.5~36	12	10	6	500	0.02	0.05	SOP8,MSOP8
TPA2671	1	4~36	10	15	38	50	3	0.5	SOT23-5,SOT353
TPA2672	2	4~36	10	15	38	50	3	0.5	MSOP8,TSSOP8,SOP8
TPA2674	4	4~36	10	15	38	50	3	0.5	SOP14,TSSOP14

Table 4. Recommended 3PEAK Voltage References

Part Number	Vin (min) (V)	Vin (max) (V)	Accuracy (max)	TC (-40 to 125 ℃) (ppm/℃)	Output Voltage Noise 0.1 to 10 Hz (μVpp)	Package
TPR70	max (Ver+0.2, 3)	15	0.05%	3	2.5	SOP8
TPR50	max (Ver+0.2, 3)	15	0.05%	6	7.5	MSOP8, SOP8

Tape and Reel Information



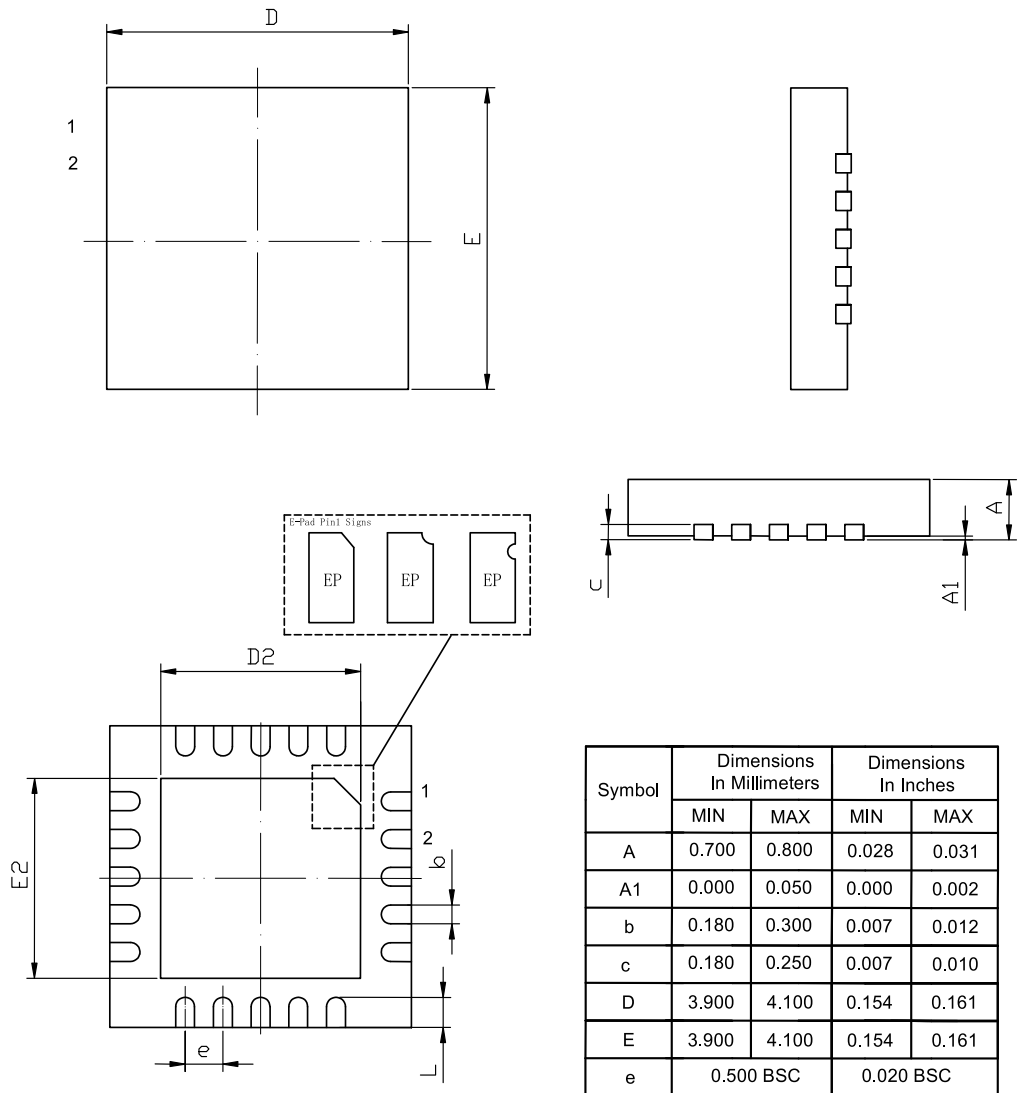


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPC51701-QFOR	QFN4X4-20	330	17.6	4.3	4.3	1.1	8.0	12.0	Q2

Package Outline Dimensions

QFN4X4-20

Package Outline Dimensions QFO(QFN4X4-20-B)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.180	0.300	0.007	0.012
c	0.180	0.250	0.007	0.010
D	3.900	4.100	0.154	0.161
E	3.900	4.100	0.154	0.161
e	0.500 BSC		0.020 BSC	
L	0.300	0.500	0.012	0.020
D2	2.500	2.700	0.098	0.106
E2	2.500	2.700	0.098	0.106

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPC51701-QFOR	−40 to 125°C	QFN4X4−20	51701	3	Tape and Reel, 3000	Green

(1) For future products, contact the 3PEAK factory for more information and sample.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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