16-Bit SAR ADC with Pseudo-Differential Input

Features

- 16-Bit SAR ADC with Zero Latency
  - Throughput Speed: 600 kSPS
- Pseudo-Differential Analog Input
  - 0 V to V_{REF}
- External V_{REF}
  - 2.5 V to V_{DD}
- High Linearity
  - INL: ±1.5 LSB Typical
  - DNL: ±0.5 LSB Typical
  - THD: −102 dB at 1 kHz
- High Dynamic Range and Noise Performance
  - SNR: 89.9 dB at 1 kHz
  - Dynamic Range: 90 dB at 1 kHz
- Serial Interface
  - SPI Compatible
- Daisy-Chain Is Supported
- Package: MSOP10
- Wide Operating Temperature Range
  - −40°C to +125°C

Applications

- Data Acquisitions
- Instruments
- Industry Measurement and Control
- Medical Equipment
- Automatic Test Equipment

Description

The TPC5161 is a 16-bit analog-to-digital converter (ADC). The device supports unipolar, pseudo-differential input, and the input range is 0 to V_{REF}.

The device operates with a 2.5-V to V_{DD} external reference.

The device offers an SPI-compatible interface, and supports daisy-chain operation for multiple device applications.

The device also offers an optional busy indicator bit which can be used to synchronize with the host.

Typical Application Circuit

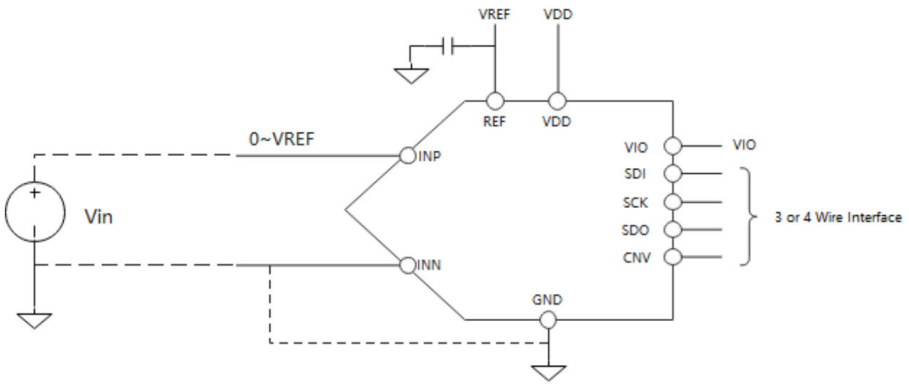


Table of Contents

Product Family Table

Order Number	Resolution	Input Range	Throughput Speed	Package
TPC5161-VS2R	16	0 to V_{REF}	600 kSPS	MSOP10

Revision History

Date	Revision	Notes
2022-05-23	Rev.Pre.0	Pre-release version.
2023-01-17	Rev.Pre.1	Updated the diagram and Electrical Characteristics table.
2023-04-19	Rev.Pre.2	Updated the Electrical Characteristics table and timing specification.
2023-08-26	Rev.A.0	Initial release.
2024-11-26	Rev.A.1	Updated to a new datasheet format. Updated tape and reel information

Pin Configuration and Functions

TPC5161
MSOP10
Top View

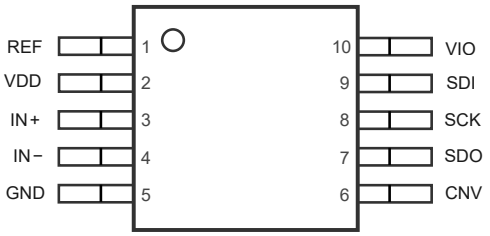


Table 1. Pin Functions

Pin No.	Name	I/O	Description
1	REF	I	Reference voltage.
2	VDD	O	Power supply.
3	IN+	O	Positive analog input.
4	IN−	I	Negative analog input.
5	GND	–	Power ground.
6	CNV		• Conversion input. • It initiates the conversion of the device, and selects the interface mode together with SDI. – Chain mode: SDI is low during the CNV rising edge. – $\overline{CS}$ mode: SDI is high during the CNV rising edge.
7	SDO		Serial data output.
8	SCK		Serial data clock.
9	SDI		• Serial data input. • It selects the serial mode together with CNV.
10	VIO		Digital interface power.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Analog Voltage	IN+, IN− to GND	−0.3	V_{DD} + 0.3	V
	V_{REF} to GND	−0.3	V_{DD} + 0.3	V
Digital Voltage	Digital Inputs to GND	−0.3	V_{IO} + 0.3	V
	Digital Outputs to GND	−0.3	V_{IO} + 0.3	V
Supply Voltage	V_{DD} to GND	−0.3	6	V
	V_{IO} to GND	−0.3	V_{DD} + 0.3	V
T_J	Maximum Junction Temperature	−40	150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	2,000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1,500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
V_{DD}	4.5	5	5.5	V
REF	2.5	5	V_{DD}	V
V_{IO}	1.71	3.3	V_{DD}	V

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
MSOP10	125	48	°C/W

Electrical Characteristics

All test conditions: V_{DD} = 5 V, V_{IO} = 1.71 V to 5 V, T_A = −40°C to +125°C, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
AC Accuracy							
SNR	Signal-to-Noise Ratio	f_{IN} = 1 kHz	REF = 5 V	87	89.9		dB
			REF = 3 V		85.5		dB
SINAD	Signal-to-Noise and Distortion Ratio	f_{IN} = 1 kHz	REF = 5 V		89		dB
			REF = 3 V		84.5		dB
	Dynamic Range	f_{IN} = 1 kHz	REF = 5 V		90		dB
			REF = 3 V		86		dB
THD	Total Harmonic Distortion	f_{IN} = 1 kHz	REF = 5 V		−102		dB
SFDR	Spurious-Free Dynamic Range	f_{IN} = 1 kHz	REF = 5 V		−104		dB
DC Accuracy							
N	Resolution	No missing code		16			Bits
DNL	Differential Nonlinearity	REF = 5 V		−0.99	±0.5	1.1	LSB
		REF = 3 V			±0.5		
INL	Integral Nonlinearity	REF = 5 V		−2.5	±1.5	2.5	LSB
		REF = 3 V			±1.5		
	Transition Noise	REF = 5 V			0.6		LSB
		REF = 3 V			1		
GE	Gain Error			−15	±10	15	LSB
	Gain Error Drift				±0.35		ppm/℃
	Zero Code Error			−0.5	±0.08	0.5	mV
	Zero Code Error Drift				±0.35		ppm/℃
	Power Supply Sensitivity	AVDD ± 5%			±3		LSB
Analog Input							
	Voltage Range	(IN+) − (IN−)		0		V_{REF}	V
	Operating Input Voltage	IN+		−0.1		V_{REF} + 0.1	V
		IN−		−0.1		0.1	V
	Analog Input CMRR				60		dB
	Leakage Current at 25℃				1		nA
C_{IN}	Input Capacitance				33		pF
Throughput							
	Conversion Rate	V_{IO} ≥ 2.3 V up to 85°C, V_{IO} ≥ 3.3 V above 85°C up to 125°C			0.6		MHz
		V_{IO} ≥ 1.71 V, V_{IO} ≤ 3.3 V up to 125°C			0.6		MHz
	Acquisition Time				860		ns

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
	Conversion Time				780		ns
	Transient Response				860		ns
Reference							
	Reference Voltage Range (1)			2.5		V_{DD}	V
	Reference Load Current	600 kSPS, REF = 5 V			130		µA
Sampling Dynamics							
f_{-3dB}	−3-dB Bandwidth				20		MHz
	Aperture Delay				4		ns
Digital Input							
V_{IH}	High-Level Input Voltage	V_{IO} > 3 V		0.7 × V_{IO}			V
V_{IL}	Low-Level Input Voltage	V_{IO} > 3 V				0.3 × V_{IO}	V
V_{IH}	High-Level Input Voltage	V_{IO} ≤ 3 V		0.7 × V_{IO}			V
V_{IL}	Low-Level Input Voltage	V_{IO} ≤ 3 V				0.3 × V_{IO}	V
I_{IH}	High-Level Input Current	Input current		−1		1	µA
I_{IL}	Low-Level Input Current	Input current		−1		1	µA
Digital Output							
	Data Format			Serial 16-bit straight binary			
	Pipeline Delay			Conversion results available immediately after completed conversion			
V_{OH}	High-Level Output Voltage	Output logic high voltage	Current source = 500 µA	V_{IO} − 0.2			V
V_{OL}	Low-Level Output Voltage	Output logic low voltage	Current sink = 500 µA			0.2	V
Power Supply							
V_{DD}				4.5		5.5	V
V_{IO}				1.8		V_{DD}	V
	Standby Current				3,200		µA
I_{VDD}	V_{DD} Current	Operating	fs = 1 kHz		3.3		mA
		Operating	fs = 600 kHz		4.8		mA

(1) Parameters are provided by lab bench tests and design simulation.

Timing Requirements (1)

All test conditions: V_{DD} = 5 V, V_{IO} = 1.71 V to 5 V, T_A = −40°C to +125°C, C_{LOAD} = 20 pF, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
t_{CONV}	Conversion Time: CNV Rising Edge to Data Available	772	812	853	ns
t_{ACQ}	Acquisition Time	813			ns
t_{CYC}	Time between Conversions	1,666			ns
t_{CNVH}	CNV Pulse Width (CS Mode)	9			ns
t_{SCK}	SCK Period (CS Mode)				
	V_{IO} above 4.5 V	16			ns
	V_{IO} above 3.3 V	17			ns
	V_{IO} above 1.7 V	25			ns
t_{SCK}	SCK Period (Chain Mode)				
	V_{IO} above 4.5 V	16			ns
	V_{IO} above 3.3 V	17			ns
	V_{IO} above 1.7 V	25			ns
t_{SCKL}	SCK Low Time	5			ns
t_{SCKH}	SCK High Time	5			ns
t_{HSDO}	SCK Falling Edge to Data Remains Valid	3.5			ns
t_{DSDO}	SCK Falling Edge to Data Valid Delay				
	V_{IO} above 4.5 V			14	ns
	V_{IO} above 3.3 V			15	ns
	V_{IO}above 1.7 V			23	ns
t_{EN}	CNV or SDI Low to SDO D15 MSB Valid (CS Mode)				
	V_{IO} above 4.5 V			12	ns
	V_{IO} above 3.3 V			13	ns
	V_{IO} above 1.7 V			21	ns
t_{DIS}	CNV or SDI High or Last SCK Falling Edge to SDO High Impedance (CS Mode)			10	ns
$t_{SSDICNV}$	SDI Valid Setup Time from CNV Rising Edge	8			ns
$t_{HSDICNV}$	SDI Valid Hold Time from CNV Rising Edge (CS Mode)	0			ns
$t_{HSDICNV}$	SDI Valid Hold Time from CNV Rising Edge (Chain Mode)	0			ns
$t_{SSCKCNV}$	SCK Valid Setup Time from CNV Rising Edge (Chain Mode)	8			ns

Symbol	Parameter	Min	Typ	Max	Unit
$t_{HSCKCNV}$	SCK Valid Hold Time from CNV Rising Edge (Chain Mode)	0.5			ns
$t_{SSDISCK}$	SDI Valid Setup Time from SCK Falling Edge (Chain Mode)	0			ns
$t_{HSDISCK}$	SDI Valid Hold Time from SCK Falling Edge (Chain Mode)	0.5			ns
$t_{DSDOSDI}$	SDI High to SDO High (Chain Mode with Busy Indicator)			9	ns

(1) Parameters are provided by lab bench tests and design simulation.

Typical Performance Characteristics

All test conditions: V_{DD} = 5 V, T_A = +25°C, unless otherwise noted.

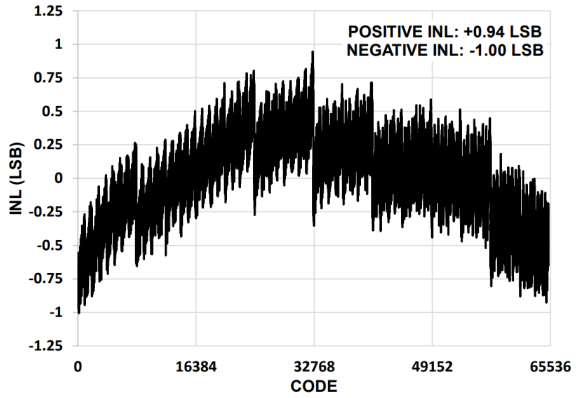


Figure 1. Integral Nonlinearity vs. Code, REF = 5 V

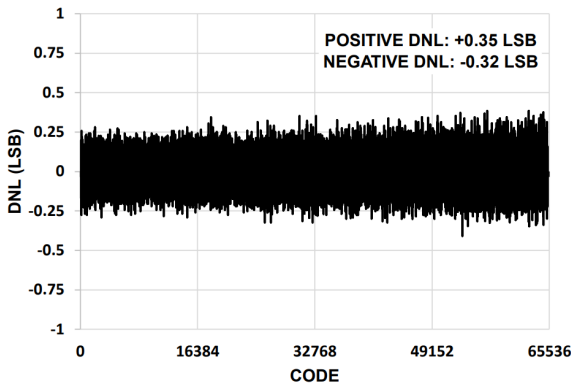


Figure 2. Differential Nonlinearity vs. Code, REF = 5 V

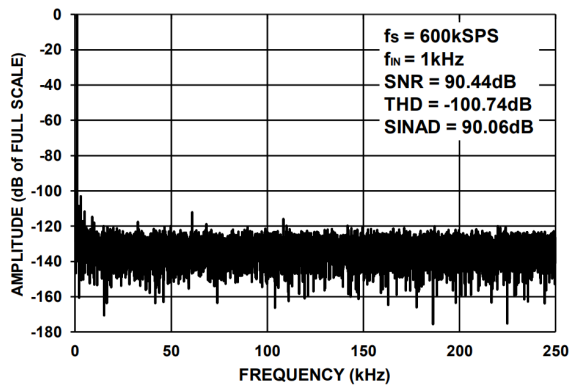


Figure 3. FFT Plot, REF = 5 V

Detailed Description

Overview

The TPC5161 is a 16-bit successive approximation register (SAR) ADC. The device is able to convert analog input into digital output without latency or pipeline delay, so it is ideal for multiple-channel applications.

When a conversion is initiated, the analog input is sampled on the internal capacitor, and then converted based on charge redistribution with the internal clock. During conversion, the input is disconnected from the internal capacitor.

After conversion, the device reconnects the sampling capacitors to input pins, and enters the acquisition phase.

Feature Description

Analog Input

Figure 4 is the equivalent input sampling circuit. The sampling switch is represented by a resistance in series with the ideal switch. The electrostatic discharge (ESD) protection diodes from both analog inputs are also shown in Figure 4.

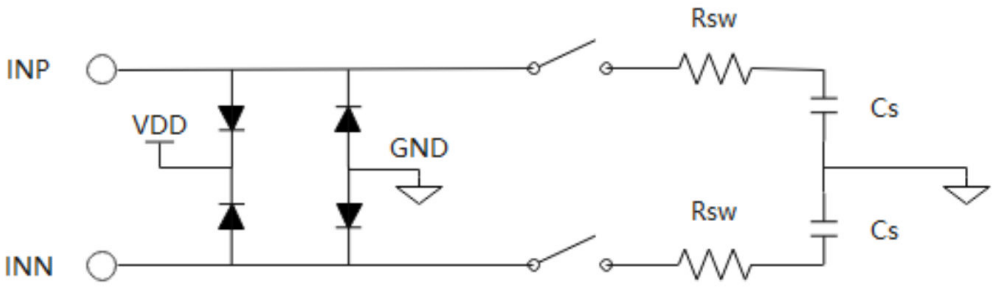


Figure 4. Equivalent Input Sampling Circuit

Reference

The device operates with an external reference voltage. During conversion, the internal capacitors are switched onto the reference terminal, and the dynamic charge is required. The switching frequency is proportional to the internal conversion clock frequency. A reference driver circuit is required to support the dynamic charge so that the noise and linearity performance of the device are not degraded.

ADC Transfer Function

The TPC5161 is a unipolar, pseudo-differential input device, and the output is in straight binary format.

The full-scale range for the ADC input (INP – INN) is equal to the reference input voltage to the ADC (VREF). The transfer equation is shown in the following table:

Description	Analog Input	Digital Output Code (Hex)
Full-Scale Range	V_{REF}	–
Least Significant Bit (LSB)	V_{REF} / 65536	–
Positive Full Scale	V_{REF} – 1 LSB	FFFF
Midscale	V_{REF} / 2	8000
Midscale – 1 LSB	(V_{REF} / 2) – 1 LSB	7FFF
Negative Full Scale	0 V	0000

Device Function Modes

The device offers $\overline{CS}$ mode and daisy-chain mode for interfacing with the host.

The mode in which the device operates depends on the SDI level when the CNV rising edge occurs. The device operates in $\overline{CS}$ mode if SDI is high at the CNV rising edge. The device operates in daisy-chain mode, if SDI is low at the CNV rising edge, or if SDI and CNV are connected together.

In $\overline{CS}$ mode, the device is compatible with SPI hosts. This interface can use a 3-wire or 4-wire interface. The 3-wire interface using CNV, SCK, and SDO signals, minimizes the wiring connections, so it is useful for isolation applications. The 4-wire interface using SDI, CNV, SCK, and SDO signals, allows users to sample the analog input independent of the serial interface timing, so is useful to control an individual device while having multiple similar devices on board.

In daisy-chain mode, multiple devices can be cascaded on a single data line similar to a shift register. This mode helps reduce component counts and signal traces on the board.

In both modes, the device can either operate with or without a busy indicator, where the busy indicator is a bit preceding the output data bits that can be used to interrupt the digital host and trigger the data transfer.

$\overline{CS}$ Mode

The device operates in $\overline{CS}$ mode if SDI is high at the CNV rising edge. There are four different interface options available in this mode: 3-wire $\overline{CS}$ mode without a busy indicator, 3-wire $\overline{CS}$ mode with a busy indicator, 4-wire $\overline{CS}$ mode without a busy indicator, and 4-wire $\overline{CS}$ mode with a busy indicator.

3-Wire $\overline{CS}$ Mode without a Busy Indicator

This mode is useful when a single ADC is connected to an SPI-compatible digital host.

In this mode, SDI can be connected to VIO. The CNV rising edge samples the input signal, causing the device to enter a conversion phase, and SDO is forced to 3-state. Conversion is done with the internal clock and continues regardless of the state of CNV. Therefore, CNV can be pulled low to select other devices on the board.

However, CNV must return and hold high before the conversion time elapses. A high level on CNV at the end of the conversion ensures that the device does not generate a busy indicator.

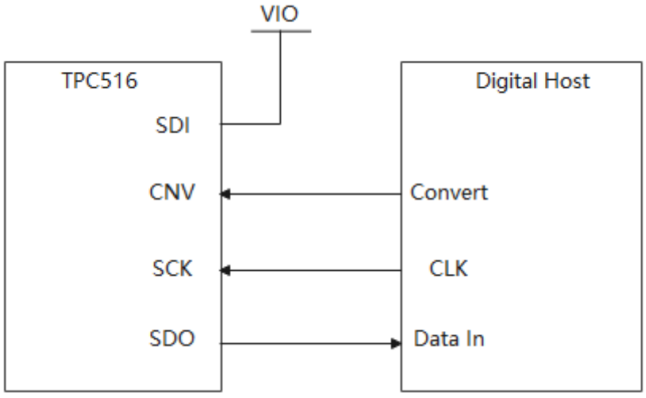


Figure 5. Connection Diagram: 3-Wire $\overline{CS}$ Mode without a Busy Indicator

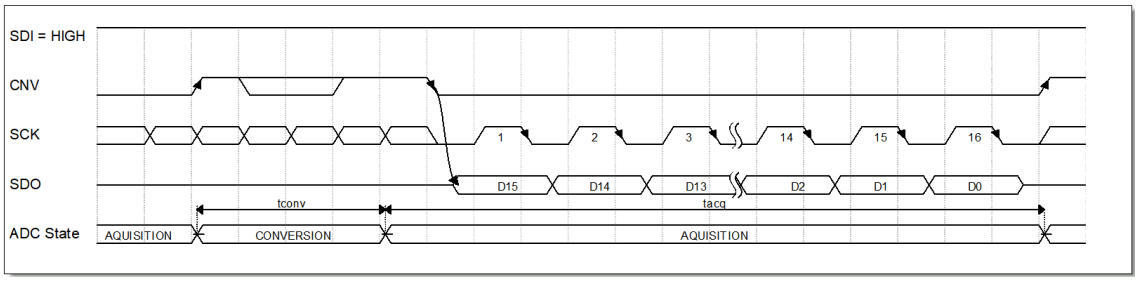


Figure 6. Timing Diagram: 3-Wire $\overline{CS}$ Mode without a Busy Indicator

On the CNV falling edge, SDO comes out of 3-state and the device outputs the MSB of the data at first, and then low data bits on subsequent SCK falling edges.

The data is valid on both SCK edges. The rising edge can be used to capture the data, and the SCK falling edge allows a faster reading rate if there is an acceptable hold time.

SDO goes to 3-state after the 16th SCK falling edge or when CNV goes high, whichever occurs first.

3-Wire $\overline{CS}$ Mode with a Busy Indicator

This mode is useful when a single ADC is connected to an SPI-compatible digital host and an interrupt-driven data transfer is required.

In this mode, SDI can be connected to VIO. The CNV rising edge samples the input signal, causing the device to enter a conversion phase, and SDO is forced to 3-state.

Conversion is done with the internal clock and continues regardless of the state of CNV. Therefore, CNV can be pulled low then to select other devices on the board.

A pull-up resistor on the SDO pin ensures that the $\overline{IRQ}$ pin of the digital host is held high when SDO is in 3-state.

However, CNV must be pulled low before the conversion time elapses. A low level of CNV at the end of the conversion ensures that the device generates a busy indicator.

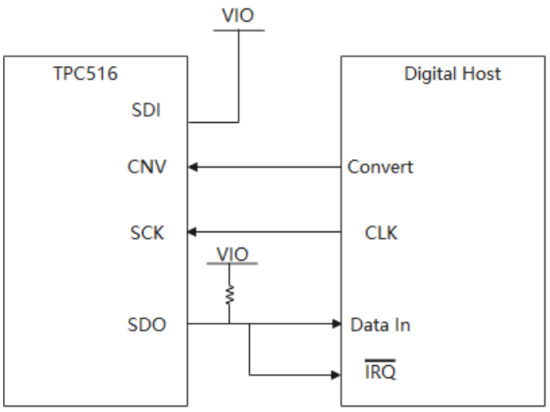


Figure 7. Connection Diagram: 3-Wire $\overline{CS}$ Mode with a Busy Indicator

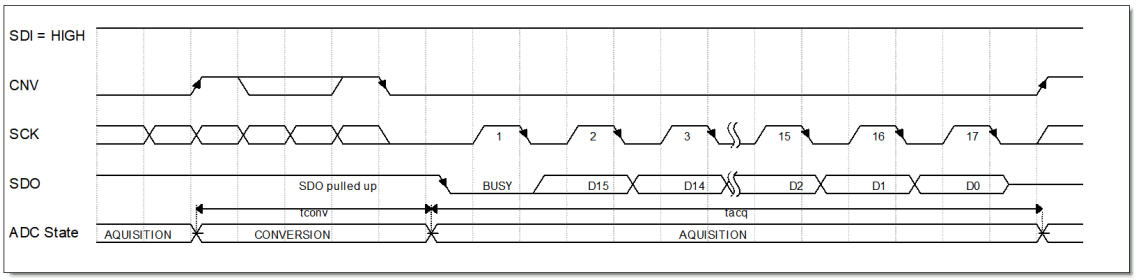


Figure 8. Timing Diagram: 3-Wire $\overline{CS}$ Mode with a Busy Indicator

When the conversion is complete, the device enters an acquisition state. SDO comes out of 3-state, and outputs a busy indicator bit (low level). This feature provides a high-to-low transition on the $\overline{IRQ}$ pin of the digital host.

Then the data bits are clocked out on the subsequent SCLK falling edges, MSB first.

The data is valid on both SCK edges. The rising edge can be used to capture the data, and the SCK falling edge allows a faster reading rate if there is an acceptable hold time.

SDO goes to 3-state after the 17th SCK falling edge or when CNV goes high, whichever occurs first.

4-Wire $\overline{CS}$ Mode without a Busy Indicator

This mode is useful when one or more ADC(s) are connected to an SPI-compatible digital host. Following is the connection diagram of the two ADCs.

In this mode, SDI is controlled by the digital host and functions as $\overline{CS}$.

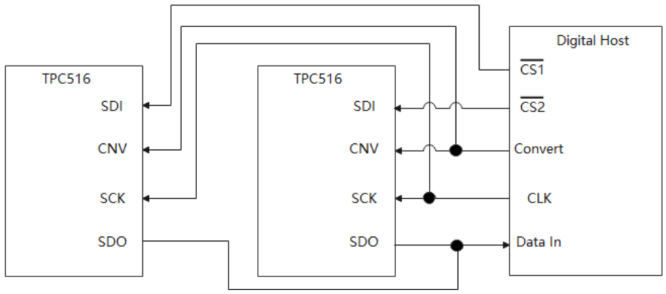


Figure 9. Connection Diagram: Two ADCs with 4-Wire $\overline{CS}$ Mode without a Busy Indicator

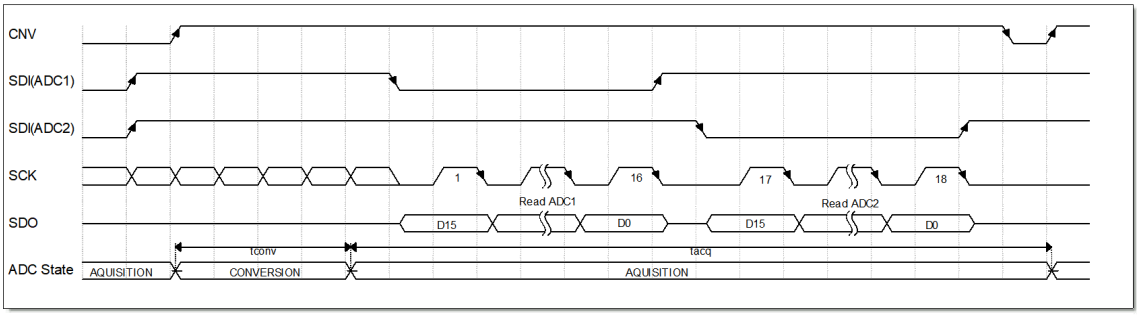


Figure 10. Timing Diagram: Two ADCs with 4-Wire $\overline{CS}$ Mode without a Busy Indicator

When SDI is high, the CNV rising edge samples the input signal, causes the device to enter a conversion phase, and forces SDO to 3-state.

In this mode, CNV must be held high from the start of the conversion until all data bits are read.

Conversion is done with the internal clock regardless of the state of SDI. Therefore, SDI (functioning as $\overline{CS}$) can be pulled low to select other devices on the board.

However, SDI must return and hold high before the conversion time elapses. A high level on SDI at the end of the conversion ensures that the device does not generate a busy indicator.

On the SDI falling edge, SDO comes out of 3-state and the device outputs the MSB of the data at first, and then low data bits on subsequent SCK falling edges.

The data is valid on both SCK edges. The rising edge can be used to capture the data, and the SCK falling edge allows a faster reading rate if there is an acceptable hold time.

SDO goes to 3-state after the 16th SCK falling edge or when SDI goes high, whichever occurs first.

When multiple devices are connected together on the same data bus, the SDI of the second device (functioning as $\overline{CS}$ for the second device) can go low after the first device data is read, and the SDO of the first device is in 3-state.

Be careful that the CNV and SDO of the device are not low together during the read cycle.

4-Wire $\overline{CS}$ Mode with a Busy Indicator

This mode is most useful when a single ADC is connected to a digital host and an interrupt-driven data transfer is desired.

In this mode, SDI is controlled by the digital host and functions as $\overline{CS}$.

A pull-up resistor on the SDO pin ensures that the $\overline{CS}$ pin of the digital host is held high when SDO is in 3-state.

When SDI is high, the CNV rising edge samples the input signal, causes the device to enter a conversion phase, and forces SDO to 3-state.

In this mode, CNV must be held high from the start of the conversion until all data bits are read.

Conversion is done with the internal clock regardless of the state of SDI. Therefore, SDI (functioning as $\overline{CS}$) can be pulled low to select other devices on the board.

However, CNV must be pulled low before the conversion time elapses. A low level of CNV at the end of the conversion ensures that the device generates a busy indicator.

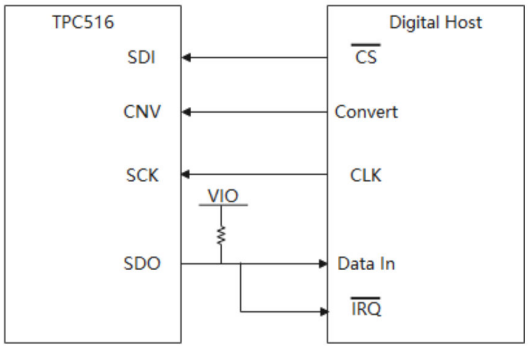


Figure 11. Connection Diagram: 4-Wire $\overline{CS}$ Mode with a Busy Indicator

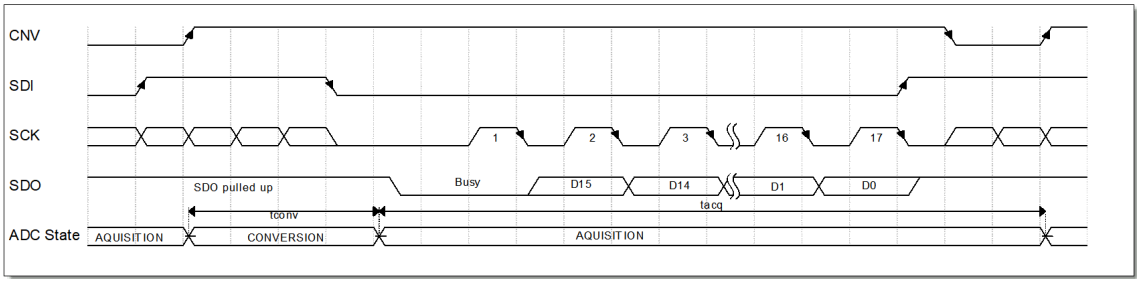


Figure 12. Timing Diagram: 4-Wire $\overline{CS}$ Mode wth a Busy Indicator

When the conversion is complete, the device enters an acquisition state. SDO comes out of 3-state, and outputs a busy indicator bit (low level). This feature provides a high-to-low transition on the $\overline{IRQ}$ pin of the digital host.

Then the data bits are clocked out on the subsequent SCLK falling edges, MSB first.

The data is valid on both SCK edges. The rising edge can be used to capture the data, and the SCK falling edge allows a faster reading rate if there is an acceptable hold time.

SDO goes to 3-state after the 17th SCK falling edge or when SDI goes high, whichever occurs first.

Be careful that the CNV and SDO of the device are not low together during the read cycle.

Daisy-Chain Mode

Daisy-chain mode is selected if SDI is low at the CNV rising edge or if SDI and CNV are connected together.

Daisy-Chain Mode without Busy Indicator

This mode is useful in applications where the digital host has limited interfacing capability with multiple ADCs.

In this mode, the CNV pins of all ADCs in the chain are connected together and controlled by a single pin of the digital host. The SCK pins are also connected together and controlled by a single pin of the digital host.

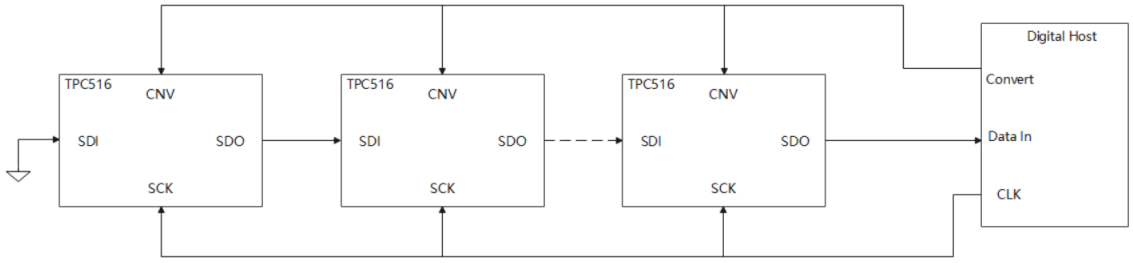


Figure 13. Connection Diagram: Daisy-Chain Mode without a Busy Indicator

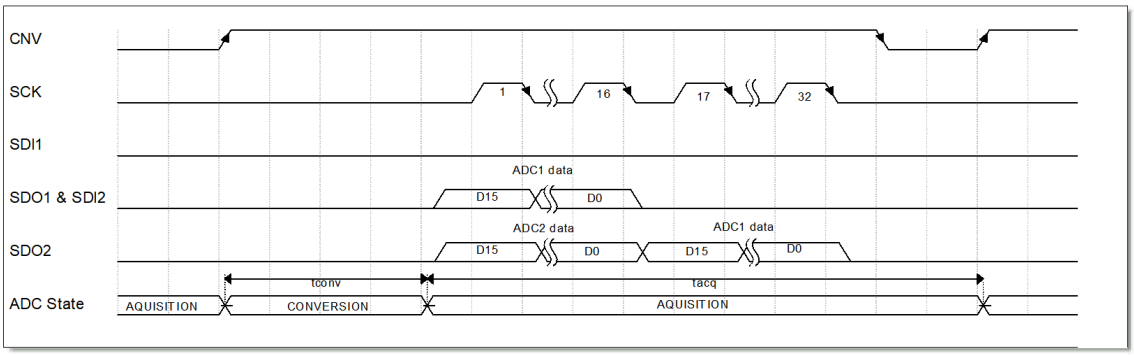


Figure 14. Timing Diagram: Daisy-Chain Mode without a Busy Indicator

The SDO pin is driven low when SDI and CNV are both low.

The CNV rising edge with SDI low selects daisy-chain mode, samples the analog input, and causes the device to enter a conversion phase.

In this mode, CNV must remain high from the start of the conversion until all data bits are read. When started, the conversion continues with the internal clock, regardless of the state of SCK.

However, SCK must be low at the CNV rising edge so that the device does not generate a busy indicator at the end of the conversion.

At the end of the conversion, every ADC in the chain outputs the MSB bit of the conversion result on its own SDO pin. The internal shift register of each ADC latches the data available on its SDI pin and shifts out the next bit of data on its SDO pin on every subsequent SCK falling edge.

Therefore, the digital host receives the data of ADC N at first (MSB first), followed by the data of ADC N–1, and so on. A total of 16 x N SCK falling edges are required to capture the outputs of all N devices in the chain.

The data is valid on both SCK edges. The rising edge can be used to capture the data, and the SCK falling edge allows a faster reading rate if there is an acceptable hold time.

Daisy-Chain Mode with a Busy Indicator

This mode is useful in applications where the digital host has limited interfacing capability with multiple ADCs, and an interrupt-driven data transfer is desired.

In this mode, the CNV pins of all ADCs in the chain are connected together and controlled by a single pin of the digital host. The SCK pins are also connected together and controlled by a single pin of the digital host.

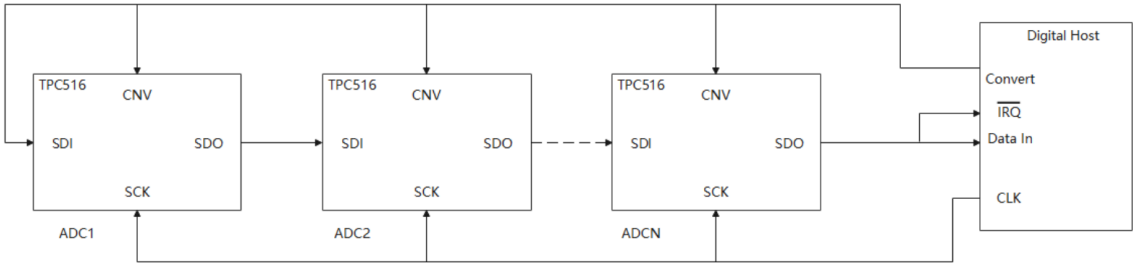


Figure 15. Connection Diagram: Daisy-Chain Mode with a Busy Indicator

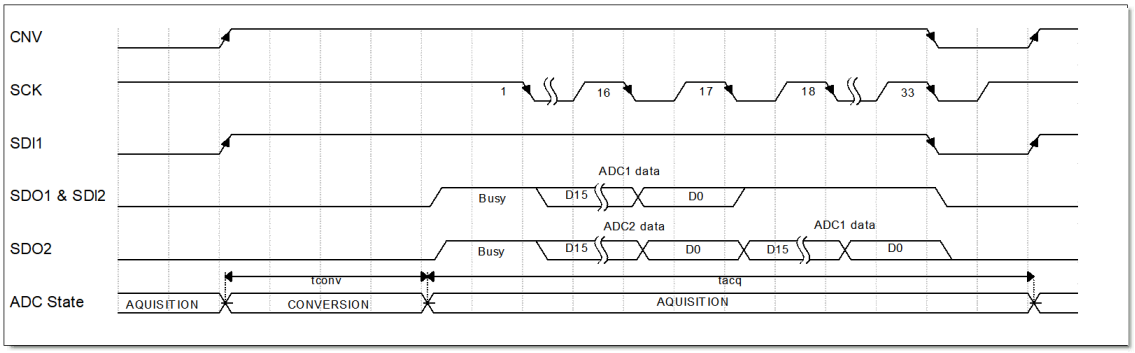


Figure 16. Timing Diagram: Daisy-Chain Mode with a Busy Indicator

The SDO pin is driven low when SDI and CNV are both low.

The CNV rising edge with SDI low selects daisy-chain mode, samples the analog input, and causes the device to enter a conversion phase.

In this mode, CNV must remain high from the start of the conversion until all data bits are read. When started, the conversion continues with the internal clock, regardless of the state of SCK.

However, SCK must be high at the CNV rising edge so that the device generates a busy indicator at the end of the conversion.

At the end of the conversion, every ADC in the chain forces its SDO pin high, providing a low-to-high transition on the $\overline{IRQ}$ pin of the digital host. The internal shift register of each ADC latches the data available on its SDI pin and shifts out the next bit of data on its SDO pin on every subsequent SCK falling edge. Therefore, the digital host receives the interrupt signal followed by the data of ADC N (MSB first), and then the data of ADC N–1, and so on. A total of (16 × N) + 1 SCK falling edges are

required to capture the outputs of all N devices in the chain. The busy indicator bits of ADC 1 to ADC N–1 do not propagate to the next device in the chain.

The data is valid on both SCK edges. The rising edge can be used to capture the data, and the SCK falling edge allows a faster reading rate if there is an acceptable hold time.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Typical Application

Figure 17 shows the typical application schematic.

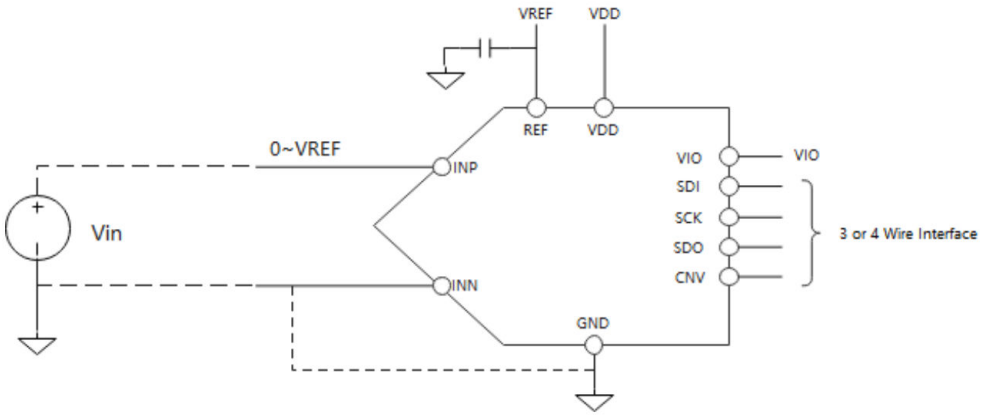
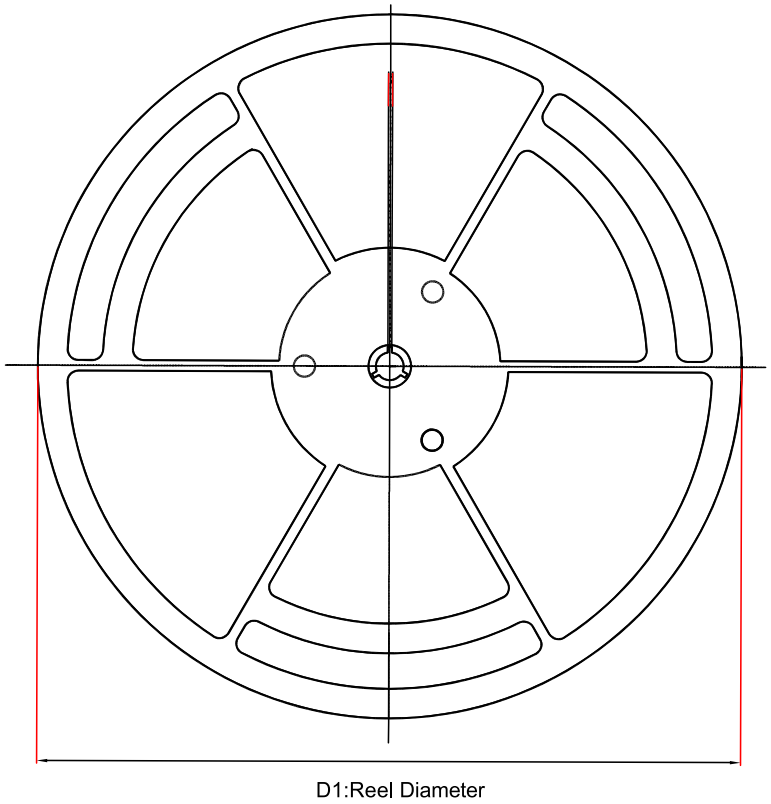
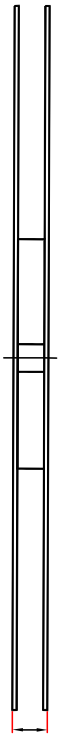
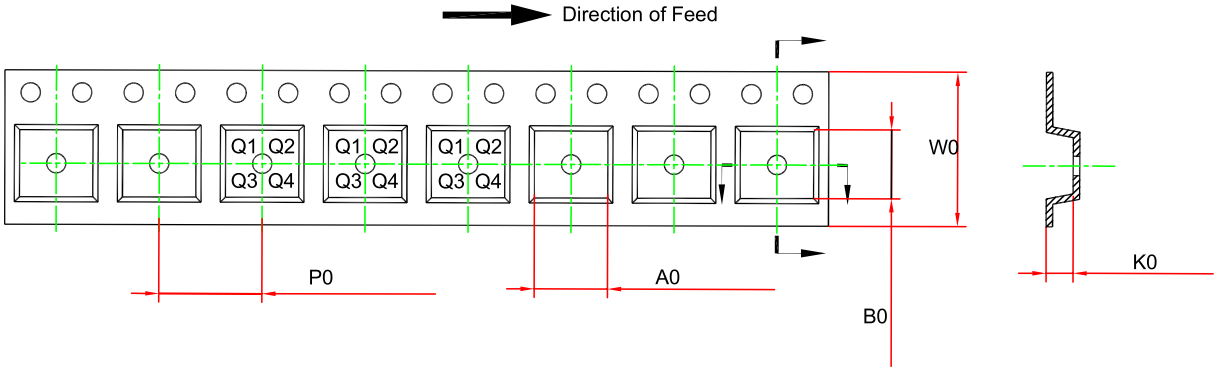


Figure 17. Typical Application Circuit

Tape and Reel Information





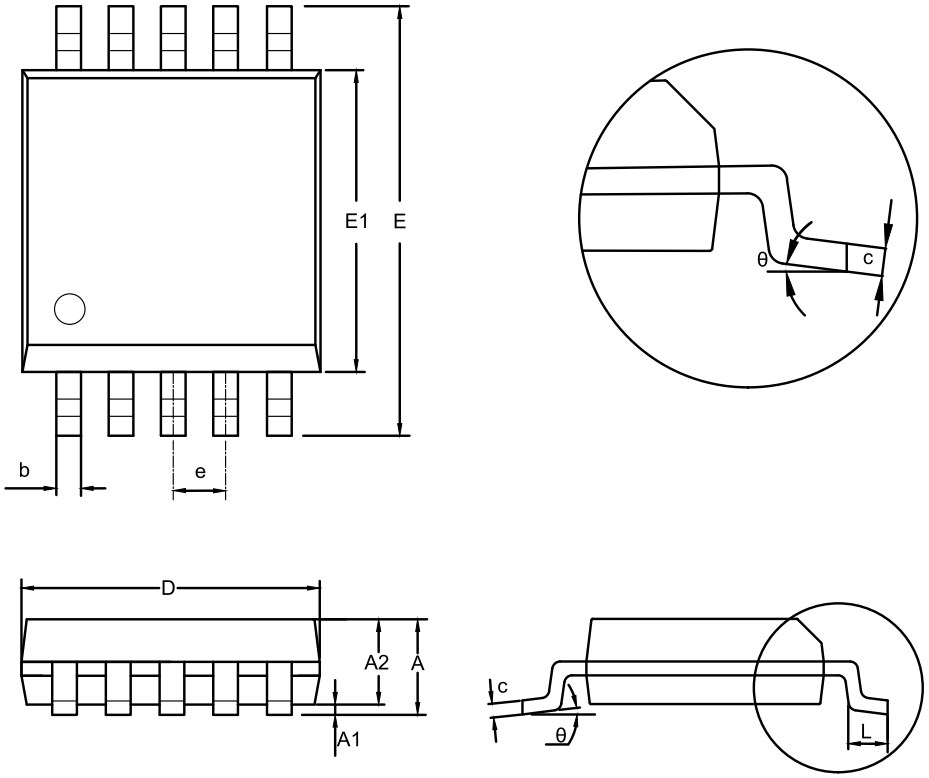


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPC5161-VS2R	MSOP10	330	17.6	5.3	3.4	1.4	8	12	Q1

Package Outline Dimensions

MSOP10

Package Outline Dimensions VS2(MSOP-10-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	1.100	0.031	0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	4.700	5.100	0.185	0.201
E1	2.900	3.100	0.114	0.122
e	0.500 BSC		0.020 BSC	
L	0.400	0.800	0.016	0.031
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPC5161-VS2R	−40 to 125°C	MSOP10	5161	1	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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