12-Bit 8-Channel SAR ADC with I²C Interface

Features

- 12-Bit SAR ADC with I²C Interface
- Unipolar, Differential Analog Input
- Reference
  - Internal 2.5-V Reference
  - External Reference
- I²C Interface supports following Modes:
  - Standard
  - Fast
  - High-Speed
- Package
  - TSSOP16
- Wide Operating Temperature Range
  - −40°C to +125°C

Applications

- Data Acquisitions
- Instruments
- Industry Measurement and Control
- Automatic Test Equipment
- Voltage Supply Monitoring

Description

The TPC502200 is a 12-bit analog-to-digital converter (ADC). The device supports 8-channel inputs with a multiplexer, and the inputs can be controlled by multiplexer configuration. The device has an internal reference, and also supports external reference.

The device has a serial I²C interface. The two-wire interface makes it suitable for multi-device applications on the same signal bus, or for applications with isolation.

The device is available in TSSOP-16 package.

Typical Application Circuit

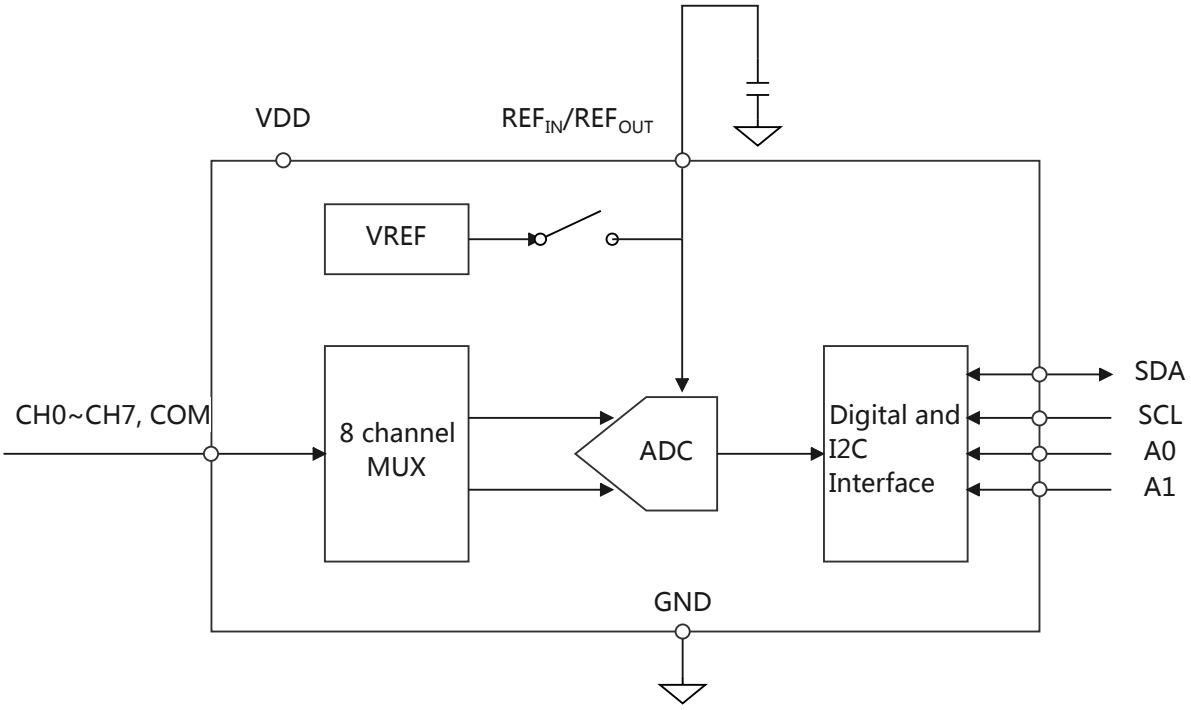


Table of Contents

Product Family Table

Order Number	ADC Channel	Interface	Package
TPC502200-TS3R-S	8	I²C	TSSOP16

Revision History

Date	Revision	Notes
2023-08-30	Rev.A.0	Initial released
2024-07-31	Rev.A.1	1. Updated Timing specification 2. Changed Figure 4, 5, and 6 3. Updated Additional description of reading in F/S mode 4. Added Typical performance characteristics figures 5. Added Example board layout

Pin Configuration and Functions

TPC502200
TSSOP16
Top View

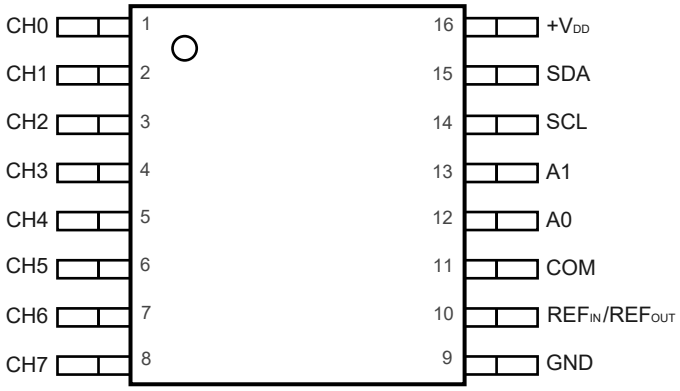


Table 1. Pin Functions: TPC502200

Pin		I/O	Description
No.	Name		
1	CH0	Input	Analog Input 0
2	CH1	Input	Analog Input 0
3	CH2	Input	Analog Input 0
4	CH3	Input	Analog Input 0
5	CH4	Input	Analog Input 0
6	CH5	Input	Analog Input 0
7	CH6	Input	Analog Input 0
8	CH7	Input	Analog Input 0
9	GND	Power	Ground
10	REFIN/REFOUT	Input/Output	Internal Reference, and External Reference Input
11	COM	Input	Common analog Input
12	A0	Input	Slave address bit 0
13	A1	Input	Slave address bit 1
14	SCL	Input	Serial clock
15	SDA	Input/Output	Serial data
16	VDD	Power	Power supply

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
	VDD to GND	–0.3	6	V
	Digital IO to GND	–0.3	VDD + 0.3	V
	Analog IO to GND	–0.3	VDD + 0.3	V
	Operating Temperature	−40	125	°C
T_{STG}	Storage temperature, Tstg	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Nom	Max	Unit
V_{DD}	Analog Supply Voltage	2.7		5	V
T_A	Operating Ambient Temperature	–40		125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
TSSOP16	114	50	°C/W

Electrical Characteristics

All test conditions is at VDD = 2.7 V to 5 V, T_A = −40°C to +125°C, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit
Analog Input					
Full-Scale Input Scan	Positive Input - Negative Input	0		V_{REF}	V
Absolute Input Range	Positive Input	−0.2		+VDD+0.2	V
	Negative Input	−0.2		0.2	V
Capacitance			16		pF
Leakage Current		−10	±1	10	μA
System Performance					
No Missing Codes		12			Bits
Integral Linearity Error	VDD = 5 V, V_{REF} = 5 V	−1	±0.4	+1	LSB
Differential Linearity Error	VDD = 5 V, V_{REF} = 5 V	−0.99	±0.3	+1	LSB
Offset Error	VDD = 2.7 V, V_{REF} = 2.5 V	−2	±0.75	+2	LSB
	VDD = 5 V, V_{REF} = 5 V	−2	±0.75	+2	LSB
Offset Error Match	VDD = 2.7 V, V_{REF} = 2.5 V		±0.5		LSB
	VDD = 5 V, V_{REF} = 5 V		±0.5		LSB
Gain Error	VDD = 2.7 V, V_{REF} = 2.5 V	−3	±0.75	+3	LSB
	VDD = 5 V, V_{REF} = 5 V	−2.5	±0.75	+2.5	LSB
Gain Error Match	VDD = 2.7 V, V_{REF} = 2.5 V		±0.25		LSB
	VDD = 5 V, V_{REF} = 5 V		±0.5		LSB
Power-Supply Rejection			79		dB
Sampling Dynamics					
Throughput Frequency	High Speed Mode: SCL = 3.4 MHz			40	kHz
	Fast Mode: SCL = 400 kHz			8	kHz
	Standard Mode: SCL = 100 kHz			2	kHz
Conversion Time			3.5		μs
AC Accuracy					
Total Hatmonic Distortion	Vin at 1 kHz VDD = 5 V, V_{REF} = 5 V		−89		dB
Signal-to-Noise Ratio	Vin at 1 kHz VDD = 5 V, V_{REF} = 5 V		72		dB
Signal-to-(Noise+Distortion) Ratio	Vin at 1 kHz VDD = 5 V, V_{REF} = 5 V		72		dB
Voltage Reference Output					
Range		2.475	2.5	2.525	V
Internal Reference Drift			8		ppm/℃
Output Impedance	Internal Reference ON		25		Ω

Parameter	Conditions		Min	Typ	Max	Unit
Voltage Reference Input						
Range			0.05		VDD	V
Resistance				29.4		kΩ
Current Drain	High Speed Mode: SCL = 3.4 MHz			85		μA
Digital Input/Output						
Logic Family				CMOS		
Logic Levels:V_{IH}			VDD*0.7			V
V_{IL}					VDD*0.3	V
V_{OL}					0.4	V
Input Leakage: I_{IH}	V_{IH} = VDD +0.3			10		μA
I_{IL}	V_{IL} = −0.3			-10		μA
Data Format				Straight Binary		
HARDWARE ADDRESS				10010		Binary
Power Supply Requirements						
Power-Supply Voltage, VDD	Specified Performance		2.7		5.25	V
Quiscent Current	2.7-V Supply	High Speed Mode: SCL = 3.4 MHz		210		μA
	5-V Supply	High Speed Mode: SCL = 3.4 MHz		210		μA
Power-Down Mode w/ Wrong Address Selected	2.7-V Supply	High Speed Mode: SCL = 3.4 MHz		200	250	μA
	5-V Supply	High Speed Mode: SCL = 3.4 MHz		210	300	μA
Full Power-Down	SCL Pulled HIGH,SDA Pulled HIGH			20		μA
Temperature Range						
Specified Performance			−40		+125	℃

Timing Requirements (1)

All test conditions is at VDD = 2.7 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise noted.

Parameter		Conditions	Min	Max	Units
f_{SCL}	SCL Clock Frequency	Standard Mode		100	kHz
		Fast Mode		400	kHz
		High-Speed Mode, C_B = 100 pF max		3.4	MHz
		High-Speed Mode, C_B = 400 pF max		1.7	MHz
t_{BUF}	Bus Free Time Between a STOP and START Condition	Standard Mode	4.7		µs
		Fast Mode	1.3		µs
$t_{HD;STA}$	Hold Time (Repeated) START Condition	Standard Mode	4		µs
		Fast Mode	600		ns
		High-Speed Mode	160		ns
t_{LOW}	LOW Period of the SCL Clock	Standard Mode	4.7		µs
		Fast Mode	1.3		µs
		High-Speed Mode, C_B = 100 pF max	160		ns
		High-Speed Mode, C_B = 400 pF max	320		ns
t_{HIGH}	HIGH Period of the SCL Clock	Standard Mode	4		µs
		Fast Mode	600		ns
		High-Speed Mode, C_B = 100 pF max	60		ns
		High-Speed Mode, C_B = 400 pF max	120		ns
$t_{SU;STA}$	Setup Time for a Repeated START Condition	Standard Mode	4.7		µs
		Fast Mode	600		ns
		High-Speed Mode	160		ns
$t_{SU;DAT}$	Data Setup Time	Standard Mode	250		ns
		Fast Mode	100		ns
		High-Speed Mode	10		ns
$t_{HD;DAT}$	Data Hold Time	Standard Mode	0	3.45	µs
		Fast Mode	0	0.9	µs
		High-Speed Mode, C_B = 100 pF max	0	70	ns
		High-Speed Mode, C_B = 400 pF max	0	150	ns
t_{RCL}	Rise Time of SCL Signal	Standard Mode		1000	ns
		Fast Mode	20 + 0.1C_B	300	ns
		High-Speed Mode, C_B = 100 pF max	10	40	ns
		High-Speed Mode, C_B = 400 pF max	20	80	ns
t_{RCL1}	Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge Bit	Standard Mode		1000	ns
		Fast Mode	20 + 0.1C_B	300	ns
		High-Speed Mode, C_B = 100 pF max	10	80	ns

Parameter		Conditions	Min	Max	Units
		High-Speed Mode, C_B = 400 pF max	20	160	ns
t_{FCL}	Fall Time of SCL Signal	Standard Mode		300	ns
		Fast Mode	20 + 0.1C_B	300	ns
		High-Speed Mode, C_B = 100 pF max	10	40	ns
		High-Speed Mode, C_B = 400 pF max	20	80	ns
t_{RDA}	Rise Time of SDA Signal	Standard Mode		1000	ns
		Fast Mode	20 + 0.1C_B	300	ns
		High-Speed Mode, C_B = 100 pF max	10	80	ns
		High-Speed Mode, C_B = 400 pF max	20	160	ns
t_{FDA}	Fall Time of SDA Signal	Standard Mode		300	ns
		Fast Mode	20 + 0.1C_B	300	ns
		High-Speed Mode, C_B = 100 pF max	10	80	ns
		High-Speed Mode, C_B = 400 pF max	20	160	ns
$t_{SU;\ STO}$	Setup Time for STOP Condition	Standard Mode	4		μs
		Fast Mode	600		ns
		High-Speed Mode	160		ns
C_B	Capacitive Load for SDA and SCL Line			400	pF
t_{SP}	Pulse Width of Spike Suppressed	Fast Mode		50	ns
		High-Speed Mode		25	ns
V_{NH}	Noise Margin at the HIGH Level for Each Connected Device (Including Hysteresis)	Standard Mode	0.2VDD		V
		Fast Mode			
		High-Speed Mode			
V_{NL}	Noise Margin at the LOW Level for Each Connected Device (Including Hysteresis)	Standard Mode	0.1VDD		V
		Fast Mode			
		High-Speed Mode			

(1) Parameters are provided by lab bench test and design simulation.

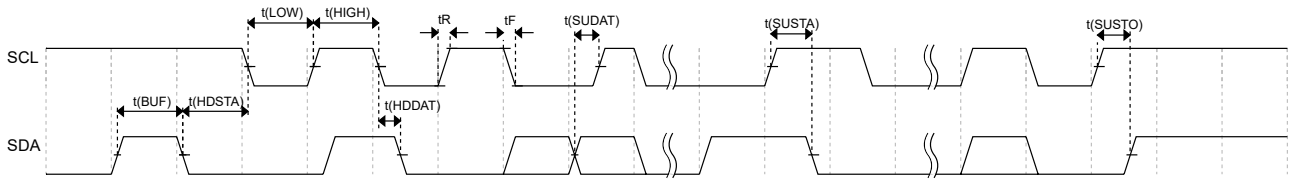


Figure 1. Timing Diagram

Typical Performance Characteristics

All test conditions: V_{REF} = 2.5 V External, VDD = 2.7 V, f_{SAMPLE} = 50 kHz, f_{IN} = 1 kHz, T_A = 25°C, unless otherwise noted.

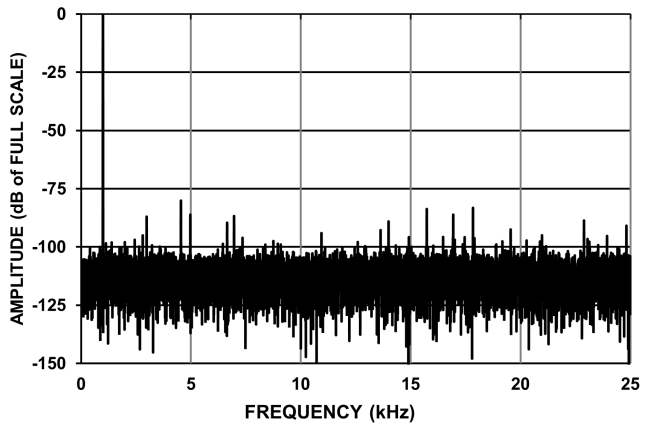


Figure 2. FFT

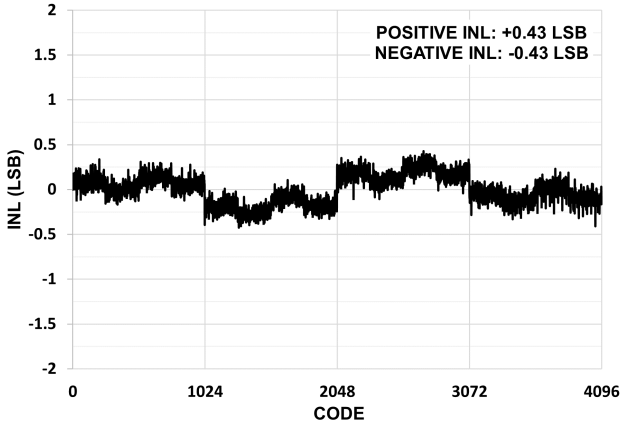


Figure 3. INL 2.5V Internal Reference

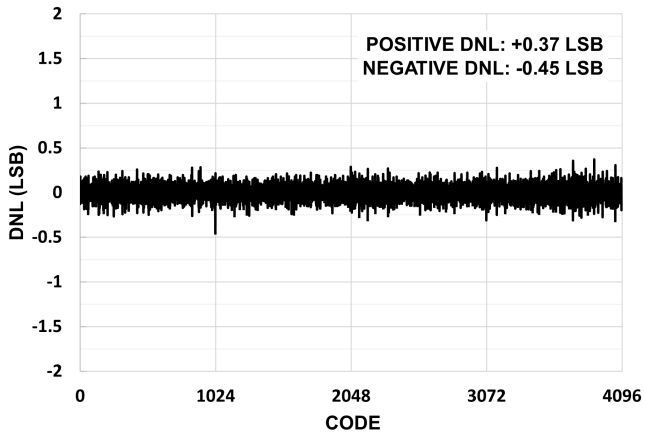


Figure 4. DNL 2.5V Internal Reference

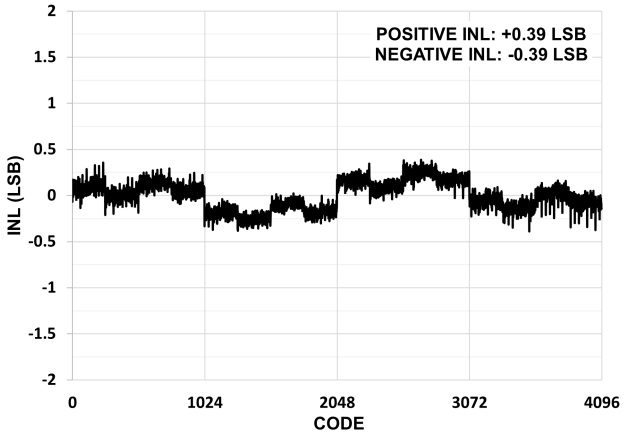


Figure 5. INL 2.5V External Reference

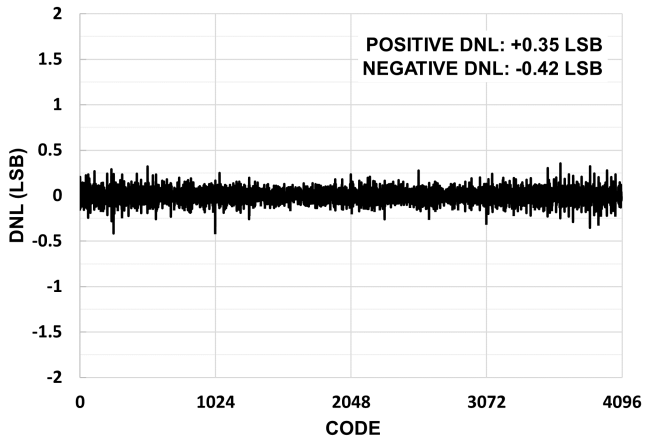


Figure 6. DNL 2.5V External Reference

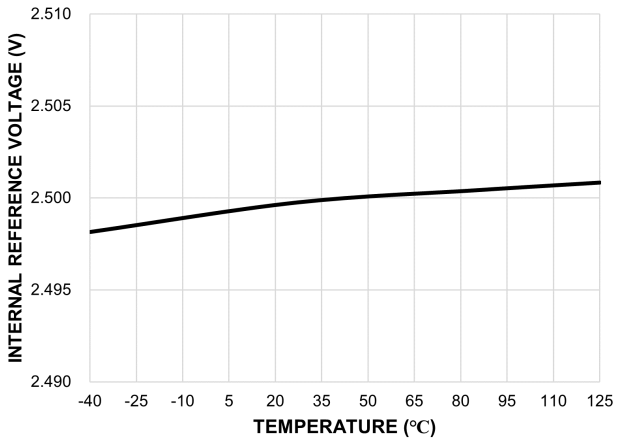


Figure 7. Internal Reference Voltage vs. Temperature

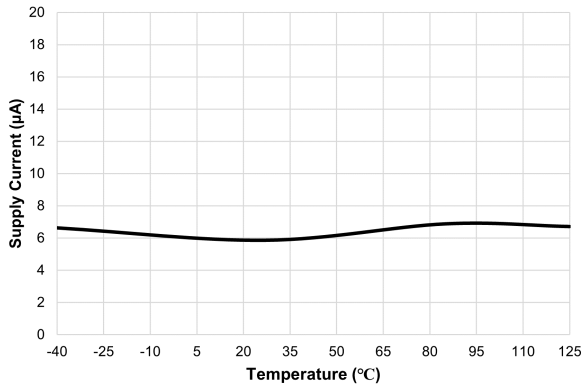


Figure 8. Power-Down Supply Current vs. Temperature

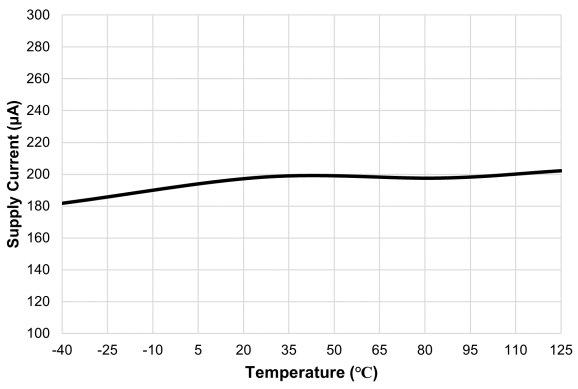


Figure 9. Supply Current vs. Temperature

Detailed Description

Overview

The TPC502200 is a 12-bit successive approximation register (SAR) ADC with I²C interface. The device is capable to convert analog input into digital output without latency or pipeline delay, so it is ideal for multiple channel applications. When a conversion is initiated, the analog input is sampled on the internal capacitor, and then converted based on charge redistribution with an internal clock. During conversion, the input is disconnected from the internal capacitor.

After conversion, the device reconnects the sampling capacitors to input pins and enters the acquisition phase.

Functional Block Diagram

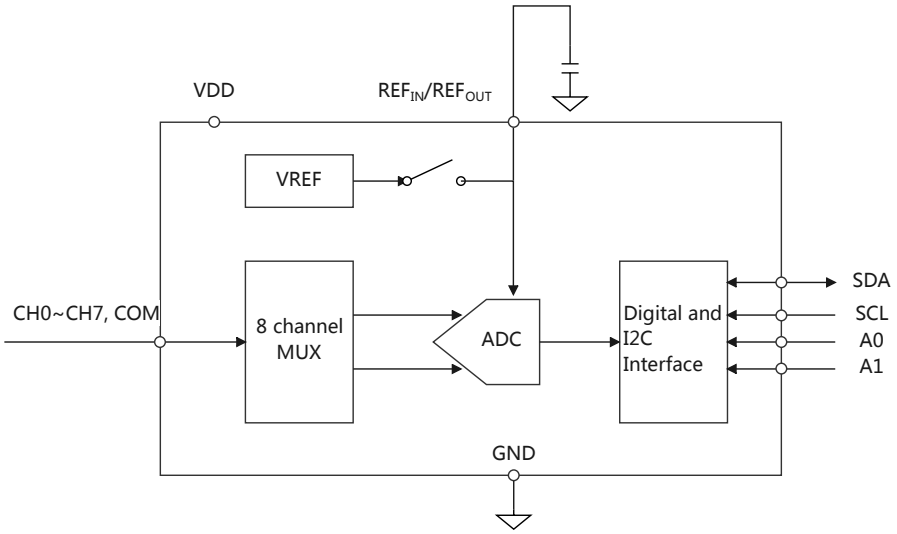


Figure 10. Functional Block Diagram

Analog Input

When the converter is in hold mode, it samples the voltage at the selected CHx pin and stores it in the internal capacitor array. The amount of current drawn from the analog inputs depends on the conversion rate of the device. During the sampling period, it is essential for the source to charge the internal sampling capacitor, typically 16 pF. Once the capacitor is fully charged, there is no further input current. The quantity of charge transferred from the analog source to the converter is determined by the conversion rate.

Reference

The device offers the flexibility of using either an internal 2.5-V reference or an external reference for operation. In cases where a +5-V supply is employed, an external +5-V reference becomes necessary to maximize the dynamic range for analog inputs spanning from 0 V to $+V_{DD}$. This external reference can be as low as 50 mV. However, when utilizing a +2.7-V supply, the internal +2.5-V reference suffices to cover the full dynamic range for analog inputs ranging from 0 V to $+V_{DD}$.

Digital Interface

The device is compatible with the I2C serial bus and data transmission protocol, supporting all three modes: standard, fast, and high-speed. Within this protocol, a device responsible for transmitting data onto the bus is referred to as a transmitter, while a device receiving data is known as a receiver. The device initiates and controls the communication process is designated as the "master," while the devices under the master's control are called "slaves." It is crucial for the bus to be under the control of a master device, which performs tasks such as generating the serial clock (SCL), managing bus access, and initiating the START and STOP conditions. In the context of I2C, the ADC operates as a slave device on the bus. Connections to the bus are established via the open-drain I/O lines, specifically SDA and SCL.

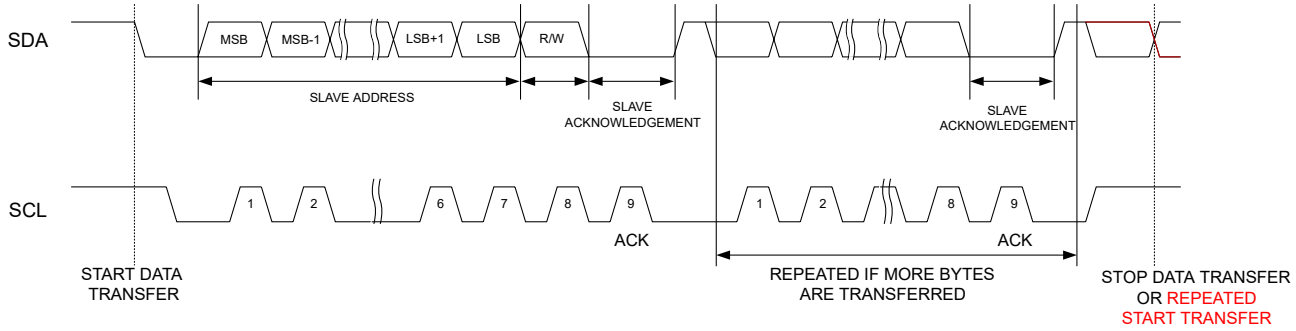


Figure 11. Basic Operation Diagram

The bus protocol has been defined as follows:

- In the defined bus protocol, it's specified that data transfer can only be initiated when the bus is not currently engaged or "busy". This means that before starting any data transfer, it is essential to check and ensure that the bus is in an idle state, available for communication.
- The data line must maintain a stable state when the clock line is in a HIGH state. Any alterations or changes in the data line while the clock line is HIGH will be interpreted as control signals rather than data bits.
- Bus not busy: Both data and clock lines are HIGH.
- Start data transfer: During a start condition, the SDA (Serial Data) line transitions from high to low while the SCL (Serial Clock) line is high. This signals the beginning of a data transfer or communication session.
- Stop data transfer: During a stop condition, the SDA line transitions from low to high while the SCL line is high. This signals the end of the communication session, and the bus is released.
- Data valid: The data line (SDA) is considered to be in a state of valid data when, following a START condition, the data on the SDA line remains stable and can be reliably read for the entire duration of the HIGH period of the clock signal (SCL). There is one clock pulse per bit of data.
  Each data transfer begins with a START condition and ends with a STOP condition. The number of data bytes that can be transferred between the START and STOP conditions is not limited and it is determined by the master device. After each byte of data is transferred, the receiving device (the slave) acknowledges the receipt of the data by sending an acknowledgment bit (ACK) or not-acknowledgment bit (NACK) as the ninth bit.
  The I²C bus specification defines three different modes of operation based on clock rates: standard mode (100 kHz clock rate), fast mode (400 kHz clock rate), and highspeed mode (3.4 MHz clock rate). The device supports all the modes.
- Acknowledgment: This a signal sent by the receiving device (usually a slave device) to acknowledge the successful receipt of data from the transmitting device (usually the master device) each byte. After the transmission of each byte, the sender releases the SDA (Serial Data) line and waits for the receiver's acknowledgment. The receiver (slave) acknowledges the successful reception of the data byte by pulling the SDA line low for a brief moment during the ACK bit time (usually the ninth clock cycle). This brief low pulse of the SDA line serves as an acknowledgment, indicating that the data was received without error and that the receiver is ready to accept the next byte of data.

Address Byte

The address byte represents the initial byte received immediately after the master device initiates the START condition. Within this address byte, the first five bits, also referred to as the Most Significant Bits (MSBs), are pre-programmed at the factory to a fixed value of 10010. The subsequent two bits in the address byte, designated as the device select bits A1 and A0, are determined by the state of input pins A1 through A0 on the device itself. These two bits are responsible for specifying the unique device address for each individual device. Consequently, it is possible to connect a maximum of four devices that share this pre-set code on the same bus simultaneously.

The state of the A1 and A0 Address Inputs can be configured by connecting them to either V_{DD} (the power supply voltage) or digital ground (GND). It's important to note that the device address for the ADC is determined by the specific state of these A1 and A0 pins while powering up.

The last bit within the address byte, known as the R/$\overline{W}$ (Read/Write) bit, specifying the type of operation to be executed. When the bit is set to 1, it signifies that a read operation is selected. Conversely, when the R/W bit is set to 0, it signifies a write operation. Following the initiation of the START condition, the device observes the state of the SDA bus, where the device type identifier is being transmitted. Upon successful reception of the complete identifier, which is the 10010 code, the appropriate device select bits, and the R/$\overline{W}$ bit in the correct sequence, the slave device promptly responds by transmitting an acknowledge signal along the SDA line. This acknowledgment signal serves as confirmation that the ADC has identified the master's request and is prepared to proceed with the requested read or write operation.

Address Byte							
MSB	6	5	4	3	2	1	LSB
1	0	0	1	0	A1	A0	R/$\overline{W}$

Command Byte

The operation mode of the ADC is dictated by a command byte, as shown below.

Command Byte							
MSB	6	5	4	3	2	1	LSB
SD	C2	C1	C0	PD1	PD0	X	X
SD: Single-Ended/ Differential Inputs 0: Differential Inputs 1: Single-Ended Inputs	C[2:0]: Channel Selections			PD[1:0]: Power-Down Selection 00: Power Down Between ADC Conversions 01: Internal Reference OFF and ADC ON 10: Internal Reference ON and ADC OFF 11: Internal Reference ON and ADC ON		Unused	Unused

Channel Selection Control												
SD	C2	C1	C0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	0	+IN	−IN	X	X	X	X	X	X	X
0	0	0	1	X	X	+IN	−IN	X	X	X	X	X
0	0	1	0	X	X	X	X	+IN	−IN	X	X	X
0	0	1	1	X	X	X	X	X	X	+IN	−IN	X
0	1	0	0	−IN	+IN	X	X	X	X	X	X	X
0	1	0	1	X	X	−IN	+IN	X	X	X	X	X
0	1	1	0	X	X	X	X	−IN	+IN	X	X	X
0	1	1	1	X	X	X	X	X	X	−IN	+IN	X
1	0	0	0	+IN	X	X	X	X	X	X	X	−IN

Channel Selection Control												
1	0	0	1	X	X	+IN	X	X	X	X	X	−IN
1	0	1	0	X	X	X	X	+IN	X	X	X	−IN
1	0	1	1	X	X	X	X	X	X	+IN	X	−IN
1	1	0	0	X	+IN	X	X	X	X	X	X	−IN
1	1	0	1	X	X	X	+IN	X	X	X	X	−IN
1	1	1	0	X	X	X	X	X	+IN	X	X	−IN
1	1	1	1	X	X	X	X	X	X	X	+IN	−IN

Initiating Conversion

When the master device addresses the ADC for a write operation, the device activates its ADC section. It initiates analog-to-digital conversions upon receiving BIT 4 of the command byte from the master. If the received command byte is correct, the ADC responds with an ACK (acknowledgment) condition.

Reading Data

The device allows data to be read from it by read-addressing the device (setting the LSB of the address byte to 1) and then receiving the transmitted bytes. However, data can only be read from the device after a conversion has been initiated. The data returned from the ADC is provided in a 12-bit format, which is split into two bytes, Byte0 first and followed by Byte1. D11 is the MSB of the data word, and D0 is the LSB

Reading Data Byte								
	MSB	6	5	4	3	2	1	LSB
BYTE 0	0	0	0	0	D11	D10	D9	D8
BYTE 1	D7	D6	D5	D4	D3	D2	D1	D0

Reading in F/S mode

In Fast or Standard (F/S) mode of operation, the interaction between the master and the slave device is shown below. After reading the conversion data, it's possible for the master to issue a repeated START condition to the device. This action is taken to maintain bus operation for subsequent conversions of the ADC. Using a repeated START condition is considered an efficient way to perform continuous conversions without the need to release and reacquire control of the bus for each conversion cycle.

It should be noticed that the STOP after write command will be ignored in either Fast or Standard mode. The analog input will be sampled at the end of next repeated START command and converted on arrival of read command.

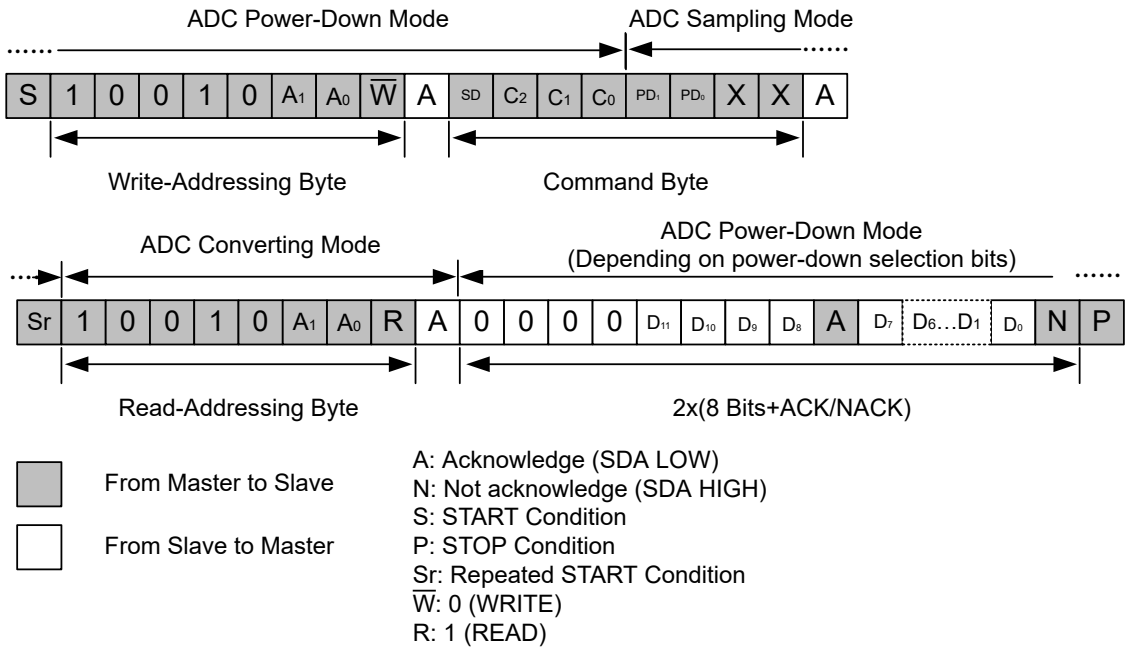


Figure 12. Typical reading in F/S mode

Reading in HS mode

In High-Speed (HS) mode of operation, the data transfer rate is sufficiently fast that individual conversion codes can be read out one at a time. However, in HS mode, there isn't enough time for a single conversion to complete between the reception of a repeated START condition and the read-addressing byte. The device employs a clock-stretching mechanism. After the read-addressing byte has been fully received, the device holds the clock signal (SCL) LOW until the ongoing conversion is complete.

The figure belowed provides a example of a typical read sequence in High-Speed (HS) mode, including the transition from Fast or Standard (F/S) mode to HS mode. In some scenarios, it can be advantageous to continue operating in HS mode after reading a conversion result. To achieve this, it's recommended to issue a repeated START condition at the end of the read sequence instead of a STOP condition. This is because issuing a STOP condition would cause the device to revert to F/S mode. By using a repeated START condition, user can effectively signal to the device that wish to maintain the HS mode for subsequent operations, avoiding the transition back to F/S mode.

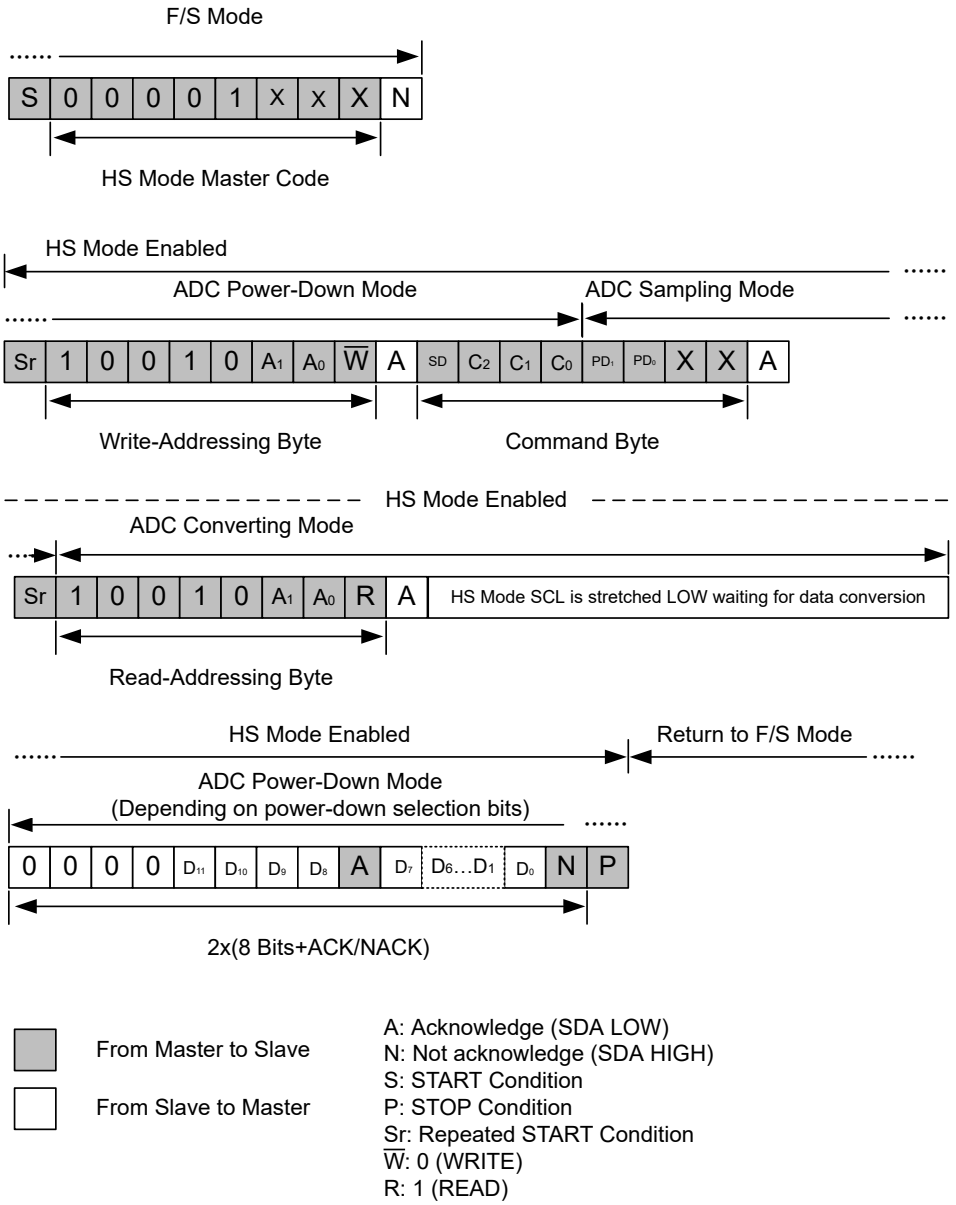


Figure 13. Typical reading in HS mode

Reading with reference on/off

The default setting for the internal reference voltage in the ADC is off when the device is powered on. To control the state of the internal reference voltage (either turning it on or off), refer to command byte table for the appropriate configuration settings. It's should be noted that if you frequently toggle the reference voltage (whether internal or external) on and off, user must account for a sufficient settling time before initiating a standard conversion cycle. The necessary settling time can vary depending on the specific configuration used.

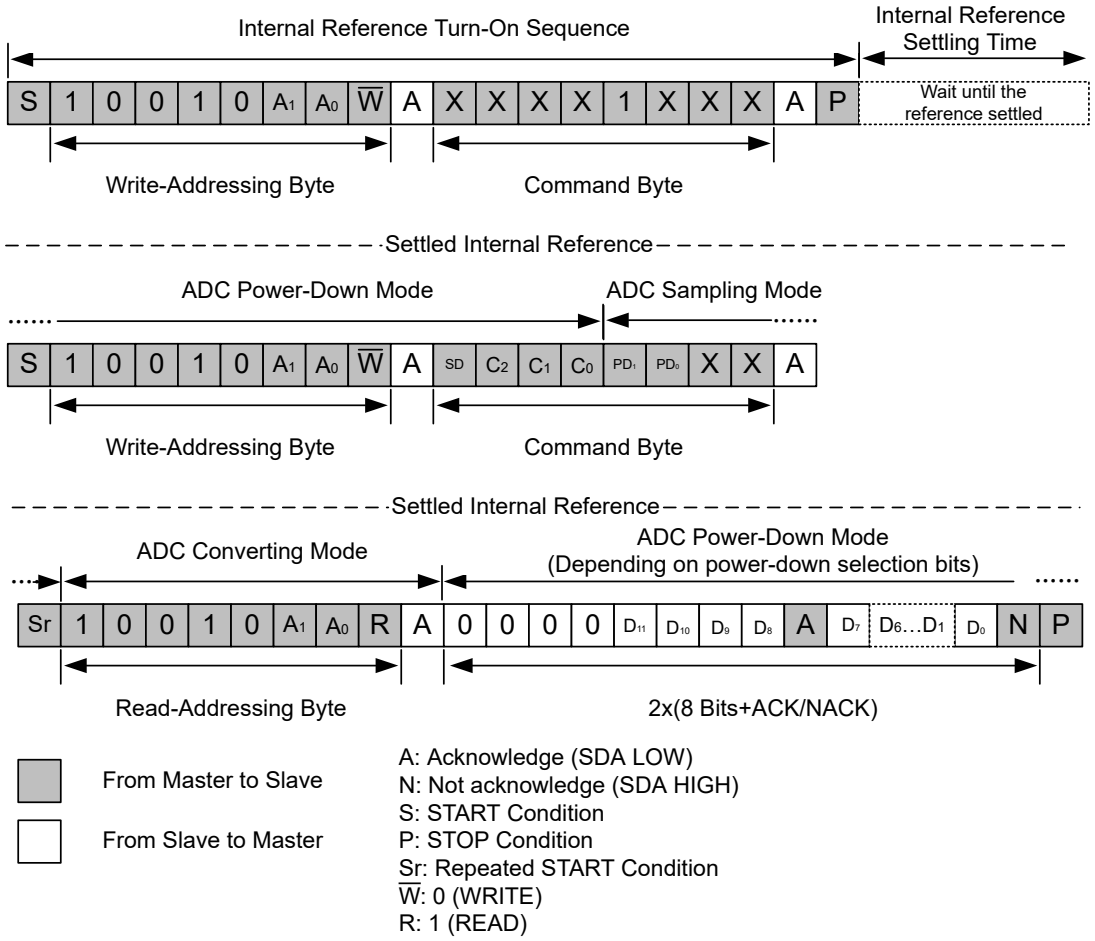


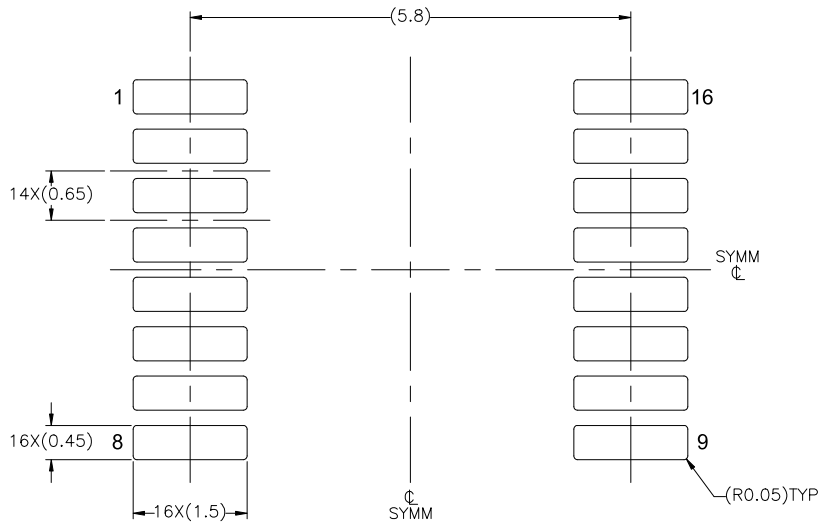
Figure 14. Typical reading in F/S mode with Reference Turn-On

Layout

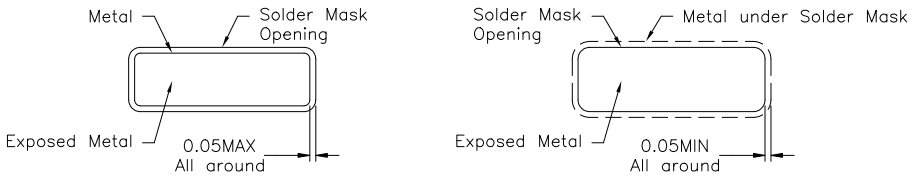
Layout Example

The figure below shows the example board layout.

Example Board Layout TS3(TSSOP-16-A)



Land Pattern Example
Exposed Metal shown



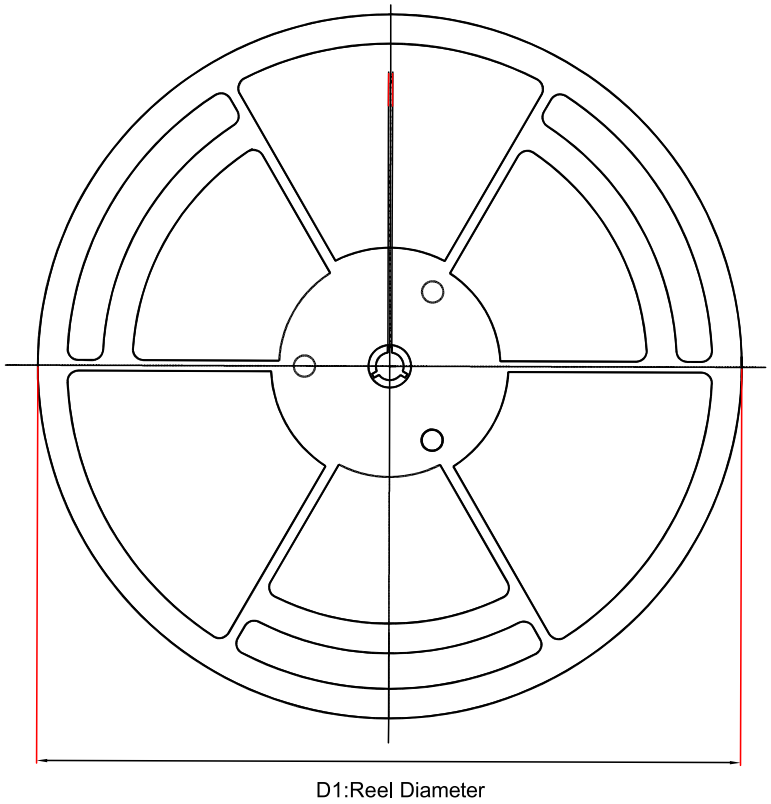
Non-Solder Mask Defined (Preferred)

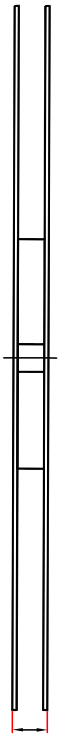
Solder Mask Defined

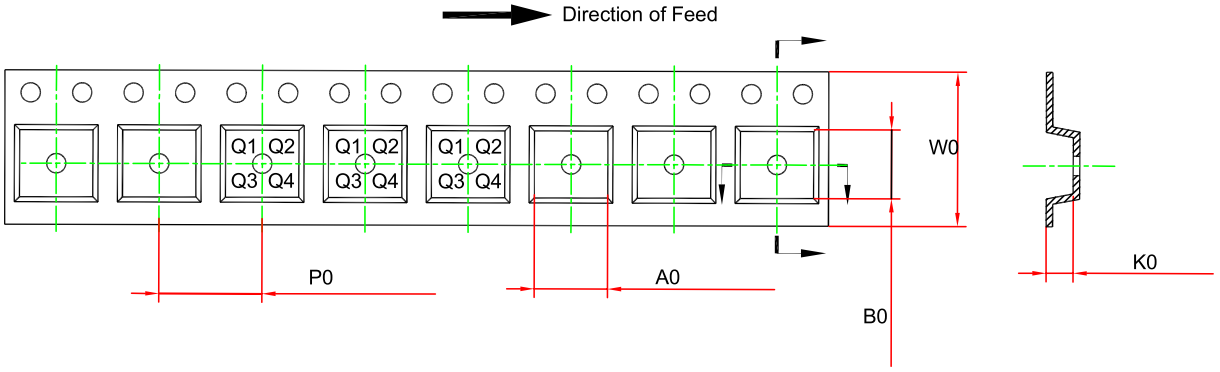
Solder Mask Details

NOTES:
1. Size of metal pad may vary due to creepage requirement.
2. Vias are optional depending on application. It is recommended that vias under paste be filled, plugged or tented.
3. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

Tape and Reel Information





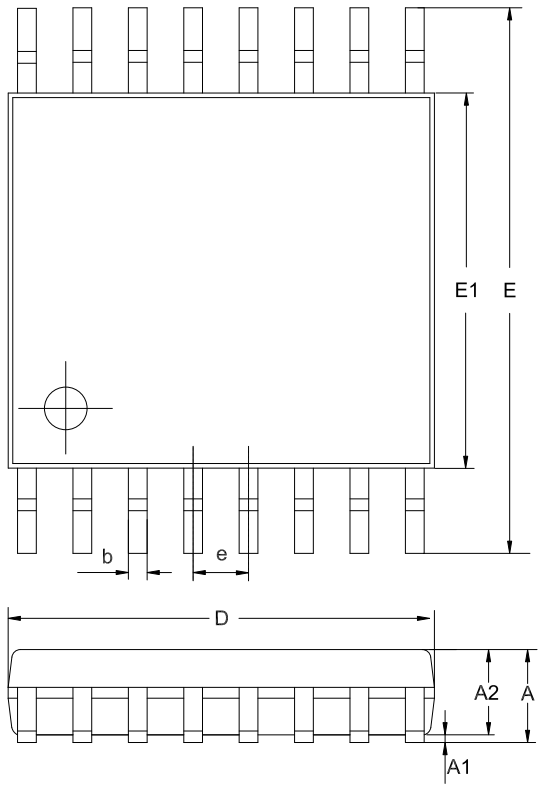


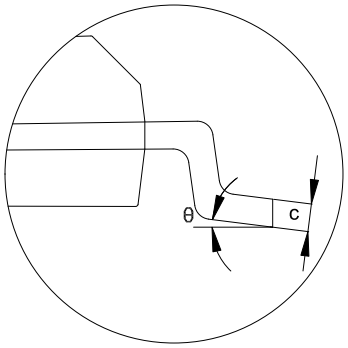
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPC502200-TS3R-S	TSSOP16	330	17.6	6.8	5.5	1.5	8.0	12.0	Q1

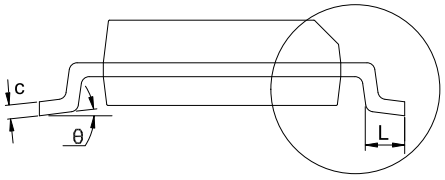
Package Outline Dimensions

TSSOP16

Package Outline Dimensions TS3(TSSOP-16-A)







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPC502200-TS3R-S	−40 to 125°C	TSSOP16	02200	1	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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