Quad Channel Current and Voltage Output DAC with ADC Readback

Features

- 16-bit Resolution and Monotonicity
- Output Ports being UIO Compatible, Terminals Tolerant to ±50 V with Diodes
- Current Output Ranges: 4 mA to 20 mA, 0 mA to 20 mA, or 0 mA to 24 mA
  - Typical ±0.05% FSR Total Unadjusted Error (TUE)
  - Leakage Compensation in Current Mode
  - HART Connectivity
- Voltage Output Ranges: 0 V to 5 V, 0 V to 10 V, ±5 V, or ±10 V
  - Typical ±0.06% FSR Total Unadjusted Error (TUE)
  - 20% Over-range Available
  - Support Four-wire Voltage in Voltage Mode
- 12-bit ADC for Readback Output Voltage & Current & AVDD
- On-chip Output Fault Detection
  - CRC Check
  - Watchdog Timer
  - Current Output Open Circuit Alarm & Negative Voltage Alarm
  - Voltage Output Overcurrent with Direction
  - Independent AVDD UVLO
  - Over Temperature
- Temperature Range: −40°C to +125°C
- QFN7×7-48 Packages

Applications

- Industrial Automation
- Process Control
- HART Network Connectivity
- PLC and DCS

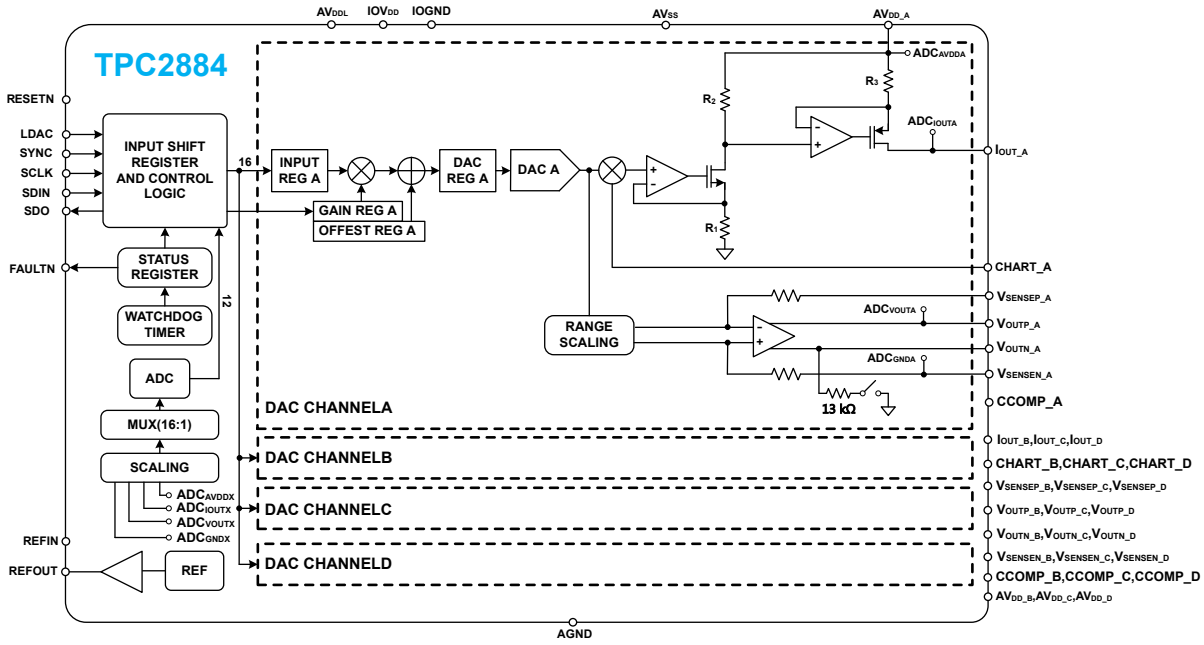
Description

The TPC2884 is a quad-channel voltage and current output digital-to-analog converter (DAC) that operates with a power supply range from −27 V to +50 V. The AV_{DD} pin for each channel provides an independent positive power supply with a range of 7 V to 50 V, which can be used with an external adaptive power supply to reduce chip heating, and External resistance can also be connected in series with the AV_{DD} to achieve a switchable HART impedance in LOOP_POWER current input mode. In the current output mode, each channel has an independent HART injection PIN to transmit HART.

The device in voltage output mode provides a five-wire output with the addition of an external diode to prevent backfill and high withstand voltage over the rail, as well as to compensate for voltage drops in traces and ports. In the current output mode, there is an output open-loop detection, and in order to reduce the leakage error of the (UIO) mode and the ADC input, the output impedance compensation is built in, and there is also a negative voltage detection to identify wiring faults. The device is UIO mode compatible, the voltage output PIN can be combined with the current output PIN, and for analog input compatibility, it can be used with external diodes to achieve port withstand voltage beyond the power rail, and the withstand voltage can reach ±50 V (± 15 V power supply).

The device has complete diagnosis, including built-in fault detection and a 12-bit ADC for port voltage readback. Built-in fault detection includes overcurrent direction of voltage output, current output loop break and negative voltage, power supply and output status, over-temperature protection, CRC calibration, SPI watchdog, etc. The built-in ADC reads back the voltage and current of each channel and the positive supply voltage, providing more flexible output monitoring.

Typical Application Circuit



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Product Family Table

Order Number	Resolution	Output	Package
TPC2884-FE6R	16	Current/Voltage	QFN7X7-48

Revision History

Date	Revision	Notes
2025-10-23	Rev.A.0	Initial released version.

Pin Configuration and Functions

TPC2884
QFN7X7-48
Top View

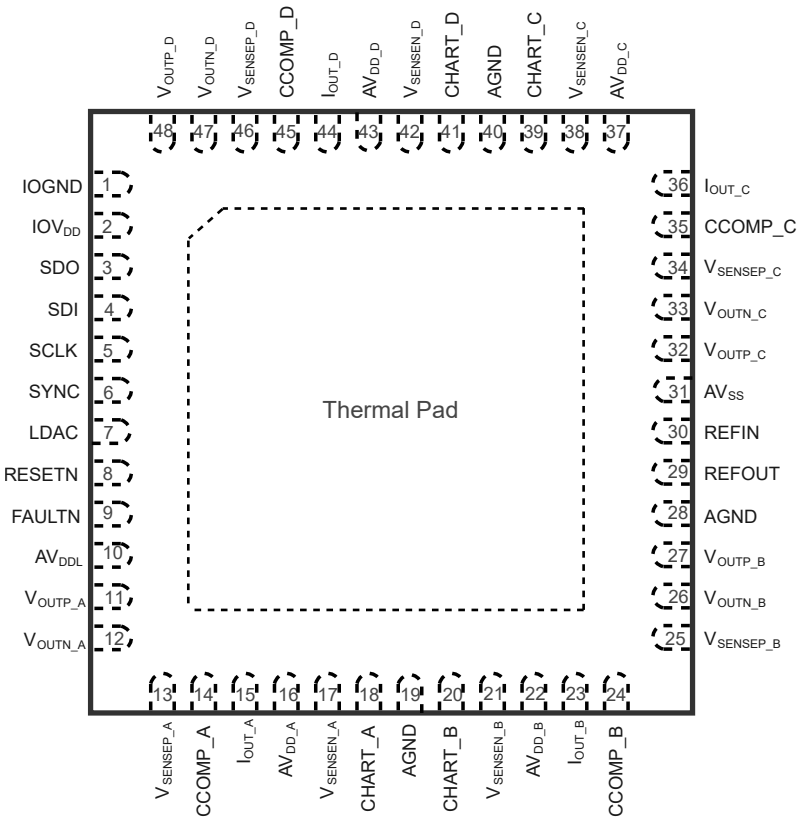


Table 1. Pin Function Descriptions

Pin No.	Pin Name	Description
6	SYNC	Enable pin of the SPI bus, high-impedance input. As an enable signal on the SPI bus, SYNC pulls low, SDO transmits data, SYNC pulls up, the SDO port is high-impedance, and the SPI bus is idle. If the LDAC continues to pull low, the rising edge of the SYNC pin triggers the transfer of newly written data to the output.
4	SDI	Data input pin of SPI bus, high impedance input. After the communication starts, enter the DAC data and configuration information.
5	SLCK	Clock input pin of the SPI bus, high-impedance input. Provides a clock for SPI communication, updating SDO data on the rising edge of the clock and reading in SDI data on the falling edge of the clock.
3	SDO	Data output pins on the SPI bus. When the SYNC is pulled down, data is transmitted, the SYNC is pulled up, and the SDO enters a high-impedance state.

Pin No.	Pin Name	Description
1	IOGND	Digital interface ground pins. For the ground of IOV_{DD} and digital modules, it is recommended to connect with AGND at a single point on the circuit board to reduce the interference of digital current to AGND.
2	IOV_{DD}	Digital interface power pins. For the power supply of the internal digital interface, a 100nF capacitor is recommended to connect the IOV_{DD} to the IOGND.
7	LDAC	DAC update pin, high impedance input, low active. The LDAC changes from high to low, triggering all channel data to be updated synchronously to the DAC output. LDAC remains low and the rising edge of the SYNC pin triggers the transfer of newly written data to the output on the SPI bus.
9	FAULTN	Chip reporting error pins, open-drain output, low validity. Errors include short circuit of output voltage, open circuit of output current, negative voltage of current output, overtemperature and protection, CRC, and Watch Dog. Built-in control registers with selectable output of error messages on the pin.
8	RESETN	On-chip reset pin, high-impedance input, active-low. The RESET pin has a minimum filtering time of 50uS to protect the safety of the function, and the chip can also be RESET through the software register, and the KEY is 0x0555. Performing RESET resets the chip to the power-up state, there is a special indicator bit in the main state register to record the RESET event, after RESET occurs, this bit becomes 1 and remains there, the state is cleared by writing to the 0x0358 in the software register.
10	AV_{DDL}	Low-voltage power supply pins. For the internal analog and digital parts, this PIN pin needs to decouple the IOGND and AGND, and it is recommended to connect the 100nF decoupling capacitor to the connection point between the IOGND and AGND to achieve decoupling and interference isolation.
29	REFOUT	Built-in reference output pin. The on-chip 4.096V reference output, the pin is connected to a 100nF capacitor to the AGND, and can be directly connected to the REFIN pin to input the reference voltage for the chip. There is no need for an internal reference, the pins can be floated
30	REFIN	Reference input pin. A 4.096V reference is provided for the internal DAC and ADC, and this pin is a resistive input with an impedance of approximately 40K ohms. Using the built-in references, REFIN can be connected to REFOUT. With an external reference, an external reference voltage can be directly connected, and the recommended decoupling capacitance of the REFIN to AGND is 100nF.
19,28,40	AGND	Chip ground pins. It provides a ground for the chip and is also a reference ground for the reference voltage and the ADC. The three AGND pins require a low-impedance connection to reduce signal cross-talk.
18,20,39,41	CHART_(A-D)	HART injection pin for current output. The registers can be optionally turned on and off with the built-in switch, with the option to turn off the HART input and the switch off, which is connected to AGND. Select to turn on the HART input, the switch is on, the HART injection point is low impedance, and the injection current amplitude is set through the external resistor.
31	AVSS	Negative high voltage power supply pin, shared by four channels, 0V to -26V range. In the case of bipolar voltage output, a negative voltage is provided to the voltage output amplifier, and a 100nF capacitor is recommended for the AGND. When the unipolar voltage output and current output are used, this pin can be connected to AGND.

Pin No.	Pin Name	Description
16,22,37,43	$AV_{DD\_(A-D)}$	High voltage power supply pins, four independent channels, power supply range 7-50V. In current output mode, load tracking can be used with an external power supply to reduce heat generation. In voltage output mode, a fixed voltage is recommended for this port. This pin also serves as an input to the internal ADC and is used to monitor changes in the voltage of each channel.
14,24,35,45	CCOMP_(A-D)	Voltage output stability compensation pin. When the voltage output load capacitance exceeds 10nF, additional stability compensation is required, and an external capacitor is connected between the voltage output and this pin.
17,21,38,42	$V_{SENSEN\_(A-D)}$	Voltage and current outputs sense negative pins. This pin is also used as an input to the internal ADC to monitor the output current of the chip, and a resistor is required to be connected to the AGND, 10 ohms is recommended, no backflow current detection is required, and this resistor can be short-circuited.
13,25,34,46	$V_{SENSEP\_(A-D)}$	The voltage output senses a positive pin. The difference between V_{SENSEP} and V_{SENSEN} is the true voltage output. This pin also acts as an input to the internal ADC and monitors the output voltage value when the voltage output is enabled. The pin to ground impedance is 1M ohms.
12,26,33,47	$V_{OUTN\_(A-D)}$	Voltage output pull-down pin. It is an open-drain output that can withstand positive and high voltages, and can be used with an external diode to achieve positive and negative high withstand voltages. This pin is connected to the V_{OUTP} to form a voltage output stage, and there is a drop-down switch connected to the AGND to control the floating state of the voltage output port.
11,27,32,48	$V_{OUTP\_(A-D)}$	Voltage output pull-up pin. It is an open-drain output that can withstand negative high voltage, and can be used with an external diode to achieve high positive and negative voltage. This pin is connected to the V_{OUTN} to form a voltage output stage, and it can also be combined with the I_{OUT}.
15,23,36,44	$I_{OUT\_(A-D)}$)	Current output pull-up pin. It is an open-drain output that can withstand negative high voltage, and can be used with an external diode to achieve high positive and negative voltage. The I_{OUT} pin also acts as an ADC input to monitor the current output port voltage. The current output port has an impedance of 1M ohms to AGND, and the built-in current compensation function can handle the resistance leakage in the application scenario.
49	EPAD	A thermal pad, located at the bottom of the chip, is equipotential with AVSS . It is recommended that the pad be thermally connected to a copper plane for enhanced thermal performance.

Specifications

Absolute Maximum Ratings (1)

All test conditions: T_A = 25°C, unless otherwise noted.

Parameter		Min	Max	Unit
AV_{DD} to AGND		−0.3	65	V
AV_{SS} to AGND		−33	0.3	V
AV_{DD} to AV_{SS}		−0.3	65	V
AV_{DDL} to AGND		−0.3	6	V
IOV_{DD} to IOGND		−0.3	6	V
IOGND to AGND		−0.3	0.3	V
$V_{SENSEP\_(A-D)}$		AGND − 65	AV_{SS} + 65	V
$V_{SENSEN\_(A-D)}$		−0.3	6	V
$V_{OUTP\_(A-D)}$		AV_{DD} − 65	AV_{DD} + 0.3	V
$V_{OUTN\_(A-D)}$		AV_{SS} − 0.3	AV_{SS} + 65	V
$I_{OUT\_(A-D)}$		AV_{DD} − 65	AV_{DD} + 0.3	V
CCOMP_(A-D)		AV_{SS} − 0.3	AV_{DD} + 0.3	V
REFIN,REFOUT,CHART_(A-D)		−0.3	6	V
Digital Inputs to IOGND		−0.3	6	V
Digital outputs to IOGND		−0.3	IOV_{DD}	V
Digital Input Current		-10	10	mA
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_J	Junction Temperature (T_J max)		150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) Power dissipated on chip must be derated to keep the junction temperature below 150 °C.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Voltage to AGND, unless otherwise noted.

Parameter	Min	Nom	Max	Unit
$AV_{DD\_(A-D)}$ ($AV_{DD\_(A-D)}$ + $\|AV_{SS}\| \le 50V$)	7	15	50	V
AV_{SS} (AV_{DD} + $\|AV_{SS}\| \le 50V$)	−27	-15	0	V
IOGND		0		V
AV_{DDL}	4.5	5	5.5	V
IOV_{DD} to IOGND	2.7	5	5.5	V
REFIN		4.096		V
Voltage Output Load Current	−10		10	mA
Voltage Output Cap-load	0	1	2000	nF
AV_{DD} to I_{OUT} Voltage (Output = 24 mA)	2.7			V
Specified Performance Temperature	−40		125	°C

Thermal Information

Package Type	$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	$R_{\theta JC(bot)}$	Unit
QFN7x7-48	20	7	3	2	°C/W

Electrical Characteristics

All test conditions: $AV_{DD\_(A-D)}$ = 7 V to 50 V, AV_{SS} = −27 V to −2.5 V/0 V, $AV_{DD\_(A-D)}$ + |AV_{SS}| ≤ 50 V, AV_{DDL} = 4.5 V to 5.5 V, AGND = 0 V, REFIN = 4.096 V external, IOV_{DD} = 2.7 V to 5.5 V. V_{OUT}: R_{LOAD} = 1 kΩ, C_L = 200 pF, I_{OUT}: R_{LOAD} = 250 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Unit
Voltage Output					
Output Voltage Ranges	Ranges	0		5	V
		0		10	V
		−5		5	V
		−10		10	V
	Overranges	0		6	V
		0		12	V
		−6		6	V
		−12		12	V
Resolution		16			Bits
Bipolar Supply	$AV_{DD\_(A-D)}$ = 15 V, AV_{SS} = −15 V, loaded and unloaded				
Total Unadjusted Error (TUE)	T_A = 25°C	−0.05	±0.03	0.05	%FSR
	T_A = −40°C to + 125°C	−0.09		0.09	%FSR
Relative Accuracy (INL)		−0.01		0.01	%FSR
Differential Nonlinearity (DNL)		−1		1.5	LSB
Zero-Scale Error		−0.05	±0.03	0.05	%FSR
Zero-Scale TC			0.83		ppm FSR/°C
Full-Scale Error		−0.05	±0.03	0.05	%FSR
Full-Scale TC			0.82		ppm FSR/°C
Offset Error		−0.05	±0.03	0.05	%FSR
Offset TC			0.79		ppm FSR/°C
Gain Error		−0.06	±0.03	0.06	%FSR
Gain TC			0.92		ppm FSR/°C
Unipolar Supply	$AV_{DD\_(A-D)}$ = 15 V , AV_{SS} = 0 V, On Unipolar Ranges,Code from 256				
Total Unadjusted Error (TUE)	T_A = 25°C	−0.05	±0.03	0.05	%FSR
	T_A = −40°C to +125°C	−0.09		0.09	%FSR
Relative Accuracy (INL)		−0.01		0.01	%FSR
Differential Nonlinearity (DNL)		−1.0		1.5	LSB

Parameter	Test Conditions	Min	Typ	Max	Unit
Zero-Scale Error	Sink 1 mA from $V_{OUTN\_(A-D)}$, TA = 25°C	−0.22	±0.17	0.22	%FSR
Full-Scale Error		−0.07	±0.03	0.07	%FSR
Offset Error		−0.06	±0.03	0.06	%FSR
Gain Error		−0.07	±0.04	0.07	%FSR
Output Characteristics					
Headroom	V_{OUTP}		1.5	2	V
Footroom	V_{OUTN}		1.2	1.7	V
Short-Circuit Current	Source and Sink		±20		mA
Load	T_A = 25°C	1.0			kΩ
$V_{SENSEP\_(A\_D)}$ Impedance	T_A = 25°C		1.0		MΩ
Capacitive Load Stability	R_{LOAD} = ∞			10	nF
	R_{LOAD} = 1 kΩ			100	nF
	R_{LOAD} = ∞ External compensation capacitor of 47 pF connected, and 30 ohm resistor connected in series with output pin			2	µF
DC Output Impedance	T_A = 25°C		0.15		Ω
DC PSRR $AV_{DD\_(A-D)}$	T_A = 25°C		1.4		µV/V
DC PSRR AV_{DDL}	T_A = 25°C		190		µV/V
DC PSRR AV_{SS}	T_A = 25°C		2.5		µV/V
DC Crosstalk	T_A = 25°C		10		µV
Current Output					
Output Current Ranges		0		24	mA
		0		20	mA
		4		20	mA
	LOOP-POWER Input	24.6	25.0		mA
Resolution		16			Bits
Current Accuracy	$AV_{DD\_(A-D)}$ = 15 V, AVSS = 0				
Total Unadjusted Error (TUE)	T_A = 25°C	−0.06	±0.04	0.06	%FSR
	T_A = −40°C to + 85°C	−0.1		0.1	%FSR
	T_A = −40°C to + 125°C	−0.15		0.15	%FSR
Relative Accuracy (INL)		−0.015		0.015	%FSR
Differential Nonlinearity (DNL)		−1.0		1.5	LSB
Offset Error		−0.055	±0.02	0.055	%FSR
Offset Error TC			1.28		ppm FSR/°C

Parameter	Test Conditions	Min	Typ	Max	Unit
Gain Error		−0.15	±0.04	0.15	%FSR
Gain TC			5.83		ppm FSR/°C
Full-Scale Error		−0.15	0.04	0.15	%FSR
Full-Scale TC			5.35		ppm FSR/°C
Zero-Scale Error	T_A = 25°C	−0.18		0.18	%FSR
	T_A = −40°C to +125°C	−0.2		0.2	%FSR
Current Output Characteristics	$AV_{DD\_(A-D)}$ = 15 V , AV_{SS} = 0				
Current Output Headroom			1.6	2.7	V
Resistive Load				1000	Ω
$I_{OUT\_(A-D)}$ Impedance	$I_{OUT\_(A-D)}$ to AGND, T_A = 25°C		1		MΩ
Output Negative Voltage Detect Vth	Fall Edge	−4		-2.5	V
Output Negative Voltage Detect Vth	Rise Edge	−3		-2	V
DC PSRR AV_{DD}	T_A = 25°C		0.05		μA/V
DC PSRR AV_{DDL}	T_A = 25°C		0.3		μA/V
DC Crosstalk	T_A = 25°C		0.063		μA
ADC	Internal Reference				
Range	$AV_{DD\_(A-D)}$, $I_{OUT\_(A-D)}$ Voltage Range	0.0		37.5	V
	$V_{SENSEP\_(A-D)}$ Voltage Range	−12.5		12.5	V
	Ground Current Voltage Range	−312.5		312.5	mV
R_{IN}	$AV_{DD\_(A-D)}$, $I_{OUT_(A-D)}$Readback Impedance to AGND, T_A = 25°C		2.0		MΩ
	Ground Current Impedance, T_A = 25°C		50.0		kΩ
Relative Accuracy (INL)	T_A = 25°C		0.2		%FSR
Total Unadjusted Error(TUE)		−1	±0.5	1	%FSR
Data Rate	T_A = 25°C		48		KSPS
Resolution			12.0		Bits
Average Rate		1.0	4.0	16.0	
Reference Input					
Reference Input Voltage			4.096		V
DC Input Impedance			40		kΩ
Reference Output					
Output Voltage	T_A = 25°C	4.094	4.096	4.098	V

Parameter	Test Conditions	Min	Typ	Max	Unit
Reference TC		−10.0	±5	10.0	ppm/°C
Output Noise (0.1 Hz to 10 Hz)	T_A = 25°C		7.6		µVp-p
Noise Spectral Density	At 10 kHz		390		nV/√Hz
Output Voltage Drift vs. Time	Drift after 1000 hours, T_A = 125°C		165		ppm
Capacitive Load	T_A = 25°C		100		nF
Load Current	T_A = 25°C		10		mA
Short-Circuit Current	T_A = 25°C		20		mA
Line Regulation	T_A = 25°C		20		ppm/V
Load Regulation	T_A = 25°C		62		ppm/mA
Digital Inputs					
Input High Voltage, V_{IH}	Rate of IOV_{DD}	0.7			
Input Low Voltage, V_{IL}	Rate of IOV_{DD}			0.3	
Input Current		−1		1	µA
Hysteresis	IOV_{DD} > 2.7 V	0.08			V
Pin Capacitance			5.0		pF
Digital Outputs					
SDO					
Output Low Voltage, V_{OL}	Sinking 200 µA			0.4	V
Output High Voltage, V_{OH}	Sourcing 200 µA	IOV_{DD} − 0.5			V
High Impedance Leakage Current		−1		1	µA
High Impedance Output Capacitance			5		pF
FAULTN					
Output Low Voltage, V_{OL}	10 kΩ Pull-up Resistor to IOV_{DD}			0.4	V
Output High Voltage, V_{OH}	10 kΩ Pull-up Resistor to IOV_{DD}	IOV_{DD} − 0.1			V
Power Requirements					
Power Range					
$AV_{DD\_(A-D)}$	($AV_{DD\_(A-D)}$ + |AV_{SS}| ≤ 50 V)	7	15	50	V
AV_{SS}		−27	-15	0	V
IOV_{DD}		2.7	5	5.5	V
AV_{DDL}		4.5	5	5.5	V
Power UVLO					
$AV_{DD\_(A-D)}$	Rise Threshold, T_A = 25°C		6.05		V
$AV_{DD\_(A-D)}$	Fall Threshold, T_A = 25°C		5.35		V

Parameter	Test Conditions	Min	Typ	Max	Unit
AV_{DDL}	Rise Threshold, T_A = 25°C		3.60		V
AV_{DDL}	Fall Threshold, T_A = 25°C		3.20		V
IOV_{DD}	Threshold, T_A = 25°C		1.78		V
Current Requirements					
$AV_{DD\_(A-D)}$	All Voltage Output Enable, non-loaded		4.17	6.56	mA
	All Current Output Enable		2.97	3.94	mA
	All Output Disable		1.14	2.16	mA
AV_{SS}	All Voltage Output Enable, non-loaded	−4.64	3.15		mA
	All Current Output Enable	−1.67	0.99		mA
	All Output Disable	−1.67	0.99		mA
AV_{DDL}	All Channels Output Enable, CODE=65535, No Load, & ADC is Enabled		6.01	8.93	mA
	All Channels Output Disable & ADC is Disabled		1.84	3.47	mA
IOV_{DD}	All Channels Output Enable, CODE=65535, No SPI Flip		0.005	0.017	mA

All test conditions: $AV_{DD\_(A-D)}$ = 15 V, AV_{SS} = −15 V, AV_{DDL} = 5 V, AGND = 0 V, REFIN = 4.096 V external, IOV_{DD} = 2.7 V to 5.5 V. V_{OUT}: R_{LOAD} = 2 kΩ, C_L = 200 pF, I_{OUT}: R_{LOAD} = 250 Ω; all specifications T_A = 25°C, unless otherwise noted.

Table 2. AC Performance Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Dynamic Performance					
Voltage Output					
Output Voltage Settling Time	5 V Range, step to ±0.1 % FSR		20		µs
	10 V Range, step to ±0.1 % FSR		27		µs
	20 V Range, step to ±0.1 % FSR		65		µs
Output Noise (0.1 Hz to 10 Hz Bandwidth)	Midscale Output,0 V to 10 V Range		0.1		LSBp-p
Output Noise Spectral Density	Measured at 10 kHz, Midscale Output, 0 V to 10 V Range		390		nV/√Hz
Slew Rate	10 V Range		0.87		V/µs
Power-On Glitch	Output unload		1		mV
Enable Glitch	10 V Range, Code = 0x0000		160		mV
Disable Glitch	10 V Range, Code = 0x0000		200		mV
Digital-to-Analog Glitch Energy	10 V Range, Zero Output		16		nV-sec
Digital Feedthrough	10 V Range, Zero Output		1.0		nV-sec
AC PSRR AV_{DD}	200 mV 50 Hz/60 Hz Sine-wave Superimposed on Power Supply Voltage		−74		dB
AC PSRR AV_{DDL}	200 mV 50 Hz/60 Hz Sine-wave Superimposed on Power Supply Voltage		−78		dB
AC PSRR AV_{SS}	200 mV 50 Hz/60 Hz Sine-wave Superimposed on Power Supply Voltage		−76		dB
Current Output					
Output Current Settling Time	step to ±0.1 % FSR (0 mA to 24 mA)		48		µs
Output Noise (0.1 Hz to 10 Hz Bandwidth)	Midscale output, 0 mA to 24 mA range		0.32		LSB p-p
Output Noise Spectral Density	Measured at 10 kHz, Midscale output, 0 mA to 24 mA range		0.8		nA/√Hz
Power-On Glitch	R_{LOAD}= 250 Ω		3.2		µA
Enable Glitch	Code = 0x0000, 0 mA to 24 mA range		1		µA
Disable Glitch	Code = 0x0000, 0 mA to 24 mA range		60		µA
AC PSRR AVDD	250 Ω Load, 200 mV 50 Hz/60 Hz Sine-wave Superimposed on Power Supply Voltage		−82		dB
AC PSRR AVDDL	250 Ω Load, 200 mV 50 Hz/60 Hz Sine-wave Superimposed on Power Supply Voltage		−78		dB

Timing Requirements

$AV_{DD\_(A-D)}$ = 15 V, AV_{SS} = −15 V, AV_{DDL} = 5 V, AGND = 0 V, REFIN = 4.096 V external, IOV_{DD} = 2.7 V to 5.5 V. V_{OUT}: R_{LOAD} = 1 kΩ, C_L = 200 pF, I_{OUT}: R_{LOAD} = 250 Ω, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3. Timing Characteristics

Parameter (1) (2)	Description	Min	Typ	Max	Unit
t_1	SCLK cycle time	50.0			ns
t_2	SCLK high time	17.0			ns
t_3	SCLK low time	17.0			ns
t_4	SYNC falling edge to SCLK falling edge setup time	20.0			ns
t_5	Final SCLK falling edge to SYNC rising edge	15.0			ns
t_6	SYNC high time following a configuration write	2.0			µs
	SYNC high time following a DAC update write	5.0			µs
	SYNC high time following a DAC update write (slew rate control enabled)	20.0			µs
t_7	Data setup time	15.0			ns
t_8	Data hold time	10.0			ns
t_9	SYNC rising edge to LDAC falling edge (applies to any channel with digital slew rate control enabled)	20.0			µs
	SYNC rising edge to LDAC falling edge (applies to any channel with digital slew rate control disabled)	5.0			µs
t_{10}	LDAC pulse width low	10.0			ns
t_{11}	LDAC falling edge to DAC output response time			2.0	µs
t_{12}	SYNC rising edge to DAC output response time with LDAC is 0	5.0			µs
t_{13}	LDAC falling edge to SYNC rising edge	500.0			ns
t_{14}	RESET pulse width	50.0			µs
t_{15}	SCLK rising edge to SDO valid			45	ns

(1) Guaranteed by characterization; not production tested.
(2) CL SDO = 20 pF.

Timing Diagrams

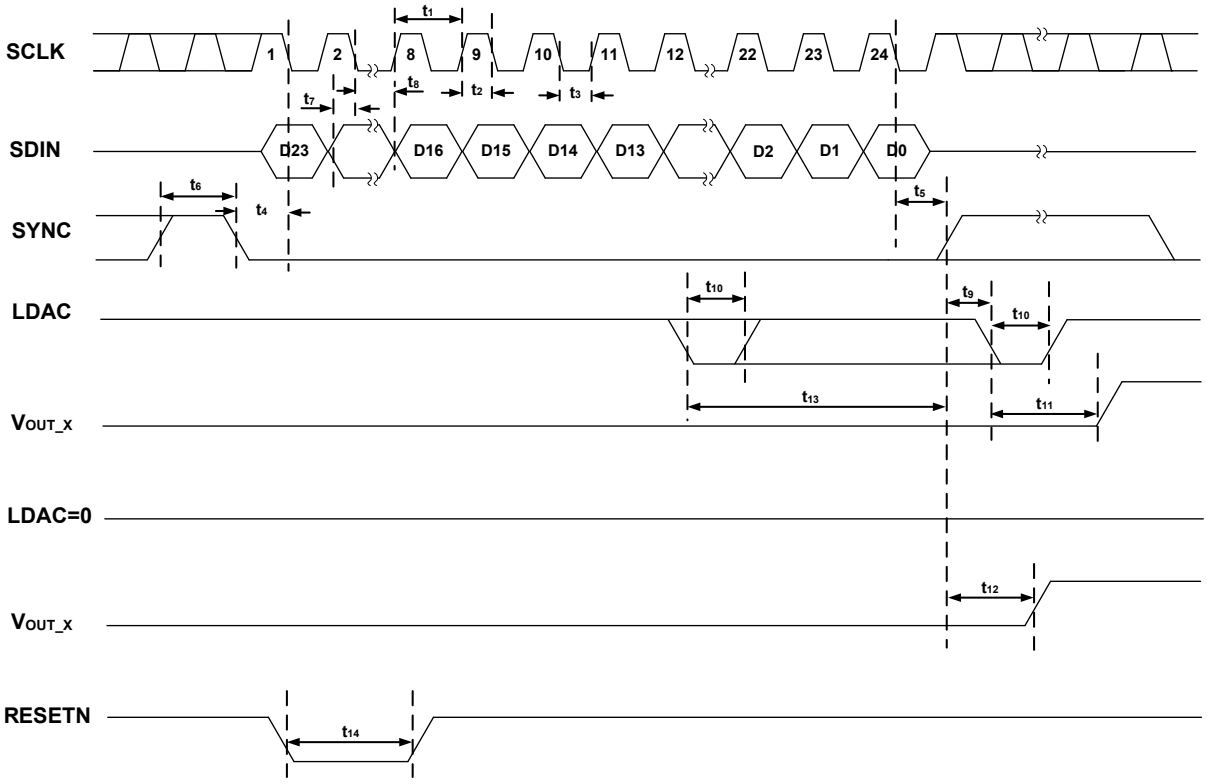


Figure 1. Write Mode Timing Diagram

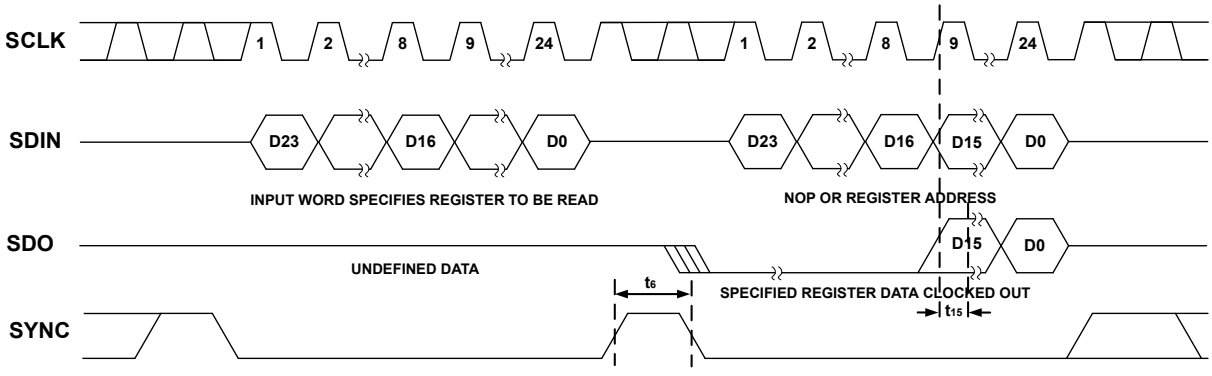


Figure 2. Readback Mode Timing Diagram

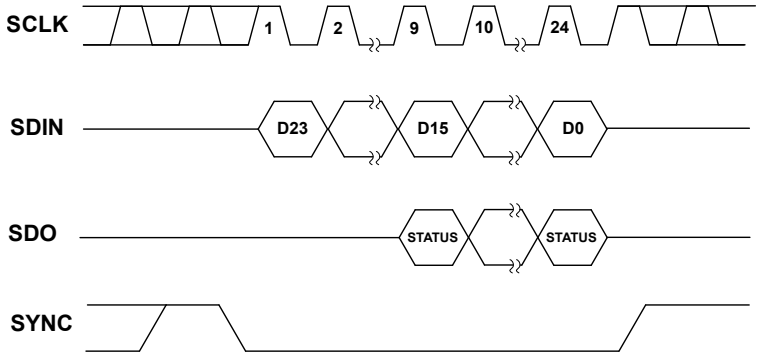


Figure 3. Status Readback during Write

Typical Performance Characteristics

General

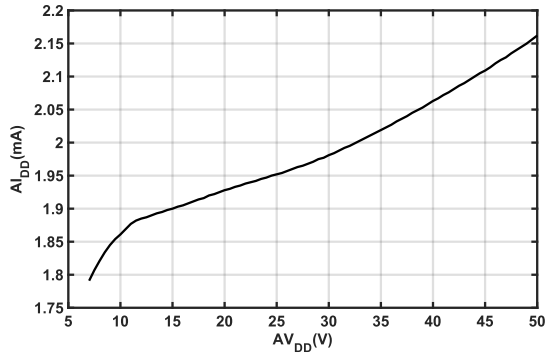


Figure 4. AI_{DD} vs. AV_{DD}

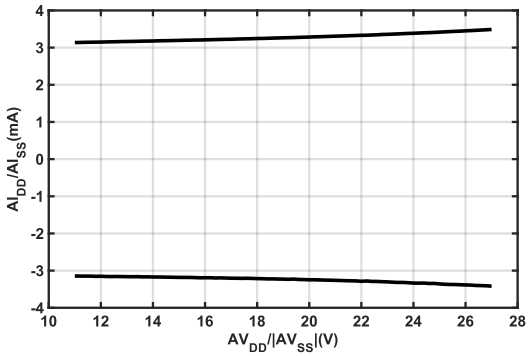


Figure 5. AI_{DD}/AI_{SS} vs. AV_{DD}/AV_{SS}

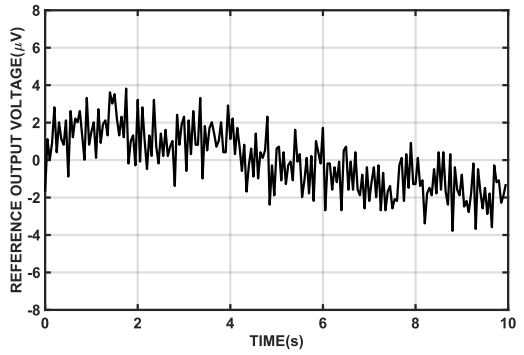


Figure 6. Reference Noise(0.1-Hz to 10-Hz Bandwidth)

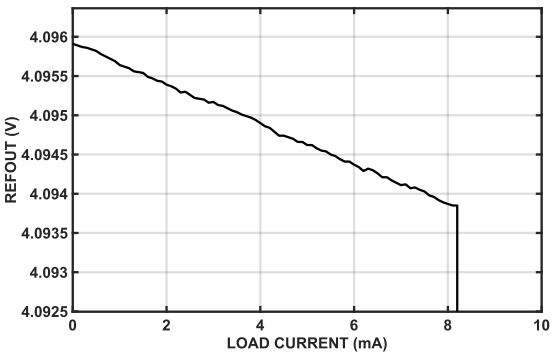


Figure 7. Reference Voltage vs. Load Current

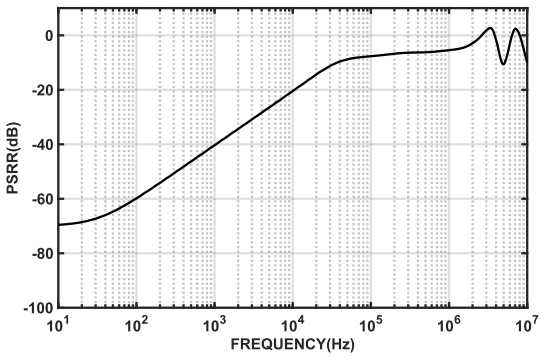


Figure 8. Reference PSRR

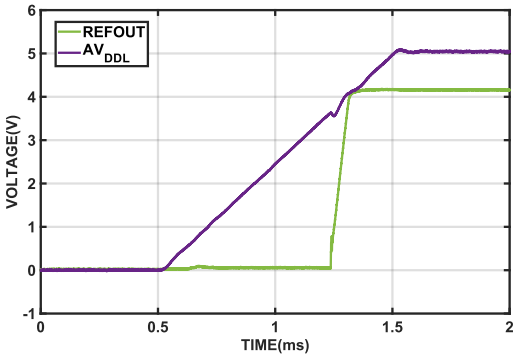


Figure 9. Reference Turn-on Transient

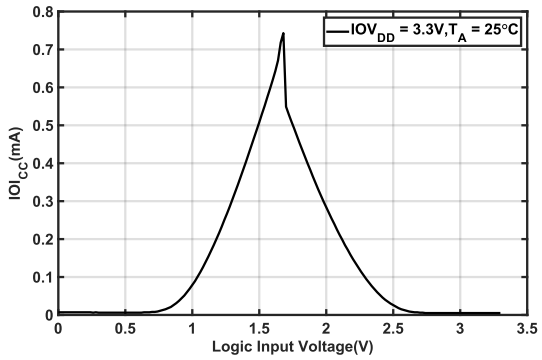


Figure 10. IOI$_{DD}$ vs. Input Voltage (3.3 V)

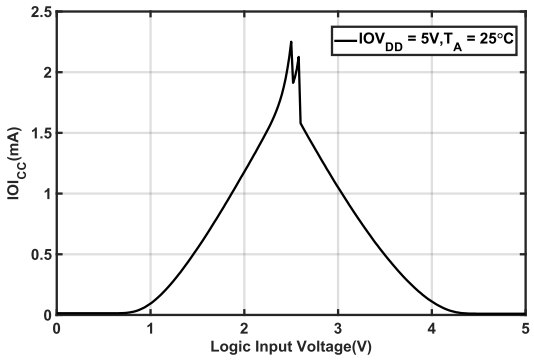


Figure 11. IOI$_{DD}$ vs. Input Voltage (5 V)

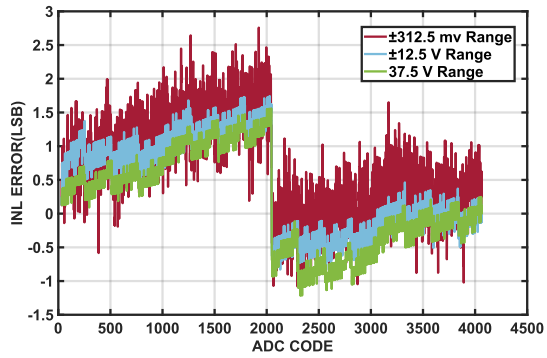


Figure 12. ADC INL

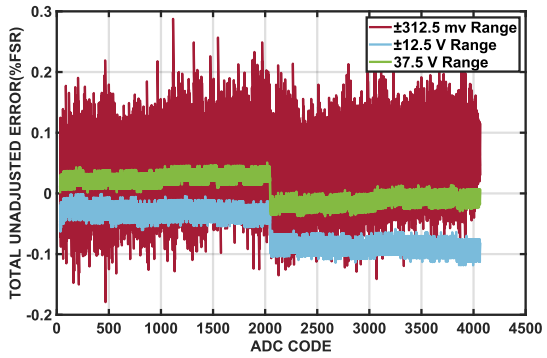


Figure 13. ADC TUE

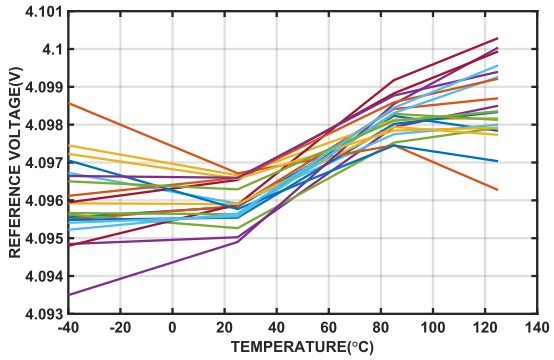


Figure 14. Reference TC

Voltage Output

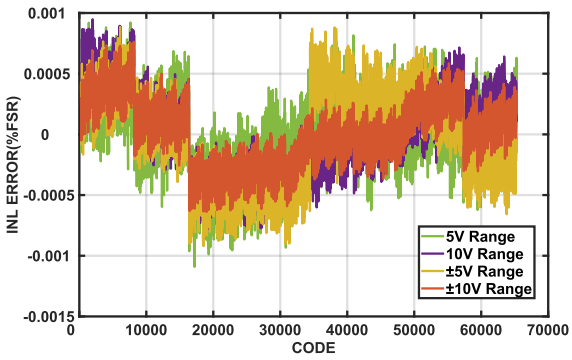


Figure 15. INL vs. DAC Code

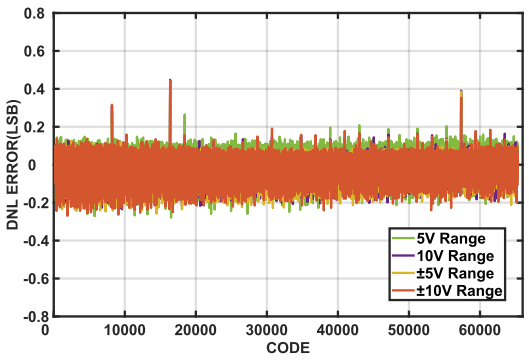


Figure 16. DNL vs. DAC Code

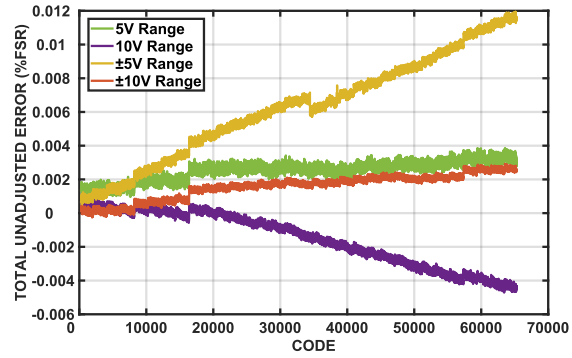


Figure 17. TUE vs. DAC Code

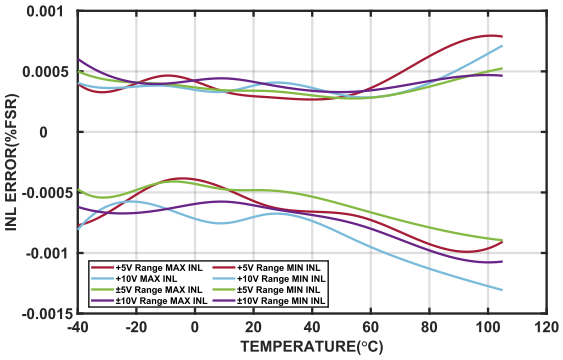


Figure 18. INL vs. Temperature

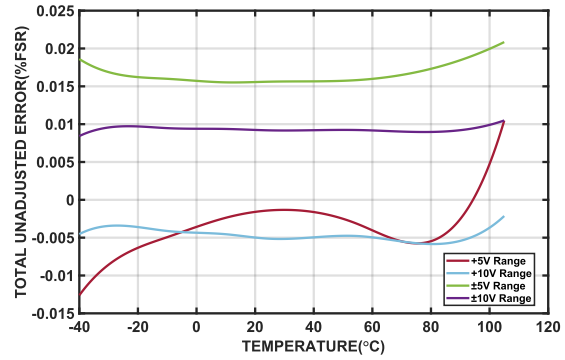


Figure 19. TUE vs. Temperature

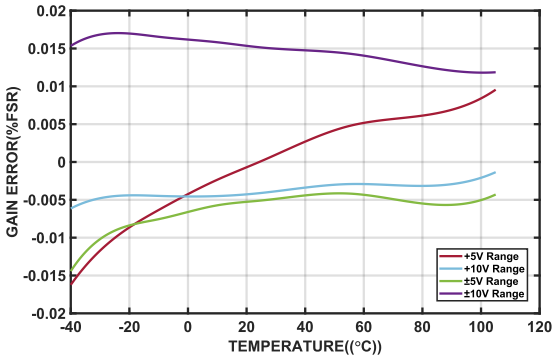


Figure 20. Gain Error vs. Temperature

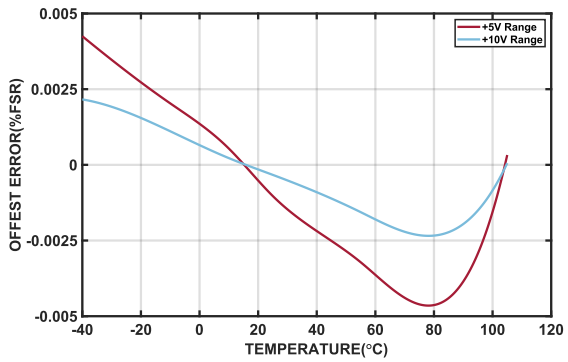


Figure 21. Offset Error vs. Temperature

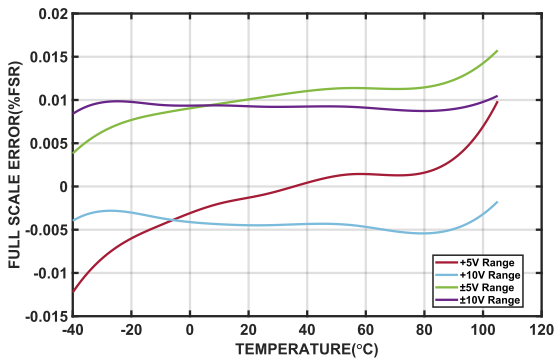


Figure 22. Full-Scale Error vs. Temperature

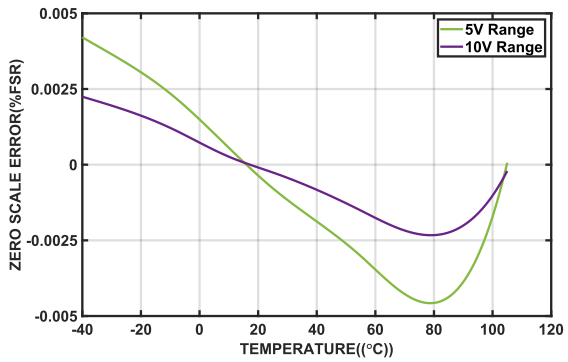


Figure 23. Zero-Scale Error vs. Temperature

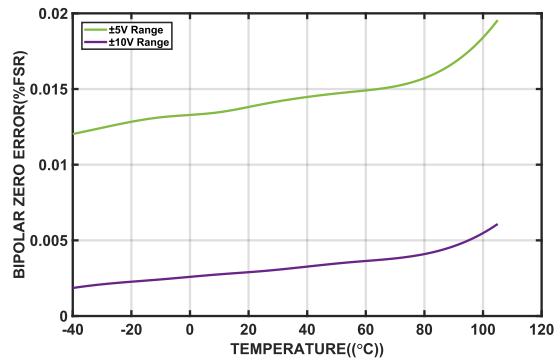


Figure 24. Bipolar-Zero Error vs. Temperature

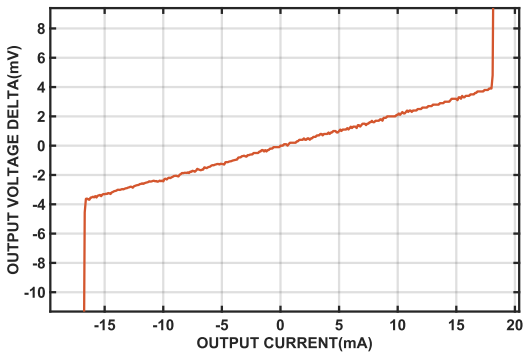


Figure 25. Source/Sink Capability, Full Scale Code Loaded

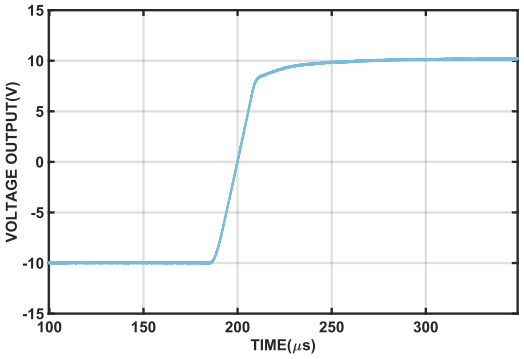


Figure 26. Full-Scale Positive Step

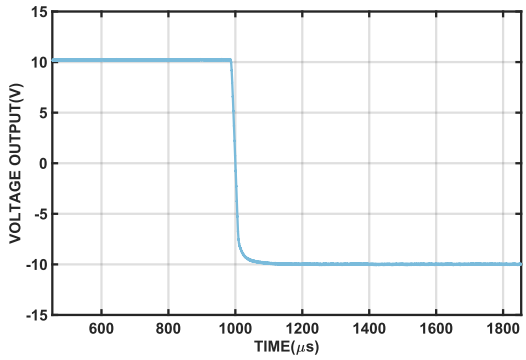


Figure 27. Full-Scale Negative Step

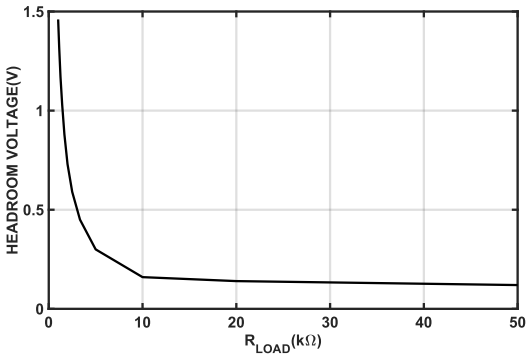


Figure 28. V_{OUT} Headroom

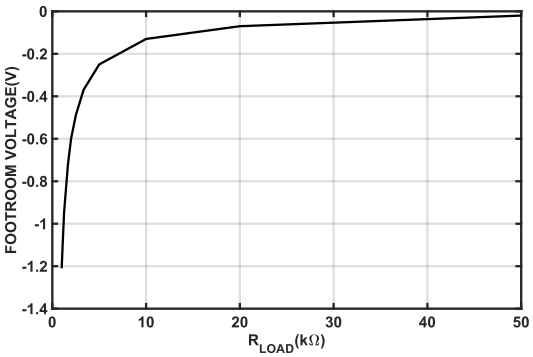


Figure 29. V_{OUT} Footroom

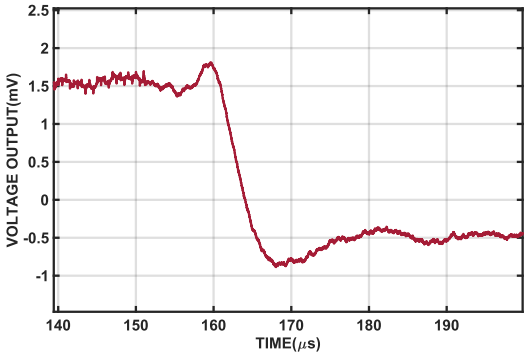


Figure 30. Digital to Analog Glitch (0x7FFF to 0x8000)

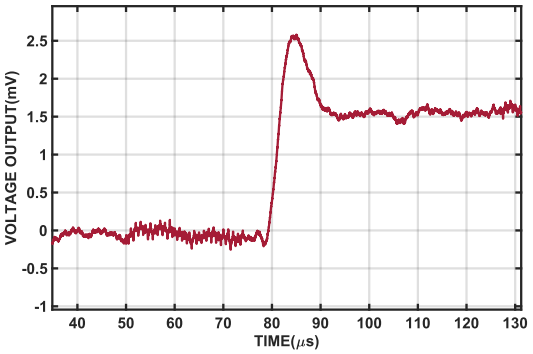


Figure 31. Digital to Analog Glitch (0x8000 to 0x7FFF)

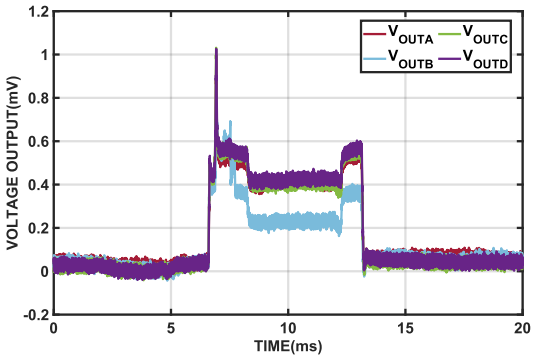


Figure 32. V_{OUT} vs. Time on Power Up

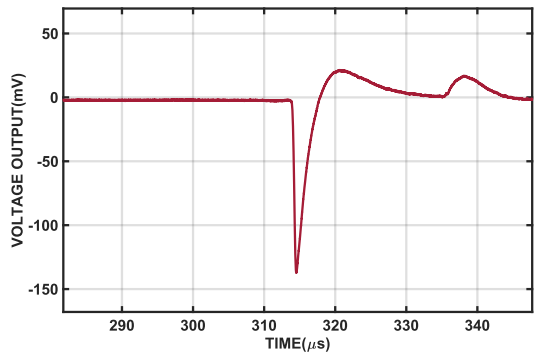


Figure 33. V_{OUT} vs. Time on Output Enable (POC = 0)

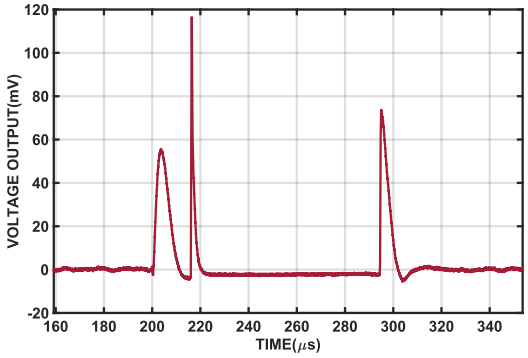


Figure 34. V_{OUT} vs. Time on Output Enable (POC = 1)

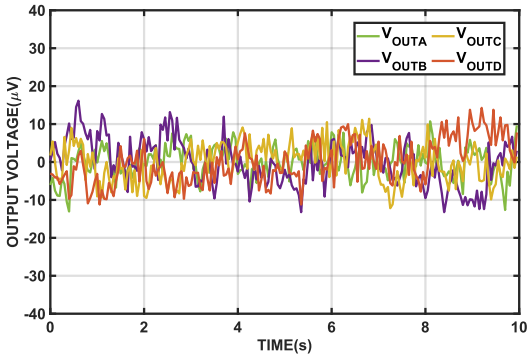


Figure 35. Peak-to-Peak Noise (0.1 Hz to 10 Hz Bandwidth)

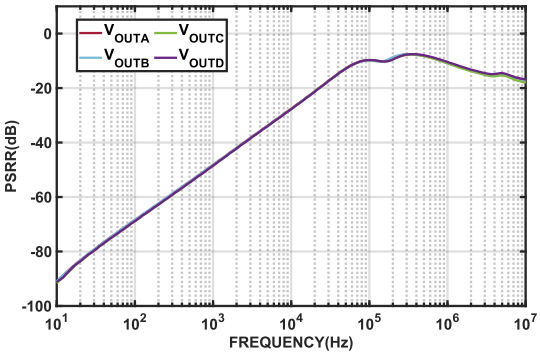


Figure 36. V_{OUT} AC PSRR vs. Frequency (AVDD)

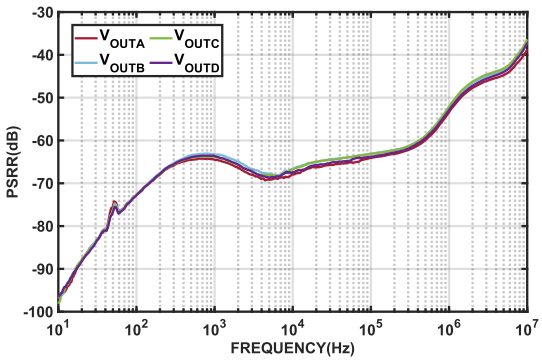


Figure 37. V_{OUT} AC PSRR vs. Frequency (AVSS)

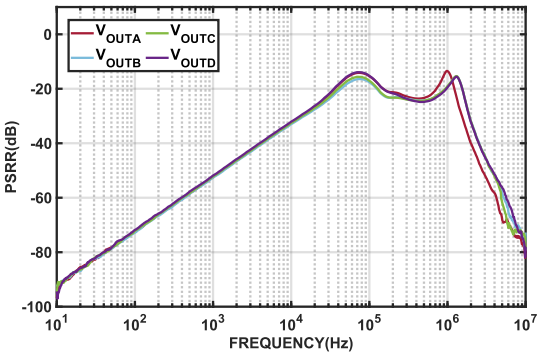


Figure 38. V_{OUT} AC PSRR vs. Frequency (AVDDL)

Current Output

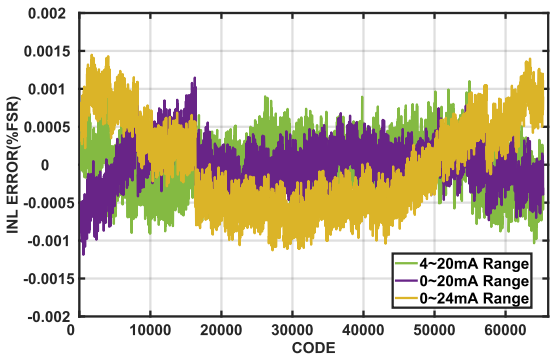


Figure 39. INL vs. DAC Code

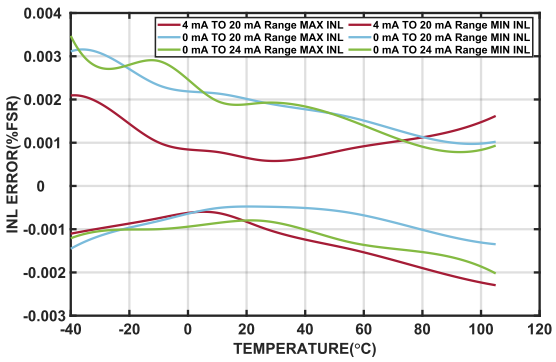


Figure 40. INL vs. Temperature

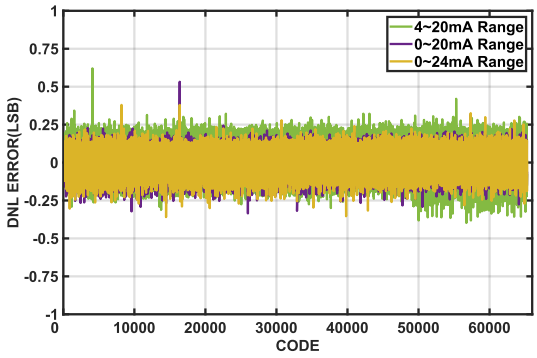


Figure 41. DNL vs. DAC Code

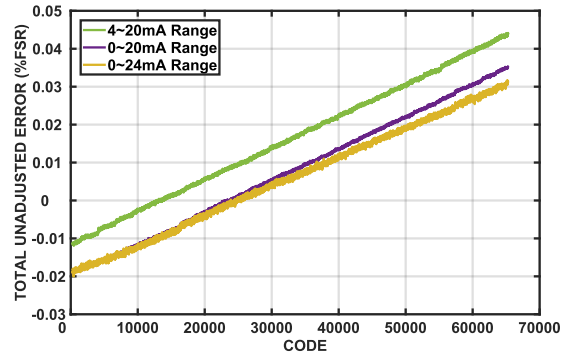


Figure 42. TUE vs. DAC Code

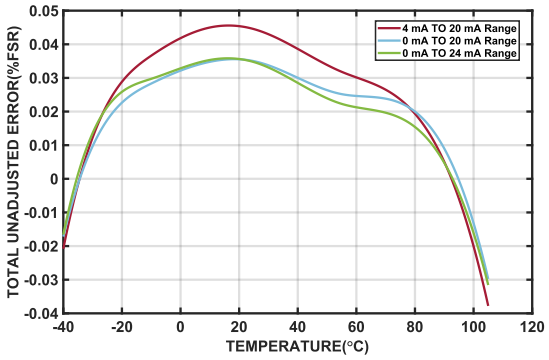


Figure 43. TUE vs. Temperature

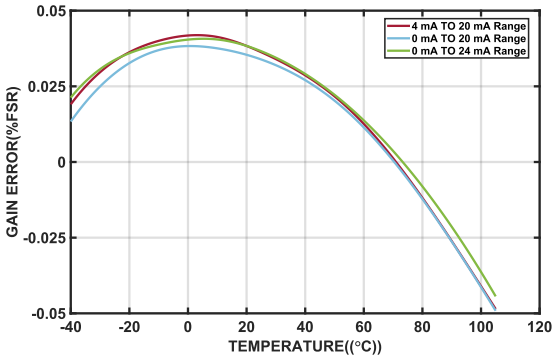


Figure 44. Gain Error vs. Temperature

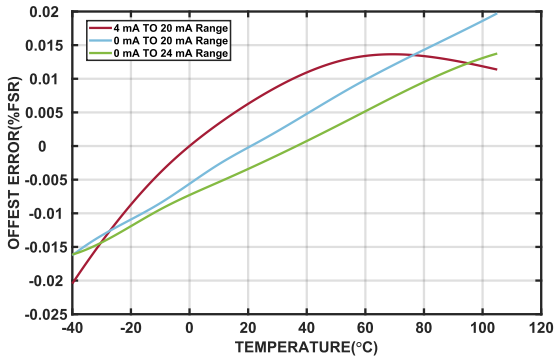


Figure 45. Offset Error vs. Temperature

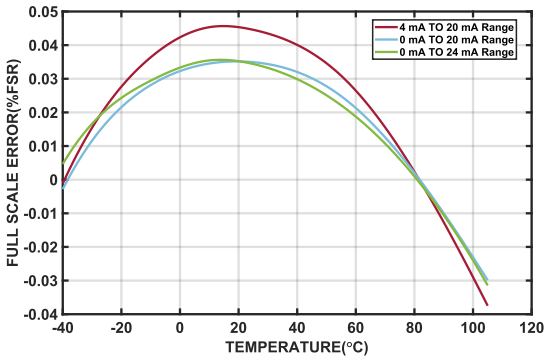


Figure 46. Full-Scale Error vs. Temperature

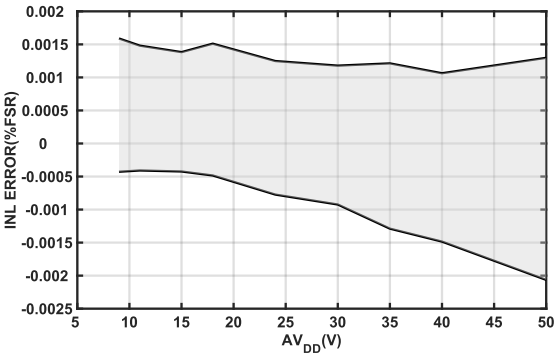


Figure 47. INL vs. AV_{DD}

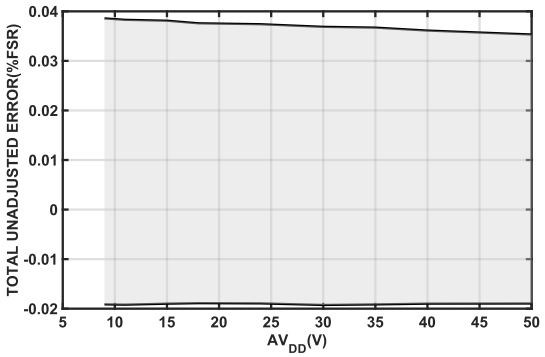


Figure 48. TUE vs. AV_{DD}

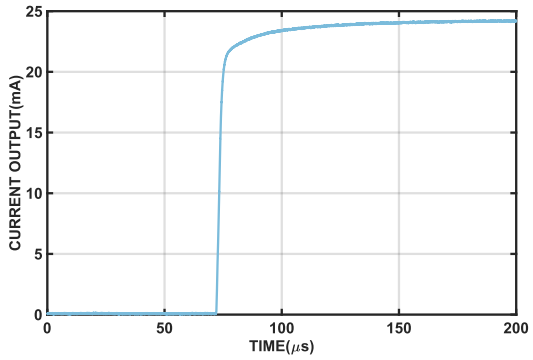


Figure 49. I_{OUT} Full-Scale Positive Step

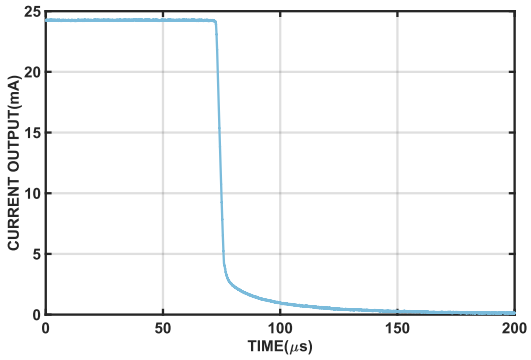


Figure 50. I_{OUT} Full-Scale Negative Step

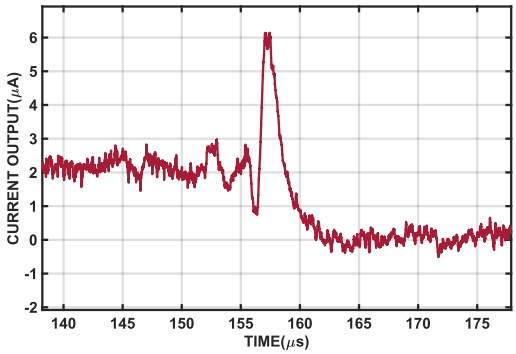


Figure 51. Digital to Analog Glitch (0x7FFF->0x8000)

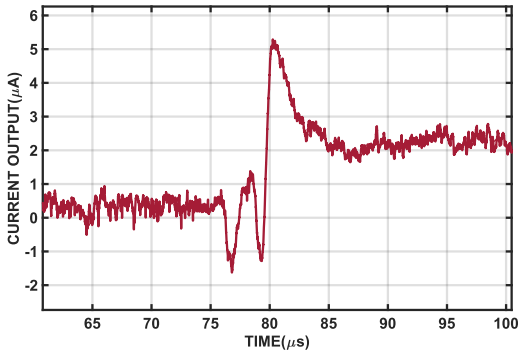


Figure 52. Digital to Analog Glitch (0x8000->0x7FFF)

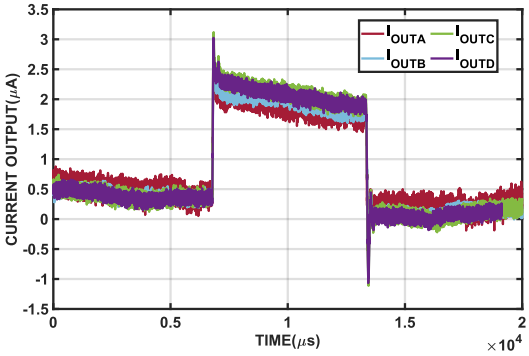


Figure 53. I_{OUT}vs. Time on Power-Up

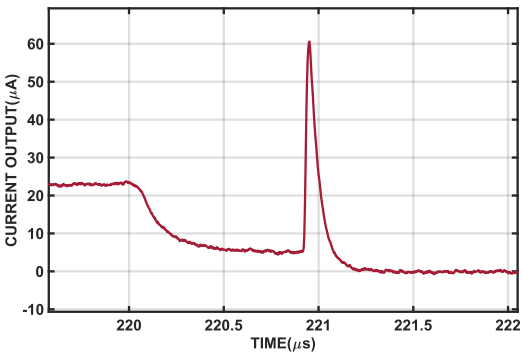


Figure 54. I_{OUT} vs. Time on Disable

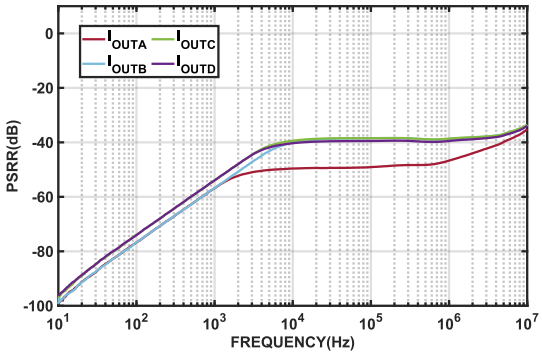


Figure 55. I_{OUT} AC-PSRR vs. Frequency (AVDD)

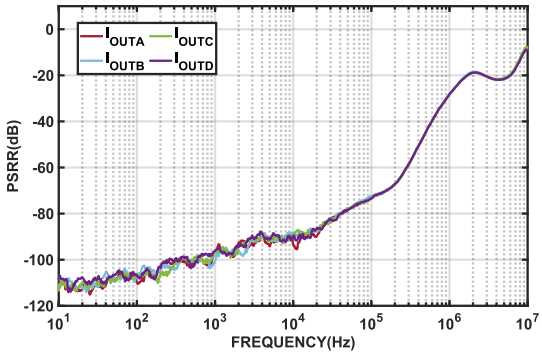


Figure 56. I_{OUT} AC-PSRR vs. Frequency (AVSS)

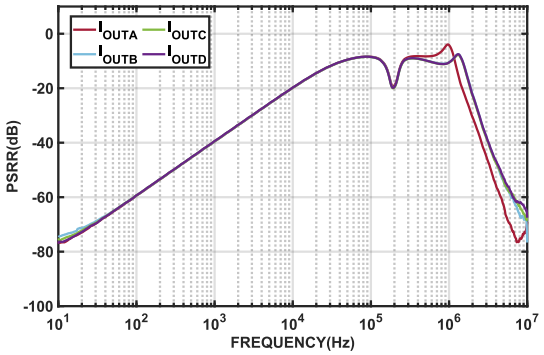


Figure 57. I_{OUT} AC-PSRR vs. Frequency (AVDDL)

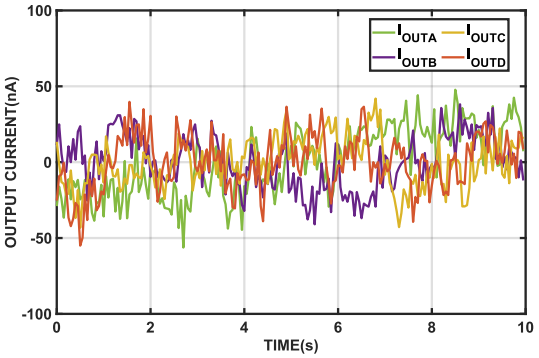


Figure 58. Peak-to-Peak Noise (0.1 Hz to 10 Hz Bandwidth)

Detailed Description

Overview

The TPC2884 is a series of high-precision, quad-channel digital-to-analog converters that offer a fully integrated, single-chip solution for industrial process control applications. These converters are capable of generating both current loop and unipolar/bipolar voltage outputs with exceptional precision. The available current ranges for these converters are 0 mA to 20 mA, 0 mA to 24 mA, and 4 mA to 20 mA. For voltage output, the options include 0 V to 5 V, ±5 V, 0 V to 10 V, and ±10 V, each with the capability of a 20% overrange. Both the current and voltage outputs are accessible via separate pins, it can be used with external diodes to achieve port withstand voltage beyond the power rail, and the withstand voltage can reach ±50 V (± 15 V power supply). The user can select the desired output configuration through the control register, ensuring that only one type of output is active at any given time. TPC2884 has complete on-chip diagnostics and an integrated 12-bit ADC for reading back voltages from four channels, including AV_{DD}, V_{SENSEP}, V_{SENSEN}, I_{OUT} pins.

Functional Block Diagram

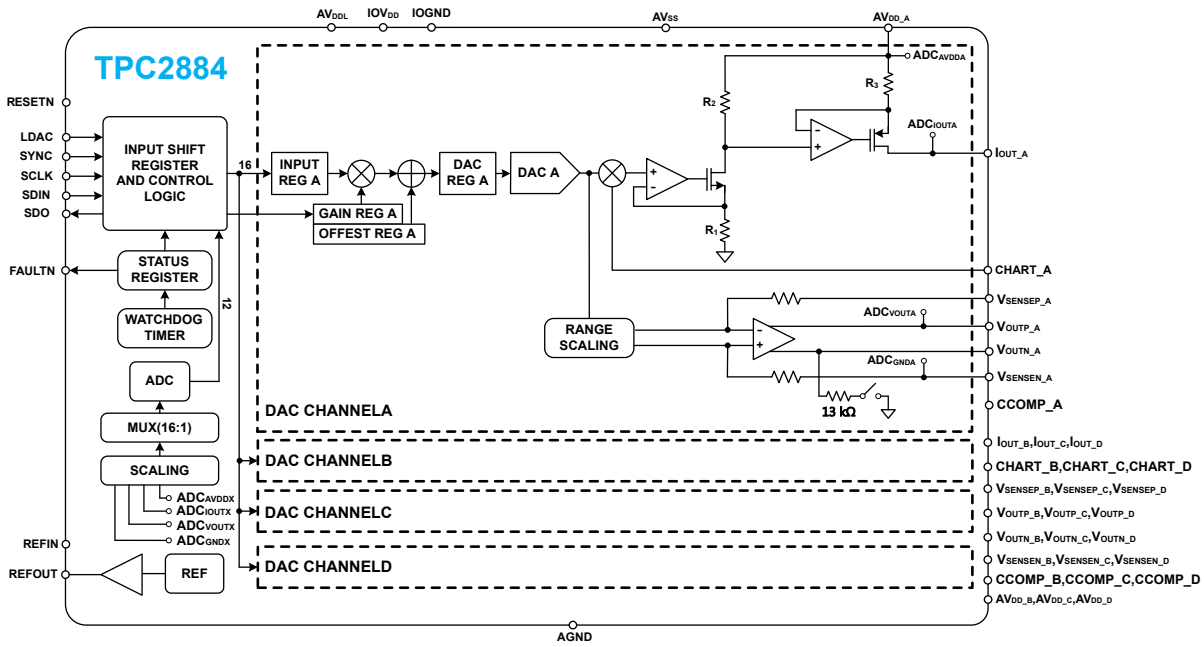


Figure 59. Functional Block Diagram

Feature Description

The TPC2884 is a quad-channel voltage and current output digital-to-analog converter (DAC) that operates with a power supply range from −27 V to +50 V. The AV_{DD} pin for each channel provides independent positive power supply with a range of 7 V to 50 V, which can be used with an external adaptive power supply to reduce chip heating, and External resistance can also be connected in series with the AV_{DD} to achieve a switchable HART impedance in LOOP_POWER current input mode. In the current output mode, each channel has an independent HART injection PIN to transmit HART.

Analog Power Supply

After powering up, it is required that a hardware reset be issued using the RESETN pin. The reset event is recorded in the MAIN_STATUS_REG RESET_NOTE_STATUS, and clearing the reset record requires the 0x0358 to be written to the SOFTWARE_REG.

The TPC2884 has a total of six analog power supply ports, namely AV_{DD_A}, AV_{DD_B}, AV_{DD_C}, AV_{DD_D}, AV_{SS}, and AV_{DDL}. Among them, the power supply range for AV_{DD_A} to AV_{DD_B} is 7 V to 50 V. The voltage range for AV_{SS} is -27 V to 0 V, and the voltage range for AV_{DDL} is 4.5 V to 5.5 V. Note that the sum of the absolute values of AV_{DD} and AV_{SS} must be less than 50 V. Recommended Operating Conditions shows the maximum and minimum allowable limits for all the power supplies when TPC2884 is powered using external power supplies.

Digital Power Supply

The TPC2884 has only one digital power supply port, which is IOV_{DD}, with a voltage range of 2.7 V to 5.5 V.

DAC Ladder Structure

The DAC core architecture of the TPC2884 is an R-2R DAC ladder shown below:

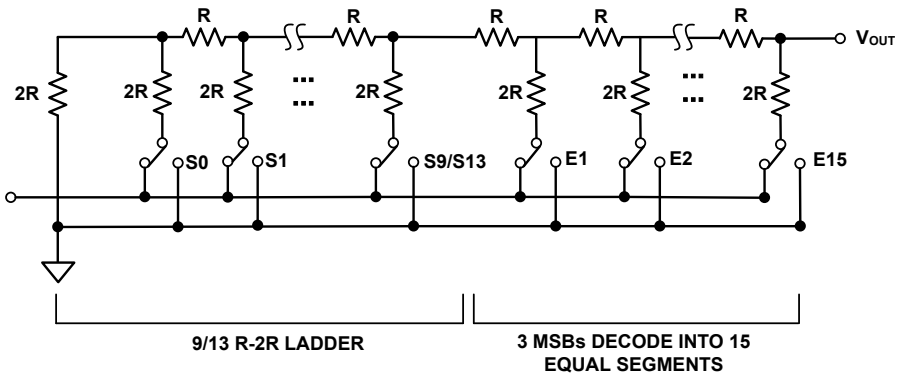


Figure 60. TPC2884 DAC Ladder Structure

Current Output Stage

Each channel's current output stage consists of a pre-conditioner and a precision current source as shown in Figure 61. This stage provides a current output according to the DAC code. The output range can be programmed as 0 mA to 20 mA, 0 mA to 24 mA or 4 mA to 20 mA.

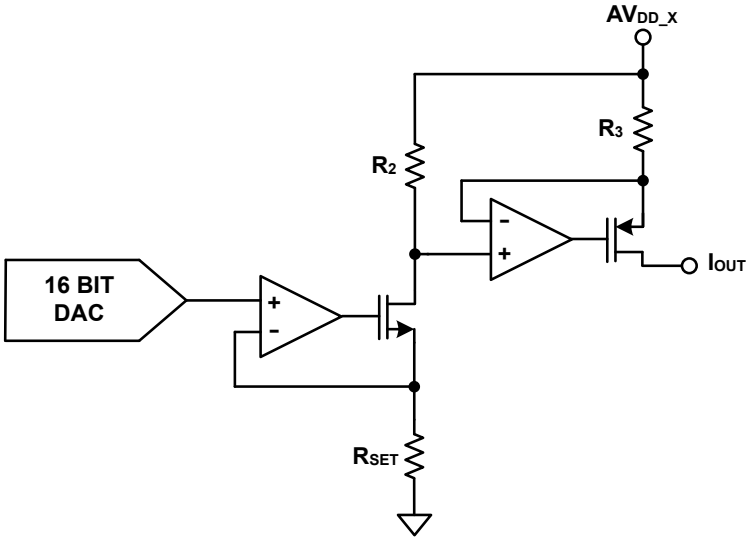


Figure 61. Voltage to Current Conversion Circuit

The 16 bit data can be written to TPC2884 using address 0x00,0x01,0x02,0x03.

For a 0-mA to 20-mA output range:

$$I_{OUT\_X} = 20\ mA \times \frac{Code}{2^N} \quad (1)$$

For a 0-mA to 24-mA output range:

$$I_{OUT\_X} = 24\ mA \times \frac{Code}{2^N} \quad (2)$$

For a 4-mA to 20-mA output range:

$$I_{OUT\_X} = 4\ mA + 16\ mA \times \frac{Code}{2^N} \quad (3)$$

Where:

- Code is the decimal equivalent of the code loaded to the DAC;
- N is the bits of resolution; 16.

Voltage Output Stage

The voltage output stage as conceptualized in Figure provides the voltage output according to the DAC code and the output range setting. The output range can be programmed as 0 V to +5 V or 0 V to +10 V for unipolar output mode, and ±5 V or ±10 V for bipolar output mode. In addition, an option is available to increase the output voltage range by 20%. The output current drive can be up to 10 mA. The output stage has short-circuit current protection that limits the output current to 20 mA.

The voltage output is designed to drive capacitive loads of up to 2 µF. For loads greater than 10 nF, an external compensation capacitor can be connected between CCOMP_X and V_{OUT_X} to keep the output voltage stable at the expense of reduced bandwidth and increased settling time. Note that, a step response (due to input code change) on the voltage output pin loaded with large capacitive load (> 20 nF) will trigger the short circuit limit circuit of the output stage. This will result in setting the short circuit alarm status bits. Therefore, it is recommended to use slew rate control for large step change, when the voltage output pin is loaded with high capacitive loads.

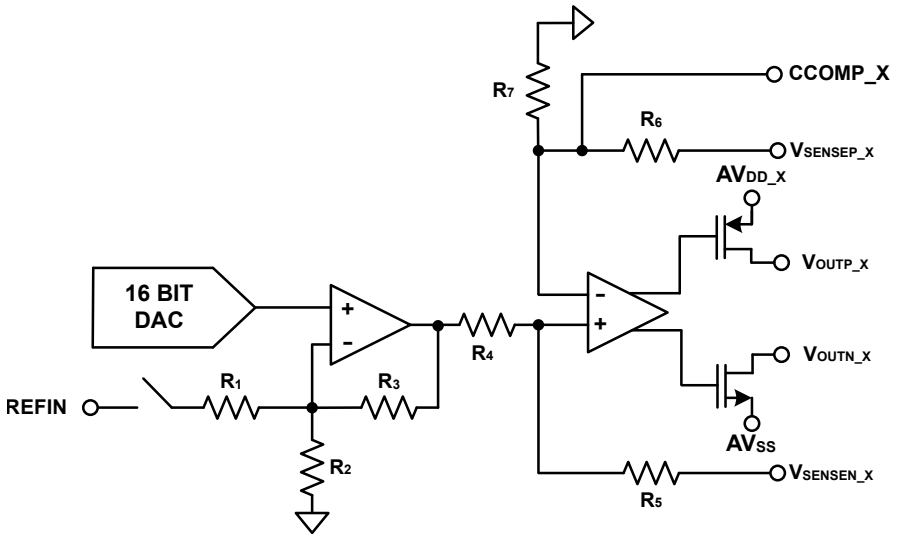


Figure 62. Voltage Output Circuit

The V_{SENSEP_X} pin is provided to enable sensing of the load. Ideally, it is connected to V_{OUT_X} at the terminals. Additionally, it can also be used to connect remotely to points electrically "nearer" to the load. This allows the internal output amplifier to ensure that the correct voltage is applied across the load as long as headroom is available on the power supply. However, if this line is cut, the amplifier loop would be broken. Therefore, an optional resistor can be used between $V_{OUT_X}$and V_{SENSEP_X} to prevent this.

The V_{SENSEN_X} pin can be used to sense the remote ground and offset the V_{OUT_X} pin accordingly.

The 16-bit data can be written to TPC2884 as shown in DAC data registers.

For unipolar output mode:

$$V_{OUT\_X} = VREFIN \times GAIN \times \frac{Code}{2^N} \quad (4)$$

For bipolar output mode:

$$V_{OUT\_X} = VREFIN \times GAIN \times \left(\frac{Code}{2^N} - 0.5\right) \quad (5)$$

Where:

- CODE is the decimal equivalent of the code loaded to the DAC.
- N is the bits of resolution: 16.
- VREFIN is the reference voltage; for internal reference, VREFIN = +4.096 V.
- GAIN is automatically selected for a desired voltage output range.

Voltage Output Short Current Protection

The voltage output buffer sources or sinks 10-mA current in normal mode. The maximum current of the buffer can output is 20 mA even if the buffer short-circuited to power or ground.

Voltage Output Over-range

The voltage output features an over-range capability. This functionality can be activated through the control register, which typically extends the chosen output range by approximately 20%.

Voltage Output using Force and Sense

The V_{SENSEP} and V_{SENSEN} terminals are designed to enable the remote monitoring of the load connected to the voltage output. By sensing the voltage at the load's end, especially if it's connected via a lengthy or high-impedance cable, the output amplifier can adjust accordingly. This adjustment ensures that the precise voltage is maintained across the load. The effectiveness of this feature is contingent upon the power supply's available headroom.

DRIVING LARGE CAPACITIVE LOADS

The voltage output amplifier is designed to handle substantial capacitive loads, with a capacity of up to 2 μF, by incorporating a nonpolarized 47 pF compensation capacitor between the CCOMP and Vout terminals. In the absence of this compensation capacitor, the amplifier can still manage capacitive loads of up to 10 nF.

Register Maps

Table 4. TPC2884 Address Functions

ADDRESS BYTE	FUNCTION	READ/WRITE	POWER-ON RESET VALUE	Section
0x00	DAC_A_REG	READ+WRITE	0x0000	Table 5
0x01	DAC_B_REG	READ+WRITE	0x0000	
0x02	DAC_C_REG	READ+WRITE	0x0000	
0x03	DAC_D_REG	READ+WRITE	0x0000	
0x04	GAIN_A_REG	READ+WRITE	0x0000	Table 7
0x05	GAIN_B_REG	READ+WRITE	0x0000	
0x06	GAIN_C_REG	READ+WRITE	0x0000	
0x07	GAIN_D_REG	READ+WRITE	0x0000	
0x08	OFFEST_A_REG	READ+WRITE	0x0000	Table 9
0x09	OFFEST_B_REG	READ+WRITE	0x0000	
0x0A	OFFEST_C_REG	READ+WRITE	0x0000	
0x0B	OFFEST_D_REG	READ+WRITE	0x0000	
0x0C	CLEAR_A_REG	READ+WRITE	0x0000	Table 11
0x0D	CLEAR_B_REG	READ+WRITE	0x0000	
0x0E	CLEAR_C_REG	READ+WRITE	0x0000	
0x0F	CLEAR_D_REG	READ+WRITE	0x0000	
0x10	SLEW_A_REG	READ+WRITE	0x0000	Table 13
0x11	SLEW_B_REG	READ+WRITE	0x0000	
0x12	SLEW_C_REG	READ+WRITE	0x0000	
0x13	SLEW_D_REG	READ+WRITE	0x0000	
0x14	DAC_CTRL_A_REG	READ+WRITE	0x0000	Table 15
0x15	DAC_CTRL_B_REG	READ+WRITE	0x0000	
0x16	DAC_CTRL_C_REG	READ+WRITE	0x0000	
0x17	DAC_CTRL_D_REG	READ+WRITE	0x0000	
0x18	ADC_SETUP_A&B_REG	READ+WRITE	0x0000	Table 17

ADDRESS BYTE	FUNCTION	READ/WRITE	POWER-ON RESET VALUE	Section
0x19	ADC_SETUP_C&D_REG	READ+WRITE	0x0000	Table 19
0x1A	NOP_REG	WRITE	0x0000	Table 21
0x1B	Reserved	NA	0x0000	
0x1C	ADC_CTRL_REG	READ+WRITE	0x0000	Table 23
0X1D	MAIN_CTRL_REG	READ+WRITE	0x0000	Table 25
0x1E	SOFTWARE_REG	WRITE	0x0000	Table 27
0x1F	FAULT_MASK_REG	READ+WRITE	0x0000	Table 29
0x20	FAULT_CLEAR_REG	WRITE	0x0000	Table 31
0x21	FAULT_STORE_REG	READ	0x0000	Table 33
0x22	MAIN_STATUS_REG	READ	0x0000	Table 35
0x23	OUT_STATUS_REG	READ	0x0000	Table 37
0x24	AVDDH_VOL_CODE_A_REG	READ	0x0000	Table 39
0x25	AVDDH_VOL_CODE_B_REG	READ	0x0000	
0x26	AVDDH_VOL_CODE_C_REG	READ	0x0000	
0x27	AVDDH_VOL_CODE_D_REG	READ	0x0000	
0x28	VOUT_VOL_CODE_A_REG	READ	0x0000	Table 41
0x29	VOUT_VOL_CODE_B_REG	READ	0x0000	
0x2A	VOUT_VOL_CODE_C_REG	READ	0x0000	
0x2B	VOUT_VOL_CODE_D_REG	READ	0x0000	
0x2C	IOUT_VOL_CODE_A_REG	READ	0x0000	Table 43
0x2D	IOUT_VOL_CODE_B_REG	READ	0x0000	
0x2E	IOUT_VOL_CODE_C_REG	READ	0x0000	
0x2F	IOUT_VOL_CODE_D_REG	READ	0x0000	
0x30	GND_CURRENT_CODE_A_REG	READ	0x0000	Table 45
0x31	GND_CURRENT_CODE_B_REG	READ	0x0000	
0x32	GND_CURRENT_CODE_C_REG	READ	0x0000	
0x33	GND_CURRENT_CODE_D_REG	READ	0x0000	

ADDRESS BYTE	FUNCTION	READ/WRITE	POWER-ON RESET VALUE	Section
0x34	ID_REG	READ	0x0B44	Table 47
0x35	DAC_ALL_REG	WRITE	0x0000	DAC_ALL_REG(address = 0x35) [reset = 0x0000]
0x36	GAIN_ALL_REG	WRITE	0x0000	GAIN_ALL_REG(address = 0x36) [reset = 0x0000]
0x37	OFFSET_ALL_REG	WRITE	0x0000	OFFEST_ALL_REG(address = 0x37) [reset = 0x0000]
0x38	CLEAR_ALL_REG	WRITE	0x0000	CLEAR_ALL_REG(address = 0x38) [reset = 0x0000]
0x39	SLEW_ALL_REG	WRITE	0x0000	SLEW_ALL_REG(address = 0x39) [reset = 0x0000]
0x3A	DAC_CTRL_ALL_REG	WRITE	0x0000	DAC_CTRL_ALL_REG(address = 0x3A) [reset = 0x0000]
0x3B	ADC_SETUP_ALL_REG	WRITE	0x0000	Table 49

DAC_A_REG~DAC_D_REG(address = 0x00~0x03) [reset = 0x0000]

Table 5. DAC_X_REG Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16-bit dac code															

Table 6. DAC_X_REG Bit Descriptions

Bit	Field	Type	Reset	Description
15:0	DAC_CODE	R/W	0x0000	DAC data，The data is in original code format, with a range of 0 to 65535 and a default value of 16'h0000.

GAIN_A_REG~GAIN_D_REG(address = 0x04~0x07) [reset = 0x0000]

Table 7. GAIN_X_REG Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16-bit gain code															

Table 8. GAIN_X_REG Bit Descriptions

Bit	Field	Type	Reset	Description
15:0	GAIN_CODE	R/W	0x0000	Gain data.The data is in complement format, with a range of -32768 to 32768 and a default value of 16'h0000，CODE=DATA*((GAIN/65536/8)+1)+OFFSET/8.

OFFEST_A_REG~OFFEST_D_REG(address = 0x08~0x0B) [reset = 0x0000]

Table 9. OFFEST_X_REG Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16-bit offest code															

Table 10. OFFEST_X_REG Bit Descriptions

Bit	Field	Type	Reset	Description
15:0	OFFEST_CODE	R/W	0x0000	Offset data.The data is in complement format, with a range of -32768 to 32768 and a default value of 16'h0000，CODE=DATA*((GAIN/65536/8)+1)+OFFSET/8.

CLEAR_A_REG~CLEAR_D_REG(address = 0x0C~0x0F) [reset = 0x0000]

Table 11. CLEAR_X_REG Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16-bit clear code															

Table 12. CLEAR_X_REG Bit Descriptions

Bit	Field	Type	Reset	Description
15:0	CLEAR_CODE	R/W	0x0000	In Clear mode, writing to this register replaces the DAC data register content. The data is in raw code format, ranges from 0 to 65535, and has a default value of 16'h0000.

SLEW_A_REG~SLEW_D_REG(address = 0x10~0x13) [reset = 0x0000]

The Slew Rate Register allows for independent control of the slew configuration on a per-channel basis, as well as leakage compensation during current output operation.

Table 13. SLEW_X_REG Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ICOMP_CODE				Reserved		IOUT_SLEW_EN	VOUT_SLEW_E N	SR_CLK				Reserved	SR_STEP		

Table 14. SLEW_X_REG Bit Descriptions

Bit	Field	Type	Reset	Description
15:12	ICOMP_CODE	R/W	0000	Leakage compensation has a total of 4 bits of current DAC, each step length compensates for 2M ohms of leakage error at the current output port, with the following correspondences. 0000: not on. 0010: 1M ohm leakage, corresponding to three-wire output. 0100: 500K leakage error, corresponding to a two-wire output. 1000: 250K ohm leakage, corresponding to UIO application.
11:10	Reserved	R	00	Reserved.
9	IOUT_SLEW_EN	R/W	0	Current slew rate enables. When SLEW is enabled, the SLEW configuration is loaded once at each step. The SLEW procedure supports the modification of the target value, and the SLEW procedure provides an indication in the status register. If SLEW is disabled during SLEW, the output result is directly jumped to the target value. The current output SLEW has a HART mode in DAC_CTRL reg, which has a fixed SLEW configuration. 1: Enable. 0: Disable.
8	VOUT_SLEW_EN	R/W	0	Voltage slew rate enables. When SLEW is enabled, the SLEW configuration is loaded once at each step. The SLEW procedure supports the modification of the target value, and the SLEW procedure provides an indication in the MAIN_STATUS register. If SLEW is disabled during SLEW, the output result is directly jumped to the target value. 1: Enable. 0: Disable.
7:4	SR_CLK	R/W	0000	Slew Rate update frequency(Hz): 0000: 256K. 0001: 128k. 0010: 64k. 0011: 32k. 0100: 16k. 0101: 8k. 0110: 4k. 0111: 2K. 1000: 1k. 1001: 500. 1010: 250. 1011: 125. 1100: 64. 1101: 32. 1110: 16. 1111: 2.
3	Reserved	R	00	Reserved.

Bit	Field	Type	Reset	Description
2:0	SR_STEP	R/W	000	Slew Rate step size(bit): 000:1. 001:2. 010:4. 011:8. 100:32. 101:64. 110:128. 111:256.

CTRL_A_REG~CTRL_D_REG(address = 0x14~0x17) [reset = 0x0000]

The parameters for each output channel are controlled independently through the DAC Control Register.

Table 15. DAC_CTRL_X_REG Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Reserved	CLEAR_EN	OUT_EN	OVRNG_EN	OUT_MODE	SW_EN	SW	HART_EN	HART_SLEW_EN	Reserved	RANGE_SEL				OUT_EN_DELAY	

Table 16. DAC_CTRL_X_REG Bit Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0	Reserved.
14	CLEAR_EN	R/W	0	Channel clear enables. 1: Need main control reg CLEAR_TRIG bit to trigger a clear output. 0: Disable.
13	OUT_EN	R/W	0	The channel output features a configurable initialization delay (controlled by a 2-bit field) for both enable and disable commands. Upon enable, the output is forced to a zero-scale level for the delay duration before switching to the programmed value. Upon disable, the output returns to zero-scale for the same delay period prior to the final shutdown of the output stage. 1: Enable. 0: Disable.
12	OVRNG_EN	R/W	0	The channel over-range output function is available exclusively in voltage output mode. 1: Enable. 0: Disable.
11	OUT_MODE	R/W	0	Choose two-wire/three-wire output,POC function is invalid in current channel under two-wire. UIO mode is also considered as two-wire mode,this mode is consistent with the configuration of the circuit board, which is used to distinguish between POC functions and current compensation. 1: Two-wire output. 0: Three-wire output.

Bit	Field	Type	Reset	Description
10	SW_EN	R/W	0	Switch enable,user control the VOUTN pulldown switch independently. 1: Enable,user control the VOUTN pulldown switch independently. 0: Disable,the VOUTN pulldown switch is control by OUT_MODE & OUT_EN & POC_MASK.
9	SW	R/W	0	An externally controlled of pull-down switch can be run independently, SW is only valid when SW_EN is 1. 1: Close the V_{OUTN} pulldown switch. 0: Open the V_{OUTN} pulldown switch.
8	HART_EN	R/W	0	HART input switch,in current output mode. 1: HART switchs on.External HART signals can access the internal system. HART signal is injected through external resistance. 0: External HART signal is disconnected.
7	HART_SLEW_EN	R/W	0	HART_SLEW is valid when the HART input is enable in current output mode. 1: Configure the block with IOUT_SLEW_EN=1, SR_CLK=8 kHz, and SR_STEP=128 LSB. This configuration generates a fixed slew rate, resulting in a 64 ms full-range slew time. 0: Slew control by user SLEW_REG.
6	Reserved	R	0	Reserved.
5:2	RANGE_SEL	R/W	0000	Range select: 0000：0-5 V. 0001：0-10 V. 0010：±5 V. 0011：±10 V. 0100：4-20 mA. 0101：0-20 mA. 0110：0-24 mA. 1110：LOOP_POWER(25mA).
1:0	OUT_EN_DELAY	R/W	00	A channel enable command initiates an initialization delay to establish the operating point of the output amplifier. During this interval, the DAC output is forced to its zero-scale code (0 in unipolar mode, 32767 in bipolar mode). The delay duration, programmed by a 2-bit field, is optimized to minimize output glitches upon enable. 00:64 μs. 01:128 μs. 10:256 μs. 11:512 μs.

ADC_SETUP_A&B_REG(address = 0x18) [reset = 0x0000]

The configuration register for ADC Channels A&B selects the filter type for direct additive processing. The selectable filter types are as follows:12-bit (left-shifted with 4-bit zero-padding)14-bit (left-shifted with 2-bit zero-padding)16-bit(Averaged).

Table 17. ADC_SETUP_A&B_REG Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
VDD_B_EN		VVOUT_B_EN		IVOUT_B_EN		IVOUT_B_EN		IGND_B_EN		VDD_A_EN		VVOUT_A_EN		IGND_A_EN	

Table 18. ADC_SETUP_A&B_REG Bit Descriptions

Bit	Field	Type	Reset	Description
15:14	VDD_B_EN	R/W	00	High voltage positive Power Acquisition Configuration. 00: Disable 01: No averaging 10: 4 averages 11: 16 averages
13:12	VVOUT_B_EN	R/W	00	Voltage output acquisition configuration, use V_{SENSEP} Pin. 00: Disable. 01: No averaging. 10: 4 averages. 11: 16 averages.
11:10	IVOUT_B_EN	R/W	00	Current output pin voltage acquisition Configuration. 00: Disable 01: No averaging 10: 4 averages 11: 16 averages
9:8	IGND_B_EN	R/W	00	Voltage or current output mode, Ground current Acquisition Configuration. 00: Disable. 01: No averaging. 10: 4 averages. 11: 16 averages.
7:6	VDD_A_EN	R/W	00	High voltage positive power acquisition configuration 00: Disable. 01: No averaging. 10: 4 averages. 11: 16 averages.
5:4	VVOUT_A_EN	R/W	00	Voltage output acquisition configuration, use V_{SENSEP} PIN. 00: Disable. 01: No averaging. 10: 4 averages. 11: 16 averages.
3:2	IVOUT_A_EN	R/W	00	Current Output Pin voltage Acquisition Configuration. 00: Disable. 01: No averaging. 10: 4 averages. 11: 16 averages.
1:0	IGND_A_EN	R/W	00	Voltage or Current output mode, Ground current Acquisition Configuration.

Bit	Field	Type	Reset	Description
				00: Disable. 01: No averaging. 10: 4 averages. 11: 16 averages.

ADC_SETUP_C&D_REG(address = 0x19) [reset = 0x0000]

The configuration register for ADC Channels C&D selects the filter type for direct additive processing. The selectable filter types are as follows:12-bit (left-shifted with 4-bit zero-padding)14-bit (left-shifted with 2-bit zero-padding)16-bit(Averaged).

Table 19. ADC_SETUP_C&D_REG Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
VDD_D_EN		VVOUT_D_EN		IVOUT_D_EN		IGND_D_EN		VDD_C_EN		VVOUT_C_EN		IVOUT_C_EN		IGND_C_EN	

Table 20. ADC_SETUP_C&D_REG Bit Descriptions

Bit	Field	Type	Reset	Description
15:14	VDD_D_EN	R/W	00	High voltage positive Power Acquisition Configuration. 00: Disable. 01: No averaging. 10: 4 averages. 11: 16 averages.
13:12	VVOUT_D_EN	R/W	00	Voltage output Acquisition Configuration, use V_{SENSEP} PIN. 00: Disable. 01: No averaging. 10: 4 averages. 11: 16 averages.
11:10	IVOUT_D_EN	R/W	00	Current Output PIN voltage Acquisition Configuration 00: Disable. 01: No averaging. 10: 4 averages. 11: 16 averages.
9:8	IGND_D_EN	R/W	00	Voltage or Current output mode, Ground current Acquisition Configuration 00: Disable. 01: No averaging. 10: 4 averages. 11: 16 averages.
7:6	VDD_C_EN	R/W	00	High voltage positive Power Acquisition Configuration 00: Disable 01: No averaging 10: 4 averages 11: 16 averages
5:4	VVOUT_C_EN	R/W	00	Voltage output Acquisition Configuration, use V_{SENSEP} PIN. 00: Disable. 01: No averaging.

Bit	Field	Type	Reset	Description
				10: 4 averages. 11: 16 averages.
3:2	IVOUT_C_EN	R/W	00	Current Output PIN voltage Acquisition Configuration 00: Disable. 01: No averaging. 10: 4 averages. 11: 16 averages.
1:0	IGND_C_EN	R/W	00	Voltage or Current output mode, Ground current Acquisition Configuration 00: Disable. 01: No averaging. 10: 4 averages. 11: 16 averages.

NOP_REG(address = 0x1A) [reset = 0x0000]

No operation (NOP) or a request to read another register.

Table 21. NOP_REG Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Nop code															

Table 22. NOP_REG Bit Descriptions

Bit	Field	Type	Reset	Description
15:0	NOP_CODE	W	0x0000	No operation.

ADC_CTRL_REG(address = 0x1C) [reset = 0x0000]

The ADC control register is used to set the operational configuration. Once the ADC is enabled, an initialization time of more than 20 μs is required. After this period, the quantization process is triggered by writing the configuration data into the register.

Table 23. ADC_CTRL_REG Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Reserved										DATA_STATUS	ADC_CONVERT_MODE	TRIG_STATUS1&2		DRDY_TIME	

Table 24. ADC_CTRL_REG Bit Descriptions

Bit	Field	Type	Reset	Description
15:6	Reserved	W	0000000000	Reserved.
5	DATA_STATUS	R	0	The response to an SPI read during an ongoing ADC conversion is determined by a configuration bit:

Bit	Field	Type	Reset	Description
				1: The read operation returns the address and data of the MAIN_STATUS_REG. 0: Return the expected data address along with the old (stale) conversion data.
4	ADC_CONVERT_MODE	R/W	0	0: ADC single converts. 1: ADC continuous converts.
3:2	TRIG_STATUS1&2	R/W	00	**Available when ADC_CONVERT_MODE is 0**. 00: Default state. No conversion is started. 01: Conversion is complete. Outputs DRDY. 10: Conversion is in progress. 11: Starts a conversion. Trigger is blocked if ADC is not ready. **Available when ADC_CONVERT_MODE is 1**. 00: Default state. The ADC is idle. Writing '00' to the register will halt any ongoing conversion. 01: Writing '11' initiates a conversion. The ADC trigger is blocked if the ADC is not ready to start. 10: The ADC conversion is in progress. 11: The conversion is complete. The DRDY (Data Ready) signal is asserted for a predefined delay, after which the state automatically returns to '10 (Busy)'.
1:0	DRDY_TIME	R/W	00	Only available when ADC_CONVERT_MODE is continuous converts. 00：DRDY stays 20 μs then invalid. 01：DRDY stays 50 μs then invalid. 10：DRDY stays 100 μs then invalid. 11：DRDY stays 200 μs then invalid.

MAIN_CTRL_REG(address = 0x1D) [reset = 0x0000]

The Main Control Register serves as the primary interface for configuring the chip's global functionality and enables rapid initialization.

Table 25. MAIN_CTRL_REG Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Reserved	CRC_EN	FAULT_PD	FAULT_STORE	SLEW_ALL	ICOMP_ALL	OUT_EN_ALL	SOFT_LATCH	SOFT_CLEAR	Reserved	POC_MASK	ADC_EN	WD_TIME		WD_EN	STATUS_READ

Table 26. MAIN_CTRL_REG Bit Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0	Reserved.
14	CRC_EN	R/W	0	1: Enable CRC. 0: Disable CRC.
13	FAULT_PD	R/W	0	Fast setting of FAULT_MASK reg, it masks all fault output. 1: Enables masking. All fault outputs are suppressed.

Bit	Field	Type	Reset	Description
				0: Disables global masking. Fault outputs are then controlled by the individual bits of the FAULT_MASK register.
12	FAULT_STORE	R/W	0	Select the input data of FAULT_MSAK reg. 1: The data is from FAULT_STORE_REG. 0: The data is from MAIN_STATUS_REG.
11	SLEW_ALL	R/W	0	1: Simultaneously enables the IOUT_SLEW_EN function for all four channels, overriding individual channel settings. 0: The slew enable function for each channel is independently controlled by its respective bit in the SLEW_CTRL register.
10	ICOMP_ALL	R/W	0	Quick settings of all channel current compensation. 1: Open the ICOMP_CODE of all four channels, when OUT_MODE is 1(two wires output mode) ,ICOMP_CODE is 0100,when OUT_MODE is 0(three wires output mode), ICOMP CODE is 0010. 0: The current compensation for each channel is set independently.
9	OUT_EN_ALL	R/W	0	1: Open the OUT_EN of all four channels. 0: Each channel is enabled independently.
8	SOFT_LATCH	W	0	This bit implements a software latching function, where a data write is effective only once. Setting it updates the output with the values from all channels' DATA_REG. After a SOFT_CLEAR operation, the output reverts to the DATA_REG value, and this bit becomes the only way to write to it again. 1:Start a latch to all channels. 0:Latch by LDAC&SYNC pin.
7	SOFT_CLEAR	W	0	This function triggers a one-time clear operation for all channels. To execute it, the CLEAR_EN bit in the DAC_CTRL register must first be set to 1. Once the CLEAR_TRIG bit is set, the output of each enabled channel is updated to the value stored in its CLEAR_REG. To revert the output to the original DATA_REG value, write 1 to SOFT_LATCH. Note that the LDAC pin cannot perform this reversion; it requires rewriting the DATA_REG and initiating a separate update. 1: Clear the output to clear value of the channel which CLEAR_EN is 1 in DAC_CTRL REG. 0: No clear action.
6	Reserved	R	0	Reserved.
5	POC_MASK	R/W	0	The configuration of V_{OUTN}pull down switch is not enabled in the voltage output mode, which works on all channels. The closed impedance is 13K ohm to ensure that the output zero voltage and avoid floating jitter. This configuration is valid only in the three -line mode with independent output of voltage & current, and it is invalid in the mode of voltage & current reuse. Keep the switch open and avoid current leakage. 1: Disable the POC. The pulldown switch remains open until VOUT is enabled, and can only be closed via the SW bit in the DAC_CTRL register.

Bit	Field	Type	Reset	Description
				0: The VOUTN pulldown switch shall be closed only if OUT_MODE is 0 (3-wire output mode) and OUT_EN is 0. Otherwise, it shall be open.
4	ADC_EN	R/W	0	After enabling the ADC, a mandatory initialization delay of >20 µs is required for internal bias settling. All configuration writes (enable, conversion mode, channel selection) must be completed after this delay and before initiating a new conversion. 1: When the ADC is enabled, the amplifier is also powered on. 0: When the ADC is disabled, both the amplifier is powered down and the clock is gated.
3:2	WD_TIME	R/W	00	Timeout select bits. Used to select the timeout period for the watchdog timer. 00: 5 ms. 01: 10 ms. 10: 100 ms. 11: 200 ms.
1	WD_EN	R/W	0	Enable watchdog timer. 1: Enable watchdog. 0: Disable watchdog.
0	STATUS_READ	R/W	0	When this bit is enabled, the address and content of the MAIN_STATUS register are automatically output via SDO during subsequent SPI commands. The STATUS_READ output has preemptive priority over normal register readback. For standard ADC and register read operations, this feature must be disabled. 1: Enable the auto-readback function. When enabled, the SDO line will output the contents of the MAIN_STATUS register upon receiving any SPI command. 0: Close auto readback.

SOFTWARE_REG(address = 0x1E) [reset = 0x0000]

This register groups the software register, CRC check, and fault output settings. The lower 12 bits contain an embedded key, which is used to service the watchdog timer and trigger an on-chip reset

Table 27. SOFTWARE_REG Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
FUNC_CODE															

Table 28. SOFTWARE_REG Bit Descriptions

Bit	Field	Type	Reset	Description
15:0	FUNC_CODE	W	0x0000	0x0555: To perform a full chip reset, write the value 0x0555 0x0358: The reset flag is cleared by writing 0x0358 following the next reset 0x0284: Write 0x0284 to clear the watchdog fault and feed the dog

FAULT_MASK_REG(address = 0x1F) [reset = 0x0000]

Signal is selected from the status register or FAULT_STORE_REG to generate an output error, and the selected signal is combined to form the output error signal. The selection of the signal source is controlled by the software registers, and the error reports of the status register data are refreshed in real time, and the errors in the FAULT_STORE_REG are maintained.

Table 29. FAULT_MASK_REG Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CRC_ERROR_MASK	OTP135_MASK	OTP150_MASK	SPI_ERROR_MASK	VOUT_OC_MASK				LOOP_DISCON_MASK				IOUT_NEG_VOL_MASK			

Table 30. FAULT_MASK_REG Bit Descriptions

Bit	Field	Type	Reset	Description
15	CRC_ERROR_MASK	R/W	0	1: Mask CRC error 0: Pointless
14	OTP135_MASK	R/W	0	1: Mask the over-temperature fault (135°C) 0: Pointless
13	OTP150_MASK	R/W	0	1: Mask the over-temperature fault (150°C) 0: Pointless
12	SPI_ERROR_MASK	R/W	0	1: Mask spi error 0: Pointless
11:8	VOUT_OC_MASK	R/W	0000	Only in voltage output mode 1000: Mask D channel fault 0100: Mask C channel fault 0010: Mask B channel fault 0001: Mask A channel fault 0000: Pointless
7:4	LOOP_DISCON_MASK	R/W	0000	Only in current output mode, excluding LOOP_POWER mode. 1000: Mask D channel fault. 0100: Mask C channel fault. 0010: Mask B channel fault. 0001: Mask A channel fault. 0000: Pointless.
3:0	IOUT_NEG_VOL_MASK	R/W	0000	In current output mode and LOOP POWER mode. 1000: Mask D channel fault. 0100: Mask C channel fault. 0010: Mask B channel fault. 0001: Mask A channel fault. 0000: pointless.

FAULT_CLEAR_REG(address = 0x20) [reset = 0x0000]

This register provides a bit-wise clear function for the FAULT_STORE_REG. A clear command, once written, is latched (the bit value remains set), but the actual clearing operation for the corresponding fault bit is executed only once upon writing

Table 31. FAULT_CLEAR_REG Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CRC_ERROR_CLEAR	OTP135_CLEAR	OTP150_CLEAR	SPI_ERROR_CLEAR	VOUT_OC_CLEAR				LOOP_DISCON_CLEAR				IOUT_NEG_VOL_CLEAR			

Table 32. FAULT_CLEAR_REG Bit Descriptions

Bit	Field	Type	Reset	Description
15	CRC_ERROR_CLEAR	W	0	1: Clear CRC fault. 0: Pointless.
14	OTP135_CLEAR	W	0	1: Clear the over-temperature fault (135°C). 0: Pointless.
13	OTP150_CLEAR	W	0	1: Clear the over-temperature fault (150°C). 0: Pointless.
12	SPI_ERROR_CLEAR	W	0	1: Clear spi fault. 0: Pointless.
11:8	VOUT_OC_CLEAR	W	0000	1000: Clear the output voltage short-circuit fault on Channel D. 0100: Clear the output voltage short-circuit fault on Channel C. 0010: Clear the output voltage short-circuit fault on Channel B. 0001: Clear the output voltage short-circuit fault on Channel A. 0000: Pointless.
7:4	LOOP_DISCON_CLEAR	W	0000	1000: Clear the output current open-circuit fault on Channel D. 0100: Clear the output current open-circuit fault on Channel C. 0010: Clear the output current open-circuit fault on Channel B. 0001: Clear the output current open-circuit fault on Channel A. 0000: Pointless.
3:0	IOUT_NEG_VOL_CLEAR	W	0000	1000: Clear the negative voltage detection fault on Current Channel D. 0100: Clear the negative voltage detection fault on Current Channel C. 0010: Clear the negative voltage detection fault on Current Channel B. 0001: Clear the negative voltage detection fault on Current Channel A. 0000: Pointless.

FAULT_STORE_REG(address = 0x21) [reset = 0x0000]

The register that records the occurrence of the error event is controlled by the software register, and once the error occurs, it will be recorded and maintained, so that the customer can debug the instantaneous error report.

Table 33. FAULT_STORE_REG Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CRC_ERROR_STORE	OTP135_STORE	OTP150_STORE	SPI_ERROR_STORE	VOUT_OC_STORE				LOOP_DISCON_STORE				IOUT_NEG_VOL_STORE			

Table 34. FAULT_STORE_REG Bit Descriptions

Bit	Field	Type	Reset	Description
15	CRC_ERROR_STORE	R	0	1: A CRC error has been detected. 0: Pointless.
14	OTP135_STORE	R	0	1: Indicates that an OTP135 error has occurred. 0: Pointless.
13	OTP150_STORE	R	0	1: Indicates that an OTP150 error has occurred. 0: Pointless.
12	SPI_ERROR_STORE	R	0	1: Indicates that an SPI communication error has occurred. 0: Pointless.
11:8	VOUT_OC_STORE	R	0000	1000: D channel VOUT over current flag has occurred,include source or sink over current error. 0100: C channel VOUT over current flaghas occurred,include source or sink over current error. 0010: B channel VOUT over current flag has occurred,include source or sink over current error. 0001: A channel VOUT over current flag has occurred,include source or sink over current error. 0000: Pointless.
7:4	LOOP_DISCON_STORE	R	0000	1000: D channel IOUT diisconnect flag has occurred. 0100: C channel IOUT diisconnect flag has occurred. 0010: B channel IOUT diisconnect flag has occurred. 0001: A channel IOUT diisconnect flag has occurred. 0000: Pointless.
3:0	IOUT_NEG_VOL_STORE	R	0000	1000: D channel IOUT negative voltage flag has occurred. 0100: C channel IOUT negative voltage flag has occurred. 0010: B channel IOUT negative voltage flag has occurred. 0001: A channel IOUT negative voltage flag has occurred. 0000: Pointless.

MAIN_STATUS_REG(address = 0x22) [reset = 0x0000]

Main status reg,It is used to record the key status information of the chip, and the user can obtain the working status of the chip by reading back this register.

Table 35. MAIN_STATUS_REG Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CRC_EN_STATUS	CRC_ERROR_STATUS	OTP135_STATUS	OTP150_STATUS	SPI_ERROR_STATUS	ADC_READY_STATUS	AVDD_POWER_UP				RESET_NOTE_STATUS	SLEW_STATUS	DAC_OUT_STATUS			

Table 36. MAIN_STATUS_REG Bit Descriptions

Bit	Field	Type	Reset	Description
15	CRC_EN_STATUS	R	0	1: Indicates that the CRC check function is enabled.

Bit	Field	Type	Reset	Description
				0: Indicates that the CRC check function is disabled.
14	CRC_ERROR_STATUS	R	0	1: Indicates that a CRC error check is currently in progress. 0: No CRC fault.
13	OTP135_STATUS	R	0	1: Indicates that an OTP135 error check is currently active. 0: No OTP135 fault.
12	OTP150_STATUS	R	0	1: Indicates that an OTP150 error has been detected. When this bit is set, the system immediately and automatically disables the output. 0: No OTP150 fault.
11	SPI_ERROR_STATUS	R	0	1: Indicates that the SPI watchdog timeout due to communication failure. 0: No SPI fault.
10	ADC_READY_STATUS	R	0	1:Indicates that the ADC completes the quantization of a new set of inputs. In single-shot mode, this signal remains at 1 until the next quantization begins. In continuous mode, this signal lasts for a certain period of time (set in the ADC_CTRL_REG) and then goes to zero, starting a new quantization cycle. 0:Indicates that there is no new data update.
9:6	AVDD_POWER_UP	R	0000	Indicates the power-on status of each high-voltage positive power (AV_{DD_X})supply for each channel, and the default value is 0, indicating that the high-voltage power supply is not powered on. 1 indicates that the high-voltage power supply is powered on and the UVLO has been triggered. 1000: The D channel power is enabled. 0100: The C channel power is enabled 0010: The B channel power is enabled 0001: The A channel power is enabled
5	RESET_NOTE_STATUS	R	0	Record the global reset event. 1:This bit indicates that a global reset has occurred. The reset can be triggered via two sources: writing the value 0x0555 to a software register, or through an external PIN signal (which has a 50μs debounce delay). This status bit can only be cleared by writing the key value 0x0358. 0:Means no reset.
4	SLEW_STATUS	R	0	1: This status bit is asserted when the condition of at least one channel being in the SLEW state is active. 0: means no SLEW, which can be SLEW end or SLEW is not enabled
3:0	DAC_OUT_STATUS	R	0000	This status bit indicates that the output is enabled, a condition which applies to all available output modes 1000: The D channel output is enabled. 0100: The C channel output is enabled. 0010: The B channel output is enabled. 0001: The A channel output is enabled. 0000: No channel outputs are enabled.

OUT_STATUS_REG(address = 0x23) [reset = 0x0000]

It is used to record error messages on each output channel and is a functional safety feature of the analog interface.

Table 37. OUT_STATUS_REG Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
VOUT_SOURCE_OC				VOUT_SINK_OC				LOOP_DISCONNECT				IOUT_NEG_VOL			

Table 38. OUT_STATUS_REG Bit Descriptions

Bit	Field	Type	Reset	Description
15:12	VOUT_SOURCE_OC	R	0000	The VOUT_SOURCE_OC flag indicates an over-current condition at the voltage output. This flag is only applicable in voltage output mode 1000: An over-source current condition has been detected on the D channel. 0100: An over-source current condition has been detected on the C channel. 0010: An over-source current condition has been detected on the B channel. 0001: An over-source current condition has been detected on the A channel. 0000: No over-source current condition is detected.
11:8	VOUT_SINK_OC	R	0000	The VOUT_SINK_OC flag indicates an over-current condition in the sink path. It is only valid in voltage output mode 1000: An over-sink current condition has been detected on the D channel. 0100: An over-sink current condition has been detected on the C channel. 0010: An over-sink current condition has been detected on the B channel. 0001: An over-sink current condition has been detected on the A channel. 0000: No over-sink current condition is detected.
7:4	LOOP_DISCONNECT	R	0000	Current output open circuit indication. When the output current is less than the set value, this error will be reported, and it will not necessarily be completely broken. Valid only in current output mode, excluding LOOP_POWER mode. 1000: The D channel operates in open-loop mode 0100: The C channel operates in open-loop mode 0010: The B channel operates in open-loop mode 0001: The A channel operates in open-loop mode 0000: The output operates without open circuits, and the output current accurately tracks the programmed value
3:0	IOUT_NEG_VOL	R	0000	In current output modes, including LOOP-POWER mode, the current output port has a negative voltage detection, and the negative voltage of the port will cause a large increase in heat generation, resulting in over-temperature protection and output disable. 1000: A negative voltage has been detected on output channel D.

Bit	Field	Type	Reset	Description
				0100: A negative voltage has been detected on output channel C. 0010: A negative voltage has been detected on output channel B. 0001: A negative voltage has been detected on output channel A. 0000: The current output pins do not generate negative voltages.

AVDDH_VOL_CODE_A_REG~AVDDH_VOL_CODE_D_REG(address = 0x24~0x27) [reset = 0x0000]

AV_{DD} power supply pin voltage acquisition code.

Table 39. AVDDH_VOL_CODE_X_REG Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
AVDDH VOL CODE															

Table 40. AVDDH_VOL_CODE_X_REG Bit Descriptions

Bit	Field	Type	Reset	Description
15:0	AVDDH_VOL_CODE	R	0x0000	High voltage power supply(AV_{DD_X}) quantization result register, no new sampling, data retention of the last result. The ADC resolution is 12 bits, and the registers store 16 bits of data. When there is no average, the 12-bit raw data is 4bits 0 in the lowest. 4 average, the results of four consecutive quantizations are added up, extended to 14 bits, and the low position is supplemented by 2bits 0. 16 averages, the results of 16 consecutive quantizations are added up to obtain 16-bit data.

VOUT_VOL_CODE_A_REG~VOUT_VOL_CODE_D_REG(address = 0x28~0x2B) [reset = 0x0000]

V_{OUT} output pin voltage acquisition code.

Table 41. VOUT_VOL_CODE_X_REG Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
VOUT VOL CODE															

Table 42. VOUT_VOL_CODE_X_REG Bit Descriptions

Bit	Field	Type	Reset	Description
15:0	VOUT_VOL_CODE	R	0x0000	V_{SENSEP} pin voltage quantization result register, no new sampling, data retention of the last result. The ADC resolution is 12 bits, and the registers store 16 bits of data. When there is no average, the 12-bit raw data is 4 bits 0 in the lowest. 4 average, the results of four consecutive quantizations are added up, extended to 14 bits, and the low position is supplemented by 2 bits 0. 16 averages, the results of 16 consecutive quantizations are added up to obtain 16-bit data.

IOUT_VOL_CODE_A_REG~IOUT_VOL_CODE_D_REG(address = 0x2C~0x2F) [reset = 0x0000]

I_{OUT} output pin voltage acquisition code.

Table 43. IOUT_VOL_CODE_X_REG Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IOUT VOL CODE															

Table 44. IOUT_VOL_CODE_X_REG Bit Descriptions

Bit	Field	Type	Reset	Description
15:0	IOUT_VOL_CODE	R	0x0000	I_{OUT} pin voltage quantization result register, no new sampling, data retention of the last result. The ADC resolution is 12 bits, and the registers store 16 bits of data. When there is no average, the 12-bit raw data is 4 bits 0 in the lowest. 4 average, the results of four consecutive quantizations are added up, extended to 14 bits, and the low position is supplemented by 2 bits 0. 16 averages, the results of 16 consecutive quantizations are added up to obtain 16-bit data.

GND_CURRENT_CODE_A_REG~GND_CURRENT_CODE_D_REG(address = 0x30~0x33) [reset = 0x0000]

V_{SENSEN} pin voltage acquisition code.

Table 45. GND_CURRENT_CODE_X_REG Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
GND CURRENT CODE															

Table 46. GND_CURRENT_CODE_X_REG Bit Descriptions

Bit	Field	Type	Reset	Description
15:0	GND_CURRENT_CODE	R	0x0000	Ground(V_{SENSEN}) current quantization result register, no new sampling, data retention of the last result. The ADC resolution is 12 bits, and the registers store 16 bits of data. When there is no average, the 12-bit raw data is 4 bits 0 in the lowest. 4 average, the results of four consecutive quantizations are added up, extended to 14 bits, and the low position is supplemented by 2 bits 0. 16 averages, the results of 16 consecutive quantizations are added up to obtain 16-bit data.

ID_REG(address = 0x34) [reset = 0x0B44]

Id data reg.

Table 47. ID_REG Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CHIP_VERSION				CHIP_TYPE											

Table 48. ID_REG Bit Descriptions

Bit	Field	Type	Reset	Description
15:12	CHIP_VERSION	R	0x0	Indicates the chip version, the default version 0x0, and is added as needed
11:0	CHIP_TYPE	R	0xB44	Indicates the chip model, the default 0xB44, and the conversion decimal is 2884

DAC_ALL_REG(address = 0x35) [reset = 0x0000]

The register can only be written to, and it is used for data configuration of the four channels of the TPC2884. For the specific register description, please refer to DAC_X_REG (Table 5).

GAIN_ALL_REG(address = 0x36) [reset = 0x0000]

The register can only be written to, and it is used for configuring the gain data of the four channels of the TPC2884. For the specific register description, please refer to GAIN_X_REG (Table 7).

OFFEST_ALL_REG(address = 0x37) [reset = 0x0000]

The register can only be written to, and it is used for configuring the offest data of the four channels of the TPC2884. For the specific register description, please refer to OFFEST_X_REG (Table 9).

CLEAR_ALL_REG(address = 0x38) [reset = 0x0000]

The register can only be written to, and it is used for configuring the clear data of the four channels of the TPC2884. For the specific register description, please refer to CLEAR_X_REG (Table 11).

SLEW_ALL_REG(address = 0x39) [reset = 0x0000]

The register can only be written to, and it is used for configuring the data of the slew registers for the four channels of the TPC2884. For the specific register description, please refer to SLEW_X_REG (Table 13)

DAC_CTRL_ALL_REG(address = 0x3A) [reset = 0x0000]

The register can only be written to, and it is used for configuring the data of the control registers for the four channels of the TPC2884. For the specific register description, please refer to DAC_CTRL_X_REG (Table 15)

ADC_SETUP_ALL_REG(address = 0x3B) [reset = 0x0000]

The register can only be written to, and it is used for configuring the data of the ADC setup registers for the four channels of the TPC2884.

Table 49. ADC_SETUP_ALL_REG Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Reserved								VDD_EN		VVOUT_EN		IVOUT_EN		IGND_EN	

Table 50. ADC_SETUP_ALL_REG Bit Descriptions

Bit	Field	Type	Reset	Description
15:8	Reserved	R	0x00	Reserved
7:6	VDD_EN	W	00	High voltage positive Power Acquisition Configuration 00: Disable

Bit	Field	Type	Reset	Description
				01: no averaging 10: 4 averages 11: 16 averages
5:4	VVOUT_EN	W	00	Voltage output Acquisition Configuration, use VSENSEP pin. 00: Disable 01: no averaging 10: 4 averages 11: 16 averages
3:2	IVOUT_EN	W	00	Current Output PIN voltage Acquisition Configuration 00: Disable 01: no averaging 10: 4 averages 11: 16 averages
1:0	IGND_EN	W	00	Voltage or Current output mode, Ground current Acquisition Configuration 00: Disable 01: no averaging 10: 4 averages 11: 16 averages

Functional Modes

Internal Reference

The TPC2884 includes an integrated 4.096-V reference with an initial accuracy of ±2 mV maximum and a temperature drift coefficient of 10 ppm/°C maximum. A buffered output capable of driving up to 10 mA is available on REFOUT.

Power-On-Reset

The TPC2884 contains power on reset circuits which is based on AV_{DD} and DV_{DD} power supplies. After power on, the power-on-reset circuit ensures that all registers are at their default values (see Table 4). The current and voltage output DACs are disabled. The current output pin is in high impedance state. The V_{OUTN_X} is in a 13 kΩ-to-GND state; however, the V_{SENSEP_X} pin is an open circuit. The voltage output pin impedance may be changed to high-impedance by the POC bit setting.

FAULTN Pin

The TPC2884 contains an FAULTN pin. When one or more of the following events occur, the FAULTN pin is pulled low:

- The load on any channel's I_{OUT_X} pin is in open circuit;
- The I_{OUT_X} port has detected a negative voltage at the port (< -4 V);
- The output current or input current of V_{OUT_X} exceeds 20 mA;
- The chip temperature exceeds 135℃;
- The SPI watchdog timer exceeded the timeout period (if enabled);
- The SPI frame error check (CRC) encountered an error (if enabled).

In systems where the FAULTN outputs of multiple TPC2884 devices are connected in a wired-AND fashion, the collective fault signal requires the host processor to poll the status register of each device to ascertain all individual fault conditions.The FAULTN alarm condition is cleared by one of the following actions:

- Resetting the corresponding fault bits in the status clear register (address 0x20);
- Performing software reset (write to address 0x1E,0x0555);
- Toggling hardware reset pin;
- Performing power on reset.

Status Register

Since, TPC2884 contains one FAULTN pin for the entire chip, the status of individual fault conditions can be checked using the status register. These registers (address 0x22,0x23) consist of five types of FAULTN status bits (Faults on current and voltage outputs , Over temperature condition, CRC errors and Watchdog timeout). The device continuously monitors these conditions. When a fault occurs, the FAULTN pin is pulled low and the corresponding status bit is set ('1'). Whenever one of these status bits is set, it remains set until the user clears it by writing '1' to the corresponding bit on address 0x20. The status bit can also be cleared by performing a hardware reset, software reset, or power-on reset. Note that it takes a minimum of 8 µsec for the status register to get reset. These bits are reasserted if the FAULT condition continues to exist in the next monitoring cycle.

Fault Mask

The FAULTN pin for TPC2884 is triggered by any of the alarm conditions (see FAULTN Pin). However, these different alarm conditions can be masked from creating the alarm signal at the pin by using the status mask register. The fault mask register (address 0x1F) has the same bit order as the fault register except that it can be set to mask any or all fault bits that create the alarm signal.

Programmable Slew Rate

The slew rate control feature allows the user to control the rate at which the output voltage or current changes. This feature is disabled by default and can be enabled for the selected channel by writing logic '1' to the IOUT_SLEW_EN bit or VOUT_SLEW_EN bit at address 0x10~0x14. With the slew rate control feature disabled, the output changes smoothly at a rate limited by the output drive circuitry and the attached load.With this feature enabled, the output does not slew directly between the two values. Instead, the output steps digitally at a rate defined by bits [2:0] (SR_STEP) and bits [3:0] (SR_CLK) on address 0x10~0x14.SR_CLK defines the rate at which the digital slew updates; SR_STEP defines the amount by which the output value changes at each update.

$$\text{Slew Time} = \frac{\text{Code Change}}{\text{Step Size} \times \text{Update Clock Frequency}} \quad (6)$$

Where:

- Slew Time is expressed in seconds

When the slew rate control feature is enabled, the output changes happen at the programmed slew rate. This configuration results in a staircase formation at the output. When a new DAC data is written, the output starts slewing to the new value at the slew rate determined by the current DAC code and the new DAC data. The update clock frequency for any given value is the same for all output ranges. The step size, however, varies across output ranges for a given value of step size because the LSB size is different for each output range. Note that disabling the slew rate feature while the DAC is executing the slew rate command aborts the slew rate operation and the DAC output stays at the last code after which the slew rate disable command was acknowledged.

Table 51. Slew Rate Step Size Options

SR_STEP	Slew Rate step size
0	1
1	2
10	4
11	8
100	32
101	64
110	128
111	256

Table 52. Slew Rate Update Clock Options

SR_CLK	Slew Rate update frequency (Hz)
0	256,000
1	128,000
10	64,000
11	32,000
100	16,000
101	8,000
110	4,000
111	2,000
1000	1,000
1001	500
1010	250
1011	125
1100	64
1101	32
1110	16
1111	2

Table 53. Programmable Slew Time Values in Seconds for a Full-Scale Change on Any Output Range (65535 Code)

	Slew Rate step size							
Slew Rate update frequency (Hz)	**1**	**2**	**4**	**8**	**32**	**64**	**128**	**256**
256,000	0.256	0.128	0.064	0.032	0.008	0.004	0.002	0.001
128,000	0.512	0.256	0.128	0.064	0.016	0.008	0.004	0.002
64,000	1.024	0.512	0.256	0.128	0.032	0.016	0.008	0.004
32,000	2.048	1.024	0.512	0.256	0.064	0.032	0.016	0.008

	Slew Rate step size							
16,000	4.096	2.048	1.024	0.512	0.128	0.064	0.032	0.016
8,000	8.192	4.096	2.048	1.024	0.256	0.128	0.064	0.032
4,000	16.384	8.192	4.096	2.048	0.512	0.256	0.128	0.064
2,000	32.768	16.384	8.192	4.096	1.024	0.512	0.256	0.128
1,000	65.536	32.768	16.384	8.192	2.048	1.024	0.512	0.256
500	131.072	65.536	32.768	16.384	4.096	2.048	1.024	0.512
250	262.144	131.072	65.536	32.768	8.192	4.096	2.048	1.024
125	524.288	262.144	131.072	65.536	16.384	8.192	4.096	2.048
64	1024	512	256	128	32	16	8	4
32	2048	1024	512	256	64	32	16	8
16	4096	2048	1024	512	128	64	32	16
2	32768	16384	8192	1024	256	128	64	32

HART Interface

On the TPC2884, digital communication such as HART can be modulated onto the input signal for each channel. In the case where the RANGE_SEL (address 0x14~0x17) bits are programmed such that the I_{OUT_X} is enabled, the external HART signal (ac voltage; 500 mVPP, 1200 Hz, and 2200 Hz) can be capacitively coupled in through the CHART_X pin and transferred to a current that is superimposed on the current output. The CHART_X pin has a typical input impedance of 12.5 kΩ, depending on the selected current output range, which together with the input capacitor used to couple the external HART signal into the CHART_X pin can be used to form a high-pass filter to attenuate frequencies below the HART bandpass region. In addition to this filter, an external passive filter is recommended to complete the filtering requirements of the HART specifications. Figure 63 shows a typical connection diagram of the CHART_X pin of the TPC2884. Among them, R1 = 48 kΩ, R2 = 10 kΩ, and C1 = 6.37 nF. If HART is not used, it is recommended to connect this port to AGND through a 10 kΩ resistor.

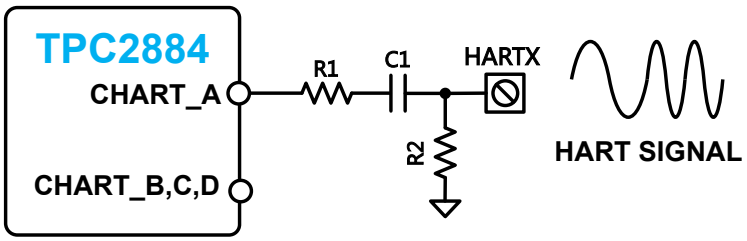


Figure 63. Typical HART Coupling Circuit of TPC2884

Watchdog Timer

This feature is useful to ensure that communication between the host processor and the TPC2884 has not been lost. It can be enabled by setting the WD_EN (address 0x1D) bit to '1'. The watchdog timeout period can be set using the WD_TIME[1:0] address 0x1D) bits. The timer period is based off an internal oscillator with a typical value of 2 MHz.

If enabled, the chip must have an SPI frame written to the device within the programmed timeout period. Otherwise, the FAULTN pin asserts low, and the SPI_ERROR_STATUS bit (address 0x22) of the status register is set to '1'. The SPI_ERROR_STATUS bit is set to '0' with a software/hardware reset, or write 0x0284 to 0x1E register, or by disabling the watchdog timer (WD_EN = '0'), or powering down the device.

Table 54. Watchdog Timeout Period

WDPD bits	WATCHDOG TIMEOUT PERIOD (Typical, ms)
00	10
01	51
10	102
11	204

Internal ADC

The TPC2884 integrates a 12-bit ADC internally, which can measure the voltage of the internal AV_{DD} port, I_{OUT} port, V_{OUT}, and V_{SENSEN} port. In addition, the internal ADC of the TPC2884 can perform averaging of 4 or 16 samples. The relevant ADC measurement ranges are as follows:

- ADC_{AVDD_X}:0~37.5 V;
- ADC_{IOUT_X}:0~37.5 V;
- ADC_{VOUTX}:-12.5 V~12.5 V;
- ADC_{GNDX}:-312.5 mV~312.5 mV.

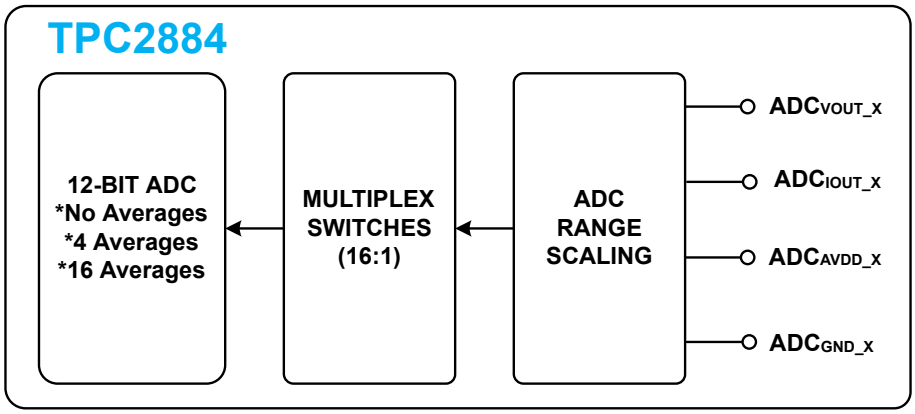


Figure 64. Internal ADC of TPC2884

The TPC2884 supports voltage reading for four ports per channel: AVDD, IOUT, VSENSEP, and VSENSEN. It also supports both continuous and single-shot readings. To read the data, the flag in the ADC control register needs to be checked. When the conversion is complete, the flag is set to 01, indicating that the data can be read correctly.

The transfer expression between the digital code and the AVDD pin voltage is given below:

$$AVDD = \frac{AVDDH\_VOL\_CODE}{65536} \times 37.5 \quad (7)$$

The transfer expression between the digital code and the V_{OUT} pin voltage is given below:

$$V_{out} = \frac{VOUT\_VOL\_CODE}{65536} \times 25 - 12.5 \quad (8)$$

The transfer expression between the digital code and the I_{OUT} pin voltage is given below:

$$V_{IOUT} = \frac{IOUT\_VOL\_CODE}{65536} \times 37.5 \quad (9)$$

The transfer expression between the digital code and the $-V_{SENSE}$ pin voltage is given below:

$$V_{GND} = \frac{GND\_CURRENT\_CODE}{65536} \times 0.625 - 0.3125 \quad (10)$$

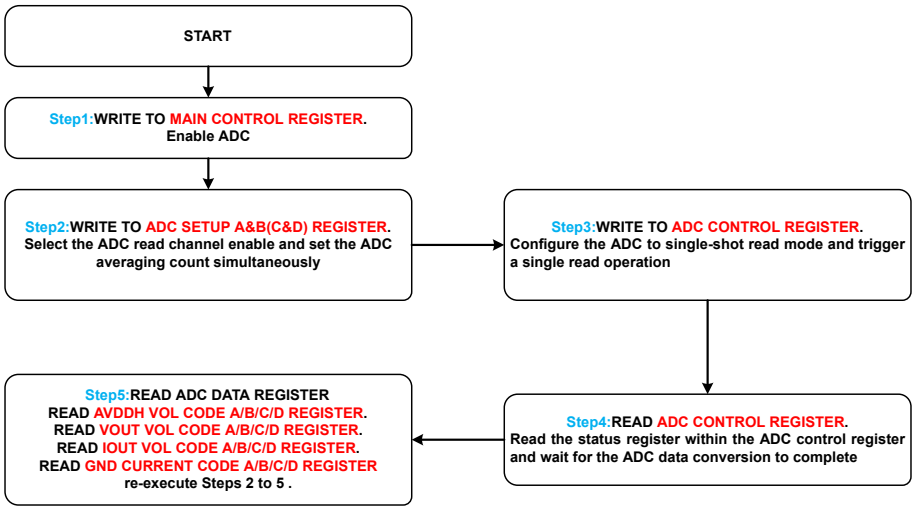


Figure 65. Flowchart of the internal ADC reading process of the TPC2884

Current Correction

When TPC2884 uses I_{OUT} for output, the output current may have errors due to port leakage. By configuring the registers 0x10 to 0x13, I_{CCOMP} can be compensated to the I_{OUT} port to avoid current output errors. The ICOMP_CODE[3:0] supports four types of resistive compensation methods, which can be configured according to different scenarios.

Serial Peripheral Interface (SPI)

The device is controlled over a versatile four-wire serial interface (SDIN, SDO, SCLK, and SYNC) that operates at clock rates of up to 20 MHz and is compatible with SPI, QSPI™, Microwire™, and digital signal processing (DSP) standards. The SPI communication command consists of a write address byte and a data word for a total of 24 bits (when CRC is disabled). The timing for the digital interface is shown in the Timing Requirements.

Stand-Alone Operation

The serial clock SCLK can be a continuous or a gated clock. When SYNC is high, the SCLK and SDIN signals are blocked and the SDO pin is in a HiZ state. Exactly 24 falling clock edges must be applied before SYNC is brought high. If SYNC is brought high before the 24th falling SCLK edge, then the data written are not transferred into the internal registers. If more than 24 falling SCLK edges are applied before SYNC is brought high, then the last 24 bits are used. The device internal registers are updated from the Shift Register on the rising edge of SYNC. In order for another serial transfer to take place, SYNC must be brought low again.

Write Operation

A typical write to program a channel of the TPC2884 consists of writing to the following registers in the sequence shown in Figure 66.

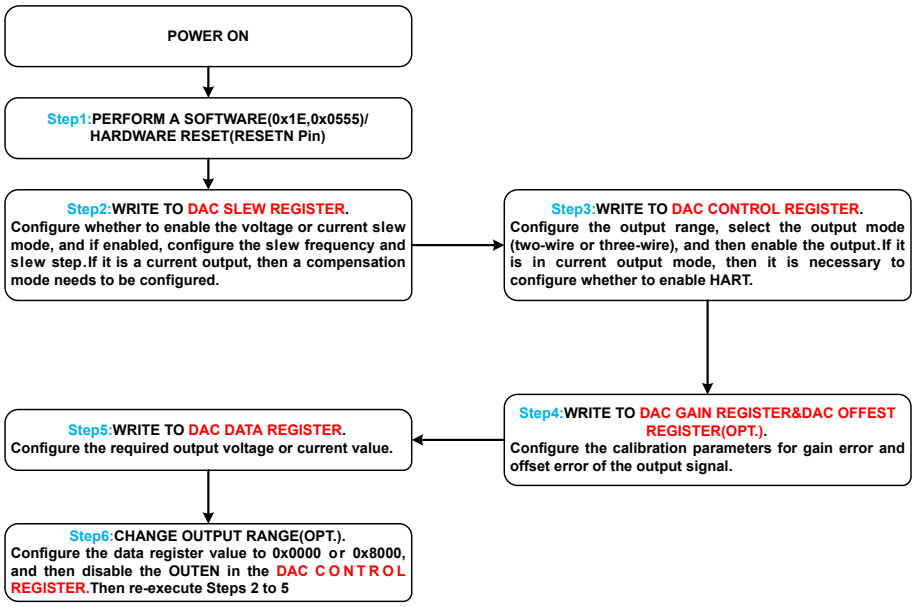


Figure 66. Typical Write to TPC2884

SPI Shift Register

The device features an input shift register that is 24 bits in width. Data is introduced into the register starting with the MSB, forming a 24-bit word. Data is clocked in on the falling edge of the SCLK signal. The input register has eight bits dedicated to address and sixteen bits for data.

Table 55. Serial Interface Access Cycle

BIT	FIELDD	DESCRIPTION
23	R/W	Identifies the communication as a read or write command to the addressed register. R/W = 0 sets a write operation. R/W = 1 sets a read operation.
22:16	A[6:0]	Register address. Specifies the register to be accessed during the read or write operation.
15:0	DI[15:0]	Data cycle bits. If a write command, the data cycle bits are the values to be written to the register with address A[6:0]. If a read command, the data cycle bits are don't care values.

Updating the DAC Outputs and LDAC Pin

Depending on the status of both SYNC and LDAC, and after data have been transferred into the DAC Data registers, the DAC outputs can be updated either in asynchronous mode or synchronous mode.

Read Operation

A read operation is accomplished when R/W is '1'. A no-operation (NOP) command should follow the read operation in order to clock out an addressed register. The read register value is output MSB first on SDO on successive falling edges of SCLK.

Table 56. SDO Output Access Cycle

BIT	FIELD	DESCRIPTION
23	R/W	Always be zero

BIT	FIELD	DESCRIPTION
22:16	A[6:0]	Echo address from previous access cycle
15:0	DO[15:0]	Readback data requested on the previous access cycle.

Asynchronous Mode

In this mode, the LDAC pin is set low before the rising edge of SYNC. This action places the TPC2884 into Asynchronous mode, and the LDAC signal is ignored. The DAC latches are updated immediately when SYNC goes high.

Synchronous Mode

To use this mode, set LDAC high before the rising edge of SYNC, and then take LDAC low after SYNC goes high. In this mode, when LDAC stays high, the DAC latch is not updated; therefore, the DAC output does not change. The DAC latch is updated by taking LDAC low any time after a certain delay from the rising edge of SYNC (see Figure 1). If this delay requirement is not satisfied, invalid data are loaded. Refer to the Timing Requirements for details.

Frame Error Checking

If the TPC2884 is used in a noisy environment, error checking can be used to check the integrity of SPI data communication between the device and the host processor. This feature can be enabled by setting the CRC_EN bit address 0x1D.

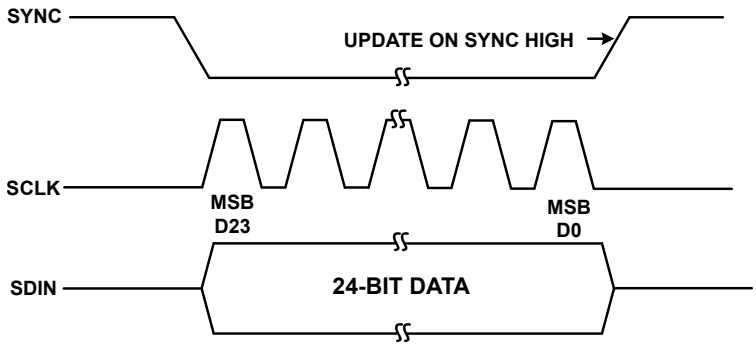
The frame error checking scheme is based on the CRC-8-ATM (HEC) polynomial $x^8 + x^2 + x + 1$ (that is, 100000111). When error checking is enabled, the SPI frame width is 32 bits, as shown in Table 57. The normal 24-bit SPI data are appended with an 8-bit CRC polynomial by the host processor before feeding it to the device. For a register readback, the CRC polynomial is output on the SDO pins by the device as part of the 32-bit frame.

Note that the user has to start with the default 24-bit frame and enable frame error checking through the CRC_EN bit and switch to the 32-bit frame. Alternatively, the user can use a 32-bit frame from the beginning and pad the 8 MSB bits as the device only uses the last 24 bits until the CRC_EN bit is set.

Table 57. SPI Frame with Frame Error Checking Enabled

BIT 31:BIT 8	BIT 7:BIT 0
Normal SPI frame data	8-bit CRC polynomial

The TPC2884 decodes the 32-bit input frame data and calculates the CRC remainder. If the frame contains no errors, the CRC remainder becomes zero. When the remainder is non-zero (indicating single- or multiple-bit errors in the input frame), the FAULTN pin is driven low and the CRC_ERROR_STATUS bit in the main status register (address 0x22) is set to '1'. Note that the FAULTN pin may also be pulled low under other conditions, as described in the FAULTN Pin. The CRC_ERROR_STATUS bit is cleared to '0' by a software/hardware reset, writing the correct SPI frame, disabling frame error checking, or powering down the device. A CRC error results in the corresponding SPI frame being blocked from write access



24-BIT DATA TRANSFER—NO ERROR CHECKING

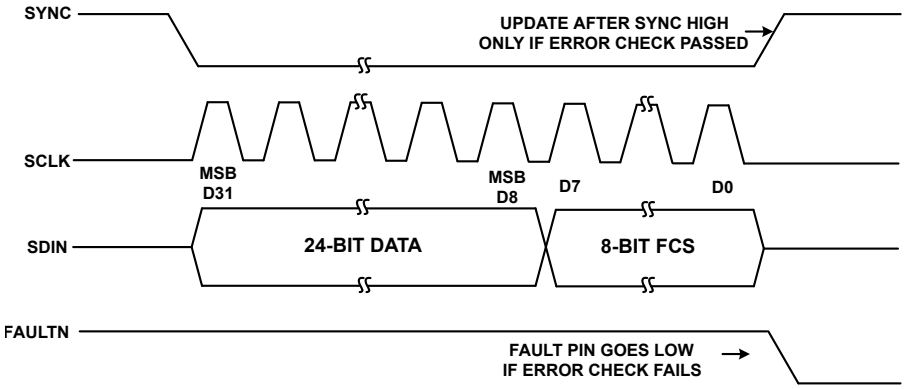


Figure 67. PEC Timing

Hardware RESETN Pin

When the RESETN pin is low, the device is in hardware reset. All the analog outputs (V_{OUT_A} to V_{OUT_D} and I_{OUT_A} to I_{OUT_D}), all the registers are set to the default reset values. In addition, the Gain and Zero registers are loaded with default values, communication is disabled, and the signals on SYNC and SDIN are ignored (note that SDO is in a high-impedance state). When the RESETN pin is high, the serial interface returns to normal operation and all the analog outputs (V_{OUT_A} to V_{OUT_D} and I_{OUT_A} to I_{OUT_D}) maintain the reset value until a new value is programmed.

Clear Function

The TPC2884 supports a software CLEAR function. To enable this function, the CLEAR_EN bit must be set to 1 (address, 0x14 to 0x17) to activate the CLEAR function for the channel. Then, configure the code values in the CLEAR_A_REG to CLEAR_D_REG registers. When the SOFT_CLEAR bit is set to 1 (address, 0x1D), the output changes to the code value stored in the CLEAR register. The previous code value before the CLEAR operation can be restored using the SOFT_LATCH function(address,0x1D).

Temperature Monitoring Function

The TPC2884 has a temperature sensor inside, which can monitor the current temperature of the chip, and there are two temperature levels for alarm and protection:

- If the chip temperature is greater than 135°C but less than 150°C (135℃ < TPC2884 < 150℃). The OTP135_STATUS in the MAIN_STATUS_REG(address,0x22) is e set to 1 and the FAULTN pin is pulled low.
- If the chip temperature is greater than 150°C (TPC2884 > 150℃),The OTP150_STATUS in the MAIN_STATUS_REG(address,0x22) is set to 1 and the FAULTN pin is pulled low. All outputs will be turned off.

DAC Data Calibration

Each channel of the TPC2884 contains a dedicated user calibration register set. This feature allows the user to trim the system gain and offset errors. Both the voltage output and the current output have common user calibration registers available.

The DAC calibration register set includes one gain calibration and one offset calibration register (16 bits for TPC2884) per channel (address 0x04~0x07 for gain calibration, address 0x08~0x0B for offest calibration). The range of gain adjustment is typically ±6.25% of full-scale with 1 LSB per step. The power-on value of the gain register is 0x0000 which is equivalent to a gain of 1. The offset code adjustment is typically ±32,768 LSBs with 1 LSB per step. The gain data and offest data are in complement format, with a range of -32768 to 32768 and a default value of 16'h0000. The gain and offset calibration is described as follows:

$$CODE = DATA \times \left(\frac{GAIN}{65536 \times 8} + 1\right) + \frac{OFFEST}{8} \quad (11)$$

Where:

- DATA is the digital code value before calibration.
- GAIN is the code value in the gain register.
- OFFEST is the code value in the offest register.

The tables for the two's complement of gain data and offset data are shown as follows:

Table 58. Table of Conversion Relationships between GAIN Register and Internal Calculation

GAIN REGISTER	GAIN
65535	-1
65534	-2
.....	.....
32769	-32767
32768	-32768
32767	32767
.....	.....
2	2
1	1
0	0

Table 59. Table of Conversion Relationships between OFFEST Register and Internal Calculation

OFFEST REGISTER	OFFEST
65535	-1
65534	-2
.....	.....
32769	-32767
32768	-32768
32767	32767
.....	.....
2	2
1	1
0	0

Therefore, the formula for calculating the value to be written into the Gain register is as follows:

$$GAIN\ CODE = \left(\frac{GAIN_{THEROY}}{GAIN_{TEST}} - 1\right) \times 8 \times 65536 + 65535 \quad (12)$$

Where:

- $GAIN_{THEROY}$ is the theoretical gain. For example, if the voltage output range is 10 V, then $GAIN_{THEROY}$ = 10/65536.
- $GAIN_{TEST}$ is the measured and fitted gain.

Therefore, the formula for calculating the value to be written into the Offest register is as follows:

$$\text{OFFEST CODE} = \frac{(\text{OFFEST}_{\text{THEROY}} - \text{OFFEST}_{\text{TEST}})}{\text{GAIN}_{\text{THEROY}}} \times 8 + 65535 \quad (13)$$

Where:

- $\text{OFFEST}_{\text{THEROY}}$ is the theoretical offest. For example, if the voltage output range is 10 V, then $\text{OFFEST}_{\text{THEROY}} = 0$.
- $\text{OFFEST}_{\text{TEST}}$ is the measured and fitted offest.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPC2884 is a quad-channel voltage and current output DAC meeting the requirements of industrial process control applications. The device also has complete diagnosis, including built-in fault detection and a 12-bit ADC for port voltage readback. This section describes the application details and application extensions of the TPC2884.

Typical Application

Voltage and Current Output Terminal Connection and Protection

The TPC2884 provides separate voltage and current outputs, which form a three-wire output with the reflow ground. These outputs may also be combined for two-wire operation. The mode is selected by the OUT-MODE bit (DAC_CTRL_X_REG), where 0 defaults to three-wire and 1 selects two-wire output.This bit governs the automatic configuration of voltage output pulldown and current output compensation; it must be set according to the external port connection. Voltage and current outputs are mutually exclusive. Switching between them requires disabling the active mode before enabling the reconfigured one.

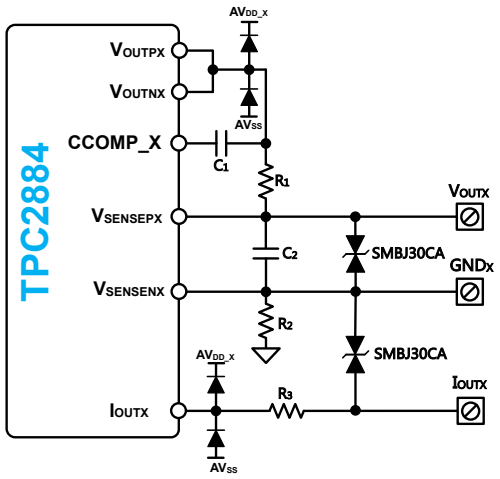


Figure 68. There-Wire & Two-Wire Output

Back-current protection for the internal open-drain outputs can be implemented using external series diodes. The configuration is mode-dependent:Three-Wire Mode: The voltage output path necessitates two series diodes for push-pull anti-backfill, while the current output requires only one.Two-Wire Mode: With the current output combined with the voltage output PMOS, two diodes provide consolidated anti-backfill protection.Selected diodes must have a reverse withstand voltage rating exceeding 65 V. This rating, under a ±15 V supply, secures an operational output range of ±50 V, safeguarding against misconnection and simplifying circuit protection. In two-wire mode, minimal diode reverse leakage current is critical to maintain current transmission accuracy.

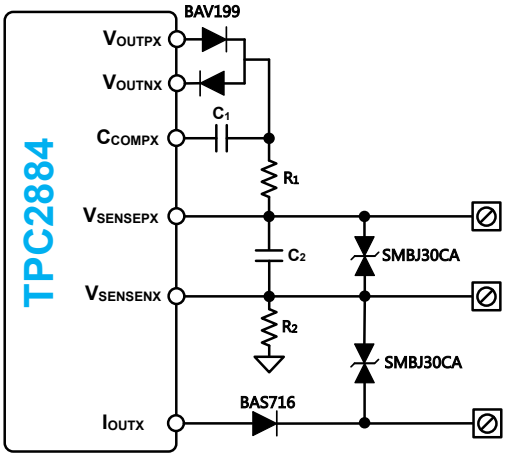


Figure 69. There-Wire Output with Anti-Backfill Diode

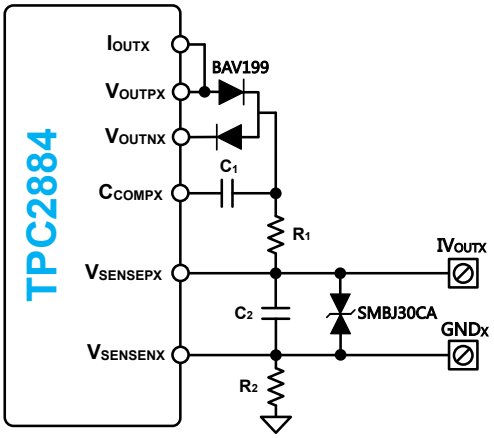


Figure 70. Two-Wire Output with Anti-Backfill Diode

The internal voltage output amplifier features an open-drain architecture with independent pull-up PMOS and pull-down NMOS, routed to dedicated external pins to extend the application voltage range. Output accuracy is maintained by a differential feedback system (V_{SENSEP}/V_{SENSEN}), which senses the actual board-level voltage, negating trace impedance effects. The V_{SENSEP} pin's ±50 V high-voltage tolerance simplifies protection circuitry and ensures accuracy. V_{SENSEN}, the output reference ground, can be low-impedance connected to AGND or imparted with impedance to improve noise immunity. When disabled, the high-impedance output is stabilized by an internal 13 kΩ pull-down resistor on V_{OUTN}. The associated switch is default-enabled at power-on, can be disabled by POC_MASK, and is also mode-dependent (auto-disconnecting in three-wire mode upon output enable, and persistently off in two-wire mode). Ultimate control is provided by the SW_X bit (DAC_CTRL_X_REG), which has highest priority.

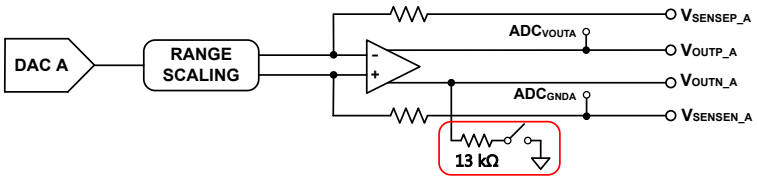


Figure 71. V_{OUT} Pull-Down Switch

The current output port is an open-drain output, which directly outputs accurate current without external feedback control. However, resistive leakage at the current output port will reduce the output current accuracy, and in three-wire mode, the ADC voltage readback of the current output port will produce a resistance to ground of 2 MΩ, and in two-wire mode, this impedance will be reduced to 500 kΩ. In this case, a built-in 4-bit impedance compensation compensates for the leakage

current caused by the output resistive load, and the ICOMP_CODE in the SLEW_X_REG is configured to compensate. The current compensation function generates a compensation current according to the voltage of the I_{OUT} pin. The input impedance of the compensation circuit is 2 MΩ, the total impedance of the IOUT pin is 1 MΩ, the resolution of the compensation is 2MΩ, and up to 15 resistors can be compensated in parallel of 2 MΩ. This compensation function can be controlled independently for each channel, setting the ICOMP_ALL in the MAIN_CTRL_REG to 1, and can also be automatically configured according to two-wire and three-wire configurations.

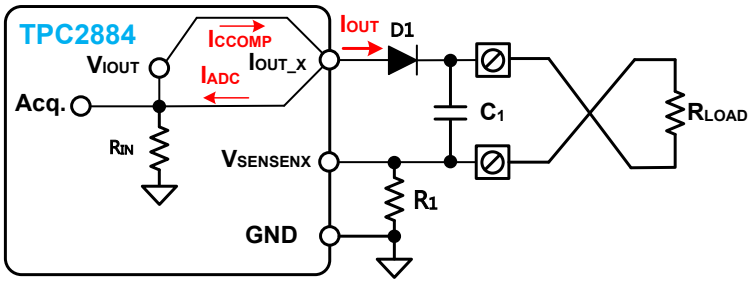


Figure 72. I_{OUT} Impedance Compensation

Enable initialization & Slew

The TPC2884's four-channel DAC has independent enable control and is disabled by default on power-up. Because a new range cannot be configured after the register is enabled, the range needs to be configured before it is enabled, and then the channel enters the initialization time. During the initialization time, the internal DAC output unipolar clamp is zero code, the bipolar output clamp is in the middle code, the DAC output is hardware enabled, and the signal link enters the established state. During initialization, the output is maintained near zero potential, and after the initialization time is over, the output switches to the voltage or current corresponding to the data register, and the DAC enters normal operation. The enable initialization time is adjustable by 2 bits, and the time is 64 μs, 128 μs, 256 μs, and 512 μs, and the default value is 64 μs. If you need to switch to a new range or turn off the output, you need to configure the enable disable in the register, and the disable initialization will also be triggered, and the time will be the same as the enable initialization. During the disabling initialization process, the output switches to zero potential, the voltage and current outputs enter the zero state, and when the set time is reached, the hardware enable of the DAC output is disabled. Both enable and disable initialization automatically set the output to zero potential or zero current, which is used to reduce the possible enable and disable glitchs of the output. In order to obtain smoother output, it is recommended to set the data registers to safe values in advance before enabling and disabling initialization.

The TPC2884 output signal is established in the order of tens of microseconds, and the built-in slew control circuit reduces the slope and overshoot of the output, and the slew control has an effect on both voltage and current output. This function can be turned on before and after the channel is enabled, and if it is turned on before the channel is enabled, the output remains near zero potential during the initialization time, and after initialization, the output climbs towards the target value set by the data register. During the output climb, the parameters and target data of the slew can be updated, and the new configuration will be updated to the output during the subsequent climb. It should be noted that in order to ensure the timeliness of channel disabling, there is no slew function in the process of channel disabling, and if you need a smooth transition of output, it is recommended to adjust the output to a safe value in advance before disabling.

Data Update & Clear

There are three ways to update the output data of TPC2884, which are divided into synchronous update and asynchronous update. Synchronous updates act on all channels and are implemented either by the falling edge of the LDAC pin or by SOFT_LATCH 1 in the MAIN_CTRL_REG, which updates the latest data in the data registers directly to the output port. Asynchronous update only acts on the currently updated data register, needs to keep the LDAC pin low. When the single-channel data is written, the SYNC pin is pulled up to automatically update the data to the corresponding channel output. When the full-channel data register is written, the SYNC is pulled up, and the data is automatically updated to all channels. In the channel-enabled state, the output data update is highly flexible, but it is invalid during the channel disable, enable and disable initialization time.

TPC2884 has an output clear function, which requires the output to be kept enabled and the CLEAR_EN function in the DAC_CTRL_X_REG turned on. When the SOFT_CLEAR in the MAIN_CTRL_REG is set to 1, the channel that meets the condition switches the output to the value set in the CLEAR_REG. If you need to revert the output to the values in the DATA_REG, you can update the output to the old data in the DATA_REG by SOFT_LATCH, or you can write to the DATA_REG again and update the output. It is important to note that LDAC does not have the ability to recover after clear is active.

On-Chip Fault

TPC2884 has complete on-chip diagnostic functions, including overcurrent and direction of voltage output, loop disconnection of current output, negative voltage of current output, power-up of AVDD, over-temperature protection, ADC conversion completion, DAC slew, SPI timeout, and CRC calibration. The above diagnostic results can be found in MAIN_STATUS_REG and OUT_STATUS_REG. In order to catch short-term error events, the built-in error storage register FAULT_STORE_REG, the error message can be maintained, and the error report of the corresponding bit can be cleared by using FAULT_CLEAR_REG. The diagnosis of register queries is often not timely, and the error output using the FAULTN pin has a better indication effect, and the error output has an independent enable control FAULT_PD in the MAIN_CTRL_REG. The FAULT_STORE in this register can select the source of the error message, the real-time data in the X_STATUS_REG or the hold data in the FAULT_STORE_REG. The error information on the FALITN pin can be selectively masked by the FALUT_MASK_REG, and the unmasked error message can be summarized on the FAULTN pin through logic AND. The FALUTN pin is an open-drain output, and an external pull-up resistor is required, which is recommended to be 10 kΩ. When an error occurs in the system, you need to immediately query the X_STATUS_REG and FAULT_STORE_REG to determine the error type, so as to facilitate the analysis of the cause of the error in the later stage.

Reset function

The MAIN_STATUS_REG contains a very important indicator RESET_NOTE_STATUS that records software and hardware reset events that have occurred on the chip, protecting the operation of the chip. After the chip is powered up, it automatically performs a reset that requires the user to write 0x0358 clear the indicator bit in the SOFTWARE_REG. The input of the hardware reset RESET pin has a 50us filtering time to improve the pin interference immunity. Software resets require 0x0555 to be written to the SOFTWARE_REG, and a reset is performed immediately.

I_{OUT} Driving Inductive Loads

When driving inductive or poorly defined loads, connect a 0.01 μF capacitor between I_{OUT} and AGND. This ensures stability with loads above 50 mH. There is no maximum capacitance limit. The capacitive component of the load may cause slower settling. The digital slew rate control feature may also prove useful in this situation.

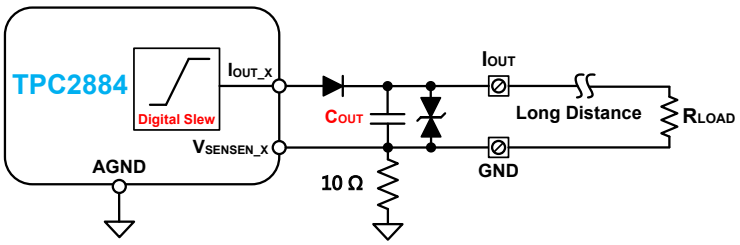


Figure 73. I_{OUT} Establishment with Large Inductance Load

V_{OUT} Driving Capacitive Loads

The voltage output has strong capacitive drive capability, and when the load capacitance is less than 10 nF, there is no need to use a compensation capacitor to connect the CCOMP and V_{OUT} pins. When the output load capacitance is greater than 10 nF, it is recommended to connect the compensation capacitor in the CCOMP and V_{OUT} pins, the compensation capacitance value is recommended to be 47 pF, and add a 30 Ω isolation resistor for better stability. This compensation configuration can be applied to any load capacitor. When the load capacitance is less than 200 nF, the voltage output slew rate is limited to the closed-loop bandwidth of the amplifier, and the output waveform transition is smooth, and the overshoot is small. When the

load capacitance is greater than 200 nF, the slew rate limit of the output voltage mainly comes from the current limit of the voltage output, which is a nonlinear large signal behavior, and the transition to the linear operating area may have a certain overshoot.

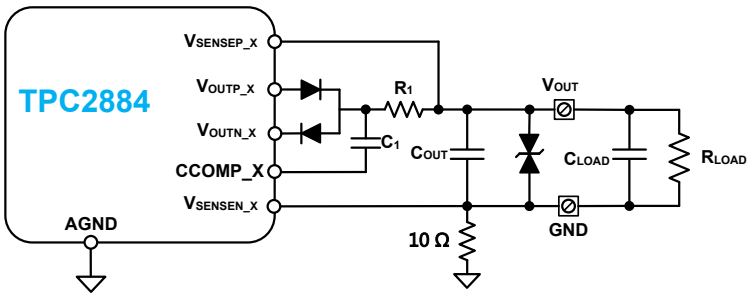


Figure 74. V_{OUT} Establishment with Large Capacitance Load

Output Applications based on Dynamic Power Control

In order to solve the problem of power consumption and heat generation of the TPC884 when the current is output, a DC-DC BUCK is used to feed back to the VFB terminal through the voltage on the R_{LOAD} at the output terminal, and adjust the output voltage of the BUCK, which is connected to the AV_{DD} of the TPC2884. The schematic diagram is shown in the following figure.

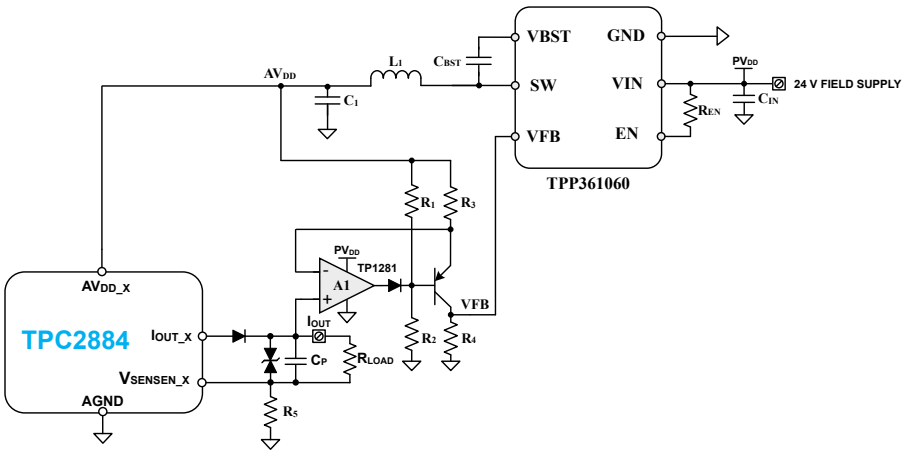


Figure 75. Block diagram of the dynamic power control scheme

The expression for the minimum output voltage is shown below:

$$AV_{DD\_MIN} = \left(\frac{R_3}{R_4}V_{FB} + V_{EB}\right)\left(1 + \frac{R_2}{R_1}\right) + V_F \quad (14)$$

Here, V_{FB} represents the feedback voltage of the BUCK converter, and in this case, V_{FB} = 0.6 V;V_F represents the forward voltage drop of the diode, which is typically 0.7 V;V_{EB} represents the voltage difference between the emitter (E) and base (B) of a PNP transistor, which is typically 0.7 V.

When the op-amp A1 is operating in a closed-loop gain configuration, the output voltage of the BUCK converter can be expressed as:

$$AV_{DD} \approx I_{OUT} \times R_{LOAD} + \frac{R_3}{R_4} \times V_{FB} \quad (15)$$

Here, I_{OUT} represents the output current of the current port of TPC2884, and R_{LOAD} represents the load resistance at the port. When the output is open-circuited, AV_{DD} becomes the maximum output voltage of the BUCK converter.

When the voltage on the R_{LOAD} is less than 1.4 V, the op amp A1 is in the open-loop working state, at this time, the negative input voltage of the op amp is about 1.4 V, when the voltage on the R_{LOAD} is greater than 1.4 V, the op amp is in the closed-loop working state, the forward input voltage of the op amp is equal to the reverse input voltage, and the op amp needs to ensure that its I_B current changes little in the open-loop and closed-loop states.

Table 60. Resistor Values in Dynamic Power Control Scheme

R_1	R_2	R_3	R_4
62 kΩ	11 kΩ	68 kΩ	8.2 kΩ
AV_{DD-MIN}	7.3826 V		

Assuming R_{LOAD} = 250 Ω and an output current of 24 mA, without the use of dynamic power control, the voltage on the TPC2884 is 18 V, the current is 24 mA, and the power consumption is 432 mW. If dynamic power control is used, the voltage on the TPC2884 is 4.9756 V, the current is 24 mA, and the power consumption is 0.1194 mW. If the TPC2884 needs to communicate with HART, a low-pass filter can be added to the front end of the op amp A1 to filter out the effects of the HART signal.

UIO Compatible

The high withstand voltage of the anti-backfill two-wire output enables the chip to be highly compatible and can be combined with analog voltage acquisition and logic ports in industrial applications to implement software configuration IO (UIO). The output current compensation function also eliminates leakage current introduced by the expansion port, simplifying the circuit design of the UIO. The four-wire feedback of the voltage output and the high withstand voltage of the VSENSEP port make it easier to obtain voltage accuracy.

Due to its high-voltage tolerance at the ports, the TPC2884 can easily implement UIO applications. We use the TPAFE51736S8 (16-Bit, 500-kSPS, 8-Channel, Bipolar Input ADC) in combination with the TPC2884 to form an AIO application. The corresponding block diagram is shown as follows.

UIO-Voltage Output

The application of the voltage output port is shown as follows: The TPAFE51736S8 acquisition port voltage is used to monitor the magnitude of the output voltage

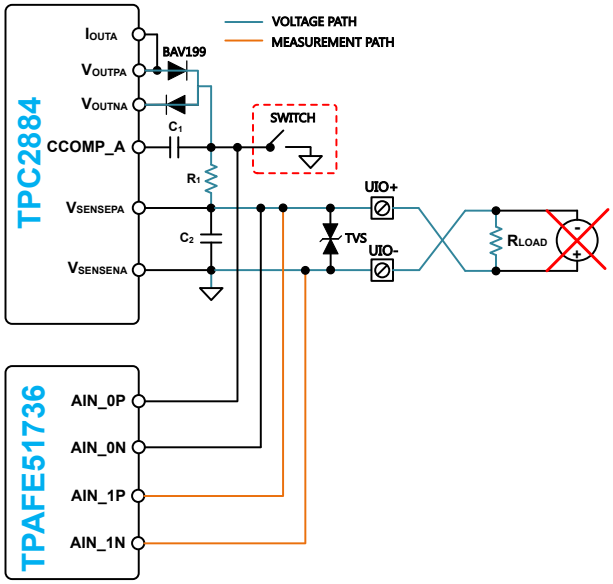


Figure 76. Voltage Output Mode Configuration

UIO-Current Output

The application of the current output port is as follows: The TPAFE51736S8 acquires the voltage across resistor R_1 to monitor the output current. Meanwhile, the TPC2884 has an internal current compensation feature that can eliminate the leakage current of the TPAFE51736S8 and the internal ADC.

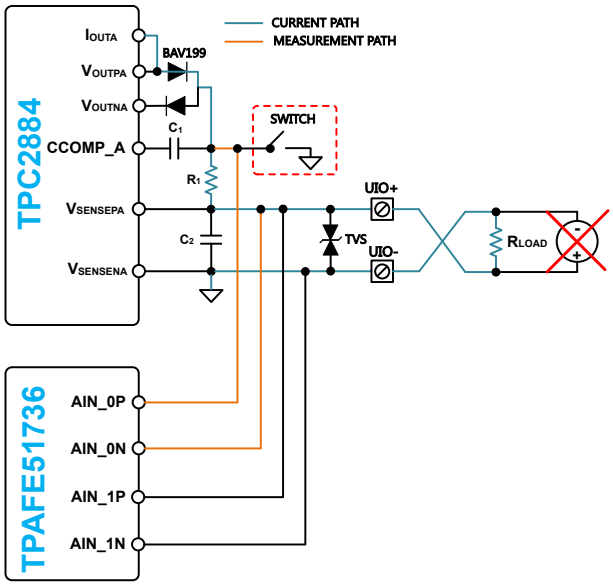


Figure 77. Current Output Mode Configuration

UIO-Voltage Input

Application of the voltage input port: The TPAFE51736S8 acquires the port voltage to directly measure the magnitude and waveform of the input voltage. All channels of the TPC2884 are in a high impedance state.

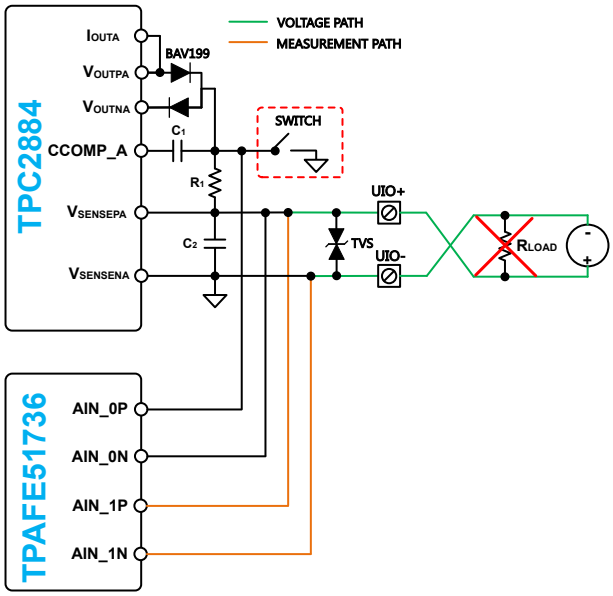


Figure 78. Voltage Input Mode Configuration

UIO-Current Input

Application of the current input port: The TPAFE51736S8 acquires the voltage across resistor R_1 to measure the input current. At this time, the SWITCH is closed, and all channels of the TPC2884 are in high impedance state.

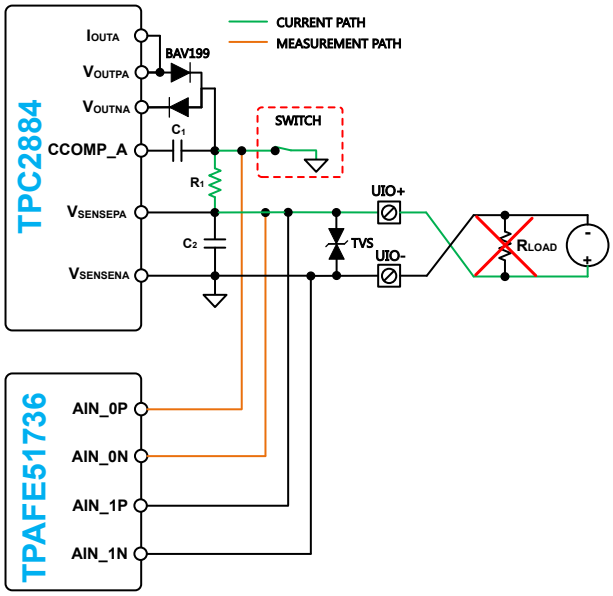


Figure 79. Current Input Mode Configuration

UIO-Current Input, Loop Powered

LOOP-POWER Mode: In this mode, the TPC2884 can be used as a power supply. The voltage output is AV_{DD}, with a maximum current output of 25 mA. By reading the voltage across R_1, the loop input current can be calculated.

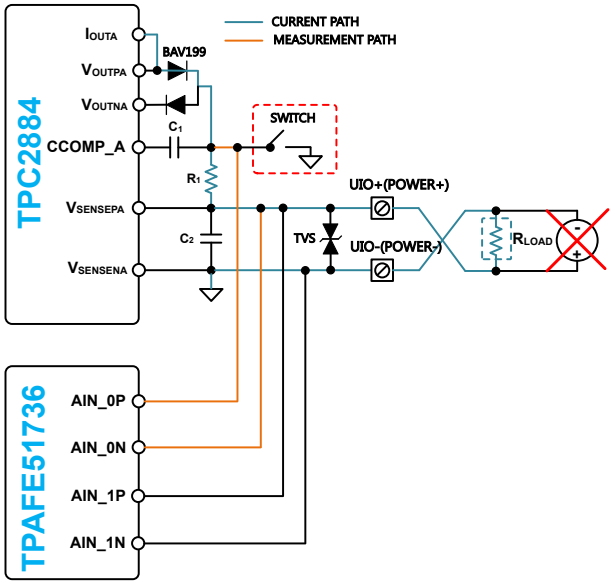


Figure 80. Current Input, Loop Powered Mode Configuration

On-chip ADC Feature

TPC2884 integrates a 12-bit ADC that can quantify the voltage of the internal AVDD port, I_{OUT} port, V_{OUT} and VSENPEN port, providing customers with software diagnostics and improving the functional safety of the product. The bipolar measurement

ranges of V_{OUT} and V_{SENSEN} are ± 12.5 V and ±312.5 mV, respectively. The AV_{DD} port and I_{OUT} port are unipolar measurement ranges, corresponding to the range of 0-37.5V, and the reference ground of all channels of the ADC is AGND. The ADC measures the VOUT port, and the signal input port is V_{SENSEP}, and the quantization range can cover the sum of the ±12 V output voltage in overrange mode and the V_{SENSEN} port voltage. When the voltage output is disabled, in order to avoid floating voltage on the port, the internal sampling circuit short-circuits to AGND and loses the voltage measurement function. V_{SENSEN} is used to measure the return current of voltage and current output, 10 Ω resistor is recommended, if there is no measurement need, V_{SENSEN} can be connected to AGND, the input impedance of this port is 50 kΩ, the measurement front end has inverting characteristics, and the digital domain negates the data again, so that the register corresponding to the measurement result is 0xFFF0 in the reset state. AV_{DD} and I_{OUT} port voltage measurement is mainly used for current output to handle complex operating conditions caused by high-voltage changing power supplies.

The ADC has a single and average function to reduce output noise up to 16 times, and each channel can be independently configured. The quantization of the ADC is sequential quantization. After a single trigger, the open channels of the 16 channels are quantified in order, and after the quantization is completed, the ADC_READY_STATUS will be set to 1 and held until the next trigger, ADC_READY_STATUS indicates the end of the ADC data update. In continuous mode, after each triggered quantization is completed, ADC_READY_STATUS set to 1 to maintain a certain waiting time, and then automatically triggers a new quantization cycle. The wait time is controlled by the configuration of the ADC_DRDY in the ADC_CTRL_REG, and this time varies between 20 μs and 200 μs. In the single trigger and continuous trigger modes of the ADC, the quantization results in the registers are maintained and will only be refreshed when new quantization results appear, and the quantization results of the ADC can be read by the customer at any time. It is recommended to read the data after setting 1 in the ADC_READY_STATUS to ensure that the read data is the latest quantitative result.

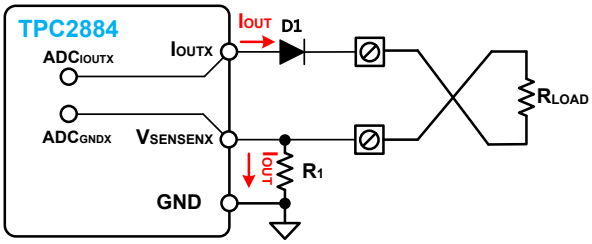


Figure 81. ADC Readback in Current Mode

The formula for monitoring the voltage at the current port and calculating the output current is shown as follows:

$$ADC_{IOUTX} = V_F(D_1) + I_{OUT} \times R_{LOAD} \quad (16)$$

$$I_{OUT} = \frac{ADC_{GNDX}}{R_1} \quad (16)$$

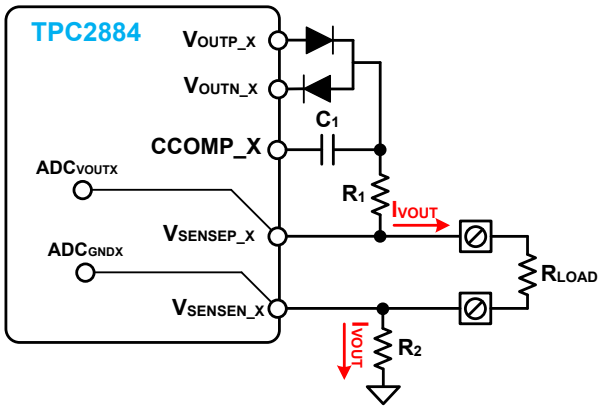


Figure 82. ADC Readback in Voltage Mode

The formula for monitoring the voltage at the voltage port and calculating the output current is shown as follows:

$$ADC_{VOUTX} = V_{OUT} \quad (17)$$

$$I_{VOUT} = \frac{ADC_{GNDX}}{R_2} \quad (17)$$

Typical Application: Quad Channel, EMC and EMI Protected Analog Output Module

Analog I/O modules are used by programmable logic controllers (PLCs) to interface with sensors, actuators, and other field instruments. These modules must meet stringent electrical specifications to ensure both accuracy and robust protection.

Typical output types include current outputs based on the 4 mA to 20 mA range (and its derivatives), as well as voltage outputs such as 0 V to 5 V, 0 V to 10 V, ±5 V, and ±10 V. A common error budget allows for a total unadjusted error (TUE) of 0.1% of the full-scale range (%FSR) at room temperature. For designs requiring higher accuracy over temperature, calibration is often implemented.

The PLC backplane usually supplies an analog power rail in the range of 12 V to 36 V, from which most analog supply voltages are derived. Analog output modules are often multi-channel designs, offering either channel-to-channel isolation or group isolation, where several channels share a common ground. As the number of channels increases, maintaining a small form factor becomes important—driving the need for high integration and low power dissipation to manage thermal load inside the PLC enclosure.

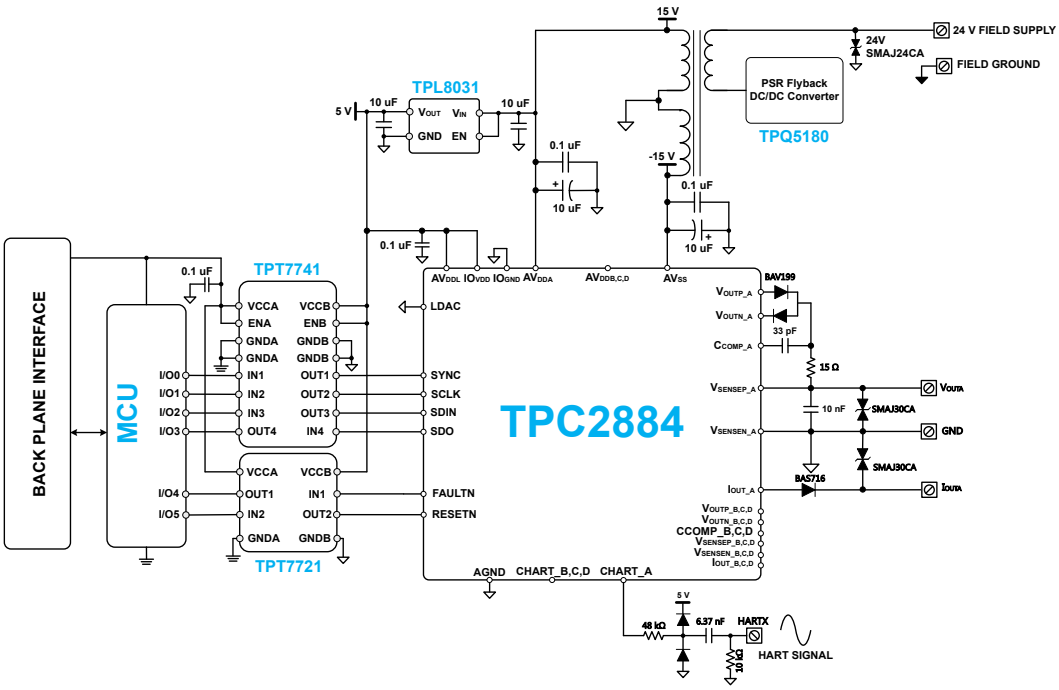


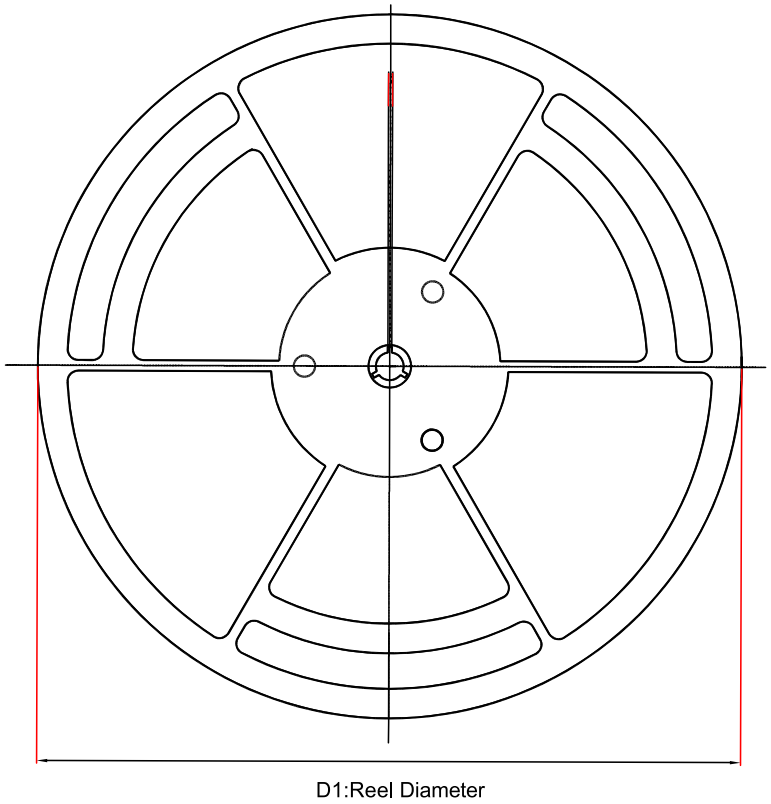
Figure 83. TPC2884 in Quad-Channel PLC AO Module

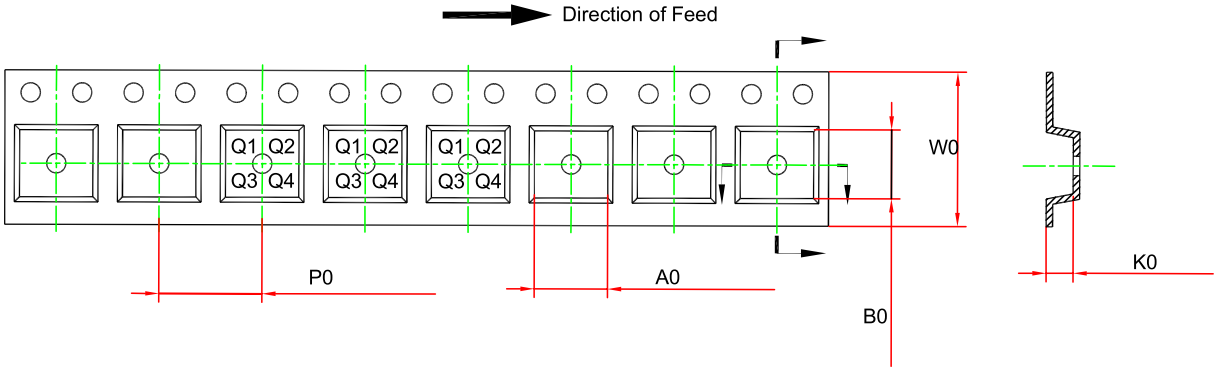
Layout

Layout Guideline

- In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance.
- Design the printed circuit board (PCB) on which the TPC2884 is mounted so that the analog and digital sections are separated and confined to certain areas of the board. If the TPC2884 is in a system where multiple devices require an analog ground-to-digital ground connection, make the connection at one point only. Establish the star ground point as close as possible to the device.
- The TPC2884 should have ample supply bypassing of 10 μF in parallel with 0.1 μF on each supply located as close to the package as possible, ideally right up against the device. The 10 μF capacitors are the tantalum bead type. The 0.1 μF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.
- The power supply lines of the TPC2884 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.
- A IOGND line routed between the SDIN and SCLK lines helps reduce crosstalk between them (this is not required on a multilayer board that has a separate ground plane, but separating the lines helps).
- It is essential to minimize noise on the REFIN line because it couples through to the DAC output, a 100nF capacitance to AGND is recommended.
- Avoid crossover of digital and analog signals. Traces on opposite sides of the PCB should run at right angles to each other. This reduces the effects of feed through the board.
- A microstrip technique is by far the best but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane, and signal traces are placed on the solder side.

Tape and Reel Information



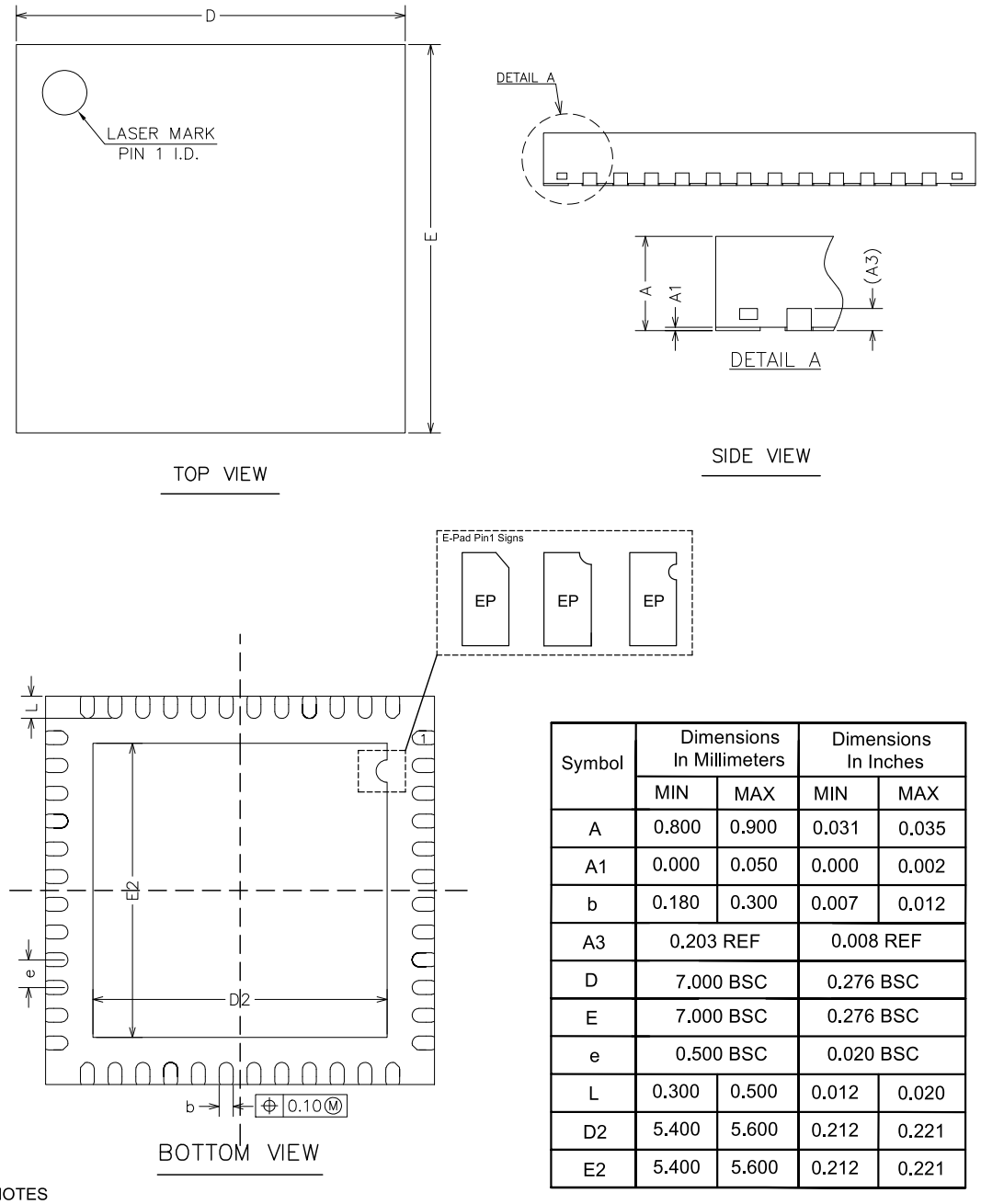


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPC2884-FE6R	QFN7X7-48	330	20.8	7.3	7.3	1.2	12	16	Q1

Package Outline Dimensions

QFN7X7-48-F

Package Outline Dimensions FE5(QFN7X7-48-F)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.031	0.035
A1	0.000	0.050	0.000	0.002
b	0.180	0.300	0.007	0.012
A3	0.203 REF		0.008 REF	
D	7.000 BSC		0.276 BSC	
E	7.000 BSC		0.276 BSC	
e	0.500 BSC		0.020 BSC	
L	0.300	0.500	0.012	0.020
D2	5.400	5.600	0.212	0.221
E2	5.400	5.600	0.212	0.221

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPC2884-FE6R	−40 to 125°C	QFN7X7-48	2884	3	Tape and Reel,3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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