16-Bit, Serial Input, Loop-Powered, 4 mA to 20 mA DAC

Features

- 16-bit resolution and monotonicity
- Pin selectable NAMUR-compliant ranges
  - 4 mA to 20 mA
  - 3.8 mA to 21 mA
  - 3.2 mA to 24 mA
- NAMUR-compliant alarm currents
  - Downscale alarm current = 3.2 mA
  - Upscale alarm current = 22.8 mA/24 mA
- Total unadjusted error (TUE): 0.133% maximum
- INL error: 0.004% FSR maximum
- Output TC: 3 ppm/°C typical
- Quiescent current: 200 µA maximum
- Flexible SPI-compatible serial digital interface with Schmitt triggered inputs
- On-chip fault alerts via FAULT pin or alarm current Automatic readback of fault register on each write cycle
- Slew rate control function
- Gain and offset adjust registers
- On-chip reference TC: 4 ppm/°C Typ.
- Selectable regulated voltage output
- Loop voltage range: 5.5 V to 60 V
- Temperature range: −40°C to +125°C
- TSSOP packages

Applications

- Industrial process control
- 4 mA to 20 mA loop-powered transmitters
- Smart transmitters
- HART network connectivity

Description

The TPC2221 is an all-in-one, loop-powered digital-to-analog converter (DAC) that is tailored to the requirements of intelligent sensor manufacturers within the industrial automation sector.This DAC offers a highly accurate, fully integrated, and cost-effective solution in a compact TSSOP package.

It features a built-in voltage regulator that not only powers the TPC2221 but also other components within the sensor, providing a stable output voltage between 1.8 V and 12 V.The TPC2221 also incorporates 1.915 V and 2.5 V reference voltages, which means there's no need for additional discrete regulators or voltage references.

It is fully compatible with the standard HART® FSK protocol used in remote sensor communication without any loss in performance.The device's high-speed serial interface operates at 30 MHz and supports easy integration with popular microprocessors and microcontrollers through a SPI-compatible, 3-wire interface.

The TPC2221 ensures monotonicity up to 16 bits and delivers exceptional performance with 0.0015% integral nonlinearity, 0.0012% offset error, and 0.0006% gain error under typical operating conditions.

Lastly, the TPC2221 is offered in a 28-lead TSSOP package and is designed to operate over an extended industrial temperature range from −40°C to +125°C.

Typical Application Circuit

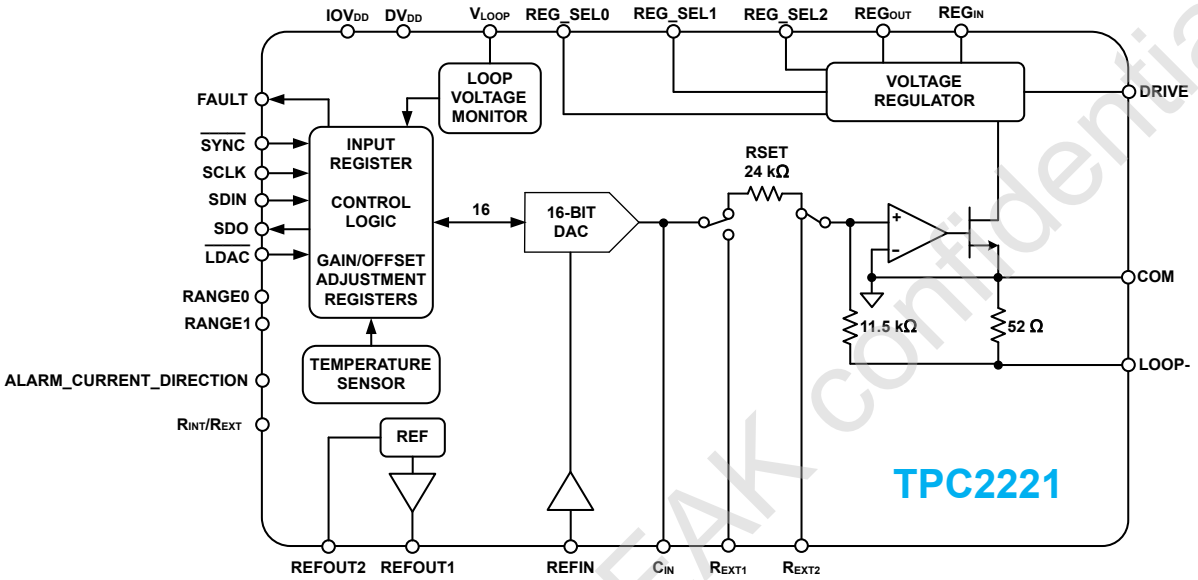


Figure 1. FUNCTIONAL BLOCK DIAGRAM

Table of Contents

Product Family Table

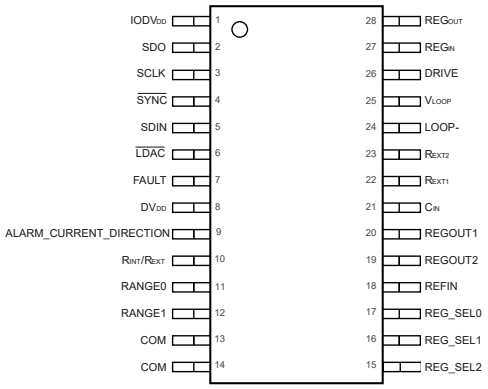
Order Number	Resolution	Output	Package
TPC2221-TSFR	16	Current	TSSOP28

Revision History

Date	Revision	Notes
2025-3-1	Rev.Pre.0	Preliminary Version.

Pin Configuration and Functions

TSSOP28 Package
Top View



QFN Package (In development)
Top View

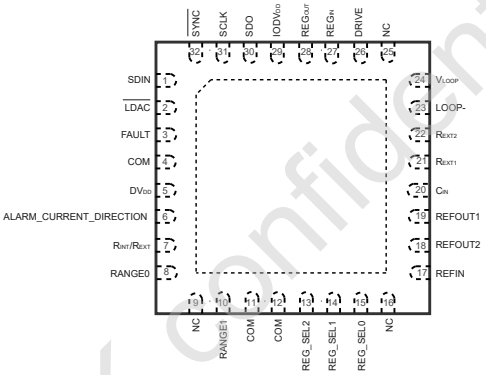


Table 1. Pin Function Descriptions

Pin No.		Mnemonic	Description
TSSOP	QFN		
1	29	$IODV_{DD}$	Digital Interface Supply Pin. Digital thresholds are referenced to the voltage applied to this pin.
2	30	SDO	Serial Data Output. Used to clock data from the input shift register. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK.
3	31	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of SCLK.
4	32	$\overline{SYNC}$	Frame Synchronization Input, Active Low. This is the frame synchronization signal for the serial interface. When $\overline{SYNC}$ is low, data is transferred on the falling edge of SCLK. The input shift register data is latched on the rising edge of $\overline{SYNC}$.
5	1	SDIN	Serial Data Input. Data must be valid on the falling edge of SCLK.
6	2	$\overline{LDAC}$	Load DAC Input, Active Low. This pin is used to update the DAC register and, consequently, the output current. If $\overline{LDAC}$ is tied permanently low, the DAC register is updated on the rising edge of $\overline{SYNC}$. The $\overline{LDAC}$ pin should not be left unconnected.
7	3	FAULT	Fault Alert Output Pin, Active High. This pin is asserted high when a fault is detected.
8	5	DV_{DD}	3.3 V Digital Power Supply Output. This pin should be decoupled to COM with 100 nF and 4.7 µF capacitors
9	6	ALARM_CURRENT_DIRECTION	Alarm Current Direction Select. This pin is used to select whether the alarm current is upscale current (22.8 mA/24 mA) or downscale (3.2 mA). Connecting this pin to DV_{DD} selects an upscale alarm current

Pin No.		Mnemonic	Description
TSSOP	QFN		
			(22.8 mA/24 mA); connecting this pin to COM selects a downscale alarm current (3.2 mA).
10	7	R_{INT}/R_{EXT}	Current Setting Resistor Select. When this pin is connected to DV_{DD}, the internal current setting resistor is selected. When this pin is connected to COM, the external current setting resistor is selected. An external resistor can be connected between the R_{EXT1} and R_{EXT2} pins.
11, 12	8, 10	RANGE0 RANGE1	Digital Input Pins. These two pins select the loop current range.
13, 14	4, 11, 12	COM	Ground Reference Pin for the device. It is recommended that a 4.7 V Zener diode be placed between the LOOP- and COM pins.
15, 16, 17	13, 14, 15	REG_SEL2, REG_SEL1, REG_SEL0	These three pins together select the regulator output (REG_{OUT}) voltage.
18	17	REFIN	Reference Voltage Input. V_{REFIN} = 2.5 V for specified performance.
19	18	REFOUT2	Internal Reference Voltage Output 2. It is recommended to connect a 100 nF capacitor from this pin to COM.
20	19	REFOUT1	Internal Reference Voltage Output 1 (2.5V). It is recommended to connect a 100 nF capacitor from this pin to COM.
21	20	C_{IN}	External Capacitor Connection and HART FSK Input. An external capacitor connected from CIN to COM implements an output slew rate control function. HART FSK signaling can also be coupled through a capacitor to this pin.
22, 23	21, 22	R_{EXT1}, R_{EXT2}	Connection for External Current Setting Resistor. A precision 24 kΩ resistor can be connected between these pins for improved performance.
24	23	LOOP-	Loop Current Return Pin. The COM and LOOP- pins can be used to sense the loop current across the internal 52 Ω resistor. Note that the voltage measured at LOOP- is be negative with respect to COM.
25	23	V_{LOOP}	Voltage Input Pin. Voltage input range is 0 V to 2.5 V. The voltage applied to this pin is digitized to eight bits, which are available in the fault register. This pin can be used for general-purpose voltage monitoring, but it is intended for monitoring of the loop supply voltage. Connecting the loop voltage to this pin via a 20:1 resistor divider allows the device to monitor and feedback the loop voltage. The device also generates an alert if the loop voltage is close to the minimum operating value.
26	26	DRIVE	Gate Connection for External Depletion Mode MOSFET.
27	27	REG_{IN}	Voltage Regulator Input. The loop voltage can be connected directly to this pin. Or to reduce on- chip power dissipation, an external pass transistor can be connected at this pin to stand off the loop voltage.

Pin No.		Mnemonic	Description
TSSOP	QFN		
28	28	REG_{OUT}	Voltage Regulator Output. Pin selectable values are from 1.8 V to 12 V via the REG_SEL0, REG_SEL1, and REG_SEL2 pins. If REGOUT is driving a microconverter supply, this pin should be decoupled to COM with a >1 µF capacitor.
N/A	9, 16, 25	NC	No Connect. Do not connect to this pin.
		EPAD	Exposed Paddle. The exposed paddle should be connected to the same potential as the COM pin and to a copper plane for optimum thermal performance.

Specifications

Absolute Maximum Ratings (1)

Parameter	Rating
REG_{IN} to COM	-0.3 V to +70 V
REG_{OUT} to COM	-0.3 V to +20 V
Digital Inputs to COM, RANGE0, RANGE1, R_{INT}/R_{EXT}, ALARM_CURRENT_DIRECTION, REG_SEL0, REG_SEL1, REG_SEL2	-0.3 V to DV_{DD}+0.3 V or +7 V (whichever is less)
Digital Inputs to COM, SCLK, SDIN, $\overline{SYNC}$, $\overline{LDAC}$	-0.3 V to $IODV_{DD}$+0.3 V or +7 V (whichever is less)
Digital Outputs to COM, SDO, FAULT	-0.3 V to $IODV_{DD}$+0.3 V or +7 V (whichever is less)
REFIN to COM	-0.3 V to +7 V
REFOUT1, REFOUT2	-0.3 V to +4.7 V
V_{LOOP} to COM	-0.3 V to +70 V
LOOP - to COM	-5 V to +0.3 V
DV_{DD} to COM	-0.3 V to +7 V
$IODV_{DD}$ to COM	-0.3 V to +7 V
R_{EXT1}, C_{IN} to COM	-0.3 V to +4.3 V
R_{EXT2} to COM	-0.3 V to +0.3 V
DRIVE to COM	-0.3 V to +11 V
Operating Temperature Range (T_A)	-40℃ to +125℃
Storage Temperature Range	-65°C to +150°C
Power Dissipation	$(T_{J\,MAX} - T_A)/\theta_{JA}$
Lead Temperature, Soldering (10 sec)	JEDEC Industry Standard J-STD-020

(1)Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter	MIN	NOM	MAX	UNIT
(REG_{IN} - LOOP-)	5.5		60	V

Parameter	MIN	NOM	MAX	UNIT
(LOOP- - COM)	-5		0	V
$IODV_{DD}$ - COM	1.7		5.5	V
DV_{DD} - COM		3.3		V
Specified performance temperature	–40		125	°C

Thermal Information

THERMAL METRIC		QFN (In Development)	TSSOP	UNIT
		32 PINS	28 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	40	32	°C/W
θ_{JC}	Junction-to-case (top) thermal resistance	7	9	°C/W

Electrical Characteristics

Loop voltage = 24 V; REFIN = 2.5 V external; R_L = 250 Ω; external NMOS connected; all loop current ranges; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

PARAMETER[1]	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ACCURACY, INTERNAL R_{SET}					
Resolution		16			Bits
Total Unadjusted Error(TUE)	T_A =-40°C to +125°C,	-0.18		0.18	%FSR
	T_A=25 ℃	-0.163		0.163	%FSR
TUE Long-Term Stability	Drift after 1000 hours at T_A = 125°C		TBD		ppm FSR/℃
Relative Accuracy (INL)	T_A =-40°C to +125°C,	-0.012		0.012	%FSR
Differential Nonlinearity (DNL)	T_A =-40°C to +125°C	−1		1	LSB
Offset Error	T_A =-40°C to +125°C	-0.056		0.056	%FSR
	T_A =25°C	-0.01		0.01	%FSR
Offset Error TC[3]			TBD		ppm FSR/℃
Gain Error	T_A =-40°C to +125°C	−0.107		0.107	%FSR
	T_A = 25°C	-0.09		0.09	%FSR
Gain Error TC[3]			TBD		ppm FSR/℃
Full-Scale Error	T_A =-40°C to +125°C	-0.126		0.126	%FSR
	T_A = 25°C	-0.1		0.1	%FSR
Full-Scale Error TC[3]			TBD		ppm FSR/℃
Downscale Alarm Current		3.19		3.21	mA
Upscale Alarm Current	4 mA to 20 mA and 3.8 mA to 21 mA ranges	22.77		22.83	mA
	3.2 mA to 24 mA range	23.97		24.03	mA
ACCURACY, EXTERNAL R_{SET}(24 kΩ)					
Resolution		16			Bits
Total Unadjusted Error (TUE)[2]	T_A =-40°C to +125°C	-0.08		0.08	%FSR
	T_A =25°C	-0.07		0.07	%FSR
TUE Long-Term Stability	Drift after 1000 hours at T_A = 125°C		TBD		ppm FSR/℃
Relative Accuracy (INL)	T_A =-40°C to +125°C	-0.012	±0.01	0.012	%FSR

PARAMETER[1]	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Differential Nonlinearity (DNL)	Guaranteed monotonic	-1		1	LSB
Offset Error	T_A=-40°C to +125°C	-0.03		+0.03	%FSR
	T_A=25°C	-0.01		+0.01	%FSR
Offset Error TC[3]			TBD		ppm FSR/℃
Gain Error	T_A=-40°C to +125°C	-0.55		0.055	%FSR
	T_A =25°C	-0.046		0.046	%FSR
Gain Error TC[3]			TBD		ppm FSR/℃
Full-Scale Error	T_A =-40°C to +125°C	-0.08		0.08	%FSR
	T_A =25°C	-0.057		0.057	%FSR
Full-Scale Error TC[3]			TBD		ppm FSR/℃
Downscale Alarm Current	Output unloaded	3.08	3	3.21	mA
Upscale Alarm Current	4 mA to 20 mA and 3.8 mA to 21 mA ranges	22.78		23	mA
	3.2 mA to 24 mA range	23.99		24.01	mA
OUTPUT CHARACTERISTICS[3]					
Loop Compliance Voltage[4]	REG_{OUT} < 5.5 V, loop current = 24 mA	LOOP− + 5.5			V
	REG_{OUT} = 12 V, loop current = 24 mA	LOOP− + 12.5			V
Loop Current Long-Term Stability	Drift after 1000 hours at T_A = 125°C, loop current = 12 mA, internal R_{SET}		TBD		ppm/FSR
	Drift after 1000 hours at T_A = 125°C, loop current = 12 mA, external R_{SET}		TBD		ppm/FSR
Loop Current Error vs. REG_{OUT} Load Current	Loop current = 12 mA, load current from REG_{OUT} = 5 mA		0.1		μA/mA
Resistive Load	See **Figure 19** for a load line graph	0		2	kΩ
Inductive Load	Stable operation		50		mH
Power Supply Sensitivity	Loop current = 12 mA		0.082		μA/V
Output Impedance		12	400		MΩ
Output TC	Loop current = 12 mA, internal R_{SET}		TBD		ppm FSR/°C
	Loop current = 12 mA, external R_{SET}		TBD		ppm FSR/°C
Output Noise					
0.1 Hz to 10 Hz			50		nAp-p

PARAMETER[1]	TEST CONDITIONS	MIN	TYP	MAX	UNIT
500 Hz to 10 kHz	HART bandwidth; measured across 500 Ω load		0.28		mV rms
Noise Spectral Density	At 1 kHz		195		nA/√Hz
	At 10 kHz		256		nA/√Hz
REFERENCE INPUT (REFIN PIN)[3]					
Reference Input Voltage[5]	For specified performance		2.5		V
DC Input Impedance		75	800		MΩ
REFERENCE OUTPUT					
REFOUT1 Pin					
Output Voltage	T_A = 25°C	2.495	2.5	2.505	V
Temperature Coefficient			4		ppm/°C
Output Noise (0.1 Hz to 10 Hz)[3]			10		μV p-p
Noise Spectral Density[3]	At 1 kHz		360		nV/√Hz
	At 10 kHz		35		nV/√Hz
Output Voltage Drift vs. Time[3]	Drift after 1000 hours at T_A = 125°C		TBD		ppm
Capacitive Load[3]	Recommended operation		100		nF
Load Current[3, 6]			1		mA
Short-Circuit Current[3]	Short circuit to COM		1.4		mA
Power Supply Sensitivity[3]			7.2	12	μV/V
Thermal Hysteresis[3]	First temperature cycle		TBD		ppm
	Second temperature cycle		TBD		ppm
Load Regulation[3]	Measured at 0 mA and 1 mA loads		0.375		mV/mA
Output Impedance			0.375		Ω
REFOUT2 Pin					
Output Voltage	T_A = 25°C		2.45		V
Output Impedance			72		kΩ
REG_{OUT} OUTPUT	Voltage regulator output				
Output Voltage	See **Table 5/Table 6**	1.8	0	20	V
Output Voltage TC[3]			TBD		ppm/°C
Output Voltage Accuracy		-4	±2	4	%
Externally Available Current[3, 6]	Assuming 4 mA is flowing in the loop and during HART communications	3.15			mA
Short-Circuit Current	Short to COM		7.05		mA

PARAMETER[1]	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Line Regulation[3]	Internal NMOS		5		μV/V
	External NMOS		2		μV/V
Inductive Load	Stable operation		50		mH
Capacitive Load	Recommended operation	2	10		μF
ADC ACCURACY					
Die Temperature			±5		℃
V_{LOOP} Input			1		%
DV_{DD} OUTPUT	Can be overdriven up to 5.5 V				
Externally Available Current[3, 6]	Assuming 4 mA is flowing in the loop and during HART communications	3.15			mA
Short-Circuit Current			4.5		mA
Load Regulation	Measured at 0 mA and 2 mA loads		4.5		mV/mA
DIGITAL INPUTS[3]	SCLK, SYNC, SDIN, LDAC				
Input High Voltage, VIH		0.7 × $IODV_{DD}$			V
Input Low Voltage, VIL				0.25 × $IODV_{DD}$	V
Hysteresis	$IODV_{DD}$ = 1.8 V		0.21		V
	$IODV_{DD}$ = 3.3 V		0.63		V
	$IODV_{DD}$ = 5.5 V		1.46		V
Input Current	Per pin	−0.015		0.015	μA
Pin Capacitance	Per pin		5		pF
DIGITAL OUTPUTS[3]					
SDO Pin					
Output Low Voltage, V_{OL}				0.4	V
Output High Voltage, V_{OH}			$IODV_{DD}$ − 0.5		V
High Impedance Leakage Current		-0.01		0.01	μA
High Impedance Output Capacitance			5		pF
FAULT Pin					
Output Low Voltage, V_{OL}				0.4	V
Output Low Voltage, V_{OH}		$IODV_{DD}$ − 0.5			V
FAULT THRESHOLDS					

PARAMETER[1]	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LOOP} Under			I_{LOOP} − 0.01% FSR		mA
I_{LOOP} Over			I_{LOOP} + 0.01% FSR		mA
Temp 140°C	Fault removed when temperature is ≤ 125°C		133		℃
Temp 100°C	Fault removed when temperature is ≤ 85°C		90		℃
V_{LOOP} 6V	Fault removed when V_{LOOP} ≥ 0.4 V		0.3		V
V_{LOOP} 12V	Fault removed when V_{LOOP} ≥ 0.7 V		0.6		V

Note:

[1] Temperature range: −40°C to +125°C; typical at +25°C. System level total error can be reduced using the offset and gain registers.

[2] Total unadjusted error is the total measured error (offset error + gain error + linearity error + output drift over temperature) after factory calibration of the TPC2221

[3] Guaranteed by design and characterization; not production tested.

[4] The voltage between LOOP− and REG_{IN} must be 5.5 V or greater.

[5] The TPC2221 is factory calibrated with an external 2.5 V reference connected to REFIN.

[6]This is the current that the output is capable of sourcing. The load current originates from the loop and, therefore, contributes to the total current consumption figure.

Loop voltage = 24 V; REFIN = REFOUT1 (2.5 V internal reference); R_L = 250 Ω; external NMOS connected; all loop current ranges; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

PARAMETER[1,2]	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ACCURACY, INTERNAL R_{SET}					
Total Unadjusted Error (TUE)[3]	T_A =-40°C to +125°C	-0.157		0.157	%FSR
	T_A =25°C	-0.141		0.141	%FSR
Relative Accuracy (INL)	T_A =-40°C to +125°C	-0.012		0.012	%FSR
	T_A =25°C	-0.01		0.01	%FSR
Offset Error	T_A =-40°C to +125°C	-0.04		0.04	%FSR
	T_A =25°C	-0.025	±0.0025	0.025	%FSR
Offset Error TC			TBD		ppm FSR/℃
Gain Error	T_A =-40°C to +125°C	−0.128		0.128	%FSR
	T_A =25°C	−0.11		0.11	%FSR
Gain Error TC			TBD		ppm FSR/°C
Full-Scale Error	T_A =-40°C to +125°C	−0.157		0.157	%FSR
	T_A =25°C	−0.134		0.134	%FSR
Full-Scale Error TC			TBD		ppm FSR/°C
ACCURACY, EXTERNAL R_{SET} (24 kΩ)					
Total Unadjusted Error (TUE)[3]	T_A =-40°C to +125°C	−0.133		0.133	%FSR
	T_A =25°C	−0.129		0.129	%FSR
Relative Accuracy (INL)	T_A =-40°C to +125°C	−0.012		0.012	%FSR
	T_A = 25°C	−0.011		0.011	%FSR
Offset Error	T_A =-40°C to +125°C	−0.029		0.029	%FSR
	T_A = 25°C	−0.01		0.01	%FSR
Offset Error TC			TBD		ppm FSR/°C
Gain Error	T_A =-40°C to +125°C	−0.106		0.106	%FSR
	T_A = 25°C	−0.097		0.097	%FSR
Gain Error TC			TBD		ppm FSR/°C
Full-Scale Error	T_A =-40°C to +125°C	−0.133		0.133	%FSR
	T_A = 25°C	−0.108		0.108	%FSR
Full-Scale Error TC			TBD		ppm FSR/°C

Note:

[1] Temperature range: −40°C to +125°C; typical at +25°C.

[2] Specifications guaranteed by design and characterization; not production tested.

[3] Total unadjusted error is the total measured error (offset error + gain error + linearity error + output drift over temperature) after factory calibration of the TPC2221. System level total error can be reduced using the offset and gain registers.

AC PERFORMANCE CHARACTERISTICS

Loop voltage = 24 V; REFIN = 2.5 V external; R_L = 250 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE[1]					
Loop Current Settling Time	To 0.1% FSR, C_{IN} = open circuit		30		µs
Loop Current Slew Rate	C_{IN} = open circuit		533		µA/µs
AC Loop Voltage Sensitivity	1200 Hz to 2200 Hz, 5 Vp-p, R_L = 3 kΩ		1.3		µA/V

Note:

[1] Temperature range: −40°C to +125°C; typical at +25°C.

Timing Requirements

Loop voltage = 24 V; REFIN = 2.5 V external; R_L = 250 Ω; all specifications T_{MIN} to T_{MAX}..

Table 2. TIMING CHARACTERISTICS

Parameter[1, 2, 3]	Description	MIN	TYP	MAX	Unit
t_1	SCLK cycle time	33			ns
t_2	SCLK high time	17			ns
t_3	SCLK low time	17			ns
t_4	$\overline{SYNC}$ falling edge to SCLK falling edge setup time	17			ns
t_5	SCLK falling edge to$\overline{SYNC}$ rising edge	10			ns
t_6	Minimum $\overline{SYNC}$ high time	25			µs
t_7	Data setup time	5			ns
t_8	Data hold time	5			ns
t_9	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge	25			µs
t_{10}	$\overline{LDAC}$ pulse width low	10			ns
t_{11}	SCLK rising edge to SDO valid ($C_{L\ SDO}$ = 30 pF)	70			ns
t_{12}	$\overline{SYNC}$ falling edge to SCLK rising edge setup time	0			ns
t_{13}	$\overline{SYNC}$ rising edge to SDO tristate ($C_{L\ SDO}$ = 30 pF)	70			ns

[1]Guaranteed by design and characterization; not production tested.

[2]All input signals are specified with t_R = t_F = 5 ns (10% to 90% of DVDD) and timed from a voltage level of 1.2 V

$C_{L\ SDO}$= capacitive load on SDO output

Table 3. SPI Watchdog Timeout Periods[1]

T0	T1	T2	Min	Typ	Max	Unit
0	0	0	43	50	59	ms

T0	T1	T2	Min	Typ	Max	Unit
0	0	1	87	100	117	ms
0	1	0	436	500	582	ms
0	1	1	873	1000	1163	ms
1	0	0	1746	2000	2326	ms
1	0	1	2619	3000	3489	ms
1	1	0	3493	4000	4652	ms
1	1	1	4366	5000	5814	ms

Note:

[1]Specifications guaranteed by design and characterization; not production tested.

Timing Diagrams

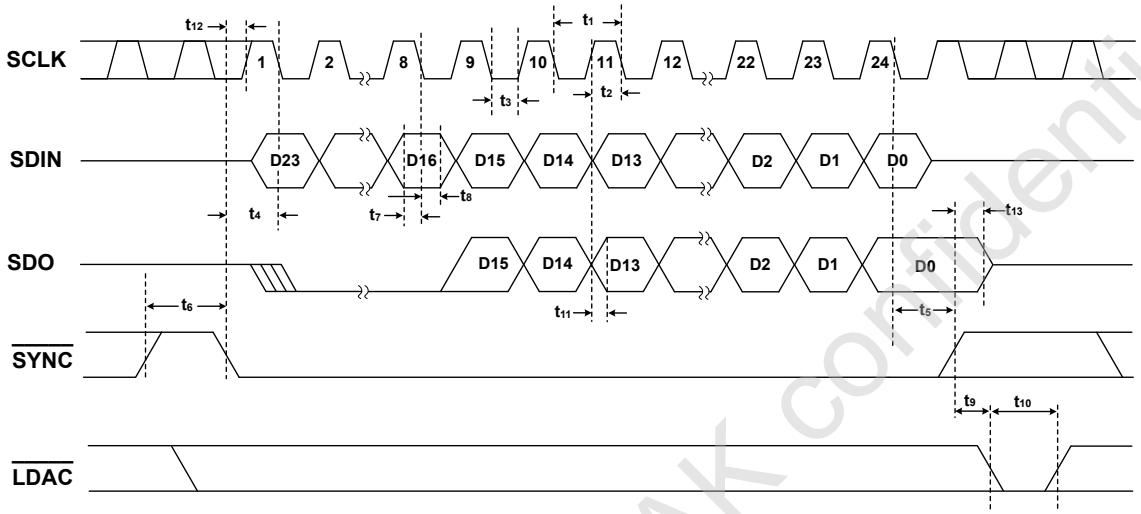


Figure 2. Write Mode Timing Diagram

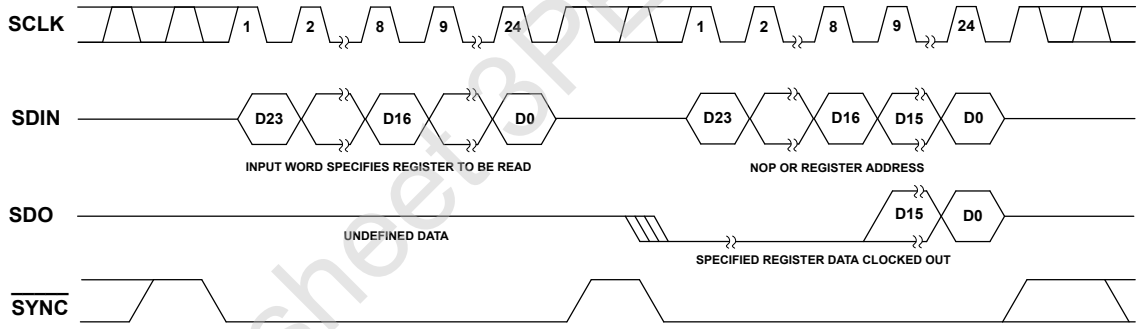


Figure 3. Readback Mode Timing Diagram

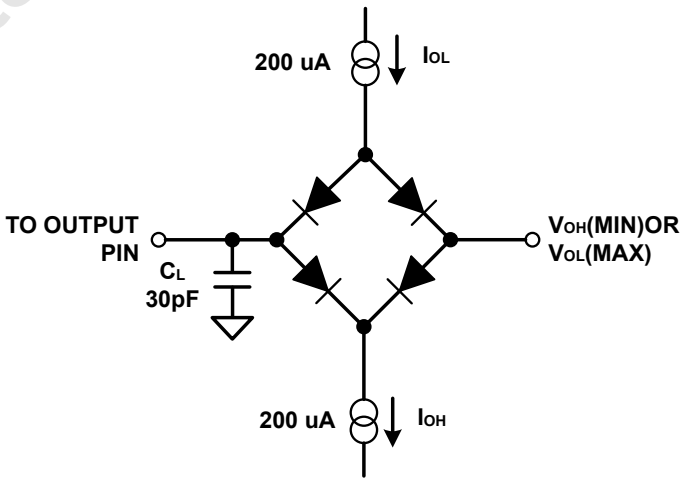


Figure 4. SDO Load Diagram

Typical Performance Characteristics

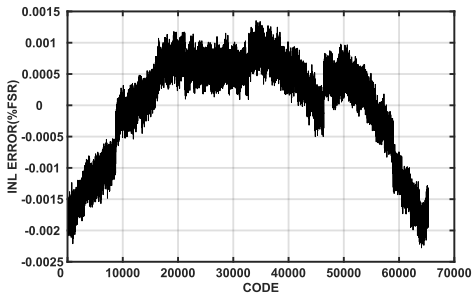


Figure 5. Integral Nonlinearity Error vs. Code

- V_{LOOP} = 24 V;EXT NMOS;R_{LOAD} = 250 Ω;T_A = 25°C;4mA TO 20mA RANGE;EXT V_{REF};EXT R_{SET}

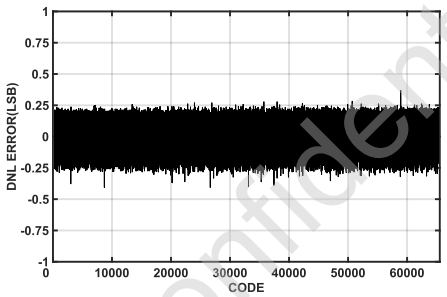


Figure 6. Differential Nonlinearity Error vs. Code

- V_{LOOP} = 24 V;EXT NMOS;R_{LOAD} = 250 Ω;T_A = 25°C;4mA TO 20mA RANGE;EXT V_{REF};EXT R_{SET}

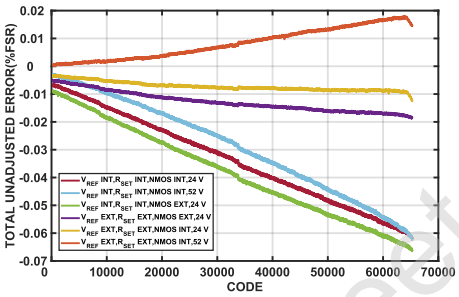


Figure 7. Total Unadjusted Error vs. Code

- V_{LOOP} = 24 V;EXT NMOS;R_{LOAD} = 250 Ω;T_A = 25°C

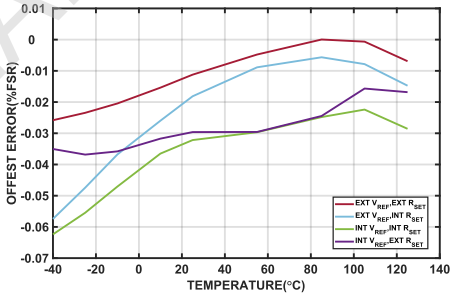


Figure 8. Offset Error vs. Temperature

- V_{LOOP}= 24 V;R_{LOAD} = 250 Ω;4 mA to 20 mA Range;EXT NMOS

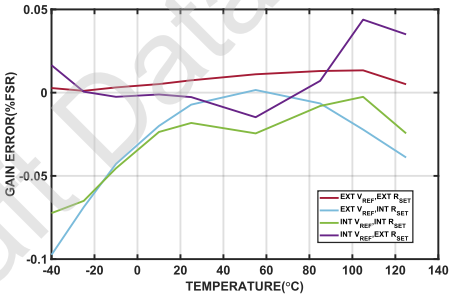


Figure 9. Gain Error vs. Temperature

- V_{LOOP} = 24 V;R_{LOAD} = 250 Ω;4 mA to 20 mA Range;EXT NMOS

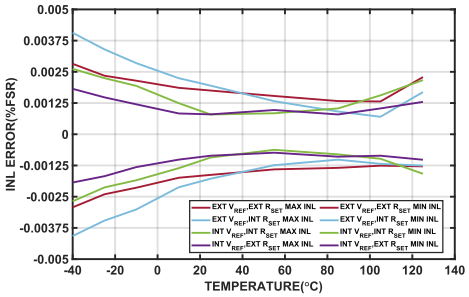


Figure 10. Integral Nonlinearity Error vs. Temperature

- V_{LOOP} = 24 V;R_{LOAD} = 250 Ω;4 mA to 20 mA Range;EXT NMOS

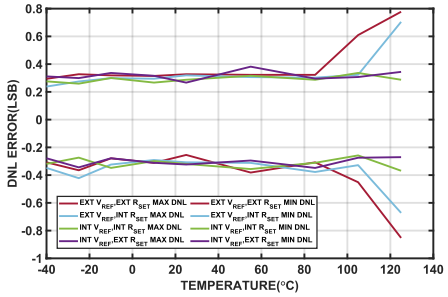


Figure 11. Differential Nonlinearity Error vs. Temperature

- V_{LOOP} = 24 V;R_{LOAD} = 250 Ω;4 mA to 20 mA Range;EXT NMOS

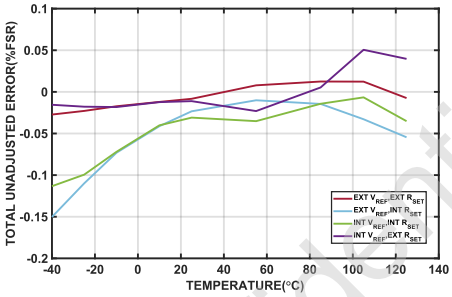


Figure 12. Total Unadjusted Error vs. Temperature

- V_{LOOP} = 24 V;R_{LOAD} = 250 Ω;4 mA to 20 mA Range;EXT NMOS

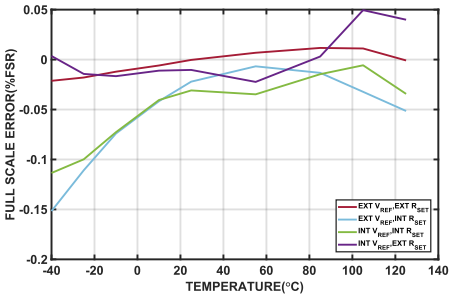


Figure 13. Full-Scale Error vs. Temperature

- V_{LOOP} = 24 V;R_{LOAD} = 250 Ω;4 mA to 20 mA Range;EXT NMOS

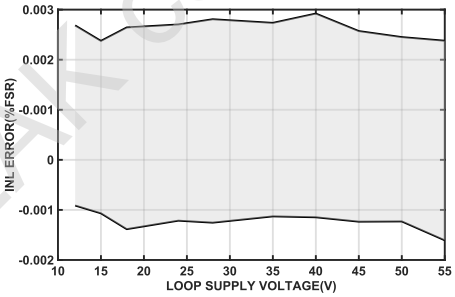


Figure 14. Integral Nonlinearity Error vs. Loop Supply Voltage

- EXT NMOS;R_{LOAD} = 250 Ω;T_A = 25°C;EXT R_{SET};EXT V_{REF};3.8 mA TO 21 mA Range

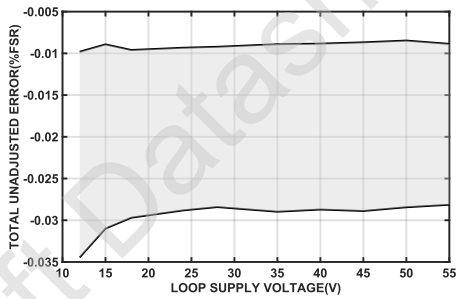


Figure 15. Total Unadjusted Error vs. Loop Supply Voltage

- EXT NMOS;R_{LOAD} = 250 Ω;T_A = 25°C;EXT R_{SET};EXT V_{REF};3.8 mA TO 21 mA Range

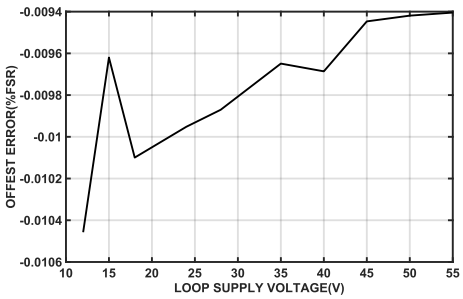


Figure 16. Offset Error vs. Loop Supply Voltage

- EXT NMOS;R_{LOAD} = 250Ω;T_A = 25°C;EXT R_{SET};EXT V_{REF};3.8 mA TO 21 mA Range

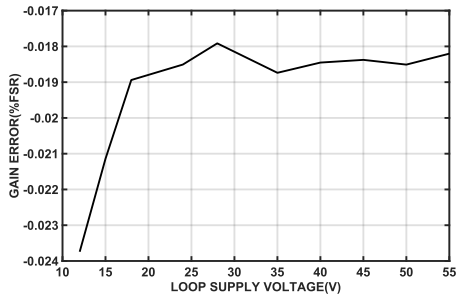


Figure 17. Gain Error vs. Loop Supply Voltage

- EXT NMOS;R_{LOAD} = 250Ω;T_A = 25°C;EXT R_{SET};EXT V_{REF};3.8 mA TO 21 mA Range

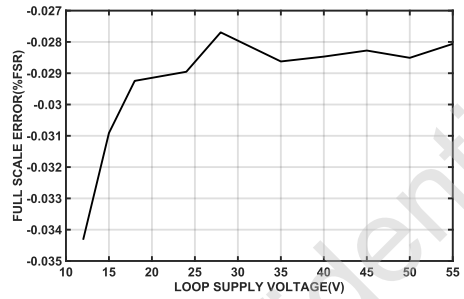


Figure 18. Full-Scale Error vs. Loop Supply Voltage

- EXT NMOS;R_{LOAD} = 250Ω;T_A = 25°C;EXT R_{SET};EXT V_{REF};3.8 mA TO 21 mA Range

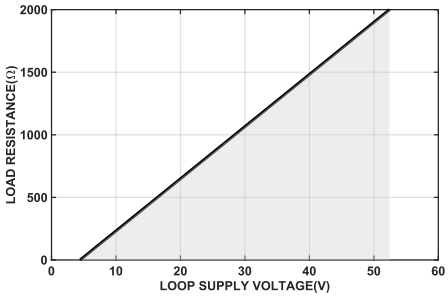


Figure 19. Load Resistance Load Line vs. Loop Supply Voltage (Voltage Between LOOP− and REG_{IN})

- T_A = 25°C;I_{LOOP} = 24 mA;EXT V_{REF};EXT R_{SET}

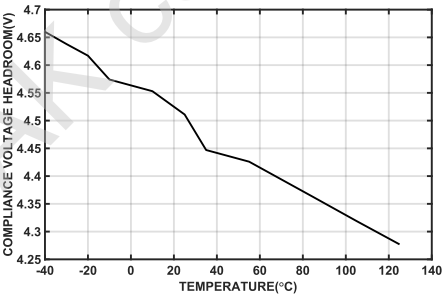


Figure 20. Compliance Voltage Headroom vs. Temperature

- R_{LOAD} = 250 Ω;T_A = 25°C;I_{LOOP} = 24mA;EXT V_{REF}

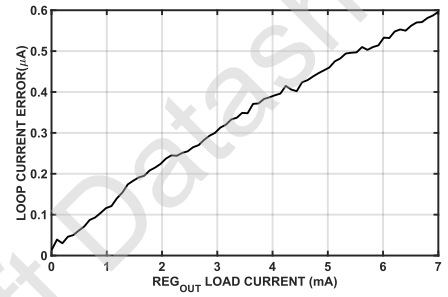


Figure 21. Loop Current Error vs. REG_{OUT} Load Current

- V_{LOOP} = 24V;EXT NMOS;R_{LOAD} = 250 Ω;T_A = 25°C;I_{LOOP} = 20mA;EXT V_{REF}

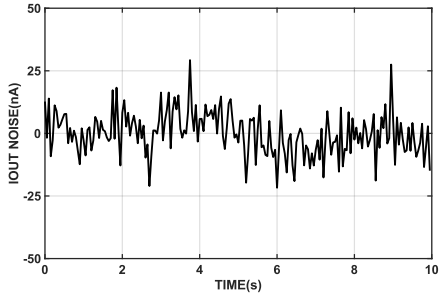


Figure 22. Loop Current Noise, 0.1 Hz to 10 Hz Bandwidth

- V_{LOOP} = 24 V;EXT NMOS;EXT V_{REF};T_A = 25°C ;I_{LOOP} = 4 mA

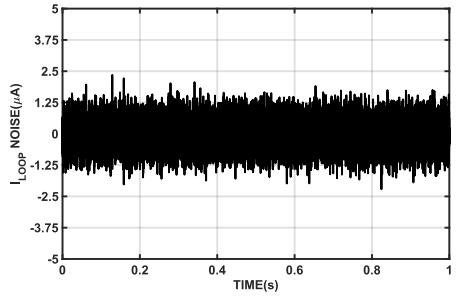


Figure 23. Loop Current Noise, 100 Hz to 10 kHz Bandwidth

- V_{LOOP} = 24 V;EXT NMOS;EXT V_{REF};I_{LOOP} = 4 mA;T_A = 25°C

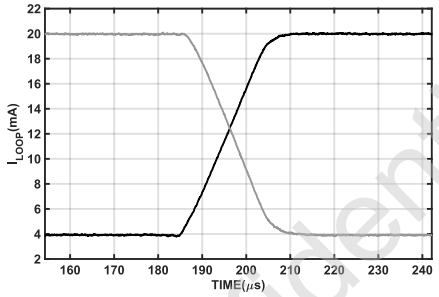


Figure 24. Full-Scale Loop Current Step

- V_{LOOP} = 24V;EXT NMOS;R_{LOAD} = 250 Ω;T_A = 25°C;C_{IN} = OPEN CIRCUIT

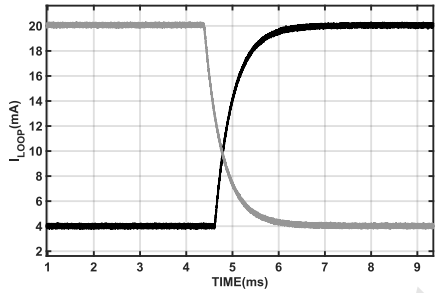


Figure 25. Full-Scale Loop Current Step, C_{IN} = 22 nF

- V_{LOOP} = 24V;EXT NMOS;R_{LOAD} = 250 Ω;T_A = 25°C;C_{IN} = 22 nF

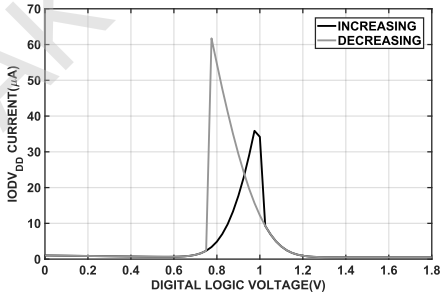


Figure 26. $IODV_{DD}$ Current vs. Digital Logic Voltage, Increasing and Decreasing, $IODV_{DD}$ = 1.8 V

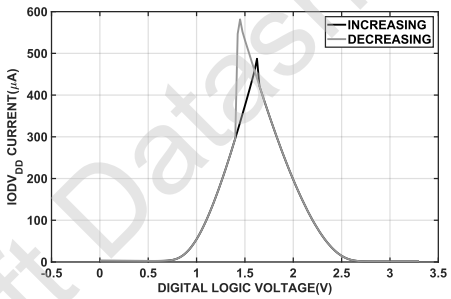


Figure 27. $IODV_{DD}$ Current vs. Digital Logic Voltage, Increasing and Decreasing, $IODV_{DD}$ = 3.3 V

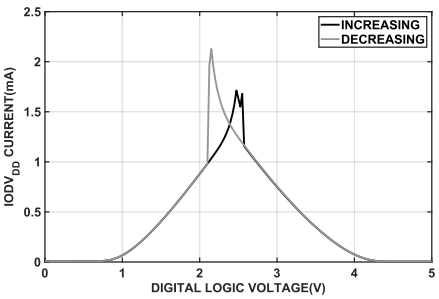


Figure 28. $IODV_{DD}$ Current vs. Digital Logic Voltage, Increasing and Decreasing, $IODV_{DD}$ = 5 V

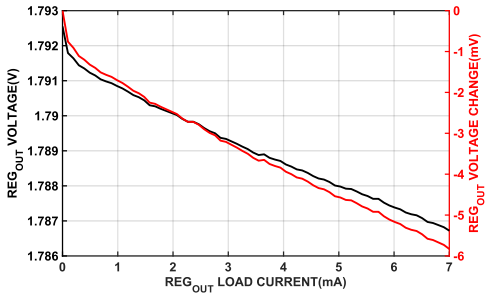


Figure 29. REG_{OUT} Voltage vs. Load Current

- V_{LOOP} = 24 V;EXT NMOS;T_A = 25°C

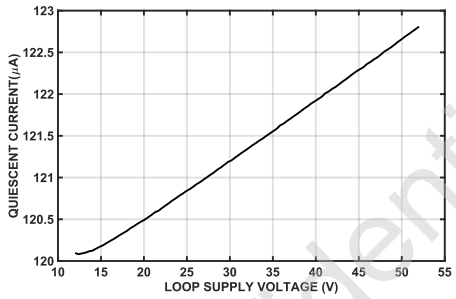


Figure 30. Quiescent Current vs. Loop Supply Voltage

- V_{LOOP} = 24 V;EXT NMOS;T_A = 25°C

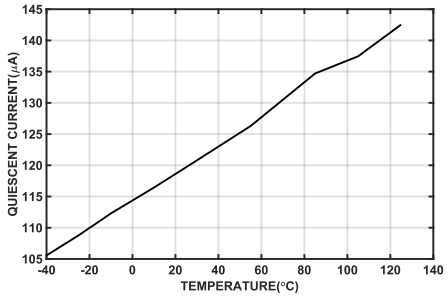


Figure 31. Quiescent Current vs. Temperature

- V_{LOOP} = 24 V;EXT NMOS;V_{IH}=IOV_{DD};V_{IL}=COM;T_A = 25°C

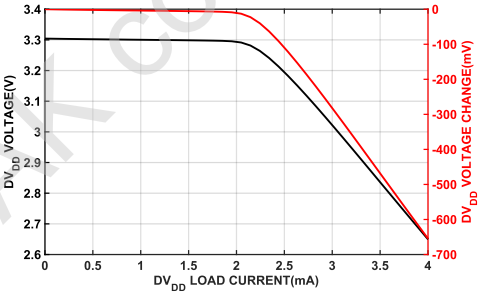


Figure 32. DV_{DD} Output Voltage vs. Load Current

- V_{LOOP} = 24 V;EXT NMOS;T_A = 25°C

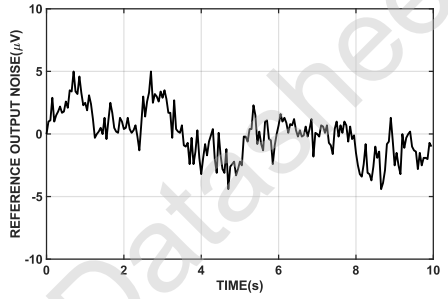


Figure 33. REFOUT1 Voltage Noise, 0.1 Hz to 10 Hz Bandwidth

- V_{LOOP} = 24 V;EXT NMOS;T_A = 25°C

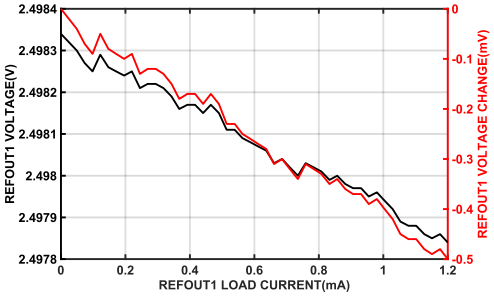


Figure 34. REFOUT1 Voltage vs. Load Current

- V_{LOOP} = 24 V;EXT NMOS;T_A = 25°C

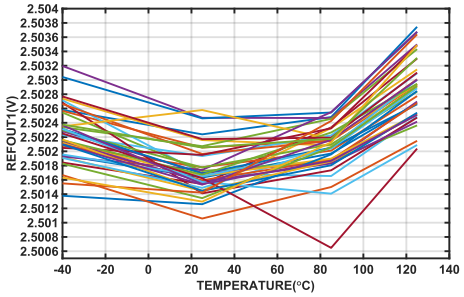


Figure 35. REFOUT1 Voltage vs. Temperature, 40 Devices Shown

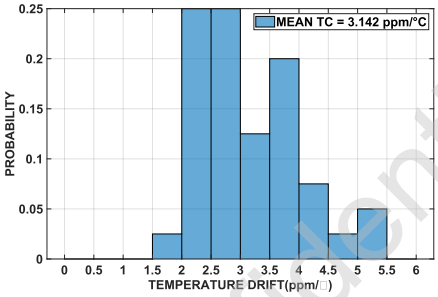


Figure 36. REFOUT1 Temperature Coefficient Histogram

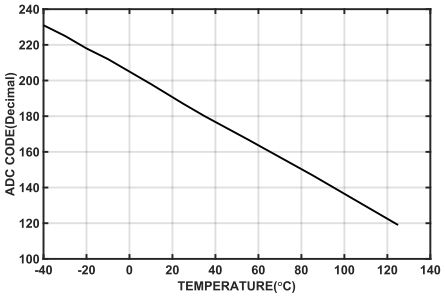


Figure 37. On-Chip ADC Code vs. Die Temperature

- V_{LOOP} = 24 V;EXT NMOS;;T_A = 25°C;R_{LOAD} = 250 Ω;I_{LOOP} = 3.2 mA

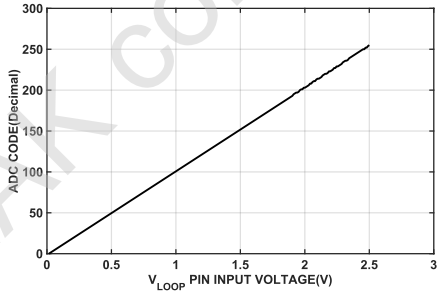


Figure 38. On-Chip ADC Code vs. V_{LOOP} Pin Input Voltage

- V_{LOOP} = 24 V;EXT NMOS;;T_A = 25°C

TERMINOLOGY

Total Unadjusted Error

Total unadjusted error (TUE) is a measure of the total output error. TUE consists of INL error, offset error, gain error, and output drift over temperature, in the case of maximum TUE. TUE is expressed in % FSR.

Relative Accuracy or Integral Nonlinearity (INL) Error

Relative accuracy, or integral nonlinearity (INL) error, is a measure of the maximum deviation in the output current from a straight line passing through the endpoints of the transfer function. INL error is expressed in % FSR.

Differential Nonlinearity (DNL) Error

Differential nonlinearity (DNL) error is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity.

Offset Error

Offset error is a measure of the output error when zero code is loaded to the DAC register and is expressed in % FSR

Offset Error Temperature Coefficient (TC)

Offset error TC is a measure of the change in offset error with changes in temperature and is expressed in ppm FSR/°C.

Gain Error

Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer function from the ideal and is expressed in % FSR.

Gain Error Temperature Coefficient (TC)

Gain error TC is a measure of the change in gain error with changes in temperature and is expressed in ppm FSR/°C.

Full-Scale Error

Full-scale error is a measure of the output error when full-scale code is loaded to the DAC register and is expressed in % FSR.

Full-Scale Error Temperature Coefficient (TC)

Full-scale error TC is a measure of the change in full-scale error with changes in temperature and is expressed in ppm FSR/°C.

Loop Compliance Voltage Headroom

Loop compliance voltage headroom is the minimum voltage between the LOOP− and REGIN pins for which the output current is equal to the programmed value

Output Temperature Coefficient (TC)

Output TC is a measure of the change in the output current at 12 mA with changes in temperature and is expressed in ppm FSR/°C.

Voltage Reference Thermal Hysteresis

Voltage reference thermal hysteresis is the difference in output voltage measured at +25°C compared to the output voltage measured at +25°C after cycling the temperature from +25°C to −40°C to +125°C and back to +25°C. The hysteresis is specified for the first and second temperature cycles and is expressed in mV.

Voltage Reference Temperature Coefficient (TC)

Voltage reference TC is a measure of the change in the reference output voltage with a change in temperature. The voltage reference TC is calculated using the box method, which defines the TC as the maximum change in the reference output voltage over a given temperature range. Voltage reference TC is expressed in ppm/°C as follows:

$$TC = \frac{(V_{REF\_MAX} - V_{REF\_MIN})}{(V_{REF\_NOM} \times Temp\_Range)} \times 10^6 \quad (1)$$

where:V_{REF_MAX} is the maximum reference output voltage measured over the total temperature range.

V_{REF_MIN} is the minimum reference output voltage measured over the total temperature range.

V_{REF_NOM} is the nominal reference output voltage, 2.5 V

Temp_Range is the specified temperature range (−40°C to +125°C)

Detailed Description

Overview

The TPC2221 is a fully integrated, loop-powered digital-to-analog converter (DAC) specifically designed to meet the needs of intelligent sensor manufacturers in the industrial automation field.

Functional Block Diagram

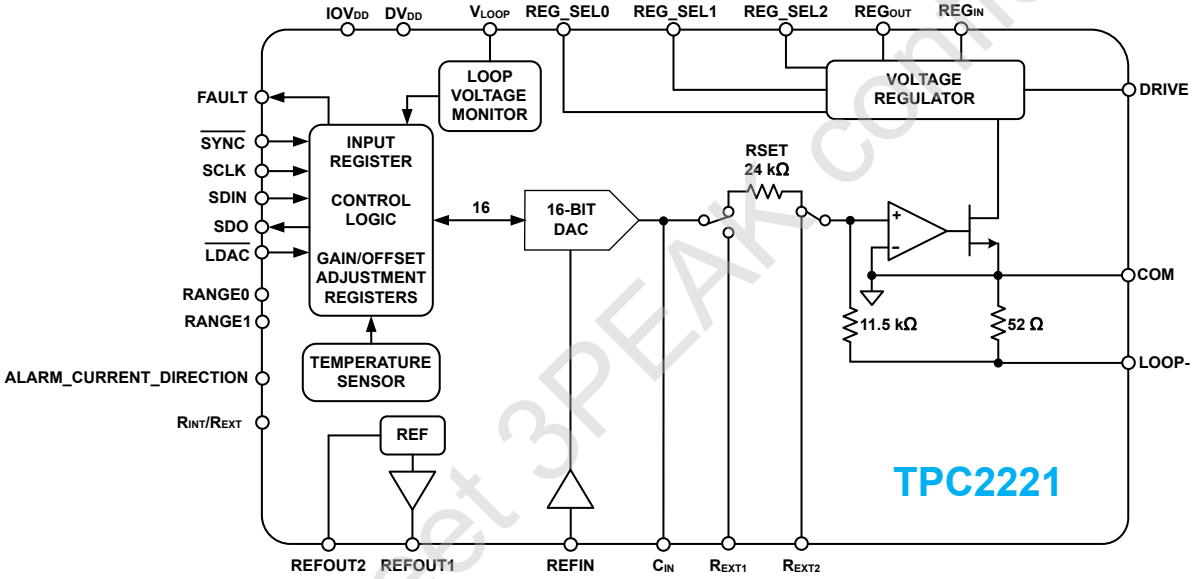


Figure 39. Functional Block Diagram

Feature Description

Functional Modes

THEORY OF OPERATION

The TPC2221 is an advanced integrated solution specifically engineered for loop-powered, 4 mA to 20 mA smart transmitter applications. Within a single chip, the TPC2221 integrates a 16-bit DAC and current amplifier for precise digital control of loop current, a voltage regulator to supply power to the entire transmitter, a stable voltage reference, fault alert functions, a versatile SPI-compatible serial interface, gain and offset adjustment registers, and additional features. The detailed characteristics of the TPC2221 are elaborated in the subsequent sections.

FAULT ALERTS

The TPC2221 incorporates several fault alert mechanisms designed to signal the controller via the FAULT pin and the fault register. In the event of communication loss between the TPC2221 and the microcontroller (SPI fault), the TPC2221 will set the loop current to an alarm value. Upon detecting the FAULT pin being set high, the controller must read the fault register to identify the specific cause of the fault. It is important to note that the watchdog timer does not reset or restart while an alarm is active. If auto fault readback is disabled and an SPI fault occurs, causing the watchdog timer to time out, the timer will

remain inactive until the status register is manually read by the user. Following this manual readback, the watchdog timer will resume its operation.

SPI FAULT

The SPI fault is triggered when valid communication with any register of the TPC2221 is not established for a duration exceeding a user-specified interval. Users have the ability to set this interval using the SPI watchdog timeout bits within the control register. The SPI fault bit in the fault register signals any issues on the SPI bus. As this fault results from a communication interruption between the controller and the TPC2221, the loop current is consequently driven to an alarm value. The direction of the alarm current, whether it increases or decreases, is determined by the ALARM_CURRENT_DIRECTION pin. Attaching this pin to DV_{DD} results in an increasing alarm current (22.8 mA/24 mA), while connecting it to COM results in a decreasing alarm current (3.2 mA).

Packet Error Checking

For ensuring data integrity in noisy conditions, the TPC2221 provides an 8-bit cyclic redundancy check (CRC)-based error detection feature. This is activated by sending a 32-bit serial frame to the TPC2221, with the last eight bits designated as the frame check sequence (FCS). The controlling device must calculate the 8-bit FCS using the specified polynomial to implement packet error checking (PEC):

$$C(x) = X^8 + X^2 + X + 1 \quad (2)$$

The 8-bit FCS is appended to the end of the data-word, and 32 data bits are sent to the TPC2221 before s is taken high. If the check is valid, the data is accepted. If the check fails, the FAULT pin is asserted and the PEC bit of the fault register is set.

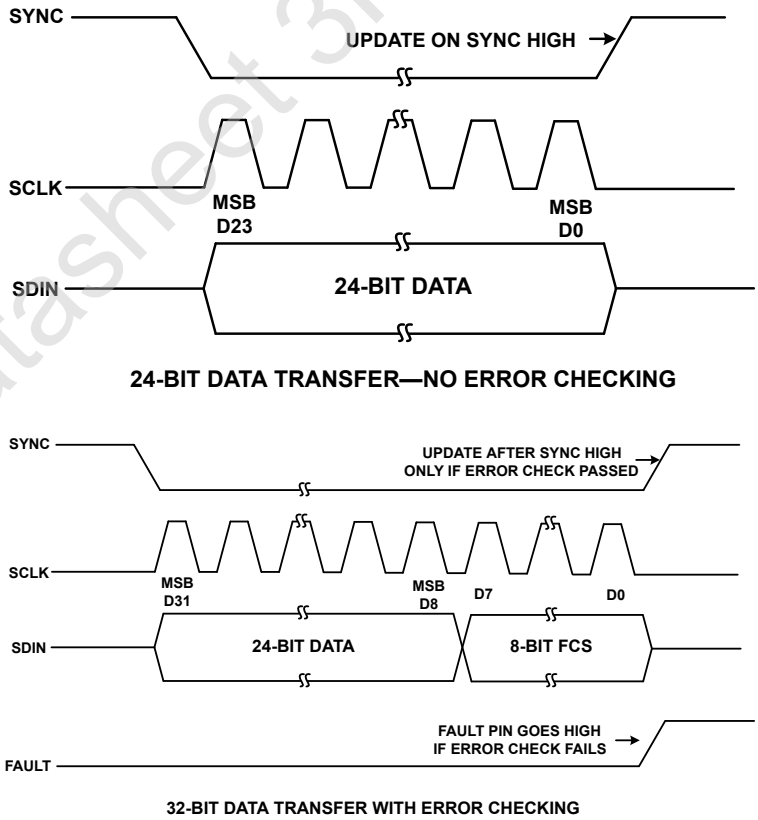


Figure 40. PEC Timing

Current Loop Fault

The I_{LOOP} fault is triggered when the actual loop current deviates from the set loop current by more than ±0.01% of the full-scale range (FSR). The fault register's I_{LOOP} Under bit is activated if the detected loop current is lower than the programmed value, while the I_{LOOP} Over bit is activated if the detected loop current exceeds the programmed value. In both scenarios, the FAULT pin is driven to a high logic level. An I_{LOOP} Over fault is indicated when the load current supplied by the TPC2221 (through REG_{OUT}, REFOUT1, REFOUT2, or DV_{DD}) surpasses the programmed loop current. Conversely, an I_{LOOP} Under fault is indicated when there is not enough compliance voltage to maintain the programmed loop current, typically due to an excessive load resistance or a low loop supply voltage.

Overtemperature Fault

The fault register contains two overtemperature alert flags: Temp 100°C and Temp 140°C. Whenever the die temperature of the TPC2221 surpasses the thresholds of 100°C or 140°C, the corresponding flag is activated. In the event that the Temp 140°C flag is triggered in the fault register, the FAULT pin is driven to a high logic state.

Loop Voltage Fault

The fault register includes two loop voltage alert flags: V_{LOOP} 12 V and V_{LOOP} 6 V. The V_{LOOP} 12 V flag is activated if the voltage across the V_{LOOP} and COM pins drops below 0.6 V, which is indicative of a 12 V loop supply voltage, and it resets when the voltage rises above 0.7 V. In a similar fashion, the V_{LOOP} 6 V flag is triggered if the voltage between the V_{LOOP} and COM pins falls below 0.3 V, corresponding to a 6 V loop supply, and it resets when the voltage exceeds 0.4 V. If the V_{LOOP} 6V flag is triggered in the fault register, the FAULT pin is driven to a high logic level.**Figure 7** depicts how a voltage divider can be used to monitor the loop supply with the V_{LOOP} input. The suggested voltage divider is composed of a 1 MΩ and a 19 MΩ resistor, creating a 20:1 ratio that enables the 2.5 V input range of the V_{LOOP} pin to oversee loop supplies up to 50 V. With this 20:1 ratio, the predefined V_{LOOP} 6V and V_{LOOP} 12 V alert flags in the fault register trigger loop supply faults at their designated voltages. If a different divider ratio is implemented, the fault flags will generate faults at voltages that are not precisely 6 V and 12 V.

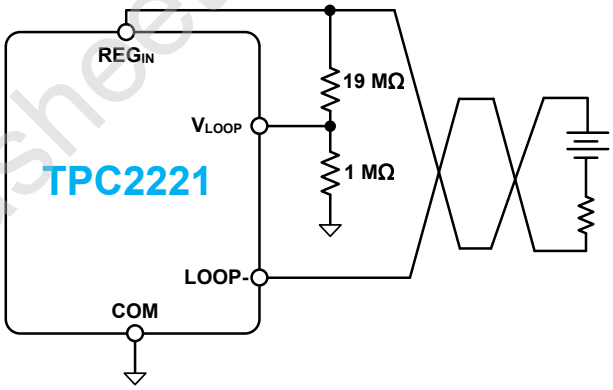


Figure 41. Resistor Divider Connection at V_{LOOP}Pin

EXTERNAL CURRENT SETTING RESISTOR

As depicted in **Figure 1**, the 24 kΩ resistor R_{SET} transforms the DAC output voltage into a current, which is subsequently amplified by a factor of 221 and directed to the LOOP− pin. The temperature stability of the loop current is contingent upon the temperature coefficient of R_{SET}.Electrical Characteristics detail the performance characteristics of the TPC2221 when utilizing both the internal R_{SET} resistor and an external 24 kΩ RSET resistor. Employing the internal R_{SET} resistor results in an unadjusted total error of less than **0.126% FSR**. Utilizing an external resistor enhances performance to **0.07% FSR**. This specification is predicated on the assumption of an ideal resistor; the actual performance is subject to the absolute value and temperature coefficient of the resistor employed. For further details, refer to the section on**Determining the Expected Total Error**.

LOOP CURRENT RANGE SELECTION

To select the loop current range, connect the RANGE0 and RANGE1 pins to the COM and DV_{DD} pins, as shown in **Table 4**.

Table 4. Selecting the Loop Current Range

RANGE1 Pin	RANGE0 Pin	Loop Current Range
COM	COM	4 mA to 20 mA
COM	DV_{DD}	3.8 mA to 21 mA
DV_{DD}	COM	3.2 mA to 24 mA
DV_{DD}	DV_{DD}	3.8 mA to 21 mA

CONNECTION TO LOOP POWER SUPPLY

The TPC2221 derives its power from a 4 mA to 20 mA current loop, which is commonly sourced from a power supply situated at a distance from the transmitter unit and typically operates at 24 V. The TPC2221 is capable of being connected directly to this loop power supply and can withstand voltages up to a maximum of **60 V**, as illustrated in **Figure 42**.

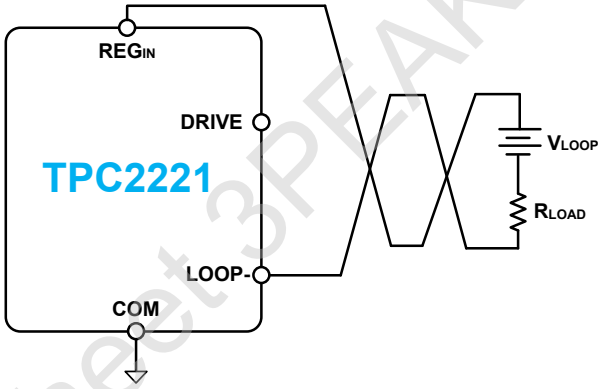


Figure 42. Direct Connection of the TPC2221 to Loop Power Supply

Figure 42 illustrates the direct connection of the TPC2221 to the loop power supply.**Figure 43**, on the other hand, presents an alternative power connection scheme that incorporates a depletion mode N-channel MOSFET bridging the TPC2221 and the loop power supply. This setup maintains the voltage drop across the TPC2221 around 12 V, thereby capping the maximum on-chip power dissipation at 288 mW (12 V × 24 mA = 288 mW). In contrast, if the TPC2221 is connected directly to the loop supply as depicted in Figure 43, the maximum on-chip power dissipation for a 24 V loop power supply would be 576 mW (24 V × 24 mA = 576 mW). It's important to note that the power dissipation varies directly with the loop power supply voltage.

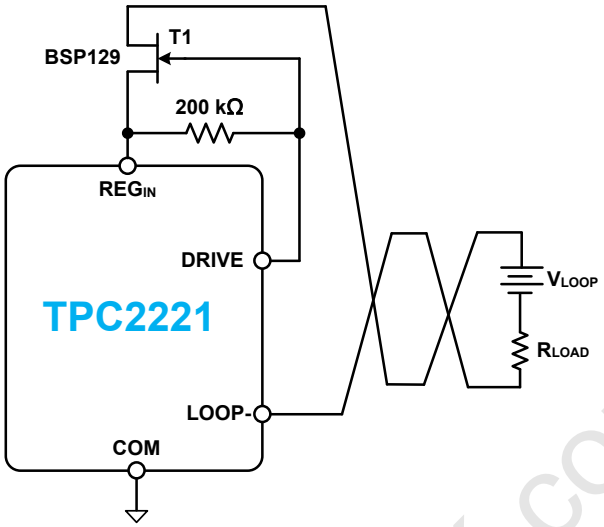


Figure 43. MOSFET Connecting the TPC2221 to Loop Power Supply

To achieve significant reductions in the rate of change, very large capacitor values are required, which may not be suitable in some applications. In this case, the digital slew rate control feature can be used. The capacitors can be used in conjunction with the digital slew rate control feature as a means of smoothing out the steps caused by the digital code increments, as shown in following figure.

ON-CHIP ADC

The TPC2221 is equipped with an integrated ADC that is tasked with measuring either the die temperature or the voltage across the V_{LOOP} and COM pins, and then feeding this data back to the fault register. The selection of the measurement parameter is determined by the select ADC input bit (Bit D8) within the control register. Initiating a conversion is done by sending the command byte 00001000, which is only required if auto fault readback is not enabled; this command activates the ADC and commences the conversion process. The result of the conversion can be retrieved by reading the fault register. For automatic readback of the fault register, the ADC must be activated by setting the on-chip ADC bit (Bit D7) in the control register.Given that the FAULT pin may remain high for up to **30 µs**, caution must be exercised when switching from a V_{LOOP} voltage reading to a die temperature measurement. To avoid false triggers (though the fault register contents remain unchanged), the FAULT pin should not be accessed within **30 µs** after making the switch from a V_{LOOP} measurement to a temperature measurement.

VOLTAGE REGULATOR

The integrated voltage regulator within the chip delivers a stable voltage output to power both the TPC2221 and the rest of the transmitter's circuitry. The output voltage can be adjusted to range between 1.8 V and 12 V, with the specific voltage level being determined by the settings of three digital input pins (refer to **Table 5** for details). The regulated output voltage is available at the REG_{OUT} pin.

Table 5. Setting the Voltage Regulator Output

REG_SEL2	REG_SEL1	REG_SEL0	Regulated Output Voltage (V)
COM	COM	COM	1.8
COM	COM	DV_{DD}	2.5
COM	DV_{DD}	COM	3.0
COM	DV_{DD}	DV_{DD}	3.3

REG_SEL2	REG_SEL1	REG_SEL0	Regulated Output Voltage (V)
DV_{DD}	COM	COM	5
DV_{DD}	COM	DV_{DD}	9
DV_{DD}	DV_{DD}	COM	12

In addition, the REGOUT of TPC2221 also supports higher voltage output, and the relationship between its output levels and REG_SEL is shown as follows.

Table 6. Setting the Voltage Regulator Output(High-voltage output)

REG_SEL2	REG_SEL1	REG_SEL0	Regulated Output Voltage (V)
COM	COM	COM	1.8
COM	COM	DV_{DD}	2.5
COM	DV_{DD}	COM	3.0
COM	DV_{DD}	DV_{DD}	3.3
DV_{DD}	COM	COM	16
DV_{DD}	COM	DV_{DD}	18
DV_{DD}	DV_{DD}	COM	20

- The high-voltage output version needs to be confirmed with 3PEAK.

LOOP CURRENT SLEW RATE CONTROL

Control over the rate of loop current change can be achieved by connecting an external capacitor from the C_{IN} pin to COM. This connection serves to slow down the rate at which the loop current changes. The output resistance of the DAC (R_{DAC}), in conjunction with the C_{SLEW} capacitor, creates a time constant that regulates the loop current's response, as depicted in **Figure 44**.

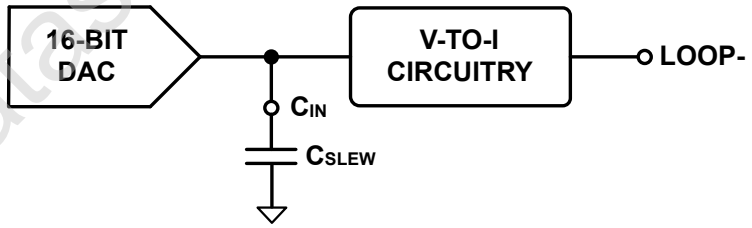


Figure 44. Slew Capacitor Circuit

The resistance of the DAC is typically 18 kΩ for the 4 mA to 20 mA , 3.8 mA to 21 mA and 3.2 mA to 24 mA loop current ranges. The time constant of the circuit is expressed as

$$\tau = R_{DAC} \times C_{SLEW} \quad (3)$$

Taking five time constants as the required time to reach the final value, C_{SLEW} can be determined for a desired response time, t, as follows:

$$C_{SLEW} = \frac{t}{5 \times R_{DAC}} \quad (4)$$

where:*t* is the desired time for the output current to reach its final value. R_{DAC} is the resistance of the DAC core, 18 kΩ, depending on the selected loop current range.The responses for both of these configurations are shown in **Figure 45**.

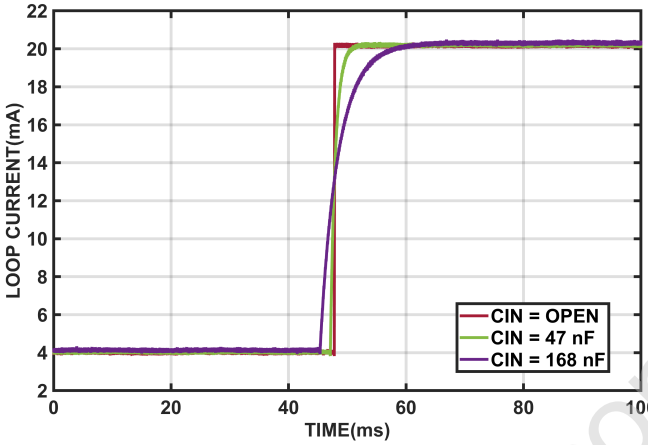


Figure 45. 4 mA to 20 mA Step with Slew Rate Control

The C_{IN} pin has the dual functionality of serving as a coupling input for HART FSK signaling, in addition to its role in controlling the loop current. It is essential that the HART signal is AC-coupled to the C_{IN} input. When calculating the total capacitance that affects the circuit, the capacitor used for coupling the HART signal must be included, resulting in a total capacitance of C_{SLEW}+ C_{HART}. For further details, refer to the section dedicated to HART Communications.

POWER-ON DEFAULT

Upon powering up, the TPC2221 initializes with all registers set to their default values and the loop current configured to an alarm state of either 3.2 mA or 22.8 mA/24 mA, depending on the ALARM_CURRENT_DIRECTION pin's state and the selected range. The device maintains this state until new programming values are input. The SPI watchdog timer is activated by default with a 1-second timeout duration. If communication with the TPC2221 ceases for 1 second after power-on, the FAULT pin is triggered.

Table 7. Power On Loop Currents for all Output Current Ranges

Range	ALARM_CURRENT_ DIRECTION	Power-On Loop Current (mA)
4 mA to 20 mA	COM	3.2
4 mA to 20 mA	DV_{DD}	22.8
3.8 mA to 21 mA	COM	3.2
3.8 mA to 21 mA	DV_{DD}	22.8
3.2 mA to 24 mA	COM	3.2
3.2 mA to 24 mA	DV_{DD}	24

HART COMMUNICATIONS

The TPC2221 can be interfaced to a HART modem to enable HART digital communications over the 2-wire loop connection.**Figure 46** shows how the modem frequency shift keying (FSK) output is connected to the TPC2221.

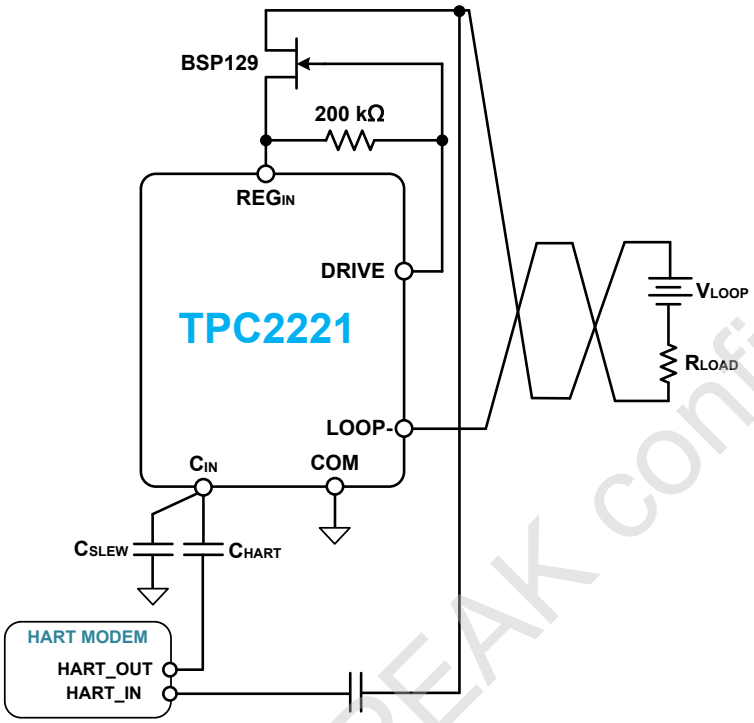


Figure 46. Connecting a HART Modem to the TPC2221

To achieve a 1 mA p-p FSK current signal on the loop, the voltage at the C_{IN} pin must be 111 mV p-p. Assuming a 500 mV p-p output from the HART modem, this means that the signal must be attenuated by a factor of 4.5. The following equation can be used to calculate the values of the C_{HART} and C_{SLEW} capacitors:

$$4.5 = \frac{C_{HART} + C_{SLEW}}{C_{HART}} \quad (5)$$

From this equation, the ratio of C_{HART} to C_{SLEW} is 1 to 3.5. This ratio of the capacitor values sets the amplitude of the HART FSK signal on the loop. The absolute values of the capacitors set the response time of the loop current, as well as the bandwidth presented to the HART signal connected at the CIN pin. The bandwidth must pass frequencies from 500 Hz to 10 kHz. The two capacitors and the internal impedance, R_{DAC}, form a high-pass filter. The 3 dB frequency of this high-pass filter should be less than 500 Hz and can be calculated as follows:

$$f_{3dB} = \frac{1}{2 \times \pi \times R_{DAC} \times (C_{SLEW} + C_{HART})} \quad (6)$$

To achieve a 500 Hz, high-pass, 3 dB frequency cutoff, the combined values of C_{HART} and C_{SLEW} should be 21 nF. To ensure the correct HART signal amplitude on the current loop, the final values for the capacitors are C_{HART} = 4.7 nF and C_{SLEW} = 16.3 nF.

SERIAL INTERFACE

The TPC2221 is governed by a flexible, 3-wire serial interface capable of operating at clock speeds up to 30 MHz. This interface is compatible with SPI, QSPI™, MICROWIRE®, and DSP protocols. As shown in **Figure 2**, the timing diagram illustrates the interface's operation, which can handle both continuous and noncontinuous gated burst clocks.The writing process initiates with a falling edge of the SYNC signal, with data being input on the SDIN line on the falling edge of SCLK. When the SYNC signal rises, the 24 bits of data are captured; this data is then routed to the designated register, and the specified function is carried out (either adjusting the DAC output or changing the operational mode).Should packet error checking be necessary on the SPI interface via cyclic redundancy codes, an additional eight bits must be transmitted to the TPC2221, extending the serial interface to 32 bits. In such cases, 32 bits are sent to the TPC2221 before the SYNC signal is raised high.

INPUT SHIFT REGISTER

The input shift register has a width of 24 bits, which expands to 32 bits if CRC error checking for the data is necessary. Data is loaded into the device in a MSB-first format as a 24- or 32-bit word, controlled by the serial clock input, SCLK. This input shift register is composed of an 8-bit address/command byte, a 16-bit data word, and an optional 8-bit CRC, as detailed in**Tables 8** and**9.**The decoding of the address/command byte is outlined in **Table 7**.

Table 8. TPC2221 Address/Command Byte Functions

Address/Command Byte	Function
00000001	Write to DAC register
00000010	Write to control register
00000011	Write to offset adjust register
00000100	Write to gain adjust register
00000101	Load DAC
00000110	Force alarm current
00000111	Reset (it is recommended to wait **50 µs** after a device reset before writing the next command)
00001000	Initiate VLOOP/temperature measurement
00001001	No operation
10000001	Read DAC register
10000010	Read control register
10000011	Read offset adjust register
10000100	Read gain adjust register
10000101	Read fault register

The 16 bits of the data-word written following a load DAC, force alarm current, reset, initiate V_{LOOP}/temperature measurement, or no operation command byte are don't cares (see **Table 8** and **Table 9**).

REGISTER READBACK

To read back a register, Bit D11 of the control register must be set to Logic 1 to disable the automatic readback of the fault register. The 16 bits of the data-word written following a read command are don't cares (see **Table 8** and **Table 9**). The register data addressed by the read command is clocked out of SDO on the subsequent write command (see **Figure 3**).

Table 9. Input Shift Register

MSB **LSB**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Address/command byte								Data-word															

Table 10. Input Shift Register with CRC

MSB **LSB**

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Address/command byte								Data-word																CRC							

DAC REGISTER

The DAC register is a read/write register and is addressed as described in **Table 7**. The data programmed to the DAC register determines the loop current, as shown in the Ideal Output Transfer Function section and in**Table 10**.

Table 11. DAC Register Bit Map

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16-bit Data															

Ideal Output Transfer Function

The transfer function describing the relationship between the data programmed to the DAC register and the loop current is expressed by the following three equations.For the 4 mA to 20 mA output range, the loop current can be expressed as follows:

$$I_{LOOP} = \left(\frac{16\ mA}{2^{16}}\right) \times D + 4mA \quad (7)$$

For the 3.8 mA to 21 mA output range, the loop current can be expressed as follows:

$$I_{LOOP} = \left(\frac{17.2mA}{2^{16}}\right) \times D + 3.8mA \quad (8)$$

For the 3.2 mA to 24 mA output range, the loop current can be expressed as follows:

$$I_{LOOP} = \left(\frac{20.8\ mA}{2^{16}}\right) \times D + 3.2\ mA \quad (9)$$

Table 12. Relationship of DAC Register Code to Ideal Loop Current (Gain = 65,536; Offset = 0)

DAC Register Code	Ideal Loop Current (mA)		
-	4 mA to 20 mA Range	3.8 mA to 21 mA Range	3.2 mA to 24 mA Range
0x0000	4	3.8	3.2
0x0001	4.00024	3.80026	3.2003
…	…	…	…
0x7FFF	11.9997	12.39974	13.5997
0x8000	12	12.4	13.6
…	…	…	…
0xFFFE	19.9995	20.99947	23.9994
0xFFFF	19.9997	20.99974	23.9997

CONTROL REGISTER

The control register, which is accessible for both reading and writing, is referenced according to the details provided in **Table 12**. The data set in the control register dictate the operational mode of the TPC2221.

Table 13. Control Register Bit Map

D15:D13			D12	D11	D10	D9	D8	D7	D6	D5	D4:D0
SPI watchdog timeout			SPI watchdog timer	Auto fault readback	Alarm on SPI fault	Set min loop current	Select ADC input	On-chip ADC	Power down internal reference	V_{LOOP} fault alert	Reserved
T0	T1	T2									

Table 14. Control Register Bit Descriptions

Control Bits	Description
SPI watchdog timeout	The T0, T1, and T2 bits allow the user to program the watchdog timeout period. The watchdog timer is reset when a valid write to any TPC2221 register occurs or when a NOP command is written.

T0	T1	T2	Timeout Period
0	0	0	50 ms
0	0	1	100 ms
0	1	0	500 ms
0	1	1	1 sec(default)
1	0	0	2 sec
1	0	1	3 sec
1	1	0	4 sec
1	1	1	5 sec

SPI watchdog timer	0 = SPI watchdog timer is enabled (default). 1 = SPI watchdog timer is disabled.
Auto fault readback	This bit specifies whether the fault register contents are automatically clocked out on the SDO pin on each write operation. (The fault register can always be addressed for readback.) 0 = fault register contents are clocked out on the SDO pin (default). 1 = fault register contents are not clocked out on the SDO pin.
Alarm on SPI fault	This bit specifies whether the loop current is forced to the alarm value when an SPI fault is detected (that is, the watchdog timer times out). When an SPI fault is detected, the SPI fault bit of the fault register and the FAULT pin are always set.
Set min loop current	0 = normal operation (default). 1 = loop current is set to its minimum value so that the total current flowing in the loop consists only of the operating current of the TPC2221 and its associated circuitry.
Select ADC input	0 = on-chip ADC measures the voltage between the V_{LOOP} and COM pins (default). 1 = on-chip ADC measures the temperature of the TPC2221 die.
On-chip ADC	0 = on-chip ADC is disabled (default). 1 = on-chip ADC is enabled.
Power down internal reference	0 = internal voltage reference is powered up (default). 1 = internal voltage reference is powered down and an external voltage reference source is required
V_{LOOP} fault alert	This bit specifies whether the FAULT pin is set when the voltage between the V_{LOOP} and COM pins falls to approximately 0.3 V. (The V_{LOOP} 6V bit of the fault register is always set.) 0 = FAULT pin is not set when the V_{LOOP} − COM voltage falls to approximately 0.3 V. 1 = FAULT pin is set when the V_{LOOP} − COM voltage falls to approximately 0.3 V.

FAULT REGISTER

The read-only fault register is addressed as described in **Table 14**. The bits in the fault register indicate a range of possible fault conditions.

Table 15. Fault Register Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7:D0
SPI	PEC	I_{LOOP} Over	I_{LOOP} Under	Temp 140°C	Temp 100°C	V_{LOOP} 6V	V_{LOOP} 12V	V_{LOOP}/temperature value

Table 16. Fault Register Bit Descriptions

Fault Alert	FAULT Pin Set	Description
SPI	Yes	This bit is set high to indicate the loss of the SPI interface signaling. This fault occurs if there is no valid communication to the TPC2221 over the SPI interface for more than the user-defined timeout period. The occurrence of this fault also forces the loop current to the alarm value if Bit D10 of the control register is at Logic 0. The alarm current direction is determined by the state of the ALARM_CURRENT_DIRECTION pin.
PEC (packet error check)	Yes	This bit is set high when an error in the SPI communication is detected using cyclic redundancy check (CRC) error detection. See the Packet Error Checking section for more information.
I_{LOOP} Over	Yes	This bit is set high when the actual loop current is greater than the programmed loop current.
I_{LOOP} Under	Yes	This bit is set high when the actual loop current is less than the programmed loop current.
Temp 140°C	Yes	This bit is set high to indicate an overtemperature fault. This bit is set if the die temperature of the TPC2221 exceeds approximately 140°C. This bit is cleared when the temperature returns below approximately 125°C.
Temp 100°C	No	This bit is set high to indicate an increasing temperature of the TPC2221. This bit is set if the die temperature of the TPC2221 exceeds approximately 100°C. This bit is cleared when the temperature returns below approximately 85°C.
V_{LOOP} 6V	Yes	This bit is set high when the voltage between the V_{LOOP} and COM pins falls below approximately 0.3 V (representing a 6 V loop supply voltage with 20:1 resistor divider connected at V_{LOOP}). This bit is cleared when the voltage returns above approximately 0.4 V.
V_{LOOP} 12V	No	This bit is set high when the voltage between the V_{LOOP} and COM pins falls below approximately 0.6 V (representing a 12 V loop supply voltage with 20:1 resistor divider connected at V_{LOOP}). This bit is cleared when the voltage returns above approximately 0.7 V.

<table>
<tr><th>Fault Alert</th><th>FAULT Pin Set</th><th>Description</th></tr>
<tr><td>V_{LOOP}/temperature value</td><td>N/A</td><td>These eight bits represent either the voltage between the V_{LOOP} and COM pins or the TPC2221 die temperature, depending on the setting of Bit D8 of the control register (see the On-Chip ADC Transfer Function Equations section).
<table>
<tr><th>8-Bit Value</th><th>V_{LOOP} − COM Voltage (V)</th><th>Die Temperature (°C)</th></tr>
<tr><td>00000000</td><td>0</td><td>300</td></tr>
<tr><td>...</td><td>…</td><td>...</td></tr>
<tr><td>11111111</td><td>2.49</td><td>-74</td></tr>
</table></td></tr>
</table>

On-Chip ADC Transfer Function Equations

The equation for the transfer function that measures the voltage across the V_{LOOP} and COM pins is as below:

$$V_{LOOP-COM} = (2.5 \div 256) \times D \quad (10)$$

where D is the 8-bit digital code returned by the on-chip ADC.

The transfer function equation for the die temperature is as follows:

$$\text{Die Temperature} = (-1.4686 \times D) + 300 \quad (11)$$

where D is the 8-bit digital code returned by the on-chip ADC.

OFFSET ADJUST REGISTER

The offset adjust register is a read/write register and is addressed as described in **Table 16**. A write command to the offset register must be followed by a write to the data register for the contents of the offset register to take effect.

Table 17. Offset Adjust Register Bit Map

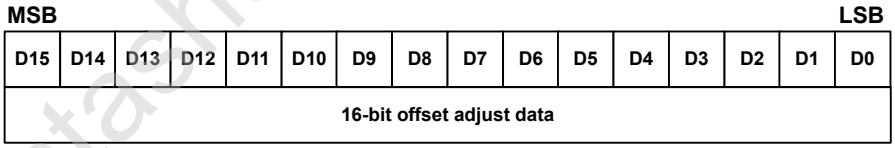


Table 18. Offset Adjust Register Adjustment Range

Offset Adjust Register Data	Digital Offset Adjustment (LSBs)
65535	+32767
65534	+32766
…	…
32769	+1
32768 (default)	0
32767	-1
…	…
1	−32767
0	−32768

GAIN ADJUST REGISTER

The gain adjust register is a read/write register and is addressed as described in **Table 18**. A write command to the gain register must be followed by a write to the data register for the contents of the gain register to take effect

Table 19. Gain Adjust Register Bit Map

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16-bit gain adjust data															

Table 20. Gain Adjust Register Adjustment Range

Gain Adjust Register Data	Digital Gain Adjustment at Full-Scale Output (LSBs)
65535 (default)	0
65534	-1
…	…
32769	-32767
32768	-32768
32767	-32769
…	…
1	−65534
0	−65535

Transfer Function Equations with Offset and Gain Adjust Values

When the offset adjust and gain adjust register values are taken into account, the transfer equations can be expressed as follows. For the 4 mA to 20 mA output range, the loop current can be expressed as follows:

$$I_{LOOP} = \left[\frac{\frac{16mA}{2^{16}} \times Gain}{2^{16}} \times D\right] + \left(4mA + \left[\left(\frac{16mA}{2^{16}}\right) \times (Offest - 32768)\right]\right) \quad (12)$$

For the 3.8 mA to 21 mA output range, the loop current can be expressed as follows:

$$I_{LOOP} = \left[\frac{\frac{17.2mA}{2^{16}} \times Gain}{2^{16}} \times D\right] + \left(3.8mA + \left[\left(\frac{17.2mA}{2^{16}}\right) \times (Offest - 32768)\right]\right) \quad (13)$$

For the 3.2 mA to 24 mA output range, the loop current can be expressed as follows:

$$I_{LOOP} = \left[\frac{\frac{20.8mA}{2^{16}} \times Gain}{2^{16}} \times D\right] + \left(3.2mA + \left[\left(\frac{20.8mA}{2^{16}}\right) \times (Offest - 32768)\right]\right) \quad (14)$$

where: D is the decimal value of the DAC register.

Gain is the decimal value of the gain adjust register.

Offset is the decimal value of the offset adjust register.

Note that the offset adjust register cannot adjust the zero-scale output value downward.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPC2221 is a complete, loop-powered, 4 mA to 20 mA digital-to-analog converter (DAC) designed to meet the needs of smart transmitter manufacturers in the industrial control industry

Typical Application

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the TPC2221 is via a serial bus that uses a protocol compatible with microcontrollers and DSP processors. The communications channel is a 3-wire minimum interface consisting of a clock signal, a data signal, and a sync signal. The TPC2221 require a 24-bit data-word with data valid on the falling edge of SCLK. For all interfaces, the DAC output update is initiated on the falling edge of LDAC. The contents of the registers can be read using the readback function.

Application Diagram for HART Capable Smart Transmitter

Figure 47 shows a typical connection diagram for the TPC2221 in a HART-enabled smart transmitter setup. To minimize power consumption on the chip, a depletion mode MOSFET (T1), such as BSP129, may be incorporated between the loop voltage and the TPC2221 as depicted in**Figure 47**. If a low loop voltage is used, T1 can be bypassed, allowing the loop voltage to connect directly to REGIN (refer to **Figure 42**). In the configuration shown in **Figure 47**, all interface signal lines are linked to the microcontroller. To streamline the interface signal lines, the LDAC signal can be connected to COM, and the SDO and FAULT lines can be left open. However, this setup forfeits the fault alert capabilities. Under typical operating conditions, the voltage between COM and LOOP− stays below 1.5 V, with LOOP− being at a negative potential relative to COM. Should there be a risk of LOOP− being forced positive relative to COM, or if the voltage differential between LOOP− and COM could exceed 5 V, a 4.7 V low leakage Zener diode should be installed between COM and the LOOP− pin, as indicated in **Figure 47**, to safeguard the TPC2221 from potential damage. Furthermore, to enhance the TPC2221's stability in long-line applications, it is necessary to install a 100 nF capacitor at the port

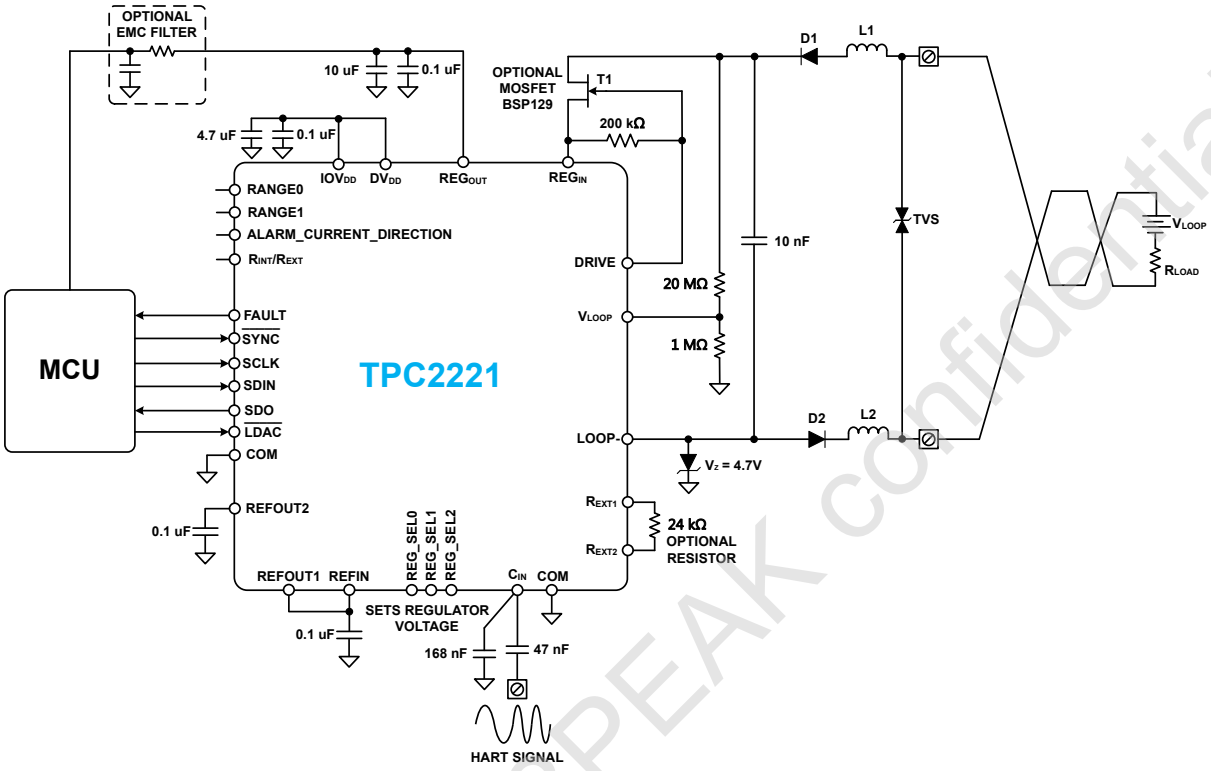


Figure 47. TPC2221 Application Diagram for HART Capable Smart Transmitter

DETERMINING THE EXPECTED TOTAL ERROR

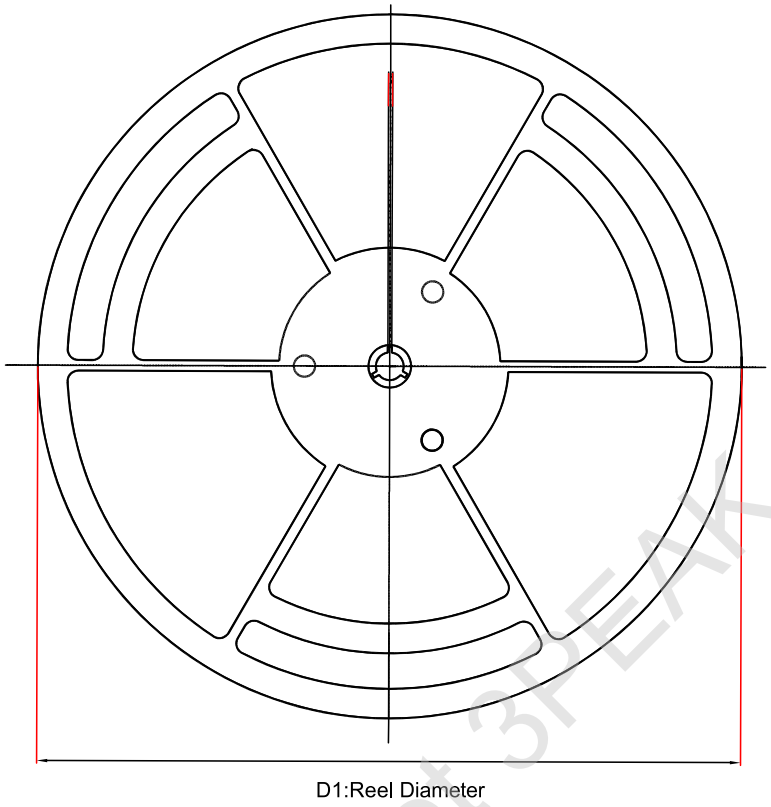
The TPC2221 offers various configuration options, each yielding different levels of precision as detailed in **Electrical Characteristics**. When operating with the internal voltage reference and internal R_{SET} resistor activated, the C grade device can anticipate a maximum total error of **0.157%** of the full-scale range across the temperature span of −40°C to +125°C. Alternative configurations may involve the use of an external voltage reference, an external R_{SET} resistor, or both. In such setups, the specifications are predicated on the assumption that the external voltage reference and R_{SET} resistor are perfect. Consequently, the errors related to these components must be added to the data sheet specifications to ascertain the overall system performance, which is contingent upon the quality of these external components.

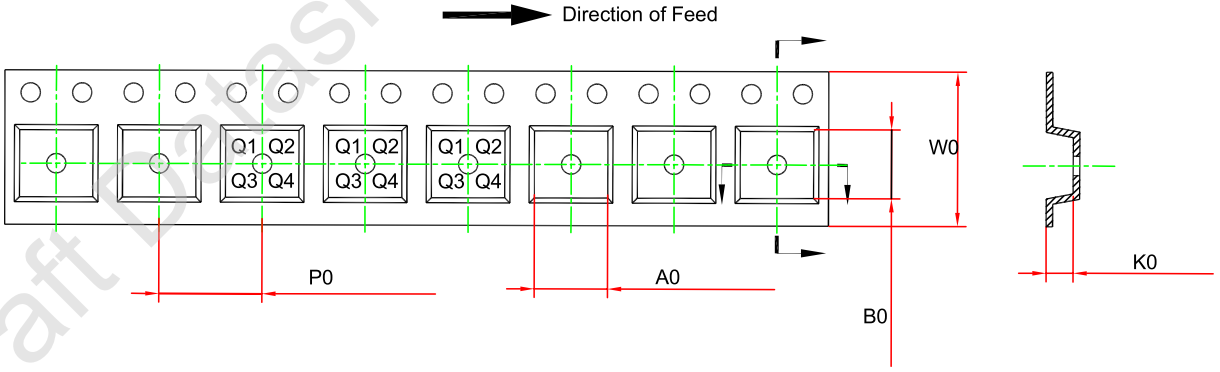
Layout

Layout Guideline

- In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance.
- Design the printed circuit board (PCB) on which the TPC2221 is mounted so that the analog and digital sections are separated and confined to certain areas of the board. If the TPC2221 is in a system where multiple devices require an analog ground-to-digital ground connection, make the connection at one point only. Establish the star ground point as close as possible to the device.
- For $IOV_{DD,}$ it is recommended to use a 4.7μF capacitor in parallel with a 100nF ceramic capacitor. For REG_{OUT}, it is recommended to use a 2.2μF capacitor in parallel with a 100nF ceramic capacitor. Both should be placed within a 3mm range of the chip's power pin
  The 0.1 μF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.
- The power supply lines of theTPC2221 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.
- Fast switching signals such as clocks should be shielded with a digital ground to avoid radiating noise to other parts of the board. Never run these near the reference inputs.
- A ground line routed between the SDIN and SCLK lines helps reduce crosstalk between them (this is not required on a multilayer board that has a separate ground plane, but separating the lines helps).
- It is essential to minimize noise on the REFIN line because it couples through to the DAC output.
- Avoid crossover of digital and analog signals. Traces on opposite sides of the PCB should run at right angles to each other. This reduces the effects of feed through the board.
- A microstrip technique is by far the best but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane, and signal traces are placed on the solder side.

Tape and Reel Information



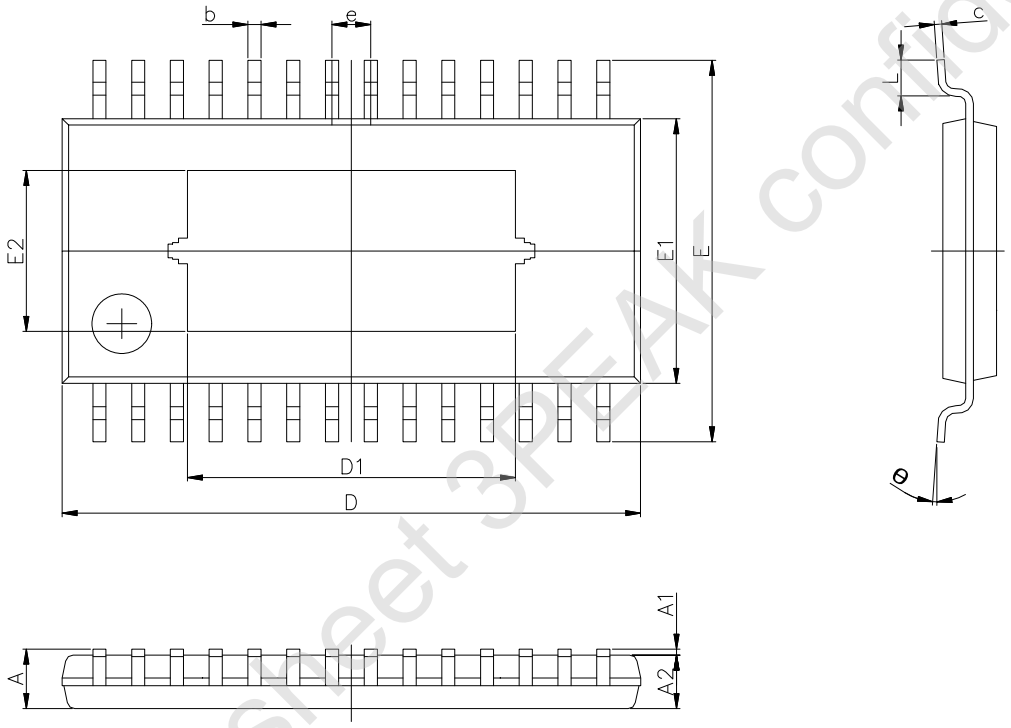


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPC2221	TSSOP28	330	17.6	6.8	5.5	1.5	8	12	Q1

Package Outline Dimensions

ETSSOP-28-D

Package Outline Dimensions TSC(ETSSOP-28-D)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	---	1.200	---	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	9.600	9.800	0.378	0.386
D1	3.510	3.760	0.138	0.148
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
E2	2.500	2.700	0.098	0.106
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0°	8°	0°	8°

NOTES
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPC2221-TSFR	−40 to 125°C	TSSOP28	2221	3	Tape and Reel, 4000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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