Single-Channel, 12-/16-Bit, Serial Input, 4 mA to 20 mA, Current Source DAC, HART Connectivity

Features

- TPC2211: 16-bit Resolution and Monotonicity
  TPC2210: 12-bit Resolution and Monotonicity
- Current Output Ranges: 4 mA to 20 mA, 0 mA to 20 mA, or 0 mA to 24 mA
  - Maximum ±0.06% FSR Total Unadjusted Error (TUE)
  - ±5.5 ppm FSR/°C Output Drift
- Flexible Serial Digital Interface
- On-chip Output Fault Detection
  - CRC Check
  - Watchdog Timer
  - Current Output Open Circuit Alarm or Compliance Voltage Violation
  - Over Temperature
- On-chip Reference: 4 ppm/°C
- Optional Regulated DV_{CC} Output
- Asynchronous Clear Function
- Power Supply Range
  - AV_{DD}: 10 V to 50 V
- Current Loop Compliance Voltage: AV_{DD} – 2 V
- Temperature Range: −40°C to +125°C
- ETSSOP24 and QFN6x6-40 Packages

Applications

- Industrial Automation
- Process Control
- PLC and DCS
- HART Network Connectivity

Description

The TPC2211/TPC2210 are low cost, precision, fully integrated 12-/ 16-bit converters offering a programmable current source output designed to meet the requirements of industrial process control applications. The output current range is programmable at 4 mA to 20 mA, 0 mA to 20 mA, or an overrange function of 0 mA to 24 mA. The output is open-circuit protected. The device operates with a power supply (AV_{DD}) range from 10.8 V to 50 V. Output loop compliance is 0 V to AV_{DD} − 2 V.

The flexible serial interface is SPI, MICROWIRE™, QSPI™, and DSP compatible and can be operated in 3-wire mode to minimize the digital isolation required in isolated applications.

The device also includes a power-on reset function, ensuring that the device powers up in a known state, and an asynchronous CLEAR pin that sets the output to the low end of the selected current range.

The total unadjusted error is typically ±0.01% FSR.

Typical Application Circuit

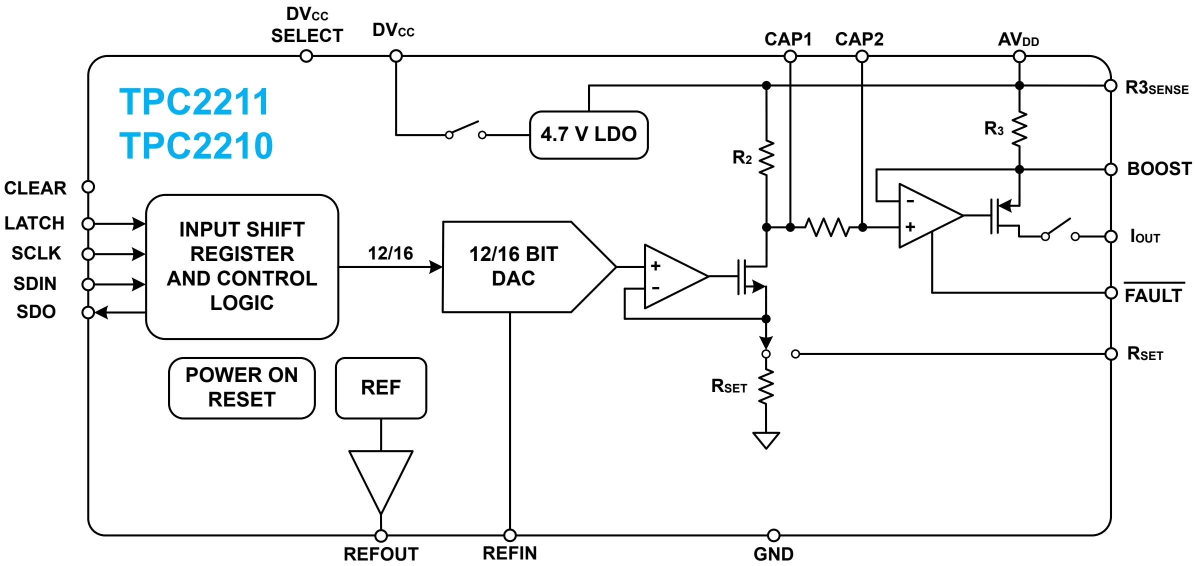


Table of Contents

Product Family Table

Order Number	Resolution	Output	Package
TPC2211-QFER (1)	16	Current	QFN6X6-40
TPC2210-QFER (1)	12	Current	QFN6X6-40
TPC2211-TSDR (1)	16	Current	ETSSOP24
TPC2210-TSDR	12	Current	ETSSOP24

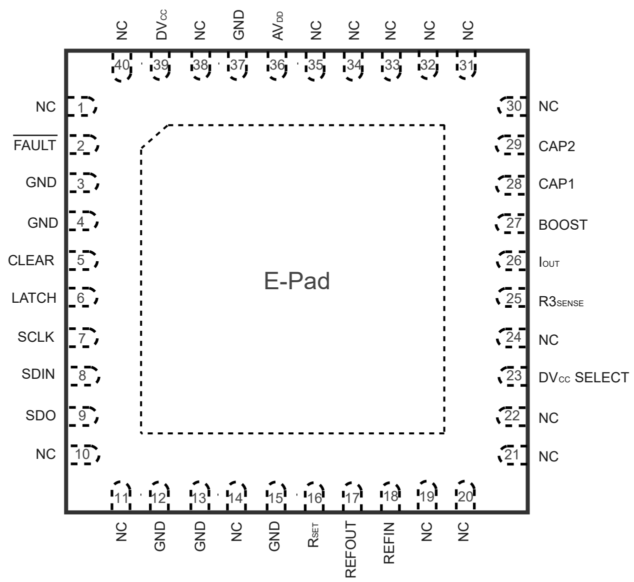
(1) For future products, contact the 3PEAK factory for more information and samples.

Revision History

Date	Revision	Notes
2025-12-11	Rev.A.0	Initial released version.

Pin Configuration and Functions

QFN6X6-40
Top View



ETSSOP24
Top View

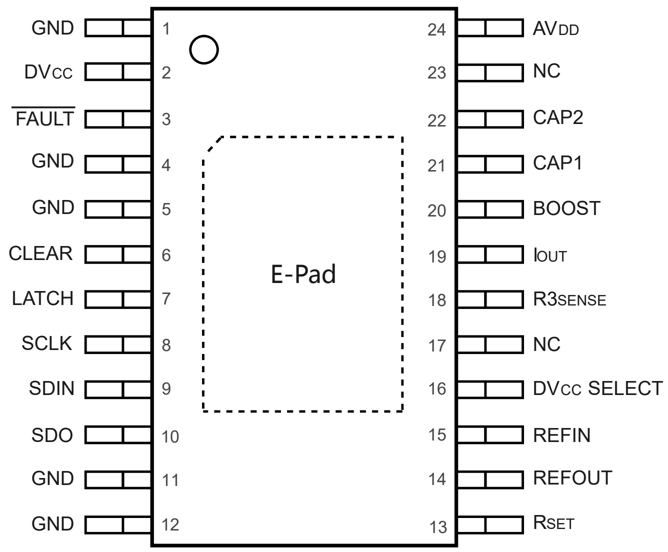


Table 1. Pin Function Descriptions

Pin No.		Pin Name	Description
ETSSOP	QFN		
1,4,5,11,12	3,4,12,13,15,37	GND	Ground Reference Pin. These pins must be connected to ground.
2	39	DV_{CC}	Digital Supply Pin. Voltage ranges from 2.7 V to 5.5 V. This pin can also be configured as a 4.7 V LDO output by leaving the DV_{CC} SELECT pin floating.
3	2	$\overline{FAULT}$	Fault Alert. This pin is asserted low when an open circuit is detected in current mode/an overtemperature/CRC/Watchdog Timer error is detected. Open drain output must be connected to a pull-up resistor.
6	5	CLEAR	Active High Input. Asserting this pin sets the current output to the bottom of the selected range or sets the voltage output to the user selected value (zero-scale or midscale).
7	6	LATCH	Positive Edge Sensitive Latch. A rising LATCH edge parallel loads the input shift register data into the DAC register, also updating the output.
8	7	SCLK	Serial Clock Input. Data is clocked into the shift register on the rising edge of SCLK. This operates at clock speeds of up to 30 MHz.
9	8	SDIN	Serial Data Input. Data must be valid on the rising edge of SCLK.
10	9	SDO	Serial Data Output. Used to clock data from the serial register in daisy-chain or readback mode. Data is valid on the rising edge of SCLK. Should be pulled up by resistors when using Daisy Chain mode.
13	16	R_{SET}	An external, precision, low drift 15 kΩ current setting resistor can be connected to this pin to improve the IOUT temperature drift performance.
14	17	REFOUT	Internal Reference Voltage Output. REFOUT = 5 V ± 5 mV.
15	18	REFIN	External Reference Voltage Input. Reference input range is 4 V to 5 V. REFIN = 5 V for a specified performance.
16	23	DV_{CC} SELECT	When connected to GND, this pin disables the internal supply, and an external supply must be connected to the DVCC pin. Leave this pin unconnected to enable the internal supply. In this case, it is recommended to connect a 0.1 µF capacitor between DVCC and GND.
17,23	1,10,11,14,19 to 22,24,30 to 35,38,40	NC	Do not connect to these pins
18	25	$R3_{SENSE}$	The voltage measured between this pin and the BOOST pin is directly proportional to the output current and can be used as a monitor/feedback feature. This should be used as a voltage sense output only; current should not be sourced from this pin.
19	26	I_{OUT}	Current Output Pin.

Pin No.		Pin Name	Description
ETSSOP	QFN		
20	27	BOOST	Optional External Transistor Connection. Connecting an external transistor reduces the power dissipated in the device.
21	28	CAP1	Connection for Optional Output Filtering Capacitor.
22	29	CAP2	Connection for Optional Output Filtering Capacitor.
24	36	AV_{DD}	Positive Analog Supply Pin. Voltage ranges from 10.8 V to 50 V.
-	-	E-pad	The exposed pad must be connected to the ground reference.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
	AV_{DD} to GND	−0.3	65	V
	DV_{CC} to GND	−0.3	6	V
	Digital Inputs to GND	−0.3	(DV_{CC} + 0.3 V) or 6 V (whichever is less)	V
	Digital Outputs to GND	−0.3	(DV_{CC} + 0.3 V) or 6 V (whichever is less)	V
	REFIN/REFOUT to GND	−0.3	6	V
	I_{OUT} to GND	−30	AV_{DD}	V
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_J	Junction Temperature (T_J max)		125	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Nom	Max	Unit
AV_{DD}		10		50	V
DV_{CC}, Internal Regulator Disabled		2.7		5.5	V
Reference Input Voltage		4.95		5.05	V
Loop Compliance Voltage (Output = 24 mA)				$AV_{DD} - 2$	V
VIH, Digital Input High Voltage		2			V
VIL, Digital Input Low Voltage	3.6 V < DV_{CC} < 5.5 V			0.8	V
	2.7 V < DV_{CC}< 3.6 V			0.6	V
Specified Performance Temperature		−40		125	°C

Thermal Information

Package Type	$R_{θJA}$	$R_{θJC(top)}$	Unit
ETSSOP24	27.4	23.8	°C/W
QFN6x6-40	25.55	17.35	°C/W

$R_{θJA}$:Junction-to-Ambient Thermal Resistance.

$R_{θJC(top)}$:Junction-to-Case (top) Thermal Resistance.

Electrical Characteristics

All test conditions: AV_{DD} = 10.8 V to 26.4 V, REFIN = 5 V external; DV_{CC} = 2.7 V to 5.5 V. I_{OUT}: R_{LOAD} = 350 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Unit
Current Output					
Output Current Ranges		0		24	mA
		0		20	mA
		4		20	mA
Accuracy(Internal R_{SET})					
Resolution	TPC2211	16			Bits
	TPC2210	12			Bits
TUE	T_A = −40°C to +125°C	−0.3		0.3	%FSR
	T_A = 25°C	−0.06	±0.01	0.06	%FSR
INL	INL is measured beginning from Code 256 for the TPC2211	−0.024		0.024	%FSR
	INL is measured beginning from Code 16 for the TPC2210	−0.032		0.032	%FSR
DNL	T_A = −40°C to +125°C, guaranteed monotonic	−1		1.5	LSB
Offset Error	T_A = −40°C to +125°C	−0.27		0.27	%FSR
	T_A = 25°C	−0.02	±0.01	0.02	%FSR
Offset Error TC	T_A = −40°C to +125°C		±2.5		ppm FSR/°C
Gain Error	T_A = −40°C to +125°C TPC2211	−0.23		0.23	%FSR
	T_A = 25°C TPC2211	−0.05	±0.01	0.05	%FSR
	T_A = −40°C to +125°C TPC2210	−0.23		0.23	%FSR
	T_A = 25°C TPC2210	−0.05	±0.01	0.05	%FSR
Gain TC	T_A = −40°C to +125°C		±18		ppm FSR/°C
Full-Scale Error	T_A = −40°C to +125°C	−0.25		0.25	%FSR
	T_A = 25°C	−0.06	±0.01	0.06	%FSR
Full-Scale TC	T_A = −40°C to +125°C		±20		ppm FSR/°C
Accuracy (External R_{SET})					
Resolution	TPC2211	16			Bits
	TPC2210	12			Bits
TUE	T_A = −40°C to +125°C	−0.15		0.15	%FSR
	T_A = 25°C	−0.06	±0.01	0.06	%FSR

Parameter	Test Conditions	Min	Typ	Max	Unit
INL	INL is measured beginning from Code 256 for the TPC2211	-0.012		0.012	%FSR
	INL is measured beginning from Code 16 for the TPC2210	-0.032		0.032	%FSR
DNL	T_A = −40°C to +125°C, guaranteed monotonic	-1		1.5	LSB
Offset Error	T_A = −40°C to +125°C	-0.1		0.1	%FSR
	T_A = 25°C	-0.03		0.03	%FSR
Offset Error TC	T_A = −40°C to +125°C		±2.5		ppm FSR/℃
Gain Error	T_A = −40°C to +125°C	-0.1		0.1	%FSR
	T_A = 25°C	-0.05		0.05	%FSR
Gain TC			±5.5		ppm FSR/°C
Full-Scale Error	T_A = −40°C to +125°C	-0.15		0.15	%FSR
	T_A = 25°C	-0.06		0.06	%FSR
Full-Scale Error TC	TA =-40°C to +125°C		±7		ppm FSR/°C
Output Characteristics					
Current Loop Compliance Voltage		0		AV_{DD}-2	V
Output Current Drift vs. Time	Internal RSET, Drift after 1000 hours, T_A = 125°C		50		ppm FSR
	External R_{SET} T_A = 25 °C, Drift after 1000 hours, T_A = 125°C		20		ppm FSR
Resistive Load				1500	Ω
Inductive Load			50		mH
DC PSRR			1		μA/V
Output Impedance			50		MΩ
Output Current Leakage When Output Disabled			2		nA
Reference Input/Output					
Reference Input					
Reference Input Voltage	For specified performance	4.95	5	5.05	V
DC Input Impedance			40		kΩ
Reference Output					
Output Voltage	T_A = 25°C	4.995	5	5.005	V
Reference TC			4	10	ppm/°C
Output Noise (0.1 Hz to 10 Hz)			11		μVp-p
Noise Spectral Density	At 10 kHz		300		nV/√Hz
Output Voltage Drift vs. Time	Drift after 1000 hours, T_A = 125°C		50		ppm
Capacitive Load			600		nF
Load Current			10		mA

Parameter	Test Conditions	Min	Typ	Max	Unit
Short-Circuit Current			20		mA
Load Regulation			95		ppm/mA
Digital Inputs					
Input High Voltage, VIH		2			V
Input Low Voltage, VIL				0.8	V
Input Current	Per pin	−1		1	µA
Pin Capacitance	Per pin		10		pF
Digital Outputs					
SDO					
Output Low Voltage, VOL	Sinking 200 µA			0.4	V
Output High Voltage, VOH	Sourcing 200 µA	DVCC−0.5			V
High Impedance Leakage Current		−1		1	µA
High Impedance Output Capacitance			5		pF
FAULT					
Output Low Voltage, VOL	10 kΩ pull-up resistor to DVCC			0.4	V
Output Low Voltage, VOL	At 2.5 mA		0.6		V
Output High Voltage, VOH	10 kΩ pull-up resistor to DVCC	3.6			V
Power Requirements					
DV_{CC}					
Input Voltage	Internal supply disabled	2.7		5.5	V
Output Voltage	DV_{CC} which can be overdriven up to 5.5 V		4.8		V
Output Load Current			10		mA
Short-Circuit Current			30		mA
Output Load Capacitor				1000	nF
AIDD	Outputs unloaded				
	Outputs disabled		1.2	1.8	mA
	Current output enabled		1.8	2.7	mA
DICC	VIH = DV_{CC}, VIL = GND			1	mA
Power Dissipation	AV_{DD} = 50 V, outputs unloaded		120		mW

All test conditions: AV = 10.8 V to 26.4 V,GND = 0 V, REFIN = 5 V external; DV_{CC} = 2.7 V to 5.5 V. I_{OUT}: R_{LOAD} = 350 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2. AC Performance Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Output Current Settling Time	16 mA step to 0.1% FSR		8		μs
	16 mA step to 0.1% FSR, L = 1 mH		14		μs
AC PSRR	200 mV 50 Hz/60 Hz sine wave superimposed on power supply voltage		−70		dB

Timing Requirements

All test conditions: AV_{DD} = 10.8 V to 26.4 V, GND = 0 V, REFIN = 5 V external; DV_{CC} = 2.7 V to 5.5 V. I_{OUT}: R_{LOAD} = 350 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3. Timing Characteristics

Parameter (1) (2) (3)		Min	Typ	Max	Unit
Write Mode					
t_1	SCLK cycle time	33			ns
t_2	SCLK low time	13			ns
t_3	SCLK high time	13			ns
t_4	LATCH delay time	14			ns
t_5	LATCH high time	5			μs
t_6	Data setup time	5			ns
t_7	Data hold time	5			ns
t_8	LATCH low time	40			ns
t_9	CLEAR pulse width	20			ns
t_{10}	CLEAR activation time			5	μs
Readback Mode					
t_{11}	SCLK cycle time	90			ns
t_{12}	SCLK low time	40			ns
t_{13}	SCLK high time	40			ns
t_{14}	LATCH delay time	13			ns
t_{15}	LATCH high time	40			ns
t_{16}	Data setup time	5			ns
t_{17}	Data hold time	5			ns
t_{18}	LATCH low time	40			ns
t_{19}	Serial output delay time ($C_{L\ SDO}$[4] = 15 pF)			35	ns
t_{20}	LATCH rising edge to SDO tristate ($C_{L\ SDO}$[4]= 15 pF)			35	ns
Daisy-Chain Mode					
t_{21}	SCLK cycle time	90			ns
t_{22}	SCLK low time	40			ns
t_{23}	SCLK high time	40			ns
t_{24}	LATCH delay time	13			ns
t_{25}	LATCH high time	40			uS
t_{26}	Data setup time	5			ns
t_{27}	Data hold time	5			ns
t_{28}	LATCH low time	40			ns
t_{29}	Serial output delay time ($C_{L\ SDO}$[4] = 15 pF)			35	ns

(1) Guaranteed by characterization; not production tested.
(2) All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of DVCC) and timed from a voltage level of 1.2 V.
(3) $C_{L\ SDO}$ = capacitive load on SDO output.

Timing Diagrams

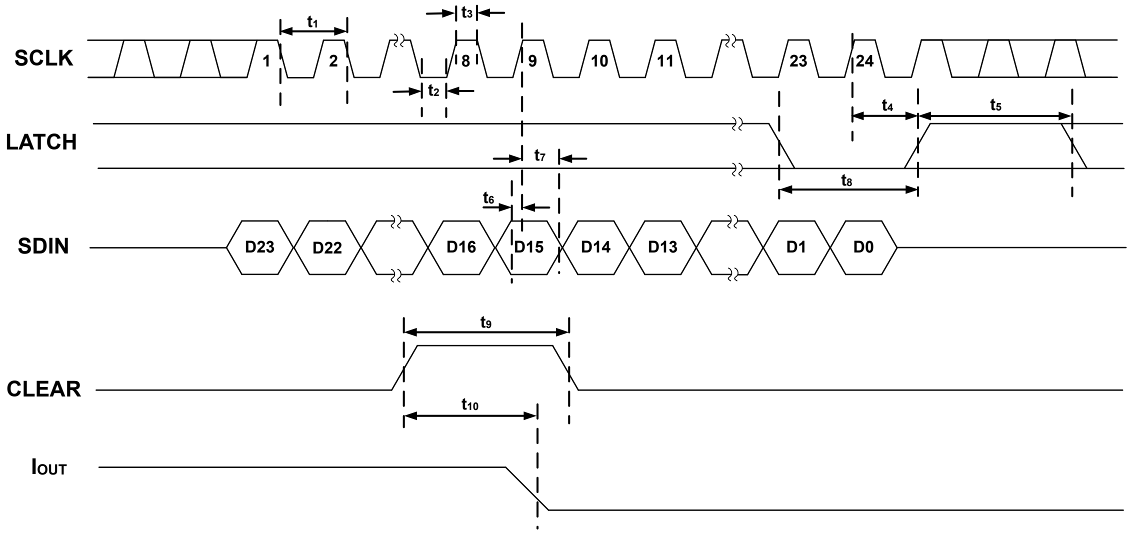


Figure 1. Write Mode Timing Diagram

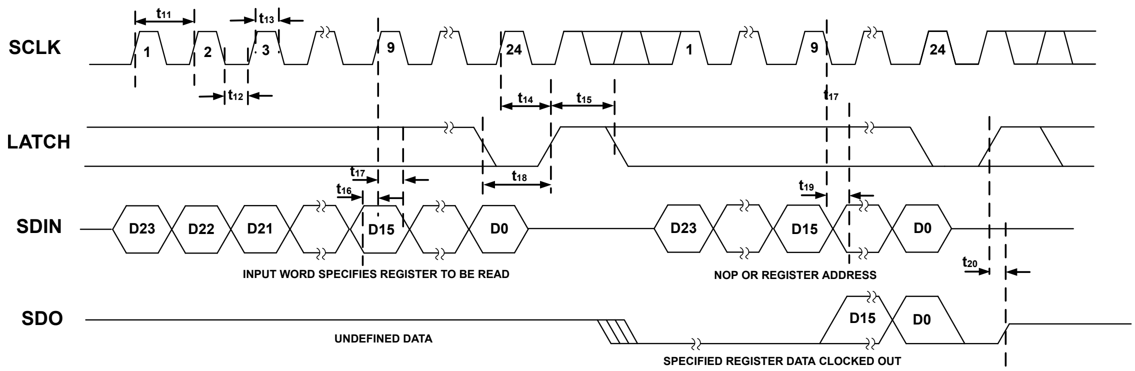


Figure 2. Readback Mode Timing Diagram

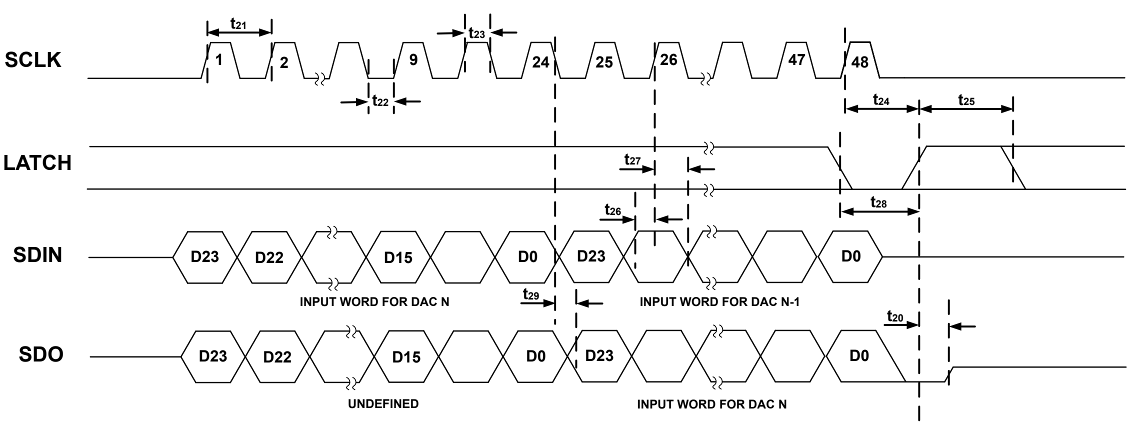


Figure 3. Daisy-Chain Mode Timing Diagram

Typical Performance Characteristics

General

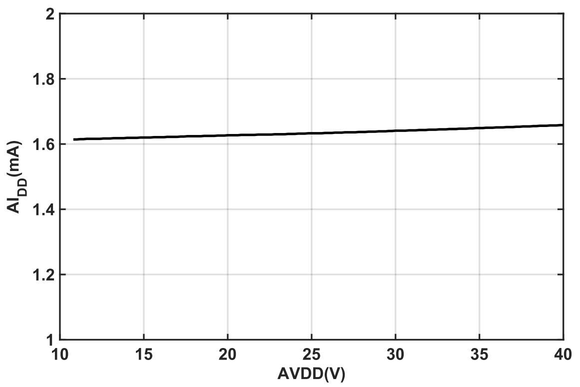


Figure 4. AI_{DD} vs. AV_{DD}

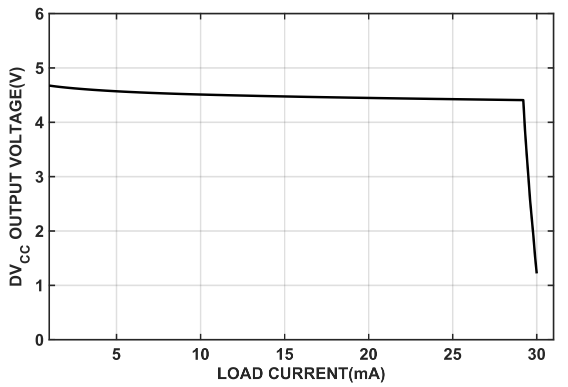


Figure 5. DVCC Output Voltage vs. Load Current

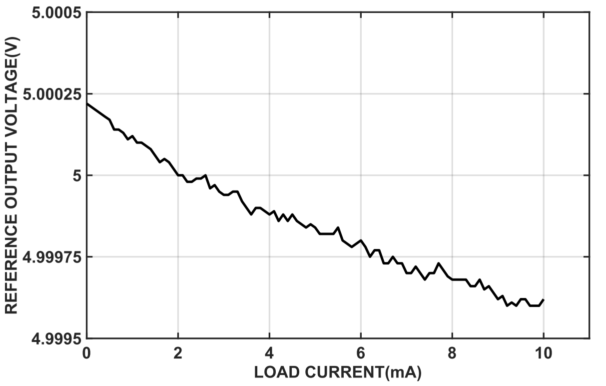


Figure 6. Reference Voltage vs. Load Current

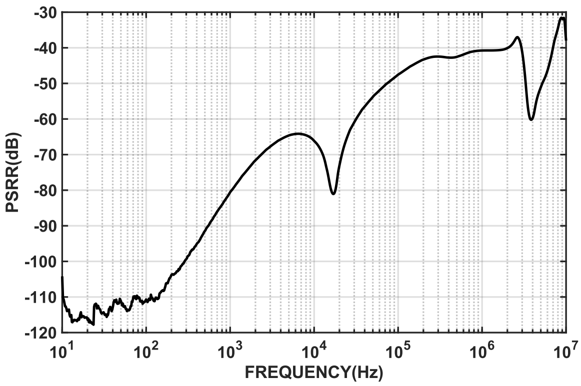


Figure 7. Reference PSRR

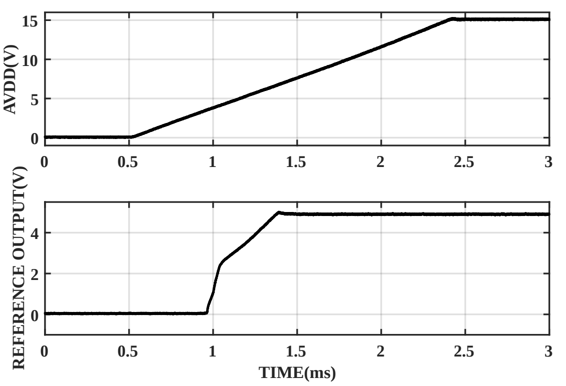


Figure 8. Reference Turn-on Transient

Current Output

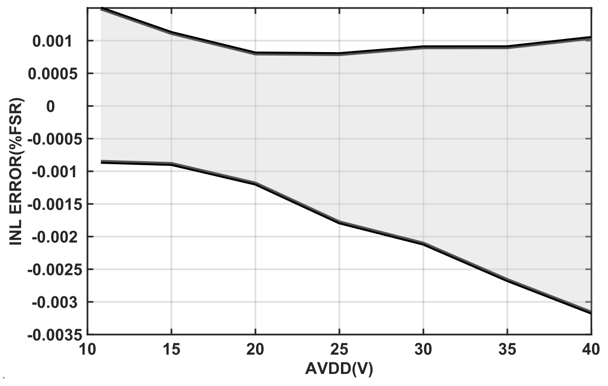


Figure 9. INL vs. AV_{DD}, External R_{SET}

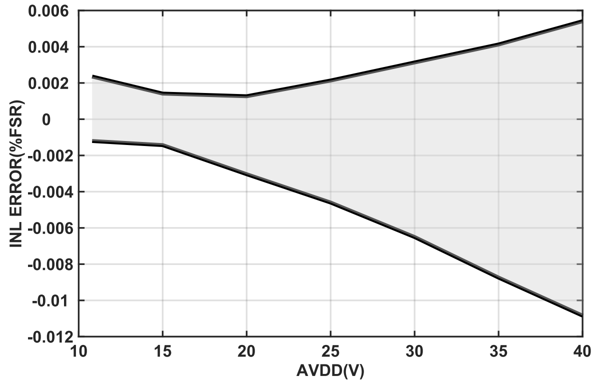


Figure 10. INL vs. AV_{DD}, Internal R_{SET}

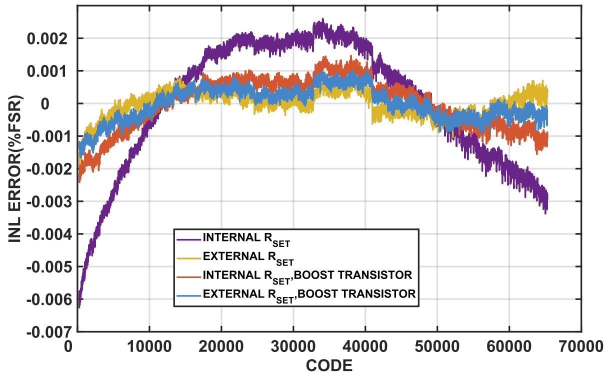


Figure 11. INL vs. Code (24mA Range)

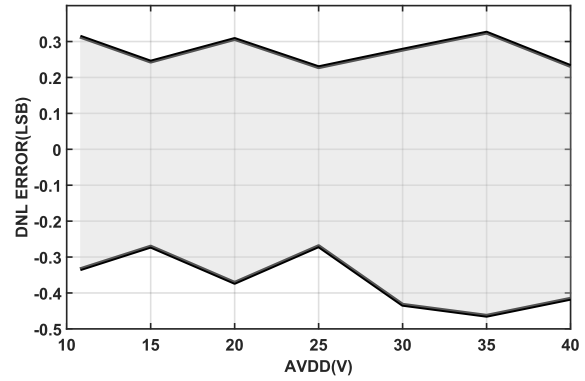


Figure 12. DNL vs. AV_{DD}, External R_{SET}

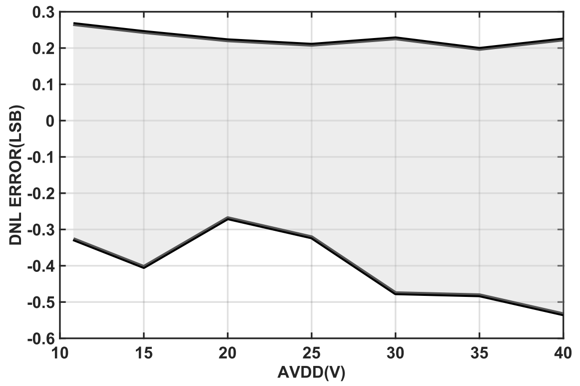


Figure 13. DNL vs. AV_{DD}, Internal R_{SET}

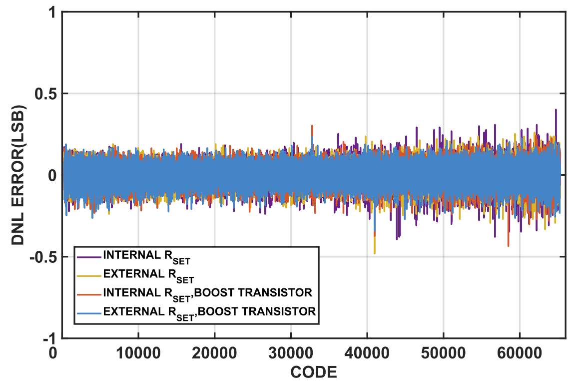


Figure 14. DNL vs. Code (24-mA Range)

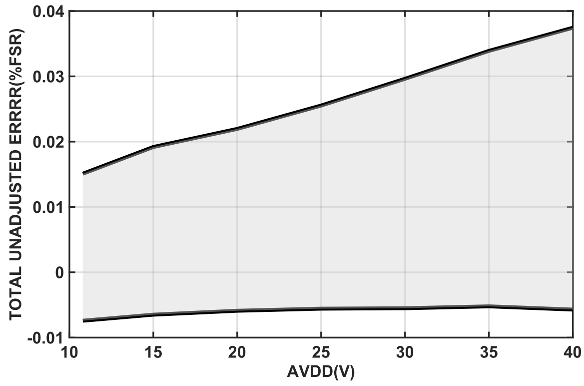


Figure 15. TUE vs. AV_{DD}, External R_{SET}

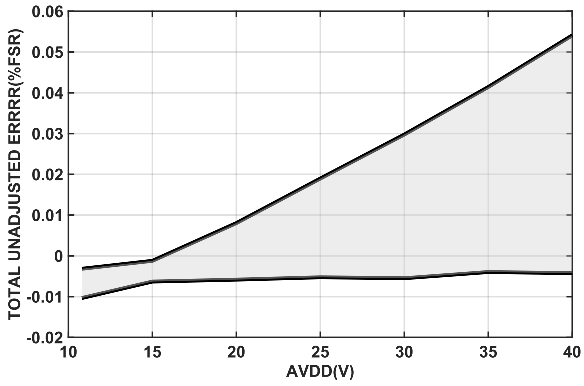


Figure 16. TUE vs. AV_{DD}, Internal R_{SET}

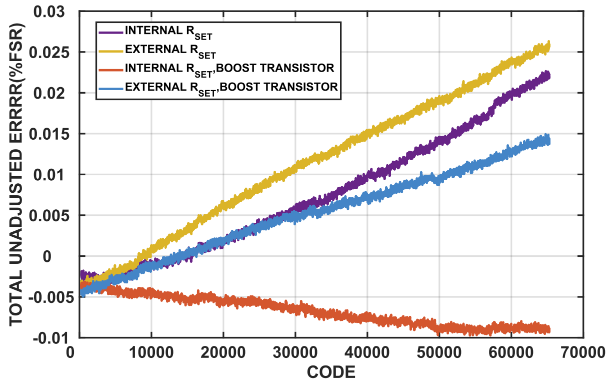


Figure 17. TUE vs. Code (24-mA Range)

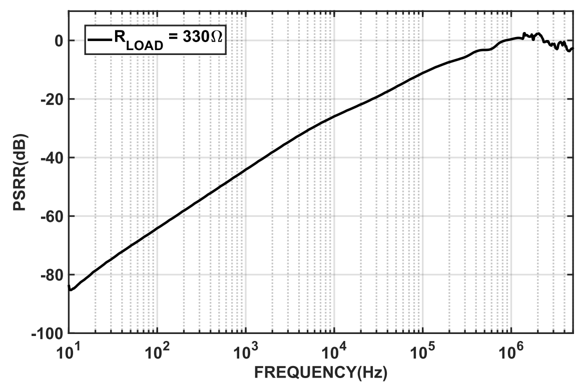


Figure 18. Output Current PSRR

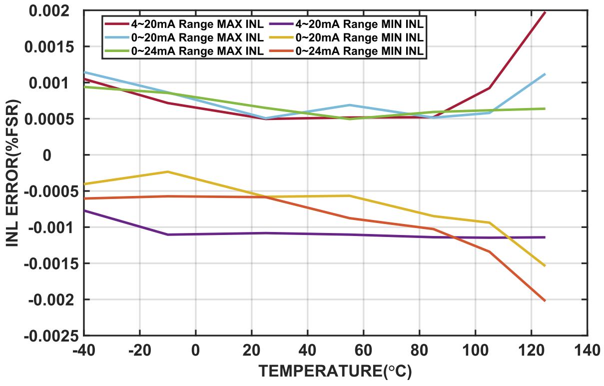


Figure 19. INL vs. Temperature, External R_{SET}

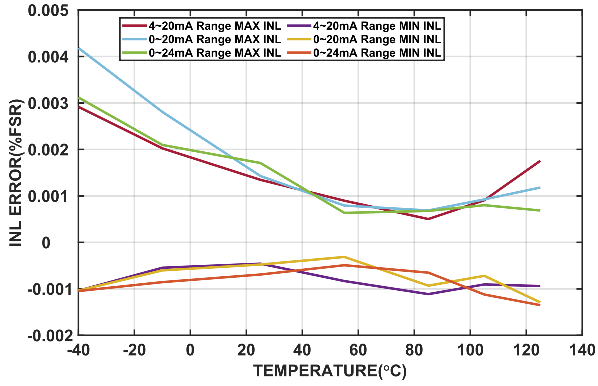


Figure 20. INL vs. Temperature, Internal R_{SET}

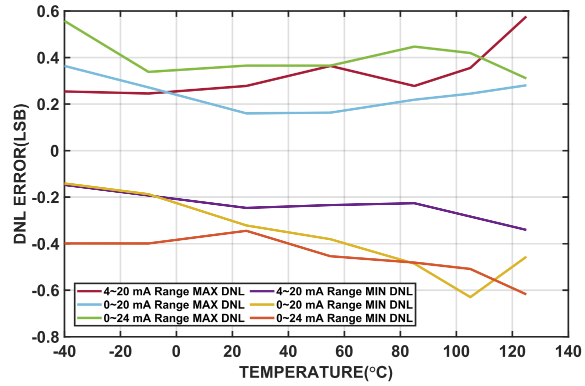


Figure 21. DNL vs. Temperature, External R_{SET}

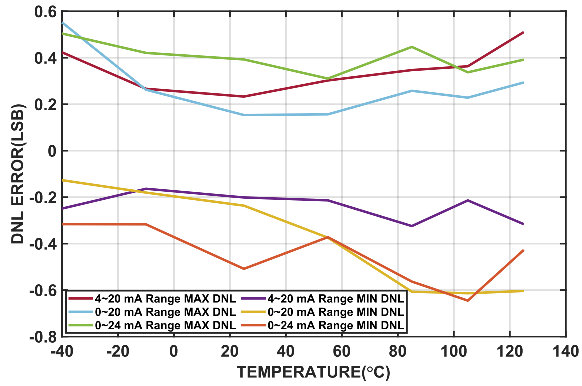


Figure 22. DNL vs. Temperature, Internal R_{SET}

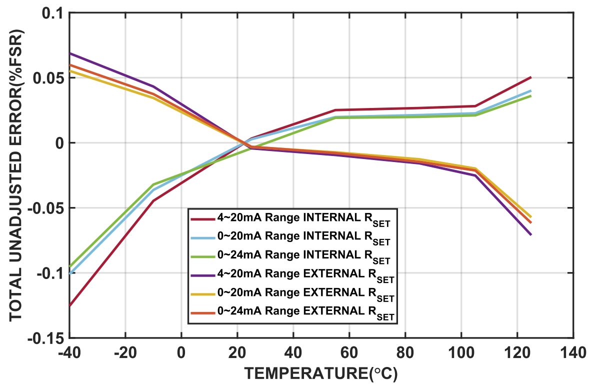


Figure 23. TUE vs. Temperature

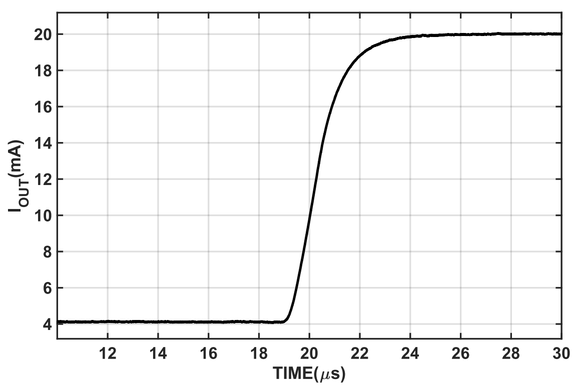


Figure 24. 4-mA to 20-mA Output Current Step - Positive

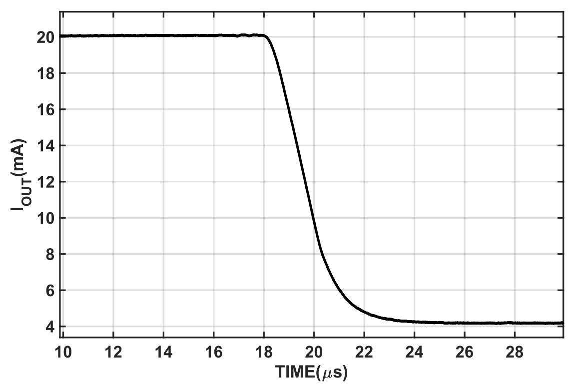


Figure 25. 4-mA to 20-mA Output Current Step - Negative

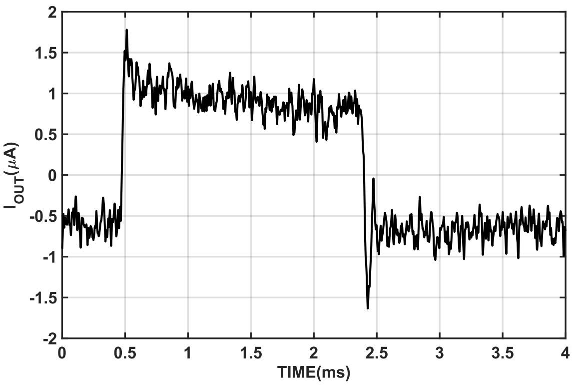


Figure 26. Output Current vs. Time on Power-Up

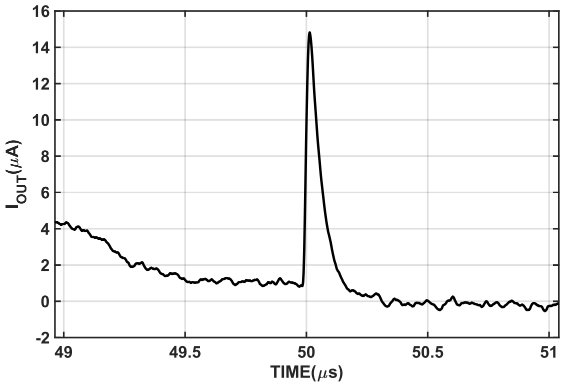


Figure 27. Output Current vs. Time on Output Enable

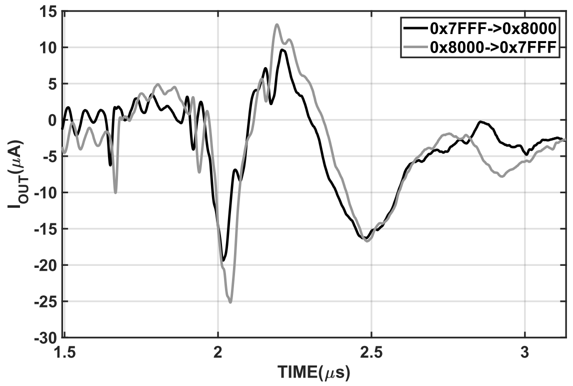


Figure 28. Digital to Analog Glitch

Detailed Description

Overview

The TPC2211 and the TPC2210 are high-precision, cost-effective digital-to-analog converters that offer a fully integrated, single-chip solution for industrial process control applications. These converters are capable of generating current loop with exceptional precision. The available current ranges for these converters are 0 mA to 20 mA, 0 mA to 24 mA, and 4 mA to 20 mA. The user can select the desired output configuration through the control register, providing flexibility in the application setup.

Functional Block Diagram

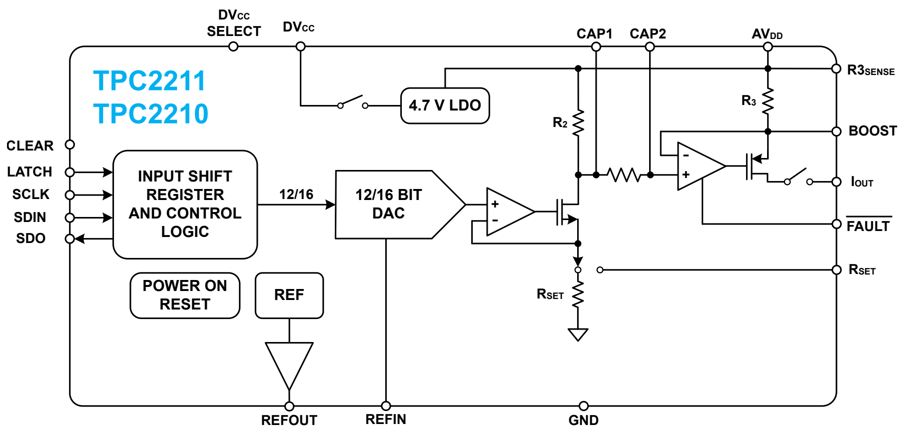


Figure 29. Functional Block Diagram

Feature Description

The TPC2211 and TPC2210 are high-precision digital-to-analog converters (DACs), specifically tailored for industrial process control needs. These devices offer a cost-effective, single-chip solution for creating precise current loops. They support current outputs ranging from 0 mA to 20 mA, 0 mA to 24 mA, and 4 mA to 20 mA. Users can select the preferred output configuration through the control register settings.

Architecture

The DAC core architecture of the TPC2211/TPC2210 is an R-2R DAC ladder shown below:

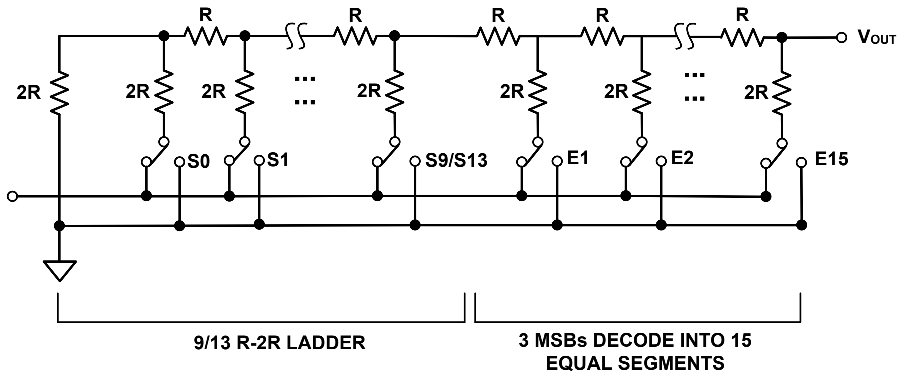


Figure 30. DAC Ladder Structure

The voltage output from the DAC core is converted to a current that is then mirrored to the supply rail so that the application simply sees a current source output with respect to ground.

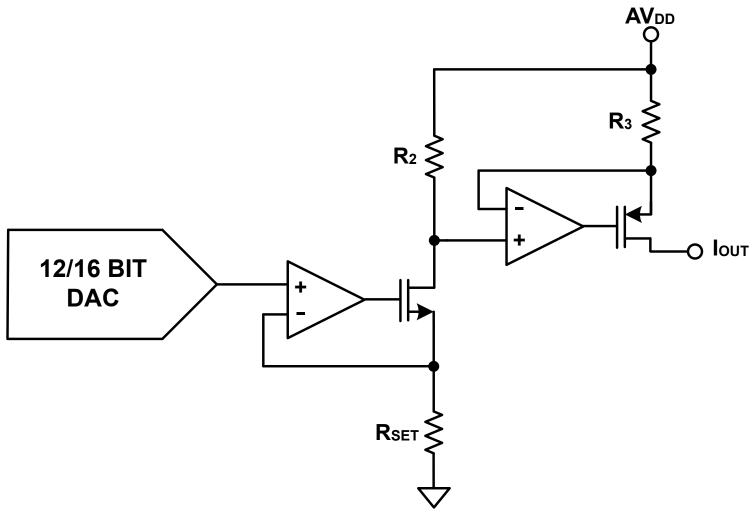


Figure 31. Voltage to Current Conversion Circuit

Serial Interface

The device is controlled by a 3-wire serial interface, and compatible with SPI standards.

Input Shift Register

The device features an input shift register that is 24-bit in width. The data is introduced into the register starting with the MSB, forming a 24-bit word. Data is clocked in on the rising edge of the SCLK signal. The input register has eight bits dedicated to address and sixteen bits for data.

The 24-bit word is latched unconditionally upon the occurrence of a rising edge on the LATCH pin. Regardless of the state of the LATCH pin, the data continues to be clocked into the shift register. When a rising edge on the LATCH pin is detected, the data present in the input register at that moment is captured. Essentially, the last 24 bits are clocked into the register prior to the rising edge of LATCH.

Table 4. Input Shift Register Format

MSB	LSB
D23 to D16	D15 to D0

MSB	LSB
Address Byte	Data word

Table 5. Write Address Byte Functions

Address Byte	Function
0x00	No operation (NOP)
0x01	Write Data register
0x02	Readback register value as per read address
0x55	Write Control register
0x56	Write Reset register
0x57	Write configuration register
0x95	Watchdog timer reset
0x96	CRC fault reset

Readback Operation

The process of invoking readback mode is initiated by setting the appropriate address byte and read address when inputting data into the input register. Subsequently, the next command sent to the device should be an NOP (No Operation), which facilitates the transmission of data from the previously addressed register. By default, the SDO pin remains inactive after the device has been set up for a read operation; it is only activated by a rising edge on the LATCH signal, preparing it to transmit data. Once the data has been successfully clocked out via the SDO pin, another rising edge on the LATCH signal deactivates (or tristate) the SDO pin. To successfully read back the data register, follow this sequence: Input the value 0x020001 into the input register. This command sets the device to read mode with the data register as the target. Immediately after, perform a second write operation with a NOP command, represented by 0x000000. During this write, the data stored in the register is clocked out onto the SDO line.

Readback mode is invoked by setting the address byte and read address when writing to the input register.

Table 6. Input Shift Register Contents for a Read Operation

Address Byte	Data Word	
D23 to D16	D15 to D6	D5 to D0
0000 0010	X (1)	Read Address

(1) X=don't care.

Table 7. Read Address Decoding

Read Address (1)	Function
XX XX00	Read status register
XX XX01	Read data register
XX XX10	Read control register
XX 1011	Read configuration register

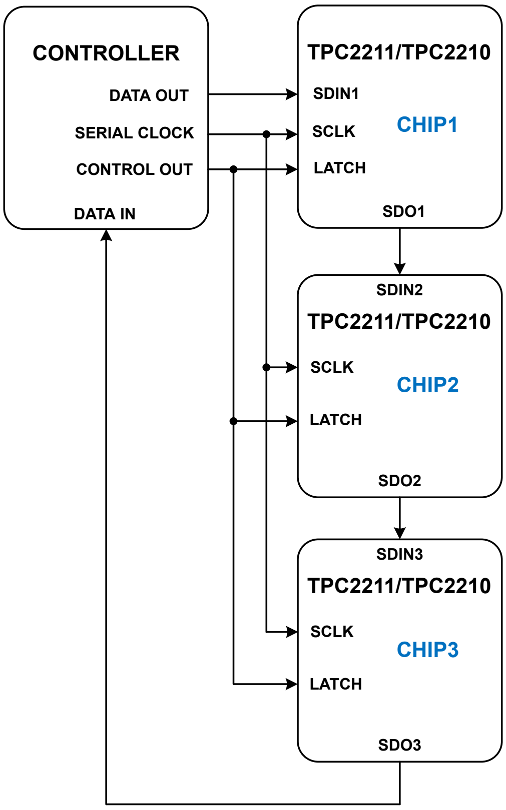
(2) X=don't care.

Standalone Operation

The serial interface is compatible with both continuous and non-continuous serial clock operations. A continuous source of SCLK is permissible only if the LATCH signal is raised after the correct sequence of data bits has been input. In the case of gated clock mode, a burst of SCLK must be provided with the precise number of cycles required, and the LATCH must be activated after the last cycle to secure the data. The initiation of the write cycle is signaled by the rising edge of SCLK that inputs the MSB of the data word. It is essential to apply precisely 24 rising edges to SCLK before the LATCH is elevated. If the LATCH is raised prior to the 24th rising edge of SCLK, the entered data is deemed invalid. Similarly, if more than 24 rising edges of SCLK are applied before the LATCH is raised, the input data becomes invalid.

Daisy-Chain Operation

In systems with multiple devices, the SDO pin facilitates a daisy-chain configuration. This setup is advantageous for system diagnostics and for minimizing the quantity of serial interface lines required. To activate daisy-chain mode, the DCEN bit in the control register should be set to 1. The write cycle commences with the first rising edge of SCLK that clocks in the MSB of the data word. SCLK continuously clocks the input shift register; if more than 24 pulses are applied, the data sequentially exits the shift register and manifests on the SDO line. The data is valid on the rising edge of SCLK, having been clocked out on the preceding falling edge of SCLK. By linking the SDO of one device to the SDIN of the next in the chain, a multi-device interface is established. Each device in the system necessitates 24 clock pulses, hence the total number of clock cycles required is 24 multiplied by n, where n represents the total count of devices in the chain. Upon completion of the serial transfer to all devices, the LATCH is raised, which locks in the input data for each device in the chain. The serial clock can operate in either a continuous or gated mode. For continuous SCLK operation, the LATCH must be elevated only after the correct number of clock cycles have been completed. In gated clock mode, a burst of SCLK must be precisely timed to match the exact number of required clock cycles, and the LATCH must be raised after the final clock pulse to secure the data.



Be careful that Latch pin can not be used as the chip selection signal to control multiple TPC2211/2210 chips. For TPC2211/2210, if the SPI communication receives more than 24 bits of data at one time, the extra data bits is discarded.

Therefore, if multiple chips share the SPI data bus, the Latch signal can only enable the chips to read the first 24 bits of data (the same data) on the bus, and it is impossible to achieve the purpose of communicating separately in terms of time.

Power On State

Upon power-on, internal calibration registers are read, and the data is applied to internal calibration circuitry. For a reliable read operation, there must be sufficient voltage on the AV_{DD} supply when the read event is triggered by the DVCC power supply powering up. Powering up the DV_{CC} supply after the AV_{DD} supply has reached at least 5 V ensures this. If DV_{CC} and AV_{DD} are powered up simultaneously, the supplies should be powered up at a rate greater than, typically, 5000 V/sec. If the internal DV_{CC} is enabled, the supplies should be powered up at a rate greater than, typically, 2000 V/sec.

If this cannot be achieved, issue a reset command to the device after power-on; this performs a power-on-reset event, reading the calibration registers and ensuring specified operation. To ensure correct calibration and to allow the internal reference to settle to its correct trim value, 100 μs should be allowed after a successful power-on reset.

Current Output

For the 0 mA to 20 mA, 0 mA to 24 mA, and 4 mA to 20 mA current output ranges, the output current is respectively expressed as

$$I_{OUT} = \left[\frac{20mA}{2^N}\right] \times D \quad (1)$$

$$I_{OUT} = \left[\frac{24mA}{2^N}\right] \times D \quad (2)$$

$$I_{OUT} = \left[\frac{16mA}{2^N}\right] \times D + 4mA \quad (3)$$

where:

D is the decimal equivalent of the code loaded to the DAC.

N is the bit resolution of the DAC.

Data Register

The data register is addressed by setting the address word of the input shift register to 0x01. The data to be written to the data register is entered in the D15 to D4 positions for the TPC2210 and the D15 to D0 positions for the TPC2211.

Table 8. Programming the TPC2210 Data register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
12-bit data-word												X	X	X	X

(1) X=don't care.

Table 9. Programming the TPC2211 Data register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16-bit data-word															

Register Maps

The following table shows available commands and registers on the devices.

Address Byte	Register / Command	Read/ Write	DATA BITS (D15:D0)															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x01	DAC Data(2)	R/W	16-bit Data															
0x02	READ	NA	X(1)											READ ADDRESS				
0x55	Control	R/W	0	0	REXT	OUTEN	SR CLOCK				SR STEP			SREN	DCEN	R2	R1	R0
0x56	RESET	W	Reserved															RESET
0x57	Configuration	R/W	Reserved											PUDSRCTL	CRCEN	WDEN	WDPD[1:0]	
0x95	Watchdog Timer	W	X(1)															
0x96	CRC Fault Reset(3)	W	X(1)															
NA	STATUS	R	Reserved											CRC-FLT	WD-FLT	IOUT fault	Slew active	Over temp

(1) X denotes don't care bits.
(2) TPC2211 (16-bit version) shown. TPC2210 (12-bit version) contents are located in DB15:DB4. For TPC2210, DB3:DB0 doesn't care about bits when writing and zeros when reading.
(3) No operation, read operation, watchdog timer reset, and CRC fault reset are commands and not registers.

Control Register

The control register is addressed by setting the address word of the input shift register to 0x55. The data to be written to the control register is entered in the D15 to D0 positions, as shown below:

D15	D14	D13	D12	D11:D8	D7:D5	D4	D3	D2	D1	D0
0	0	REXT	OUTEN	SR clock	SR step	SREN	DCEN	R2	R1	R0

The control register functions are shown below:

Table 10. Control Register Functions

Option	Description
REXT	Setting this bit selects the external current setting resistor. When using an external current setting resistor, it is recommended to only set REXT when also setting the OUTEN bit. Alternatively, REXT can be set before the OUTEN bit is set, but the range must be changed on the write in which the output is enabled.
OUTEN	Output enable. This bit must be set to enable the outputs. The range bits select which output is functional.
SR clock	Digital slew rate control
SR step	Digital slew rate control
SREN	Digital slew rate control enable.
DCEN	Daisy chain enable.
R2, R1, R0	Output range select

Table 11. Output Range Options

R2	R1	R0	Output Range Selected
1	0	1	4 mA to 20 mA current range

R2	R1	R0	Output Range Selected
1	1	0	0 mA to 20 mA current range
1	1	1	0 mA to 24 mA current range

Reset Register

The reset register is addressed by setting the address word of the input shift register to 0x56. The data to be written to the reset register is entered in the D0 position.

Table 12. Programming the Reset Register

D15:D1	D0
Reserved	Reset

Table 13. Reset Register Functions

Option	Description
Reset	Setting this bit performs a reset operation, restoring the device to its power-on state.

Configuration Register

The configuration register is written to at address 0x57.

Table 14. Programming the Configuration Register

D15:D5	D4	D3	D2	D1	D0
Reserved	PUDSRCTL	CRCEN	WDEN	WDPD[1:0]	

Table 15. Configuration Register Functions

Option	Default	Description
Reserved.	0	Reserved. User must not write any value other than zero to these bits.
PUDSRCTL	0	Power on and power down slew rate control. When setting this bit at first, and then setting SREN , the output, instead of changing directly between two values , steps digitally at a rate defined by SRCLK and SRSTEP from zero value to target value or from target value to zero value when setting or disabling OUTEN.
CRCEN	0	Enable frame error checking.
WDEN	0	Watchdog timer enable.
WDPD[1:0]	0	Watchdog timeout period.

Status Register

The status register is a read-only register.

Table 16. Decoding the Status Register

D15:D5	D4	D3	D2	D1	D0
Reserved	CRC-FLT	WD-FLT	I_{OUT} fault	Slew active	Over temp

Table 17. Status Register Functions

Option	Description
CRC-FLT	Bit = 1 indicates CRC error on the SPI frame. Bit = 0 indicates normal operation.
WD-FLT	Bit = 1 indicates watchdog timer timeout. Bit = 0 indicates normal operation.
I_{OUT} FAULT	This bit is set if a fault is detected on the I_{OUT} pin.
Slew Active	This bit is set while the output value is slewing (slew rate control enabled).
Over Temp	This bit is set if the core temperature of the device exceeds ~150°C.

Functional Modes

Fault Alarm

A fault detection function is available on this chip. When any of the fault events mentioned below occurs, the open-drain output $\overline{\text{FAULT}}$ goes low with the corresponding bit in the status register set high.

1. The die temperature of the chip exceeds 150℃. The alarm is cleared when the temperature falls back to 140 ℃.
2. The current output is open loop, or the current loop compliance voltage does not meet the requirement to ensure output accuracy.
3. The CRC mode is enabled and there is a frame error detected.
4. The watchdog timer is enabled and meanwhile a write address byte is not received within the specified period of time.

Asynchronous Clear

A CLEAR pin is provided to realize the asynchronous DAC clear function. The pin is active-high and allows the DAC data to be cleared to clear-code, which can be selected by the CLEAR_SEL pin and the CLRSEL bit in the control register. When any of them goes high, mid-scale is taken as the clear code for unipolar output range and zero-scale for the bipolar output range; otherwise, the output will be cleared to 0V. DAC remains in clear mode until the next latch, before which if there is not any data clocking in the pre-clear data can be recovered.

Digital Power Supply

An internally generated 4.7-V supply can be output on DV_{CC} by leaving the DV_{CC} SELECT pin unconnected. It is capable of supplying up to 10 mA of current. For the external supply, tie DV_{CC} SELECT to 0 V. The DV_{CC}pin accepts a power supply of 2.7 V to 5.5 V.

Internal Reference

The TPC2201 includes an integrated 5V voltage reference with an initial accuracy of ±5 mV maximum and a temperature drift coefficient of ±10 ppm/°C maximum. The reference voltage is buffered and capable of use elsewhere within the systems that need source or sink current.

External Current Setting Resistor

There is an internal current setting resistor on the chip to help with the voltage-to-current conversion. With the DAC code going high, the voltage drops over the internal R_{SET} increases, causing the precision of the output current to be affected by the voltage coefficient of the internal R_{SET}. Moreover, the temperature coefficient of the internal R_{SET} also aggravates the precision loss. To achieve better performance, the chip provides an R_{SET} pin which allows the user to connect a high-accuracy low-drift external current setting resistor. It can be selected to use internal or external R_{SET} by setting different values in the control register.

Current Boost Function

For high-accuracy application scenarios, a BOOST pin is provided to employ a discrete NPN transistor to bypass most of the current consumption off-chip, thus improving the temperature-induced drift of both on-chip reference and internal RSET. The external boost transistor should have high enough breakdown voltage between its collector and emitter to endure AV_{DD}-I_{OUT}*R_{LOAD} which supports a maximum of 50 V.

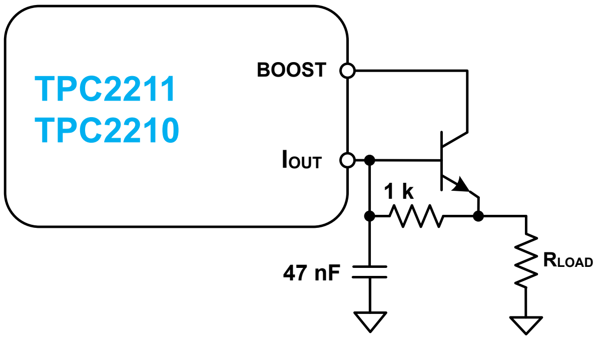


Figure 32. External Boost Configuration

Hart Communication

For HART communication applications, this chip offers three options:

1. Couple the HART signal into CAP1
   To achieve a 1 mApp current at I_{OUT}, the signal amplitude coupled at the CAP1 pin should be 39 mVpp. With the modem output signal of 500 mVpp, the capacitors C1 and C2 are recommended to be 6.4 nF and 73 nF.
2. Couple the HART signal into CAP2
   To achieve a 1mApp current at I_{OUT}, the signal amplitude coupled at the CAP2 pin should be 39 mVpp. With the modem output signal of 500 mVpp, the capacitors C1 and C2 are recommended to be 1.5 nF and 18 nF.
3. Couple the HART signal into R_{SET}
   To achieve a 1mApp current at I, the signal amplitude coupled at the R pin should be 15 µVpp. With the modem output signal of 500 mVpp, the capacitor C1 and resistor R1 are recommended to be 6.4 nF and 50 kΩ.

The following figure shows the recommended circuit for attenuating and coupling in the HART signal.

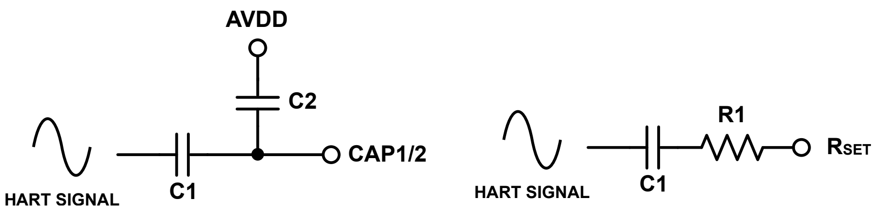


Figure 33. Schematic Diagram for the HART Coupling Configuration

Slew Rate Control

In application scenarios where the current output needs to drive a large inductor or other cases when the slew rate needs to be reduced, the slew rate control feature can be turned on by setting the SREN bit in the control register to high. The corresponding frequency and step are also set in the control register. The following table shows the coding method of SR-CLOCK and SR-STEP which define the rate the DAC DATA updates and the code it slews at a time. During a slewing period the SLEW-ACTIVE bit in the status register is held high. The staircase waveform of the output current can be smoothed by connecting filtering capacitors at the CAP1 pin and the CAP2 pin.

Table 18. Slew Rate Step Size Options

SR Step	TPC2210 Step Size (LSB)	TPC2211 Step Size (LSB)
0	1/16	1
1	1/8	2
10	1/4	4
11	1/2	8
100	1	16
101	2	32
110	4	64
111	8	128

Table 19. Slew Rate Update Clock Options

SR Clock	Update Clock Frequency (Hz)
0	257,730
1	198,410
10	152,440
11	131,580
100	115,740
101	69,440
110	37,590
111	25,770
1000	20,160
1001	16,030
1010	10,290
1011	8280
1100	6900
1101	5530
1110	4240
1111	3300

The time it takes for the output to slew over a given output range can be expressed as follows:

$$\text{Slew Time} = \frac{\text{Digital Code Change}}{\text{SR STEP} \times \text{SR CLOCK}} \qquad (4)$$

where: Slew Time is expressed in seconds. Digital Code Change is the value of the change in the data register.

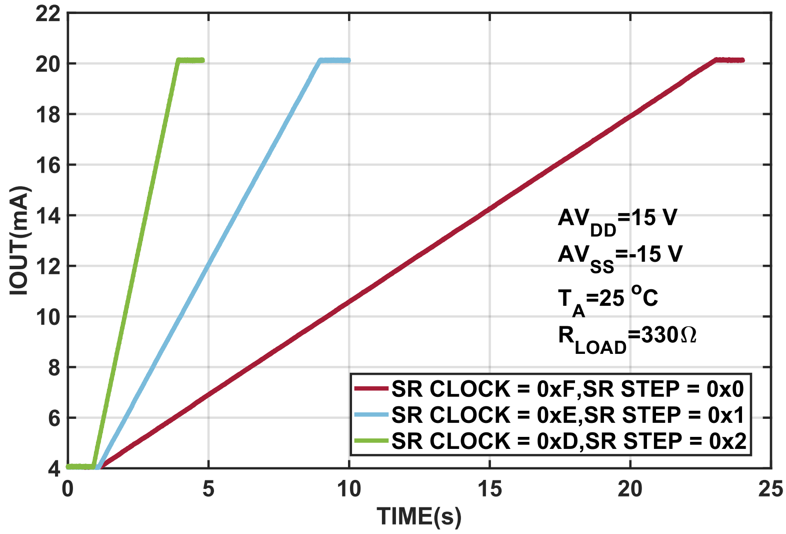


Figure 34. Output Current Slewing Under Control of the Digital Slew Rate Control Feature (1 s~10 s)

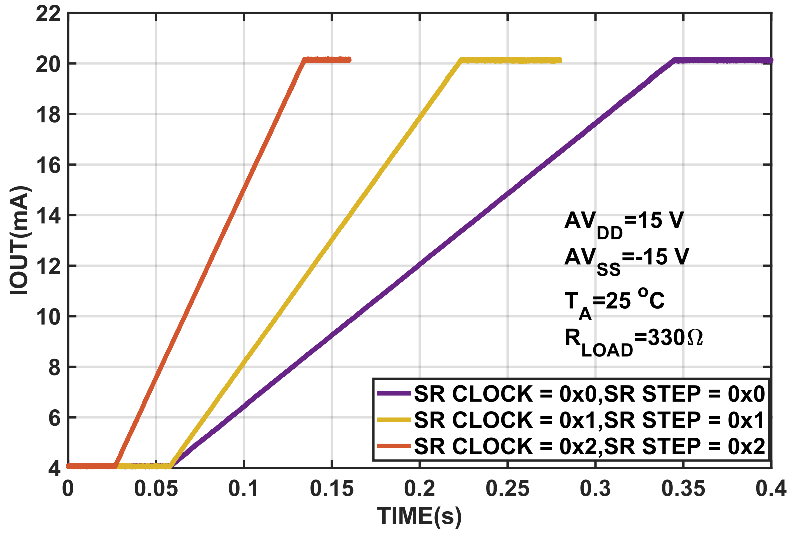


Figure 35. Output Current Slewing under Control of the Digital Slew Rate Control Feature(0.1 s~1 s)

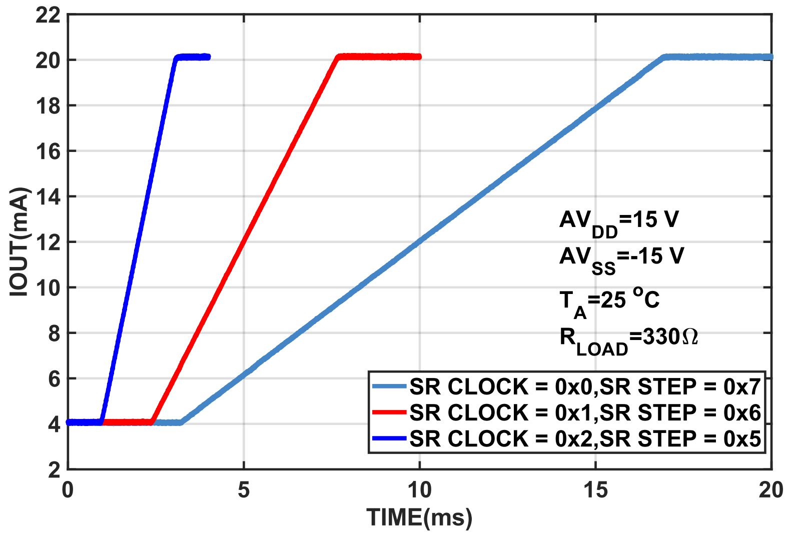


Figure 36. Output Current Slewing under Control of the Digital Slew Rate Control Feature (2 ms~0.1 s)

To avoid halting the output slew, the slew active bit can be read to check that the slew has been completed before writing to any of the TPC2211/TPC2210 registers. The update clock frequency for any given value is the same for all output ranges. The step size, however, varies across output ranges for a given value of step size because the LSB size is different for each output range. The following table shows the range of programmable slew times for a full-scale change on any of the output ranges. The values in the table are obtained using the above Slew Time calculation Equation.

Table 20. Programmable Slew Time Values in Seconds for a Full-Scale Change on Any Output Range (65535 Code)

	Step Size (LSB)							
Update Clock Frequency (Hz)	**1**	**2**	**4**	**8**	**16**	**32**	**64**	**128**
257,730	0.25	0.13	0.06	0.03	0.016	0.008	0.004	0.002
198,410	0.33	0.17	0.08	0.04	0.021	0.010	0.005	0.0026
152,440	0.43	0.21	0.11	0.05	0.027	0.013	0.007	0.0034
131,580	0.50	0.25	0.12	0.06	0.031	0.016	0.008	0.0039
115,740	0.57	0.28	0.14	0.07	0.035	0.018	0.009	0.0044
69,440	0.9	0.47	0.24	0.12	0.06	0.03	0.015	0.007
37,590	1.7	0.87	0.44	0.22	0.11	0.05	0.03	0.014
25,770	2.5	1.3	0.64	0.32	0.16	0.08	0.04	0.020
20,160	3.3	1.6	0.81	0.41	0.20	0.10	0.05	0.025
16,030	4.1	2.0	1.0	0.51	0.26	0.13	0.06	0.03
10,290	6.4	3.2	1.6	0.80	0.40	0.20	0.10	0.05
8280	7.9	4.0	2.0	1.0	0.49	0.25	0.12	0.06
6900	9.5	4.8	2.4	1.2	0.59	0.30	0.15	0.07
5530	12	5.9	3.0	1.5	0.74	0.37	0.19	0.09
4240	15	7.7	3.9	1.9	0.97	0.48	0.24	0.12
3300	20	9.9	5.0	2.5	1.24	0.62	0.31	0.16

I_{OUT} Filtering Capacitors

The digital slew rate control feature results in a staircase formation on the current output, and the staircase can be removed by connecting capacitors to the CAP1 and CAP2 pins. The capacitors form a filter on the current output circuitry.

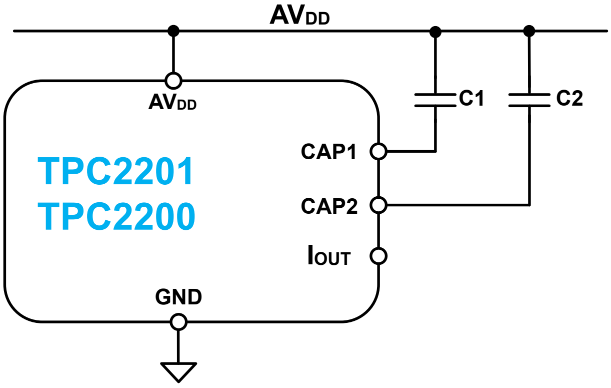


Figure 37. I_{OUT} Filtering Capacitors

With these capacitors, a filter is formed on the current output circuitry, as shown below. The filter reduces the bandwidth and the slew rate of the output current.

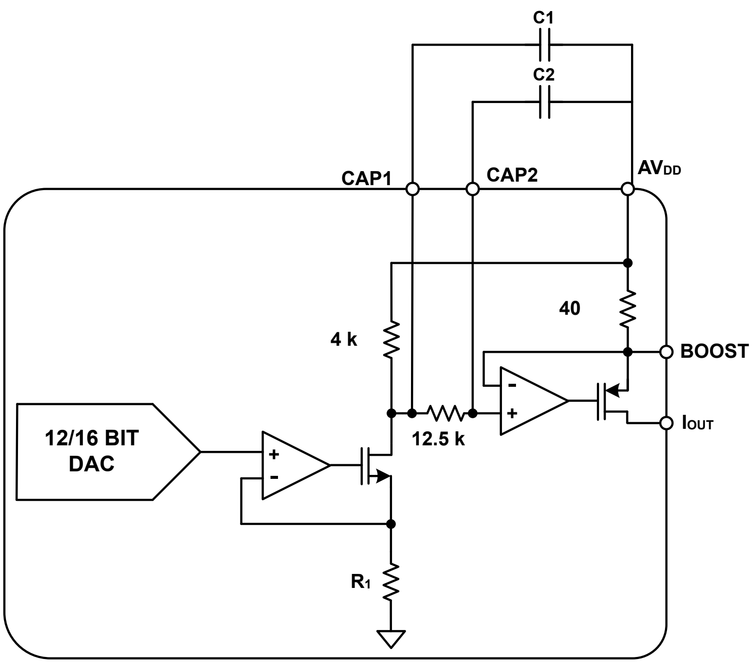


Figure 38. I_{OUT} Filter Circuitry

The following figure shows the effect the capacitors have on the slew rate of the output current.

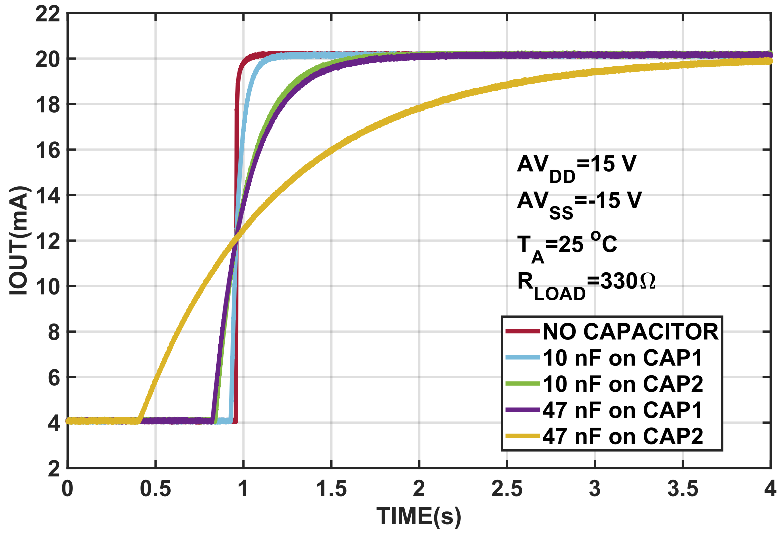


Figure 39. Slew Controlled 4 mA to 20 mA Output Current Step Using External Capacitors on the CAP1 and CAP2 Pins

To achieve significant reductions in the rate of change, very large capacitor values are required, which may not be suitable in some applications. In this case, the digital slew rate control feature can be used. The capacitors can be used in conjunction with the digital slew rate control feature as a means of smoothing out the steps caused by the digital code increments, as shown in the following figure.

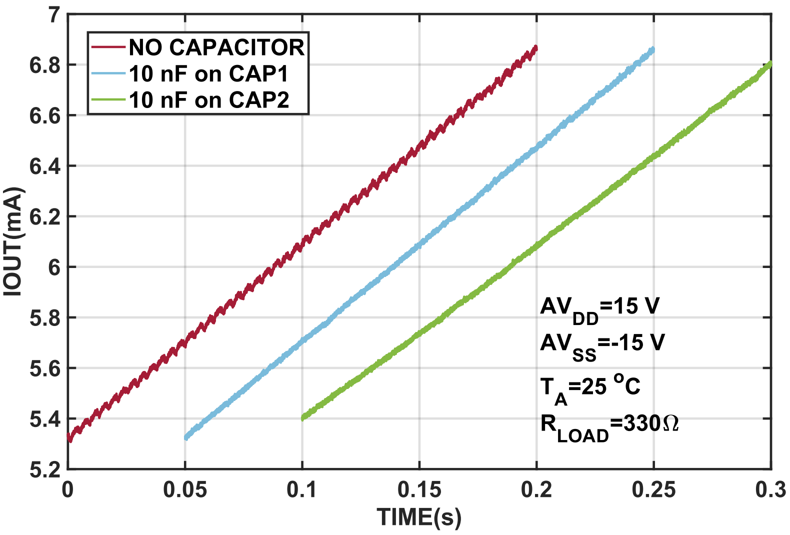


Figure 40. Smoothing Out the Steps Caused by the Digital Slew Rate Control Feature

SLEWPD Function

When using the Slewpd function, the SREN bit in the Control Register and the SLEWPD bit in the Configuration Register must be ensured as 1, and when the Slewpd function is enabled, the OUTEN bit will be enabled and disabled according to the configuration in the SR clock and SR Step.

Watchdog Timer

This feature helps ensure that communication between the host processor and the device is not lost. Enable the watchdog timer by setting the WDEN bit of the configuration register to 1. The watchdog timeout period can be set using the WDPD bit of the configuration register. The timer cycle is based on an internal oscillator with a typical value of 2 MHz. Watchdog timeout period (unit, ms) is shown in the following table. If enabled, the chip must have an SPI frame, where 0x95 is the write address byte written to the device within the programmed timeout period. And, the FAULT pin is asserted as low level, and the WD-FLT bit of the status register is set to 1. Use software to reset, disable the watchdog timer, or power down the device, which can be reset the WD-FLT bit to 0.

Table 21. Watchdog Timeout Period

WDPD bits	Watchdog Timeout Period (Typical, ms)
00	10
01	51
10	102
11	204

Frame Error Checking

The error checking can be used to check the integrity of the SPI data communication between the device and the host processor, when the device is used in a complex environment. This function can be enabled by setting the CRCEN bit of the configuration register to 1. The frame error checking scheme is based on the CRC-8-ATM (HEC) polynomial x^8+x^2+x+1 (i.e., 100000111). When the check mechanism is enabled, the SPI frame width is 32 bits, as shown in the following table. Start with the default 24-bit frame, enable frame error checking via the CRCEN bit, and the next SPI frame switch to a 32-bit frame. Before the normal 24-bit SPI data is fed to the device, the host processor attaches an 8-bit CRC polynomial to it. For register readback, the CRC polynomial is output by the device on the SDO pin as part of a 32-bit frame. When in CRC mode, the device calculates CRC words every 32 clocks, regardless of the latched pin switching time. The device decodes the 32-bit input frame data to calculate the CRC remainder. If there are no errors in the frame, the CRC remainder is zero.

When the remainder is non-zero (i.e., the input frame has a single or multiple bit errors), the FAULT pin assertion is low, and the CRC-FLT bit of the status register is also set to 1. The FAULT pin can be asserted to be low under any different conditions. To reset the CRC-FLT bit to 0, use the 0x96 write command to software reset command, disable frame error checking, or power down the device.

In the case of CRC errors, a specific SPI frame is prevented from being written to the device. If the CRC mode is enabled on the first frame sent to the device after power-up, any transient on the SCLK line is interpreted as an SCLK cycle, and an NOOP (no operation) command is sent to the device to reset the SPI clock and SPI frame alignment. To send an NOP command, simply toggle the latch pin without any SCLK cycles.

Note:

- When a CRC ERROR occurs in CRC mode, the FAULT pin is pulled low. If CRCEN is disabled, the FAULT pin will not immediately go high; it will only go high on the next rising edge of the SCLK clock.
- When a CRC ERROR occurs, at this time, only the Reset Register (0x56) and the Configuration Register (0x57) can be configured, and the command 0x960000D4 (CRC reset) can be recognized. Reading all registers is unrestricted at this time.
- Clearing the CRC ERROR can be achieved by configuring the Configuration Register (0x57) to disable CRC EN, writing to the Reset Register (0x56) to perform a soft reset, sending the CRC reset command (0x96), or by repowering the device.

Table 22. SPI Frame with Frame Error Checking Enabled

Bit 31: Bit 8	Bit 7: Bit 0
Normal SPI Frame data	8-bit CRC polynomial

Daisy Chain

For systems containing multiple devices, SDO pins can be used to connect the devices in series. This daisy chain pattern is very useful in system diagnosis and reducing the number of serial interface lines. The daisy chain mode is enabled by setting the DCEN bit in the control register to high. The SCLK clock with the first rising edge inputs the MSB of the data byte into the input shift register, marking the beginning of the write cycle. SCLK is continuously applied to input shift registers. If the applied clock pulses exceed 24, data will overflow from the shift register and appear on the SDO line. This data is valid at the rising edge of SCLK and is output by the clock at the SCLK edge of the previous falling edge. By connecting the SDO of the first device in the chain to the SDIN input of the next device, a multi-device interface can be constructed. Each device in the system requires 24 clock cycles. Therefore, the total number of clock cycles must be equal to 24 x n, where n is the total number of the devices in the chain. After the serial transmission to all devices is completed, set LATCH to a high level. This will lock the input data of each device in the daisy chain. A serial clock can be a continuous clock or a gated clock. If LATCH is set to high after the correct number of clock cycles, only continuous SCLK sources can be used. In gated clock mode, a burst clock containing an exact number of clock cycles must be used, and LATCH must be set high after the last clock to capture data.

FEEDBACK/MONITORING OF OUTPUT CURRENT

To provide feedback or monitor the output current value, a sense resistor can be connected in series with the IOUT output pin, and the voltage drop across it can be measured. However, this not only introduces an additional component but also increases the required compliance voltage. Alternatively, an existing resistor can be used for this purpose. R3, which is internal to the TPC2211/TPC2210, serves as such a resistor, as illustrated in Figure 41. By measuring the voltage between the $R3_{SENSE}$ and BOOST pins, the output current can be calculated as follows:

$$I_{OUT} = \frac{V_{R3}}{R3} - I_{BIAS}$$

where: V_{R3} is the voltage drop across R3 measured between the $R3_{SENSE}$ and BOOST pins.

I_{BIAS} is a constant bias current flowing through R3 with a typical value.

R3 is the resistance value of resistor R3 with a typical value of 40 Ω.

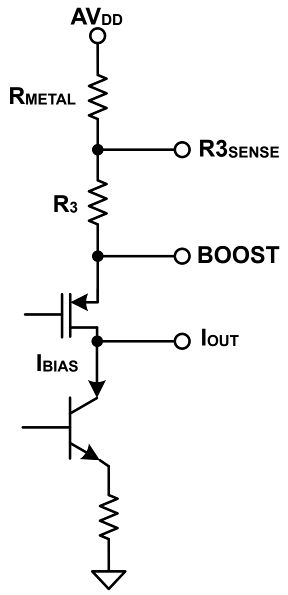


Figure 41. Structure of Current Output Circuit

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPC2211/TPC2210 are low-cost, precision, fully integrated 16/12 bit digital-to-analog converters (DAC) offering a programmable current source to meet the requirements of industrial process control applications.

Typical Application

Driving Inductive Loads

When driving inductive or poorly defined loads, connect a 0.01 µF capacitor between I_{OUT} and GND. This ensures stability with loads above 50 mH. There is no maximum capacitance limit. The capacitive component of the load may cause slower settling. The digital slew rate control feature may also prove useful in this situation. A schematic diagram of the current establishment of 90 mH is shown below:

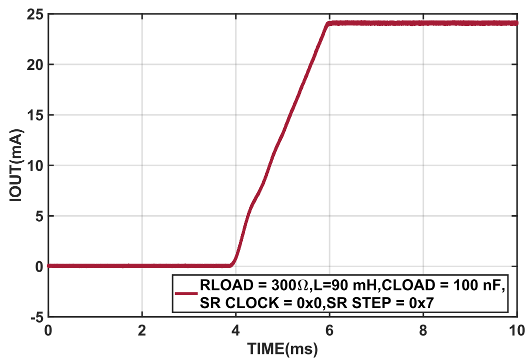


Figure 42. I_{OUT} Establishment with Large Inductance Load

Transient Voltage Protection

The TPC2211 and the TPC2210 contain ESD protection diodes that prevent damage from normal handling. The industrial control environment can, however, subject I/O circuits to much higher transients. To protect the TPC2211/TPC2210 from excessively high voltage transients, external power diodes and a surge current limiting resistor are required, as shown below. The constraint on the resistor value is that, during normal operation, the output level at I_{OUT} must remain within its voltage compliance limit of AV_{DD} – 2 V, and the two protection diodes and resistor must have appropriate power ratings. Further protection can be provided with transient voltage suppressors or transorbs; these are available as both unidirectional suppressors (protect against positive high voltage transients) and bidirectional suppressors (protect against both positive and negative high voltage transients) and are available in a wide range of standoff and breakdown voltage ratings. It is recommended that all field-connected nodes be protected.

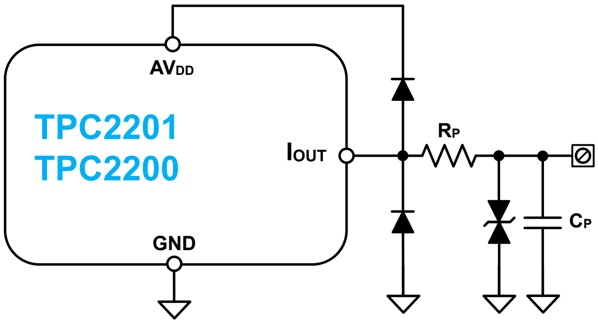
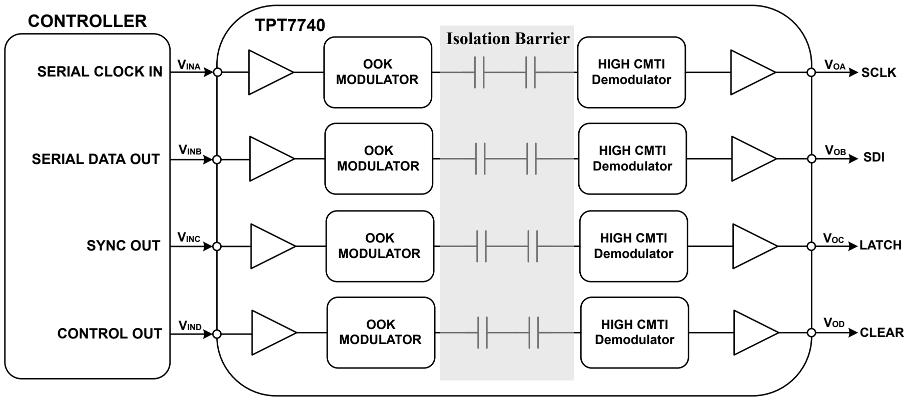


Figure 43. I_{OUT} Transient Voltage Protection

Galvanically Isolated Interface

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur. The Digital Isolator products from 3PEAK, Inc., provide voltage isolation in excess of 5 kV. The serial loading structure of the TPC2201/TPC2200 makes the parts ideal for isolated interfaces because the number of interface lines is kept to a minimum. The following figure shows a 4-channel isolated interface to the TPC2201/TPC2200 using a TPT7740. For further information, visit https://www.3peak.cn/isolation.



Microprocessor Interfacing

Microprocessor interfacing to the TPC2201/TPC2200 is via a serial bus that uses a protocol compatible with microcontrollers and DSP processors. The communications channel is a 3-wire minimum interface consisting of a clock signal, a data signal, and a latch signal. The TPC2200 requires a 24-bit data-word with data valid on the rising edge of SCLK. For all interfaces, the DAC output update is initiated on the rising edge of LATCH. The contents of the registers can be read using the readback function.

Analog Output Applications based on Dynamic Power Control

In order to solve the problem of power consumption and heat generation of the TPC2201/TPC2200 when the current is output, a DC-DC BUCK is used to feed back to the VFB terminal through the voltage on the R_{LOAD} at the output terminal, and adjust the output voltage of the BUCK, which is connected to the AV_{DD} of the TPC2201/TPC2200. The schematic diagram is shown in the following figure.

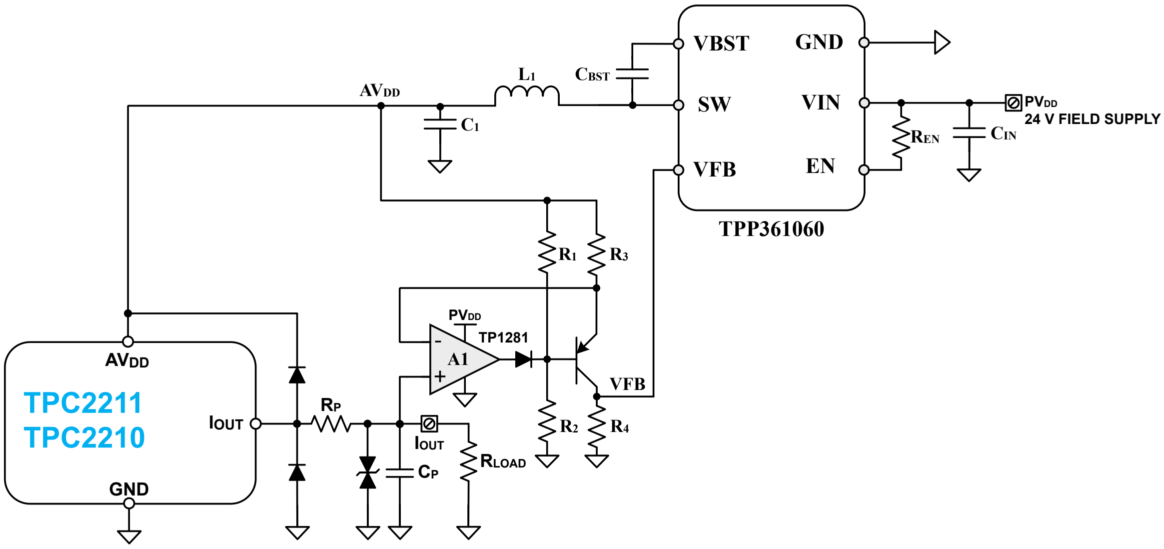


Figure 44. Block Diagram of the Dynamic Power Control Scheme

The expression for the minimum output voltage is shown below:

$$AV_{DD\_MIN} = \left(\frac{R_3}{R_4}V_{FB} + 0.7\right)\left(1 + \frac{R_2}{R_1}\right) \quad (5)$$

The dynamic power control is mainly divided into two stages. The expression for the demarcation voltage of the two states is:

$$V_{threshold} = \left(\frac{R_3}{R_4}V_{FB} + 0.7\right)\left(1 + \frac{R_2}{R_1}\right) - \frac{R_3}{R_4}V_{FB} \quad (6)$$

In general, we make R2 much smaller than R1, so the threshold voltage is about 0.7 V.

When the voltage on the R_{LOAD} is less than 0.7 V, the op amp A1 is in the open-loop working state, at this time, the negative input voltage of the op amp is about 0.7 V, when the voltage on the RLOAD is greater than 0.7 V, the op amp is in the closed-loop working state, the forward input voltage of the op amp is equal to the reverse input voltage, and the op amp needs to ensure that its I_B current changes little in the open-loop and closed-loop states.

Table 23. Resistor Values in Dynamic Power Control Scheme

R_1	R_2	R_3	R_4
68 kΩ	11 kΩ	100 kΩ	6.2 kΩ
AV_{DD-MIN}	12.0561 V		

Assuming R_{LOAD} = 250 Ω and an output current of 24 mA, without the use of dynamic power control, the voltage on the TPC2211/TPC2210 is 18 V, the current is 24 mA, and the power consumption is 432 mW. If dynamic power control is used, the voltage on the TPC2201/TPC2200 is 6.05 V, the current is 24 mA, and the power consumption is 145 mW. If theTPC2211/TPC2210 needs to communicate with HART, a low-pass filter can be added to the front end of the op amp A1 to filter out the effects of the HART signal.

INDUSTRIAL, HART COMPATIBLE ANALOG OUTPUT APPLICATION

Many industrial control applications have requirements for accurately controlled current output signals, and the TPC2211/TPC2210 are ideal for such applications. Figure 45 shows the TPC2211/TPC2210 in a circuit design for an output module specifically for use in an industrial control application. The design provides for a HART-enabled current output, with the HART capability provided by the HART modem, the industry's slowest power and smallest footprint HART-compliant IC modem. The HART_OUT signal from the modem is attenuated and ac-coupled into the CAP2 pin of the TPC2211. An alternative method of coupling the HART signal into the RSET pin (only applicable of the external RSET is used). This circuit adheres to the HART physical layer specifications as defined by the HART Communication Foundation.The module is powered from a field supply of 24 V. This supplies AV_{DD} directly. For transient overvoltage protection, transient voltage suppressors (TVS) are placed on both the I_{OUT} and field supply connections. A 24 V TVS is placed on the I_{OUT} connection, and a 36 V TVS is placed on the field supply input. For added protection, clamping diodes are connected from the I_{OUT} pin to the AV_{DD} and GND power supply pins. In this case, the input has higher transient voltage protection and should, therefore, not require additional protection circuitry, even in the most demanding of industrial environments. Isolation between the TPC2211/TPC2210 and the backplane circuitry is provided with the TPT7741 and TPT7721 iCoupler digital isolators. The internally generated digital power supply of the TPC2211/TPC2210 powers the field side of the digital isolators, removing the need to generate a digital power supply on the field side of the isolation barrier. The TPC2211/TPC2210 digital supply output supplies up to 30 mA, which is more than enough to supply the 10.8 mA requirement of the TPT7741 and TPT7721 operating at a logic signal frequency of up to 1 MHz. To reduce the number of isolators required, nonessential signals such as CLEAR can be connected to GND and FAULT, and SDO can be left unconnected, reducing the isolation requirements to just three signals. Doing so, however, disables the fault alert features of the part.

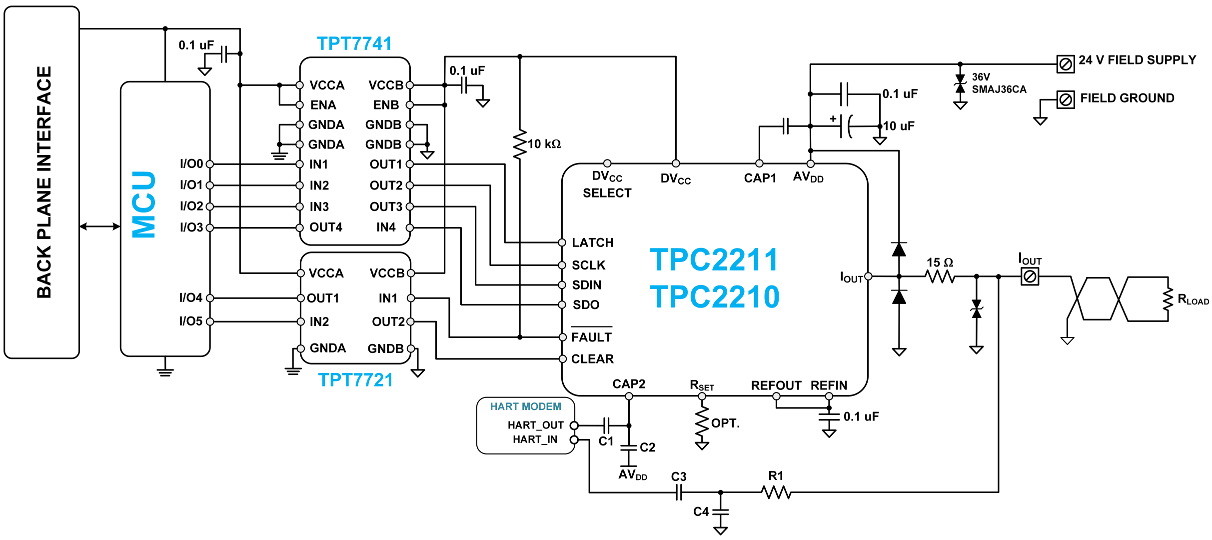


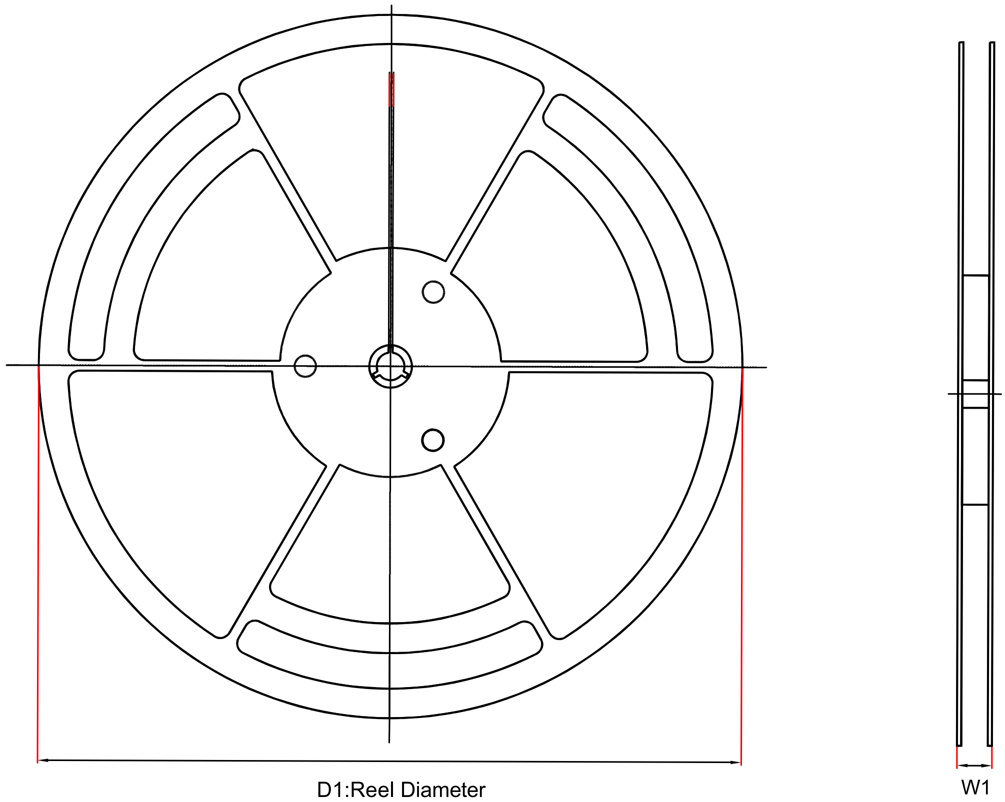
Figure 45. TPC2210/TPC2211 in an Industrial Analog Output Application

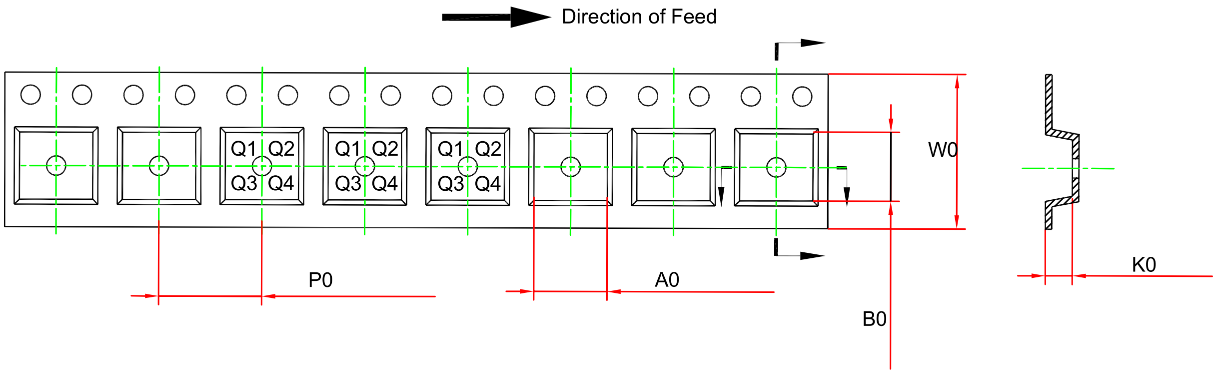
Layout

Layout Guideline

- In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance.
- Design the printed circuit board (PCB) on which the TPC2211/TPC2210 is mounted so that the analog and digital sections are separated and confined to certain areas of the board. If the TPC2211/TPC2210 is in a system where multiple devices require an analog ground-to-digital ground connection, make the connection at one point only. Establish the star ground point as close as possible to the device.
- The TPC2201/TPC2200 should have ample supply bypassing of 10 μF in parallel with 0.1 μF on each supply located as close to the package as possible, ideally right up against the device. The 10 μF capacitors are the tantalum bead type. The 0.1 μF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.
- The power supply lines of the TPC2211/TPC2210 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.
- Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board. Never run these near the reference inputs.
- A ground line routed between the SDIN and SCLK lines helps reduce crosstalk between them (this is not required on a multilayer board that has a separate ground plane, but separating the lines helps).
- It is essential to minimize noise on the REFIN line because it couples through to the DAC output.
- Avoid crossover of digital and analog signals. Traces on opposite sides of the PCB should run at right angles to each other. This reduces the effects of feed through the board.
- A microstrip technique is by far the best but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane, and signal traces are placed on the solder side.

Tape and Reel Information



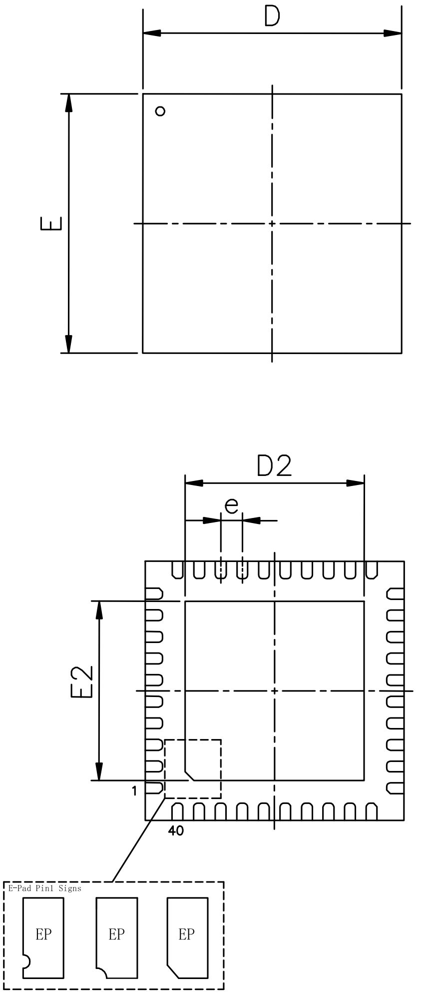


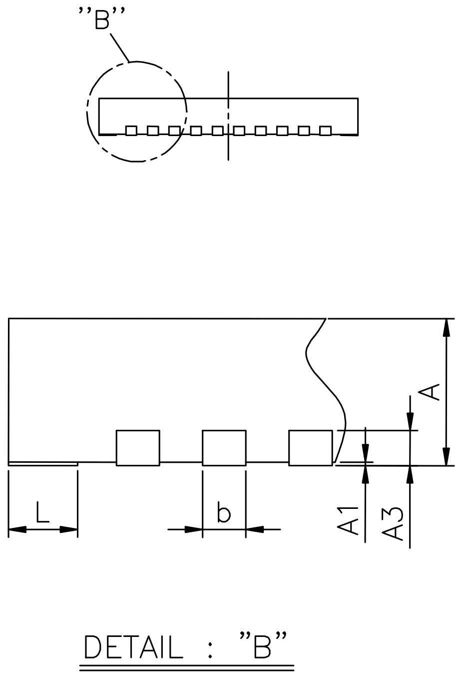
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPC2211-QFER	QFN6X6-40	329	17.6	6.3	6.3	1.1	8	12	Q2
TPC2210-QFER	QFN6X6-40	329	17.6	6.3	6.3	1.1	8	12	Q2
TPC2211-TSDR	ETSSOP24	330	21.6	6.8	8.3	1.6	8	16	Q1
TPC2210-TSDR	ETSSOP24	330	21.6	6.8	8.3	1.6	8	16	Q1

Package Outline Dimensions

QFN6X6-40

Package Outline Dimensions QFE(QFN6X6-40-A)





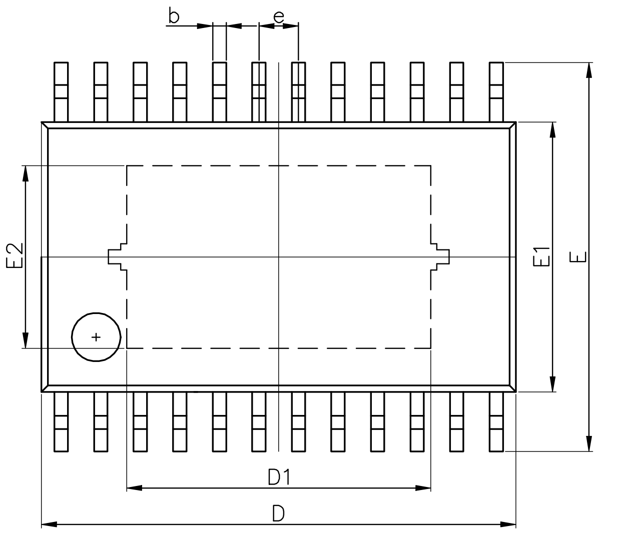
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.031	0.035
A1	0.000	0.050	0.000	0.002
b	0.180	0.300	0.007	0.012
A3	0.200 REF		0.008 REF	
D	5.900	6.100	0.232	0.240
E	5.900	6.100	0.232	0.240
e	0.500 BSC		0.020 BSC	
L	0.300	0.500	0.012	0.020
D2	4.000	4.300	0.157	0.169
E2	4.000	4.300	0.157	0.169

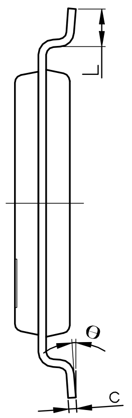
NOTES

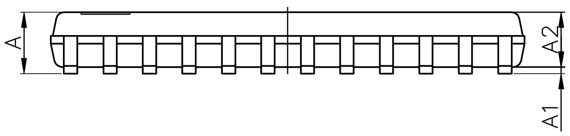
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

ETSSOP24

Package Outline Dimensions TSD(ETSSOP-24-E)







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	---	1.200	---	0.047
A1	0.020	0.150	0.001	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	7.700	7.900	0.303	0.311
E	6.250	6.550	0.169	0.177
E1	4.300	4.500	0.244	0.260
D1	4.900	5.100	0.193	0.201
E2	2.900	3.100	0.114	0.122
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPC2211-QFER (1)	−40 to 125°C	QFN6X6-40	2211	3	Tape and Reel, 3150	Green
TPC2210-QFER (1)	−40 to 125°C	QFN6X6-40	2210	3	Tape and Reel, 3150	Green
TPC2211-TSDR (1)	−40 to 125°C	ETSSOP24	2211	3	Tape and Reel, 4000	Green
TPC2210-TSDR	−40 to 125°C	ETSSOP24	2210	3	Tape and Reel, 4000	Green

(1) For future products, contact the 3PEAK factory for more information and samples.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

IMPORTANT NOTICE AND DISCLAIMER