8-channel High Precision Voltage Output DAC with Internal Reference

Features

- High Accuracy
  - INL: Typical ±8 LSB at 16-bit Resolution
- Integrated 2.5-V Internal Reference
  - Low Drift: 10ppm/℃
- Flexible Output Configuration
  - User Selectable Gain: 1/2, 1, 2
  - Reset to Zero Scale
- High Output Current Capability: 20 mA
- Serial Interfaces
  - 4-Wire SPI Compatible Serial Interface
  - Daisy Chain Operation
  - CRC Error Check
- Temperature Range: −40°C to +125°C
- Package: QFN3X3-16

Applications

- Industrial Automation
- Optical Networking
- Data Acquisition Systems

Description

The TPC2196 is a high-accuracy DAC with 16-bit resolution.

The device includes a 2.5-V internal reference, which can be used to reduce system complexity.

Several gain options can be selected to provide different full-scale output voltages: 1.25 V, 2.5 V, and 5 V.

The device operates under a single analog supply, and has a separate VIO supply for digital communication. The communication is performed through a serial interface, and can operate under wide-range V_{IO} supply voltage.

A power-on reset circuit is integrated to maintain the DAC output at zero scale or midscale.

The device is characterized for temperature range from −40℃ to 125 ℃ and is available in a small package of QFN.

Typical Application Circuit

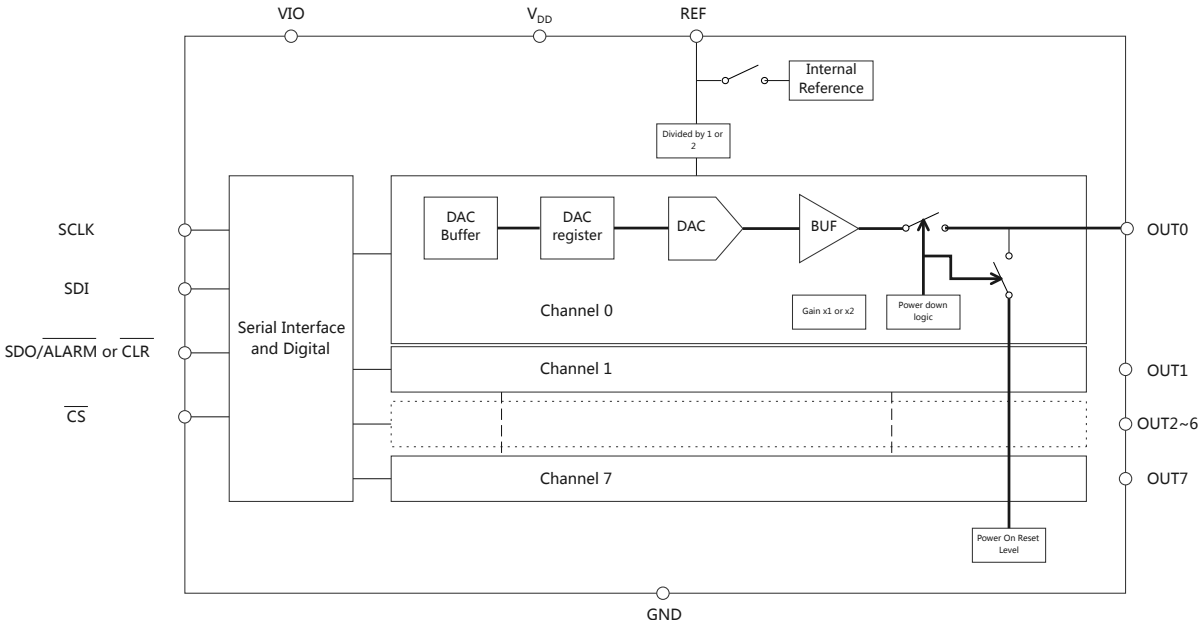


Table of Contents

Product Family Table

Order Number	Resolution	Reference	Reset	SDO or $\overline{\text{CLR}}$ Operation	Package
TPC2196-QFNR	16	Internal/External	0	SDO	QFN3X3-16

Revision History

Date	Revision	Notes
2025-01-20	A.0	Initial release.

Pin Configuration and Functions

TPC2196
QFN Package
Top View

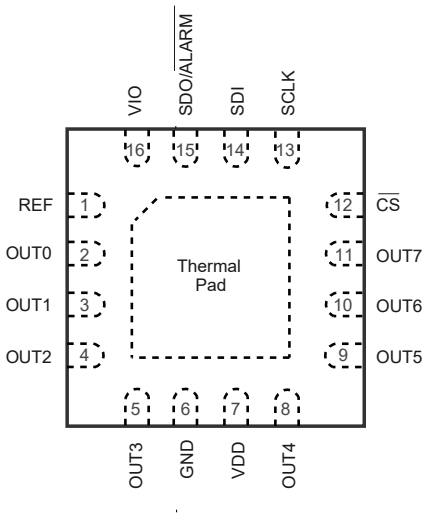


Table 1. Pin Functions: TPC2196

Pin		I/O	Description
NO. WQFN	Name		
1	REF	I/O	Reference output pin(default). Can be used as reference input pin when using external reference.
2	OUT0	O	DAC channel 0 output.
3	OUT1	O	DAC channel 1 output.
4	OUT2	O	DAC channel 2 output.
5	OUT3	O	DAC channel 3 output.
6	GND	GND	Ground pin.
7	VDD	PWR	Analog supply pin.
8	OUT4	O	DAC channel 4 output.
9	OUT5	O	DAC channel 5 output.
10	OUT6	O	DAC channel 6 output.
11	OUT7	O	DAC channel 7 output.
12	$\overline{CS}$	I	Frame synchronization signal for SPI interface.
13	SCLK	I	Clock input for SPI interface.
14	SDI	I	Data input for SPI interface.

Pin		I/O	Description
NO. WQFN	Name		
15	SDO/$\overline{\text{ALARM}}$	O	Data output for SPI interface. It is in high impedance when /CS is high. And the pin can also be configured as /Alarm pin, which is open-drain output to indicate a CRC or reference alarm event.
16	VIO	PWR	IO supply pin.
-	Thermal Pad	-	Thermal pad should be connected to the PCB ground plane.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Supply Voltage	VDD to GND	–0.3	6	V
	VIO to GND	–0.3	6	V
Pin Voltage	DAC Outputs to GND	–0.3	VDD + 0.3	V
	REF to GND	–0.3	VDD + 0.3	V
	Digital Pins to GND	–0.3	VIO + 0.3	V
Input Current	Input Current to any pin except supply pins	−10	10	mA
T_J	Junction Temperature Range	−40	150	℃
T_{stg}	Storage Temperature Range	−60	150	℃

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Nom	Max	Unit
V_{DD}	Analog Supply Voltage	2.7		5.5	V
V_{IO}	Digital IO Supply Voltage	1.7		5.5	V
	Digital Input Voltage	0		VIO	V
V_{REFIN}	Reference Divider Disabled (VDD = 2.7 to 3.3 V)	1.2		(VDD-0.2)/2	V
	Reference Divider Enabled VDD = 2.7 to 3.3 V)	2.4		VDD-0.2	V
	Reference Divider Disabled (VDD = 3.3 to 5.5 V)	1.2		VDD/2	V
	Reference Divider Enabled (VDD = 3.3 to 5.5 V)	2.4		VDD	V
T_J	Operating Junction Temperature	–40		125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
QFN3X3-16	33	29.5	°C/W
WLCSP	68	0.3	°C/W

Electrical Characteristics

All minimum/maximum specifications at V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.7 to 5.5 V, V_{REFIN} = 1.25 to 5.5 V, R_{LOAD} = 2 kΩ to GND, C_{LOAD} = 200 pF to GND, digital inputs at V_{IO} or GND, T_J = –40℃ to +125℃, and all typical specifications at T_J = 25℃, unless otherwise noted.

Parameter		Test Conditions	Min	Typ	Max	Unit
Static Performance **Note**: Static performance specified with DAC outputs unloaded for all gain options, unless otherwise noted. End point fit between codes. 16-bit: Code 256 to 65280.						
Resolution			16			Bits
DNL (TPC2196-QFNR)	Differential nonlinearity		-1	±0.5	1.5	LSB
INL (TPC2196-QFNR)	Integral nonlinearity		-8	±0.5	8	LSB
TUE	Total unadjusted error	REF- DIV = 0		±0.05		%FSR
		REF - DIV = 1		±0.05		%FSR
OE	Offset error	All Gains		±0.75	±4	mV
	Offset error temperature drift			±1.5		uV/°C
GE	Gain error	REF - DIV = 0		±0.05	±0.2	%FSR
		REF - DIV = 1		±0.05	±0.2	%FSR
	Gain error temperature drift			±1.2		ppm of FSR/°C
ZSE	Zero-scale error	DAC code = zero scale		0.5	2.5	mV
	Zero-scale error temperature drift			±1.5		uV/°C
FSE	Full-scale error	REF - DIV = 0		±0.05	±0.15	%FSR
		REF - DIV = 1		±0.05	±0.25	%FSR
	Full-scale error temperature drift			±2		ppm of FSR/°C
Output Characteristics						
	Voltage range	Gain = 2 (BUFF - GAIN = 1, REF-DIV = 0)	0		2 x V REF	V
		Gain = 1 (BUFF - GAIN = 1, REF-DIV = 1)	0		V REF	V
		Gain =1/2 (BUFF - GAIN = 0, REF-DIV = 1)	0		1/2 x V	V

Parameter		Test Conditions	Min	Typ	Max	Unit
					REF	
	Output voltage headroom	to GND or VDD (unloaded)		0.004		V
		to GND or VDD (−10 mA ≤ IOUT ≤ 10 mA)	0.3			V
	Short circuit current (1)	DAC code = full scale. Output shorted to GND		28		mA
		DAC code = zero scale. Output shorted to VDD		25		mA
CL	Capacitive load stability (2)	R_{LOAD} = ∞	0		2	nF
		R_{LOAD} = 2 kΩ	0		10	
RL	Clamp resistance			1		kΩ
	Load regulation	DAC code = midscale, -10 mA <= IOUT<= 10 mA		85		μV/mA
	DC output impedance	DAC code = midscale		0.085		Ω
Dynamic Performance						
Tst	Output voltage settling time	1/4 to 3/4 scale and 3/4 to 1/4 scale settling to ±2 LSB V_{DD} = 5.5 V, V_{REFIN} = 2.5 V, GAIN = 2		6		μs
	Slew rate	V_{DD}= 5.5 V, V_{REFIN}= 2.5 V, GAIN = 2, 10% to 90%		0.8		V/μs
Vn	Output noise	0.1 Hz to 10 Hz, midscale code, V_{DD} = 5.5 V, V_{REFIN} = 2.5 V, GAIN = 2		17		μVpp
	Output noise density	1 kHz, midscale code, V_{DD}= 5.5 V, V_{REFIN} = 2.5 V, GAIN = 2		85		nV/√Hz
		10 kHz, midscale code, V_{DD} = 5.5 V, V_{REFIN} = 2.5 V, GAIN = 2		64		
		1 kHz, midscale code, V_{DD} = 5.5 V, V_{REFIN} = 2.5 V, GAIN = 1		50		
		10kHz, midscale code, V_{DD} = 5.5 V, V_{REFIN} = 2.5 V, GAIN = 1		50		
PSRR ac	AC PSRR	Midscale code, frequency = 60 Hz, amplitude = 200 mVPP superimposed on V_{DD}		76		dB
PSRR dc	DC PSRR	Midscale code, VDD = 5 V±10%		20		uV/V
	Code change glitch impulse	1 LSB change around the major carrier		2.5		nV-s
	Power-up time	DACx-PWDWN 1 to 0 transition. DAC code = full scale. VDD = 5.5 V, VREFIN = 2.5 V, Gain = 2 (3)		14.2		μs

Parameter		Test Conditions	Min	Typ	Max	Unit
	Power-down glitch amplitude	DAC code = zero scale. VDD = 5.5 V, VREFIN = 2.5 V, Gain = 2. CLOAD = 50 pF		25		mV
	Channel-to-channel AC crosstalk	Measured DAC output at midscale, Code 32 to full-scale swing on adjacent channel		1		nV-s
	Channel-to-channel DC crosstalk	Measured DAC output at midscale, all other DAC outputs at full-scale, Gain = 1		1		µV
		Measured DAC output at midscale, all other DAC outputs at full-scale, Gain = 2		10		µV
Internal Reference Characteristics						
VREF OUT	Internal reference voltage	T_A = 25°C	2.494	2.5	2.506	V
TC	Internal reference temperature coefficient	T_J = −40°C to 125°C		8		ppm/°C
	Internal reference impedance			0.1		Ω
	Internal reference output noise	0.1 Hz to 10 Hz		15		µVPP
	Internal reference noise density	10 kHz, REFLOAD = 10 nF		370		nV/sqrtHz
	Internal reference load current			±5		mA
	Reference load regulation	source and sink		100		uV/mA
	Internal reference load cap	actual capacitance	300		2200	nF
External Reference Characteristics						
	Reference input current	V_{REFIN} = 2.5 V		25		uA
	Reference input impedance			100		kΩ
	Reference input capacitance			5		pF
Digital Input Characteristics						
VIH	High-level input voltage		0.7 × VIO			V
VIL	Low-level input voltage				0.3 × VIO	V
	Input current			±2		µA
	Input pin capacitance			2		pF
Digital Output Characteristics						
VOH	High-level output voltage	I_{LOAD} = 0.2 mA	VIO – 0.4			V
VOL	Low-level output voltage	I_{LOAD} = 0.2 mA			0.4	V
	Output pin capacitance			4		pF
Power Consumption Characteristics						
I_{VDD}	VDD supply current	Active mode. Internal reference enabled. Gain = 1.		5	6	mA

Parameter		Test Conditions	Min	Typ	Max	Unit
		DAC code = full scale. Outputs unloaded. SPI static				
		Active mode. Internal reference disabled. Gain = 1. DAC code = full scale. Outputs unloaded. SPI static		4.5	5.5	
		Power-down		15		μA
I_{VIO}	VIO supply current			6.8	15	

Timing Requirements

all minimum/maximum specifications at V DD = 2.7 to 5.5 V, VIO = 1.7 to 5.5 V, V_{REFIN} = 1.25 to 5.5 V, R_{LOAD} = 2 kΩ to GND, C_{LOAD} = 200 pF to GND, digital inputs at V_{IO} or GND, T_J = –40℃ to +125℃ and all typical specifications at T_J = 25℃.

Parameter		Min	Nom	Max	Unit
SPI Timing Requirements					
f_{SCLK}	SCLK frequency			20	MHz
$t_{SCLKHIGH}$	SCLK high time	23			ns
$t_{SCLKLOW}$	SCLK low time	23			ns
t_{SDISU}	SDI setup time	7			ns
t_{SDIHD}	SDI hold time	7			ns
t_{SDOTOZ}	SDO driven to tri-state	0		15	ns
t_{SDOTOD}	SDO tri-state to driven	0		18	ns
t_{SDODLY}	SDO output delay	0		18	ns
t_{CSSU}	CS setup time	10			ns
t_{CSHD}	CS hold time	20			ns
t_{CSHIGH}	CS high time	20			ns

(1) Values are based on design and characterization.

Timing Diagrams

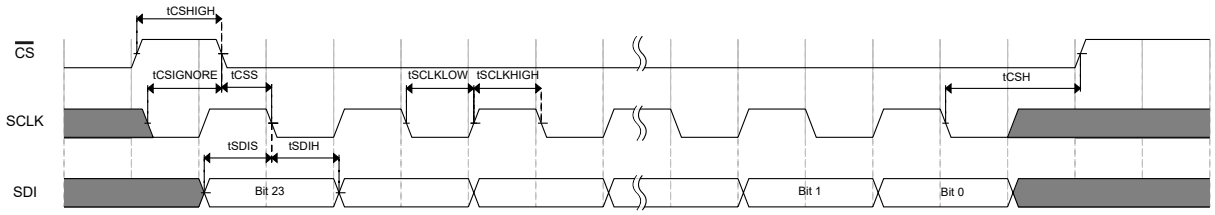


Figure 1. SPI Write Timing Diagram

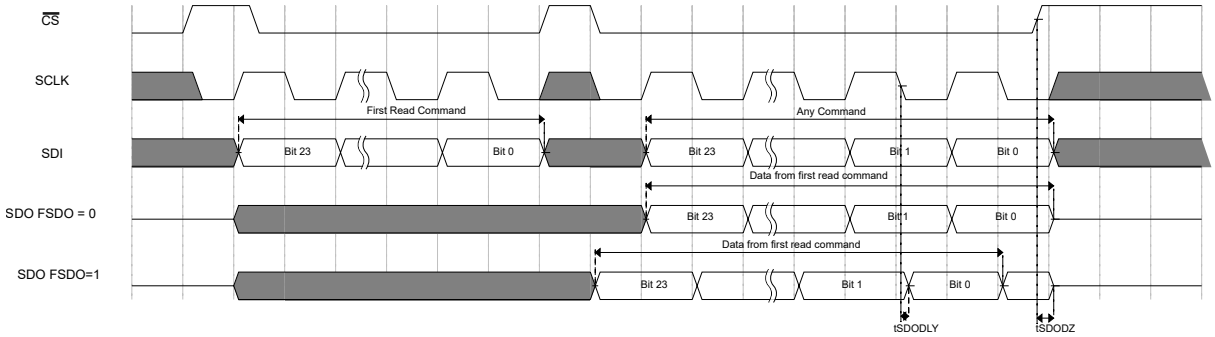


Figure 2. SPI Read Timing Diagram

Typical Performance Characteristics

All test conditions: At T_A = 25°C, V_{DD} = 5.5 V, Internal Reference = 2.5 V, Gain = 2, DAC outputs unloaded, unless otherwise noted.

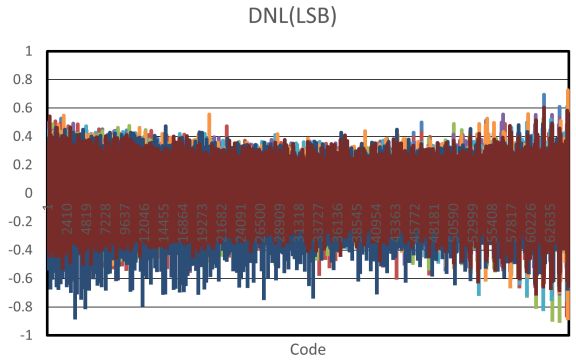


Figure 3. DNL

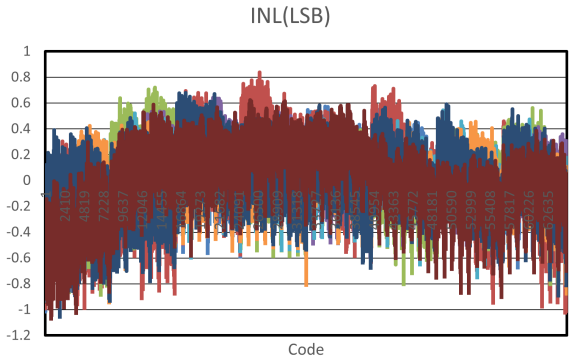


Figure 4. INL

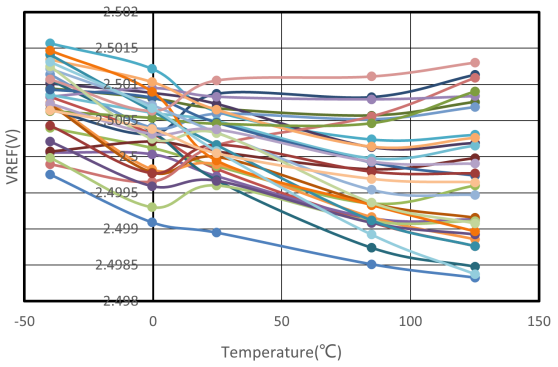


Figure 5. VREF vs. Temperature

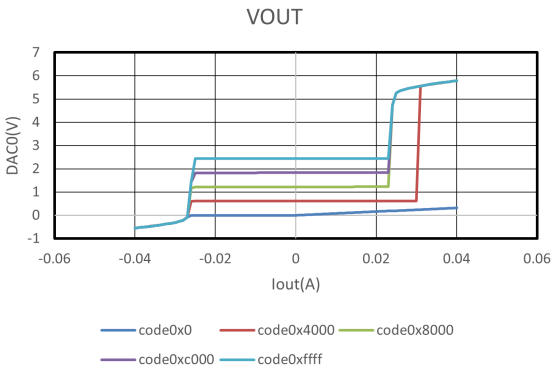


Figure 6. Vout vs. Iout

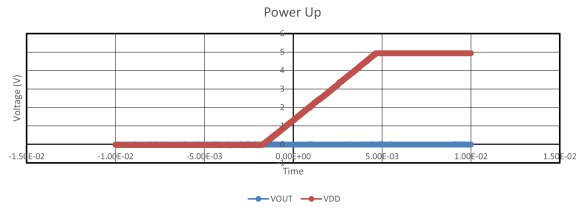


Figure 7. V_{out} at Power Up

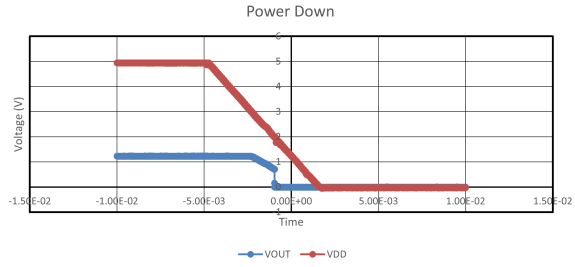


Figure 8. V_{out} at Power Down

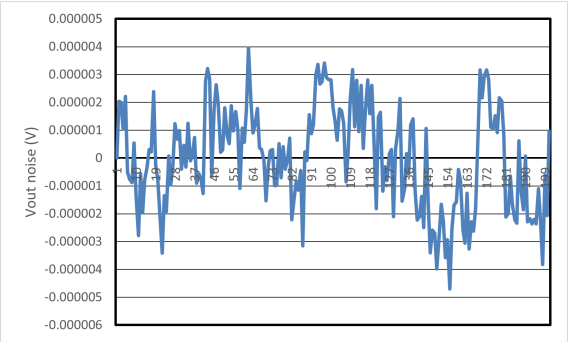
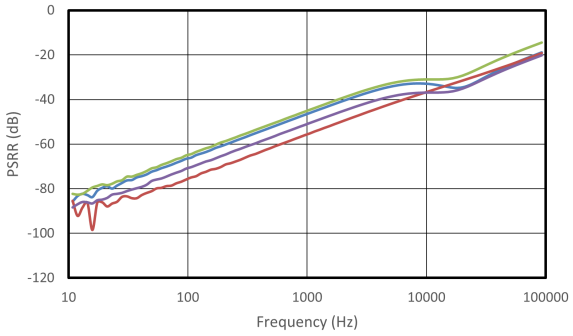


Figure 9. Vout Noise



V_{DD} = 5 V, V_{IO} = 3.3 V, Gain = 1

Figure 10. PSRR

Detailed Description

Overview

The TPC2196 is an 8-channel, high-accurate, voltage-output digital-to-analog converters (DACs), with 16-bit resolution. The device provides a 2.5-V internal reference and output range can be selected to be 1.25 V (gain = ½), 2.5 V (gain = 1) or 5 V (gain = 2).

Functional Block Diagram

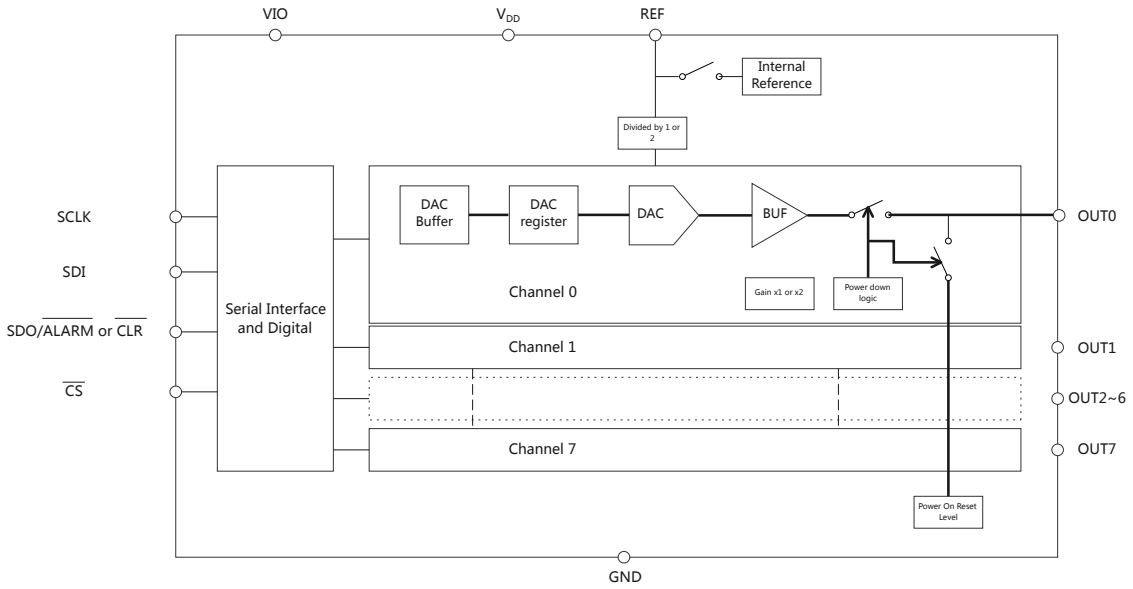


Figure 11. Functional Block Diagram

Feature Description

DAC Transfer Function

The DAC output voltage is given by the following equation:

$$V_{OUT} = \frac{CODE}{2^n} \times \frac{V_{REF}}{DIV} \times GAIN \quad (1)$$

CODE = decimal value of the binary code in the DAC register.

n: DAC resolution bits.

VREF = DAC reference voltage.

DIV: 1 or 2 as set by REF-DIV bit.

Gain: 1 or 2 as set by BUFF-GAIN bit.

DAC Register Structure

Data written to the DAC data registers is initially stored in the DAC buffer registers. And then the transfer of data from the DAC buffer registers to the active DAC registers, can be selected to happen immediately (asynchronous mode) or initiated by an LDAC trigger (synchronous mode). Once the DAC active registers are updated, the DAC outputs change to the new values. When a DAC Data register is read, the value held in the DAC buffer register is returned (not the value in the DAC active register).

The SYNC-EN bit controls the update mode for each DAC channel. In asynchronous mode, writing to the DAC data register results in an immediate update of the DAC active register and DAC output on the CS rising edge. In synchronous mode, writing to the DAC data register does not update the DAC output, but the update happens when an LDAC trigger event is generated through the LDAC bit. The synchronous update mode can update multiple DAC outputs simultaneously.

A DAC broadcast register is provided to simultaneously update multiple DAC outputs with the same value by a single register write. Each DAC channel can be configured to be updated or not by a broadcast command, through the corresponding DAC-BRDCAST-EN bit. A register write to the BRDCAST-DATA register forces selected DAC channels that have been configured for broadcast operation to update their outputs. The DAC outputs update to the broadcast value on CS rising edge independently of their synchronous mode configuration.

Reference

The device provides an internal 2.5-V reference, which is enabled by default after power up. The internal reference is available on the REF pin. External reference is supported by disabling the enable reference by the CONFIG register.

The reference voltage from the internal reference or an external one can be divided by a factor of two by setting the REF-DIV bit.

Reset Options

After power up, and the V_{DD} and V_{IO} supplies have settled, the Power On Reset (POR) function enables all registers to initialize to their default values. DAC output remains at the power-up voltage.

A software reset is provided by writing the reserved code 0x1010 to SOFT-RESET bits.

Functional Modes

Stand-Alone Operation

A serial interface access cycle can be initiated by asserting the $\overline{CS}$ pin low.

SDI data are clocked on SCLK falling edges. A regular serial interface access cycle is 24 bits long with error checking disabled and 32 bits long with error checking enabled.

If the access cycle contains more than the minimum clock edges, only the last 24 or 32 bits are used by the device.

Daisy Chain Operation

For systems that contain more than one device, the SDO pin can be used to daisy-chain them together. Daisy-chain operation is useful in reducing the number of serial interface lines.

By connecting the SDO output of the first device to the SDI input of the next device in the chain, a multiple-device interface is constructed. Each device in the system requires 24 clock pulses. As a result, the total number of clock cycles must be equal to 24 × N, where N is the total number of devices in the daisy chain.

The first falling edge on the CS pin starts the operation cycle. If more than 24 SCLK pulses are applied while the CS pin is kept low, the data ripples out of the shift register and is clocked out on the SDO pin either on the falling edge or rising edge of SCLK according to the FSDO bit.

Frame Error Checking

Error checking is provided that can be used to check the integrity of SPI data communication. This feature can be enabled by setting the CRC-EN bit.

The error checking scheme is based on the CRC-8-ATM (HEC) polynomial $x^8 + x^2 + x + 1$ (that is, 100000111).

When error checking is enabled, the serial interface access cycle width is 32 bits. The normal 24-bit SPI data is appended with an 8-bit CRC polynomial by the host processor before feeding it to the device.

Table 2. Error Checking Serial Interface Access Cycle

Bit	Field	Description
31	RW	Identifies the communication as a read or write command to the addressed register. R/W = 0 sets a write operation. R/W = 1 sets a read operation.
30	CRC-ERROR	Reserved bit. Set to zero.
29:28	Reserved	Reserved bits. Must be filled with zeros.
27:24	A[3:0]	Register address. Specifies the register to be accessed during the read or write operation.
23:8	DI[15:0]	Data cycle bits. If a write command, the data cycle bits are the values to be written to the register with address A[3:0]. If a read command, the data cycle bits are don't care values.
7:0	CRC	8-bit CRC polynomial.

The device decodes the 32-bit access cycle to compute the CRC remainder on CS rising edges. If no error exists, the CRC remainder is zero and the data is accepted by the device.

A write operation failing the CRC check causes the data to be ignored by the device. After the write command, a second access cycle can be issued to determine the error checking result (CRC-ERROR bit) on the SDO pin.

Table 3. Write Operation Error Checking Cycle

Bit	Field	Description
31	RW	Echo RW from previous access cycle (RW = 0).
30	CRC-ERROR	Returns a 1 when a CRC error is detected, 0 otherwise.
29:28	Reserved	Echo bits 29:28 from previous access cycle (all zeros).
27:24	A[3:0]	Echo address from the previous access cycle.
23:8	DO[15:0]	Echo data from the previous access cycle.
7:0	CRC	Calculated CRC value of bits 31:8.

A read operation must be followed by a second access cycle to get the requested data on the SDO pin. The error check result (CRC-ERROR bit) from the read command is output on the SDO pin.

Table 4. Read Operation Error Checking Cycle

Bit	Field	Description
31	RW	Echo RW from previous access cycle (RW = 1).

Bit	Field	Description
30	CRC-ERROR	Returns a 1 when a CRC error is detected, 0 otherwise.
29:28	Reserved	Echo bits 29:28 from the previous access cycle (all zeros).
27:24	A[3:0]	Echo address from the previous access cycle.
23:8	DO[15:0]	Readback data requested on the previous access cycle.
7:0	CRC	Calculated CRC value of bits 31:8.

Power Down Mode

The device's output amplifiers and internal reference can be independently powered down through the CONFIG register. At power-up all output channels and the device internal reference are active by default. A DAC output channel in power-down mode is connected internally to GND through a 1 kΩ resistor.

Serial Interface

The TPC219 family supports an SPI-compatible interface.

Register Table

Register	Type	Reset	Address Bits	Data Bits															
				D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NOP	W	16'h0000	7'h00	NOP															
DEVICE ID	R	-	7'h01	DEVICE ID														VERSION ID	
SYNC	R/W	16'hFF00	7'h02	DACx-BRDCAST-EN								DACx-SYNC-EN							
CONFIG	R/W	16'h0000	7'h03	Reserved		ALMSEL	ALMEN	CRCEN	FSDO	DSDO	REFPWDWN	DACx-PWDWN							
GAIN	R/W	16'h0000 16'h00FF	7'h04	Reserved					CLR-4TO7-MSK	CLR0TO3-MSK	REFDIVEN	BUFFx-GAIN							
TRIGGER	W	16'h0000	7'h05	Reserved											LDAC	SOFT-RESET[3:0]			
BRDCAST	R/W	16'h0000	7'h06	BRDCAST-DATA[15:0]															

Register	Type	Reset	Address Bits	Data Bits															
				D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	R/W	16'h0000	7'h07	Reserved															REFALM
DAC0	R/W	16'h0000 16'h8000	7'h08	DAC0-DATA[15 : 0]															
DAC1	R/W	16'h0000 16'h8000	7'h09	DAC1-DATA[15 : 0]															
DAC2	R/W	16'h0000 16'h8000	7'h0a	DAC2-DATA[15 : 0]															
DAC3	R/W	16'h0000 16'h8000	7'h0b	DAC3-DATA[15 : 0]															
DAC4	R/W	16'h0000 16'h8000	7'h0c	DAC4-DATA[15 : 0]															
DAC5	R/W	16'h0000 16'h8000	7'h0d	DAC5-DATA[15 : 0]															
DAC6	R/W	16'h0000 16'h8000	7'h0e	DAC6-DATA[15 : 0]															
DAC7	R/W	16'h0000 16'h8000	7'h0f	DAC7-DATA[15 : 0]															

NOP Register

Bit	Field	Type	Reset	Description
15:0	NOP	W	0x0000	No operation. Write 0000h for proper no-operation command

Device ID Register

Bit	Field	Type	Reset	Description
15:2	DEVICEID	R	----	Device ID: D15 Reserved - 0 D14:12 Resolution - 000 (16-bit); 001 (14-bit); 010 (12-bit) D11:8 Channels - 1000 (8 channels) D7 Reset - 0 ; 1 reset- to-midscale) D6:2 Reserved - 00101
1:0	VERSIONID	R	10	Version ID. Subject to change

Sync Register

Bit	Field	Type	Reset	Description
15	DAC7-BRDCAST-EN	R/W	1	When set to 1 the corresponding DAC is set to update its output after a serial interface write to the BRDCAST register. When cleared to 0 the corresponding DAC output remains unaffected after a serial interface write to the BRDCAST register.
14	DAC6-BRDCAST-EN	R/W	1	
13	DAC5-BRDCAST-EN	R/W	1	
12	DAC4-BRDCAST-EN	R/W	1	
11	DAC3-BRDCAST-EN	R/W	1	
10	DAC2-BRDCAST-EN	R/W	1	
9	DAC1-BRDCAST-EN	R/W	1	
8	DAC0-BRDCAST-EN	R/W	1	
7	DAC7-SYNC-EN	R/W	0	When set to 1 the corresponding DAC output is set to update in response to an LDAC trigger (synchronous mode). When cleared to 0 the corresponding DAC output is set to update immediately on a CS rising edge (asynchronous mode).
6	DAC6-SYNC-EN	R/W	0	
5	DAC5-SYNC-EN	R/W	0	
4	DAC4-SYNC-EN	R/W	0	
3	DAC3-SYNC-EN	R/W	0	
2	DAC2-SYNC-EN	R/W	0	
1	DAC1-SYNC-EN	R/W	0	
0	DAC0-SYNC-EN	R/W	0	

Config Register

Bit	Field	Type	Reset	Description
15:14	Reserved	—	00	Reserved for factory use
13	ALM-SEL	R/W	0	ALARM Select 0:$\overline{\text{ALARM}}$pin is CRC-ERROR 1: $\overline{\text{ALARM}}$ pin is REF-ALARM
12	ALM-EN	R/W	0	Configure SDO/$\overline{\text{ALARM}}$ pin. When 1: SDO/$\overline{\text{ALARM}}$ pin is an active-low, open-drain, alarm pin. An external 10 kΩ pullup resistor to V_{IO}required. FSDO and DSDO bits are ignored. When 0: SDO/ALARM pin is a serial interface, push-pull, SDO pin
11	CRC-EN	R/W	0	CRC enable bit. Set to 1 to enable CRC. Set to 0 to disable
10	FSDO	R/W	0	Fast SDO bit (half-cycle speedup). When 0, SDO updates on an SCLK rising edge. When 1, SDO updates a half-cycle earlier, during an SCLK falling edge.
9	DSDO	R/W	0	Disable SDO bit. When1, SDO is always tri-stated. When 0, SDO is driven while $\overline{\text{CS}}$ is low, and tri-stated while $\overline{\text{CS}}$ is high
8	REF-PWDWN	R/W	0	When set to 1 disables the device internal reference

Bit	Field	Type	Reset	Description
7	DAC7-PWDWN	R/W	0	When set to 1 the corresponding DAC is set in power-down mode and its output is connected to GND through a 1 kΩ internal resistor.
6	DAC6-PWDWN	R/W	0	
5	DAC5-PWDWN	R/W	0	
4	DAC4-PWDWN	R/W	0	
3	DAC3-PWDWN	R/W	0	
2	DAC2-PWDWN	R/W	0	
1	DAC1-PWDWN	R/W	0	
0	DAC0-PWDWN	R/W	0	

Gain Register

Bit	Field	Type	Reset	Description
15:11	Reserved	—	0	Reserved for factory use.
10	Reserved / CLR-4TO7-MSK	R/W	0	For non-clear pin device: Reserved for factory use. For clear pin device. When cleared to 0 the corresponding DAC group is set to clear in response to a logic-low value on the $\overline{CLR}$ pin. When set to 1 the corresponding DAC group remains unaffected by the $\overline{CLR}$ pin.
9	Reserved / CLR-0TO3-MSK	R/W	0	
8	REFDIV-EN	R/W	0/1	When set to 1 the reference voltage is internally divided by a factor of 2. When cleared to 0 the reference voltage is unaffected.
7	BUFF7-GAIN	R/W	0/1	When set to 1 the buffer amplifier for corresponding DAC has a gain of 2. Default value for the default middle scale output devices. When cleared to 0 the buffer amplifier for corresponding DAC has a gain of 1. Default value for the default zero-scale output devices.
6	BUFF6-GAIN	R/W	0/1	
5	BUFF5-GAIN	R/W	0/1	
4	BUFF4-GAIN	R/W	0/1	
3	BUFF3-GAIN	R/W	0/1	
2	BUFF2-GAIN	R/W	0/1	
1	BUFF1-GAIN	R/W	0/1	
0	BUFF0-GAIN	R/W	0/1	

Trigger Register

Bit	Field	Type	Reset	Description
15:5	Reserved	—	0	Reserved for factory use.
4	LDAC	W	0	Set this bit to 1 to synchronously load those DACs that have been set in synchronous mode in the SYNC register.
3:0	SOFT-RESET[3:0]	W	0x0	When set to the reserved code 1010 resets the device to its default state.

Broadcast Register

Bit	Field	Type	Reset	Description
15:0	BRDCAST-DATA[15:0]	R/W	0x0000	Writing to the BRDCAST register forces those DAC channels that have been set to broadcast in the SYNC register to update their active data register with the BRDCAST-DATA value. Data are MSB aligned in straight binary format and follows the format below: 16bit version: { DATA[15:0] } 14bit version: { DATA[13:0], x, x } 12bit version: { DATA[11:0], x, x, x, x } x – Don't care bits

Status Register

Bit	Field	Type	Reset	Description
15:1	Reserved	—	0	Reserved for factory use.
0	REF-ALM	R	0	Reference alarm bit. Reads 1 when the difference between V_{REF}/DIV and V_{DD} is below the required minimum analog threshold. Reads 0 otherwise.

DAC Register (Address = 0x8 to 0xF)

Bit	Field	Type	Reset	Description
15:0	DACx-DATA[15:0]	R/W	0x0000 or 0x8000	Stores the 16-, 14- or 12-bit data to be loaded to DACx in MSB aligned straight binary format. The default value is zero-code for default zero scale output version, midscale-code for the default middle scale output version. Data follows the format below: 16bit version: { DATA[15:0] } 14bit version: { DATA[13:0], x, x } 12 bit version: { DATA[11:0], x, x, x, x } x – Don't care bits

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPC2196 has high linearity, small package size, and an internal reference, which is suitable for applications such as optical networking, test equipment, industrial automation, and data acquisition systems.

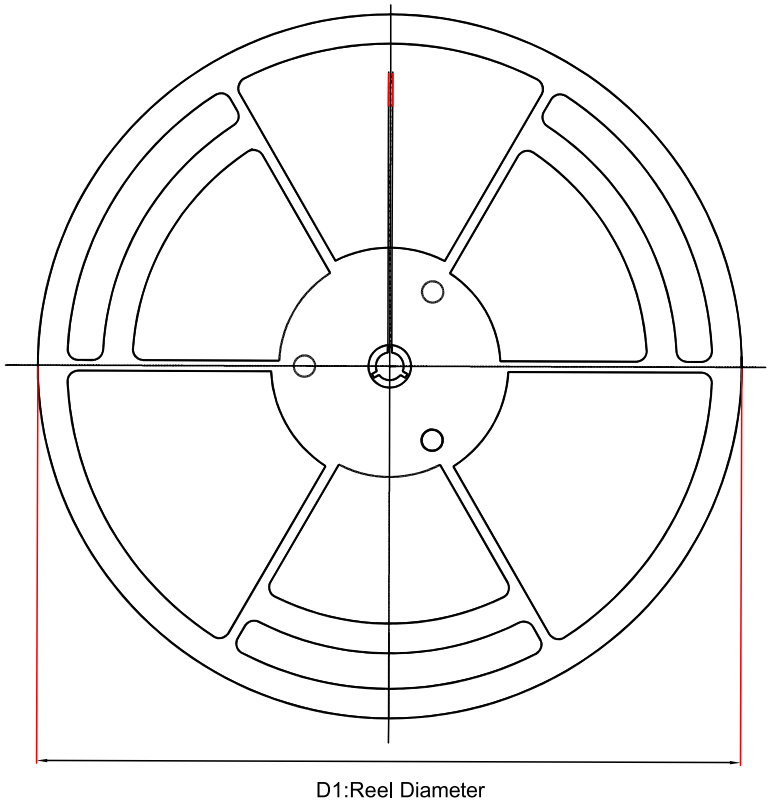
Be aware that when the external reference is used, make sure that the TPC2196 is powered up first, and then power up the external reference, to avoid forward biasing and potential damage of the parasitic diode between REF and VDD.

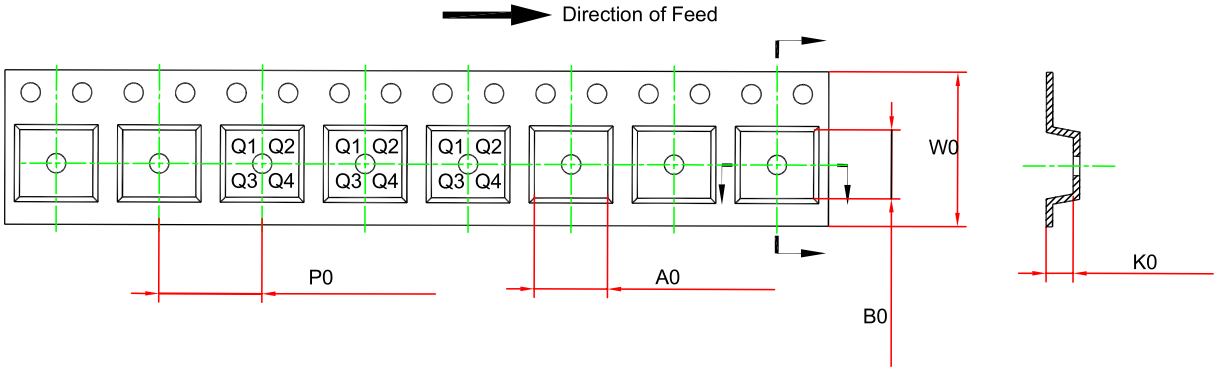
Layout

Layout Guideline

- Both input capacitors and output capacitors must be placed to the device pins as close as possible.
- It is recommended to bypass the input pin to ground with a 0.1-μF bypass capacitor.
- It is recommended to use wide and thick copper to minimize I×R drop and heat dissipation.
- Exposed pad must be connected to the PCB ground plane directly, and the copper area must be as large as possible.

Tape and Reel Information



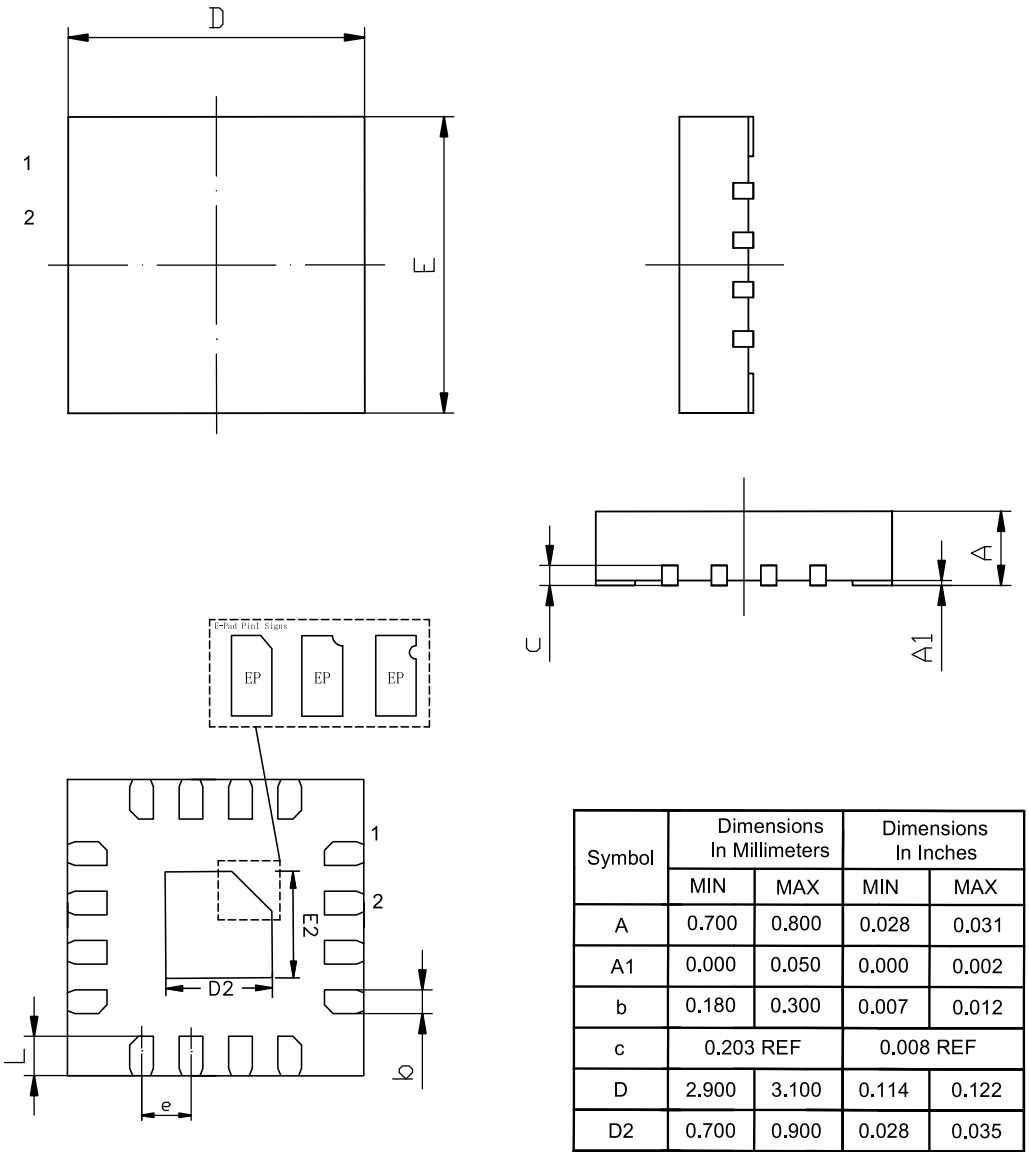


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPC2196-QFNR	QFN3X3-16	330	17.6	3.3	3.3	1.1	8	12	Q1

Package Outline Dimensions

QFN3X3-16

Package Outline Dimensions QFN(QFN3X3-16-C)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.180	0.300	0.007	0.012
c	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D2	0.700	0.900	0.028	0.035
E	2.900	3.100	0.114	0.122
E2	0.700	0.900	0.028	0.035
e	0.500 BSC		0.020 BSC	
L	0.300	0.500	0.012	0.020

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPC2196-QFNR	−40 to 125°C	QFN3X3-16	2196	1	Tape and Reel, 4000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

IMPORTANT NOTICE AND DISCLAIMER

Performance Information. Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

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