17-Channel High-Accuracy Battery Pack Monitor and Protector

Features

- Measures up to 17 Cells in Series
- Voltage Measurement
  - 2-mV Cell Voltage Measurement Accuracy (typical)
  - 50-ms Conversation Time for 17 Cells (Nominal)
- Current Measurement
  - ±100-mV Measurement Range Across Sense Resistor
  - 50-μV Current Measurement Accuracy (typical)
- Support Low Leakage Current
  - Deep Sleep Mode: 25 μA
  - Sleep Mode: 30 μA
  - Shutdown Mode: 2.5 μA
- Extensive Protection Including Voltage, Current, Temperature
- High Voltage Tolerance of ±80 V on Cell Connect
- Support for Temperature Sensing Using Internal Sensor and up to 4 External Thermistors
- Integrated Programmable Memory for Customer Use
- Integrated Secondary Chemical Fuse Drive Protection
- Autonomous or Host-controlled Cell Balance
- 1-Mbps SPI Communication Interface
- Operational Temperature Range: −40℃ to +125℃
- LQFP7x7-48 Package

Applications

- Telecom 48 V UPS
- E-bike or E-motor or LEV
- Garden Tools
- Drones

Description

The TPB76016 is a multicell battery stack monitor that measures up to 17 series battery cells with a total measurement error of less than 5 mV typical. The cell measurement range is from 0 V to 5 V, with supporting Li-ion, Li-Polymer, and LiFePO4 battery types. All 17 cells can be measured within 50 ms. The TPB76016 also integrates an ADC to measure charge/discharge current and provides a coulomb counter.

The TPB76016 integrates a safety engine that provides reliability protection for OV, UV, OTC, UTC, OTD, UTD, COC, DOC, SCD, SOV with programmable detection threshold and delay time. The COC, DOC, and SCD use a hardware comparator for fast protection.

The TPB76016 provides internal cell balance, the cell balance current is 50 mA, for a higher cell balance current, an external cell balance circuit may be used.

The device has a host communication peripheral supporting 1-Mbps SPI. The TPB76016 is available in the LQFP7x7-48 package, and the operation temperature range is from -40℃ to 125℃.

Simplified Application Circuit

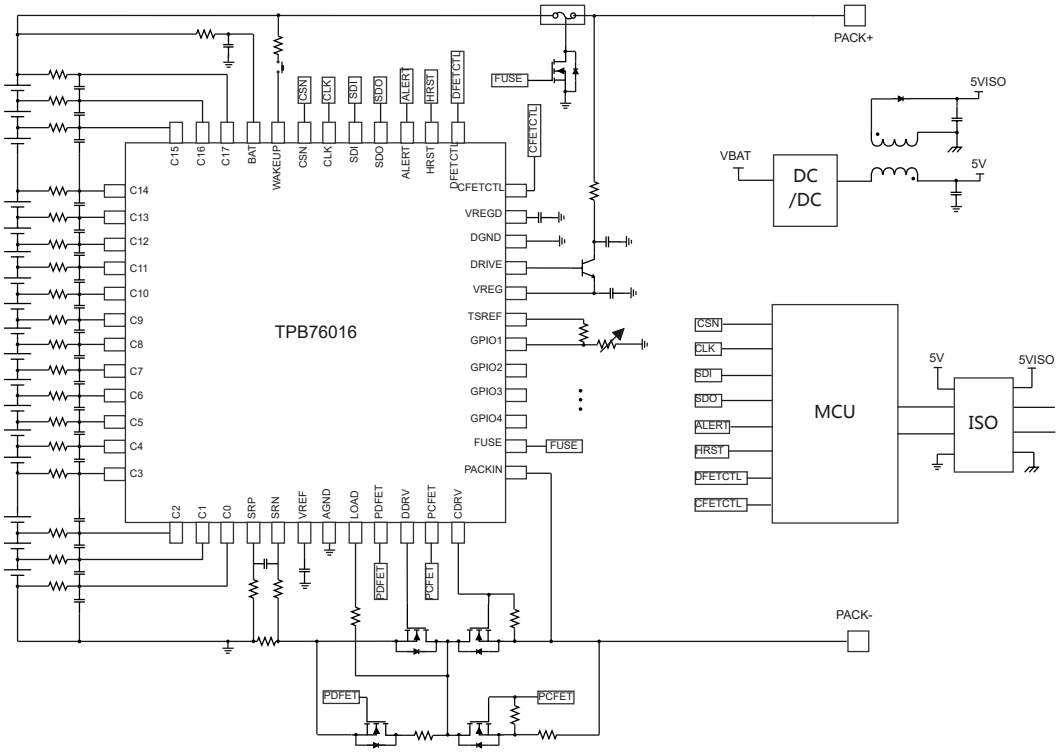


Table of Contents

Product Family Table

Order Number	MSL	Marking Information	Package
TPB76016-QP3R	3	76016	LQFP-48

Revision History

Date	Revision	Notes
2024-09-18	Rev. A.0	Initial release
2025-03-08	Rev. A.1	Corrected typo of t_{COC_DLY}, t_{DOC_DLY}, t_{SCD_DLY} in the EC table Corrected typos in description Updated ALERT pin description Updated Host mode description Updated SPI Interface description

Pin Configuration and Functions

TPB76016
LQFP7x7-48
Top View

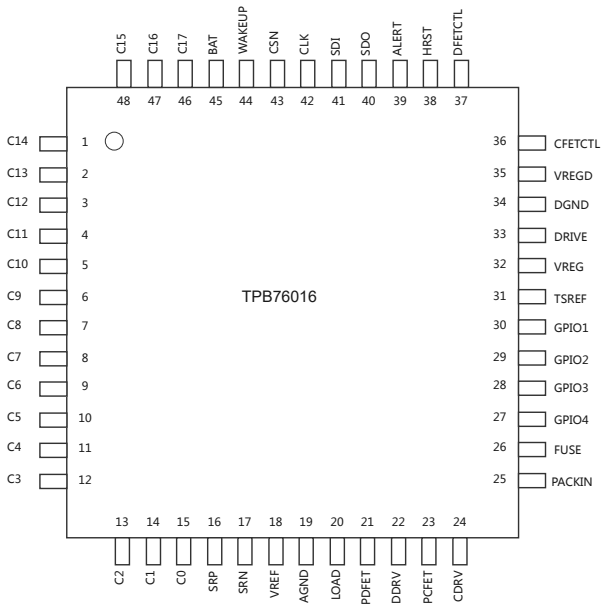


Table 1. Pin Functions: TPB76016

No	Name	I/O	Description
1	C14	I	Cell voltage sense connection 14. Connect C14 to the junction of the positive terminal of cell 14 and the negative terminal of cell 15 through a resistor.
2	C13	I	Cell voltage sense connection 13. Connect C13 to the junction of the positive terminal of cell 13 and the negative terminal of cell 14 through a resistor.
3	C12	I	Cell voltage sense connection 12. Connect C12 to the junction of the positive terminal of cell 12 and the negative terminal of cell 13 through a resistor.
4	C11	I	Cell voltage sense connection 11. Connect C11 to the junction of the positive terminal of cell 11 and the negative terminal of cell 12 through a resistor.
5	C10	I	Cell voltage sense connection 10. Connect C10 to the junction of the positive terminal of cell 10 and the negative terminal of cell 11 through a resistor.
6	C9	I	Cell voltage sense connection 9. Connect C9 to the junction of the positive terminal of cell 9 and the negative terminal of cell 10 through a resistor.

No	Name	I/O	Description
7	C8	I	Cell voltage sense connection 8. Connect C8 to the junction of the positive terminal of cell 8 and the negative terminal of cell 9 through a resistor.
8	C7	I	Cell voltage sense connection 7. Connect C7 to the junction of the positive terminal of cell 7 and the negative terminal of cell 8 through a resistor.
9	C6	I	Cell voltage sense connection 6. Connect C6 to the junction of the positive terminal of cell 6 and the negative terminal of cell 7 through a resistor.
10	C5	I	Cell voltage sense connection 5. Connect C5 to the junction of the positive terminal of cell 5 and the negative terminal of cell 6 through a resistor.
11	C4	I	Cell voltage sense connection 4. Connect C4 to the junction of the positive terminal of cell 4 and the negative terminal of cell 5 through a resistor.
12	C3	I	Cell voltage sense connection 3. Connect C3 to the junction of the positive terminal of cell 3 and the negative terminal of cell 4 through a resistor.
13	C2	I	Cell voltage sense connection 2. Connect C2 to the junction of the positive terminal of cell 2 and the negative terminal of cell 3 through a resistor.
14	C1	I	Cell voltage sense connection 1. Connect C1 to the junction of the positive terminal of cell 1 and the negative terminal of cell 2 through a resistor.
15	C0	I	Cell voltage sense connection 0. Connect C0 to the junction of the negative terminal of cell 1 through a resistor.
16	SRP	I	Current sense positive input pin.
17	SRN	I	Current sense negative input pin.
18	VREF	O	Voltage reference. Connect a bypass capacitor to ground. Do not connect any external load on this pin.
19	AGND	GND	Analog ground
20	LOAD	I	Load detect pin.
21	PDFET	O	Predischarge FET control pin.
22	DDRV	O	Discharge FET control pin.
23	PCFET	O	Precharge FET control pin.
24	CDRV	O	Charge FET control pin.
25	PACKIN	I	Pack voltage input pin.
26	FUSE	O	Fuse drive.
27	GPIO4	I/O	General purpose input/output 4. GPIO4 is configurable as an ADC input to measure an external temperature sensor (NTC) or other DC voltage.

No	Name	I/O	Description
28	GPIO3	I/O	General purpose input/output 3. GPIO3 is configurable as an ADC input to measure an external temperature sensor (NTC) or other DC voltage.
29	GPIO2	I/O	General purpose input/output 2. GPIO2 is configurable as an ADC input to measure an external temperature sensor (NTC) or other DC voltage.
30	GPIO1	I/O	General purpose input/output 1. GPIO1 is configurable as an ADC input to measure an external temperature sensor (NTC) or other DC voltage.
31	TSREF	O	Temperature bias output voltage for NTC
32	VREG	I	Input pin for internal supply. 2.2μF capacitor is recommended to connected to ground.
33	DRIVE	O	Base control for external pre-regulator transistor.
34	DGND	GND	Digital ground.
35	VREGD	O	Digital voltage supply for GPIO.
36	CFETCTL	I	Charge FET control input pin.
37	DFETCTL	I	Discharge FET control input pin.
38	HRST	I	Hardware reset pin.
39	ALERT	O	Interruption output pin. ALERT is open drain output, it outputs an 10-ms low pulse when fault occurs, if the fault persists, the ALERT output remains low.
40	SDO	O	Slave data output pin.
41	SDI	I	Slave data input pin.
42	CLK	I	Clock input pin.
43	CSN	I	Selection input pin. Active low.
44	WAKEUP	I	External wakeup pin from shutdown mode. High active. Connect to high if using this device in standalone protection mode always.
45	BAT	I	Battery stack connection.
46	C17	I	Cell voltage sense connection 17. Connect C17 to the positive terminal of top cell through a resistor.
47	C16	I	Cell voltage sense connection 16. Connect C16 to the junction of the positive terminal of cell 16 and the negative terminal of cell 17 through a resistor.
48	C15	I	Cell voltage sense connection 15. Connect C15 to the junction of the positive terminal of cell 15 and the negative terminal of cell 16 through a resistor.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
Input Voltage	BAT to AGND	−0.3	80	V
	Cn to Cn-1 (n=1 to 17)	−80	80	V
	Cn to AGND (n=1 to 17)	−0.3	80	V
	C0 to AGND	−0.3	6.5	V
	GPIOn to AGND (n=1 to 4)	−0.3	6.5	V
	CSN, SDI, CLK, CFETCTL, DFETCTL, HRST to AGND	−0.3	6.5	V
	SRN, SRP to AGND	−0.5	0.7	V
	SRN, SRP to AGND (1ms pulse, 10Ω resistor in series with pin externally)	−0.5	3.6	V
	LOAD to AGND, WAKEUP to AGND	−0.3	80	V
	PACKIN to BAT	−80	0	V
Output Voltage	VREG, VREGD to AGND	−0.3	6.5	V
	VREF, TSREF to AGND	−0.3	6.5	V
	SDO to AGND	−0.3	6.5	V
	DRIVE to AGND	−0.3	6.5	V
	CDRV, PCFET to BAT	−80	0	V
	DDRV, PDFET to AGND	−0.3	20	V
	FUSE to AGND	−0.3	20	V
Output Current	DRIVE, GPIOn(n=1-4), SDO current		10	mA
	FUSE		100	mA
	DDRV, PDFET current		50	mA
	VREGD current		40	mA
	TSREF current		20	mA
T_A	Operating Temperature Range	−40	125	°C
T_J	Junction Temperature Range	−40	150	°C
T_{STG}	Storage Temperature Range	−55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.
(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	2000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
V_{BAT}	Total Battery Module Voltage (VBAT), full functionality available	12		75	V
V_{CELL_DIFF}	Cell Differential Voltage (Cn−Cn−1, n=1 to 17)	0		5	V
V_{CELL_COM}	Cell Common Voltage (C0−AGND)	0		0.3	V
V_{IO}	GPIOn (n=1 to 4), SDI, SDO, CSN, CLK, HRST, DFETCTL, CFETCTL input voltage	0		5	V
I_{IO}	GPIOn (n=1 to 6), SDO current	−5		5	mA
I_{TSREF}	Bias Voltage for External Pull up for Temperature Current			10	mA
T_{OPR}	Operating Temperature	−40		125	℃

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
LQFP7x7-48	50.3	17.4	°C/W

Electrical Characteristics

All test conditions: V_{BAT} = 62 V, T_A = −40°C to 85°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage Measurement ADC						
V_{VADC_IN}	Input Voltage Range for Cell Voltage Measurement		0		5	V
V_{VADC_LSB}	Measurement Resolution			0.1		mV/Bit
V_{OFFSET}	ADC Offset Voltage			0.1		mV
G_{ERR}	ADC Gain Error			0.01		%
V_{TME}	Total Measurement Error	Cn − Cn-1 = 1.5 V, T_A= −20℃ to 65℃, n =1 to 17	−5.0		5.0	mV
		Cn − Cn-1 = 3.1 V, T_A= −20℃ to 65℃, n =1 to 17	−5.0		5.0	mV
		Cn − Cn-1 = 3.9 V, T_A= −20℃ to 65℃, n = 1 to 17	−5.0		5.0	mV
		Cn − Cn-1= 4.5V, T_A=-20℃ to 65℃, n=1 to 17	−5.0		5.0	mV
		Cn − Cn-1 = 1.5 V, T_A= −40℃ to 85℃, n = 1 to 17	−5.0		5.0	mV
		Cn − Cn-1 = 3.1 V, T_A= −40℃ to 85℃, n=1 to 17	−5.0		5.0	mV
		Cn − Cn-1 = 3.9 V, T_A= −40℃ to 85℃, n=1 to 17	−5.5		5.5	mV
		Cn − Cn-1 = 4.5 V, T_A= −40℃ to 85℃, n = 1 to 17	−6.0		6.0	mV
		GPIOn to AGND = 0.6 V ~3.3 V, T_A = −40°C to 85°C, n =1 to 4	−15.0		15.0	mV
		GPIOn to AGND = 0.6V ~ V_{TSREF}, T_A = −40°C to 85°C, n =1 to 4, accuracy for thermistor ratio, % of TSREF	−0.5		0.5	%
		BAT to AGND, T_A = −40°C to 85°C	−1.5		1.5	%
I_{lkg_M}	Input Leakage Current When Inputs not being Measured	Cn, n = 0 to 17		10		nA
		GPIOn, n = 1 to 4		10		nA
I_{lkg_S}	Input Leakage Current When Inputs not being Measured	Cn, n = 0 to 17		±1		μA
		GPIOn, n = 1 to 4		±1		μA

All test conditions: V_{BAT} = 62 V, T_A = -40°C to 85°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage Reference						
V_{REF}	Main Reference Voltage	VREF Pin, No Load	3.28	3.3	3.32	V
	Main Reference Voltage TC	VREF Pin, No Load		10		ppm/℃
V_{TSREF}	Buffered Reference Voltage	VTSREF Pin, No load to 1k Load	3.27	3.3	3.33	V
	Buffered Reference Voltage TC	VTSREF Pin, No Load		20		ppm/℃
Current Measurement ADC						
V_{CADC_IN}	Input Voltage Range for Current Measurement	$V_{SRP} - V_{SRN}$	−0.1		0.1	V
V_{CADC_LSB}	Current Sense Measurement Resolution			4		μV/LSB
V_{CADC_TME}	Current ADC Total Measurement Error (1)	$V_{SRP} - V_{SRN}$ = 0, T_A = 25℃	−30		30	μV
		$V_{SRP} - V_{SRN}$ = 0, T_A = −40℃ to 85℃	−90		120	μV
		$V_{SRP} - V_{SRN}$ = −0.1 V to 0.1 V, T_A = −20℃ to 65℃	−150		150	μV
		$V_{SRP} - V_{SRN}$ = −0.1 V to 0.1 V, T_A =−40℃ to 85℃	−220		220	μV
V_{CC_GAIN}	Gain error		−0.14		0.14	%
R_{CC_IN}	Effective Input Resistance			100		kΩ
General DC Specifications						
I_{BAT}	Current of BAT Pin	Shutdown Mode		2.5	4	μA
		Deep Sleep Mode		10		μA
		Sleep Mode		30		μA
		Normal Mode		30		μA
V_{BAT}	BAT Supply Voltage Range		12		75	V
I_{REG}	VREG Current	Deep Sleep Mode		10		μA
		Sleep Mode		10		μA
		Normal Mode		2.5		mA
V_{REG}	VREG Supply Voltage	no load,		5		V
V_{DRIVE}	DRIVE Output Voltage	Sourcing 1 μA		5.7		V
		Sourcing 500 μA		5.7		V
V_{REGD}	Digital Supply Voltage	5mA load		3.3		V
Passive Balancing						
R_{BAL_ON}	Internal Cell Balancing Resistance			45		Ω

(1) Guaranteed by bench test

All test conditions: V_{BAT} = 62 V, T_A = −40°C to 85°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Logic Input and Output						
V_{OH}	Logic-level Output-voltage High, SDO	I_{LOAD} = 5 mA	0.6× V_{REGD}		V_{REGD}	V
V_{OL}	Logic-level Output Low, SDO	I_{LOAD} = 5mA			0.8	V
V_{IH}	Logic-level Input-voltage High, CSN, CLK, SDI, HRST, DFETCTL, CFETCTL		0.7× V_{REGD}		V_{REGD}	V
V_{IL}	Logic-level Input-voltage Low, CSN, CLK, SDI, HRST, DFETCTL, CFETCTL				0.3× V_{REGD}	V
I_{LKG}	Input Leakage Current	SCLK,SDI			1	μA
Wakeup						
V_{IH_WAKEUP}	WAKEUP High-input Voltage	WAKEUP in shutdown mode	2			V
t_{WAKEUP_HOLD}	WAKEUP Hold Time			8		ms
Load Detection						
V_{LOAD_RM}	Load Removal Detect Voltage	V_{BAT} > 12 V		1		V
I_{LOAD}	Leakage Current	V_{LOAD} = V_{BAT} = 80 V, $R_{LOAD}$is disconnected			1	μA
R_{LOAD}	Internal Resistor to AGND	VM_PD_SEL[1:0] = 11		45		kΩ
		VM_PD_SEL[1:0] = 00		1900		kΩ
PACKIN						
$V_{PACKINH}$	Charger In Detect Voltage High			−0.3		V
V_{PACKIN_RM}	Charger Removal Detect Voltage			−0.15		V
I_{PACKIN}					1	μA
R_{PACKIN}				800		MΩ
PCFET and PDFET Drive						
V_{PCFET_ON}	Output Voltage, PCFET on	R_{load} = 1 MΩ		10		V
I_{PULLUP_PCFET}	Current Sink for PCFET		8	10	14	μA
V_{PDFET_ON}	Output Voltage, PDFET on		8	12	16	V
$R_{PULLDOWN\_PDFET}$	R Pulldown for PDFET			100		Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CDRV and DDRV						
V_{CFET_ON}	Output Voltage, CFET on	Rload = 1 M		10		V
I_{PULLUP_CFET}	Current Sink for CFET		8	10	14	μA
V_{DFET_ON}	Output Voltage, DFET on		8	12	16	V
$R_{PULLDOWN\_DFET}$	R Pulldown for DFET			100		Ω
FUSE Drive						
V_{OH}	Output Voltage High	C_L= 1 nF, 5 kΩ		12	14	V
Current Comparator Protection						
V_{COC}	Overcurrent in Charge Threshold Setting Range (1)	4-mV step	4		128	mV
V_{COCA}	V_{COC} Accuracy	Setting ≥ 16 mV		5		mV
t_{COC_DLY}	V_{COC} Delay (1)	40-ms step	10		1250	ms
V_{DOC}	Overcurrent in Discharge Threshold Setting Range (1)	6-mV step	12		198	mV
V_{DOCA}	V_{DOC} Accuracy	Setting ≥ 42 mV		5		mV
t_{DOC_DLY}	V_{DOC} Delay (1)	40-ms step	10		1250	ms
V_{SCD}	Short Current in Discharge Threshold Setting Range (1)		16		384	mV
V_{SCD_ACC}	V_{SCD} Accuracy	Setting ≥ 48 mV		5		mV
t_{SCD_DLY}	V_{SCD} Delay (1)	10-μs step	5		155	μs
SPI Timing Requirements (2) (See Figure 12)						
t_{CLK}	SPI Clock Period		1			μs
t_1	SDI Setup Time before SCLK Rising Edge		25			ns
t_2	SDI Hold Time after SCLK Rising Edge		25			ns
t_3	SCLK High		200			ns
t_4	SCLK Low		200			ns
t_5	CS Rising Edge to CS Falling Edge		0.65			μs
t_6	SCLK Rising Edge to CS Rising Edge		0.8			μs
t_7	CS Falling Edge to SCLK Falling Edge		1			μs
t_8	SCLK Falling Edge to SDO Valid				60	ns

(1) Guarantee by bench test
(2) Design Guarantee

Typical Performance Characteristics

All test conditions: V_{BAT} = 62 V, T_A = +25°C, unless otherwise noted.

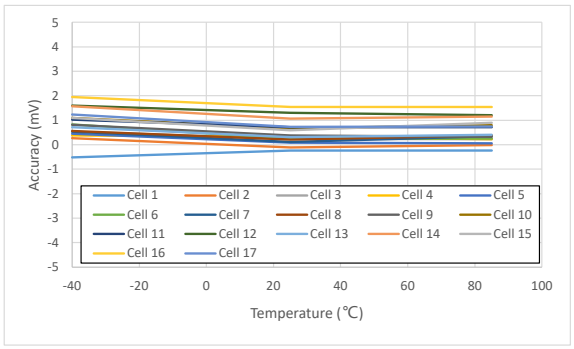


Figure 1. Cell Voltage Measurement Error vs. Temperature with Cell Voltage = 1.5 V

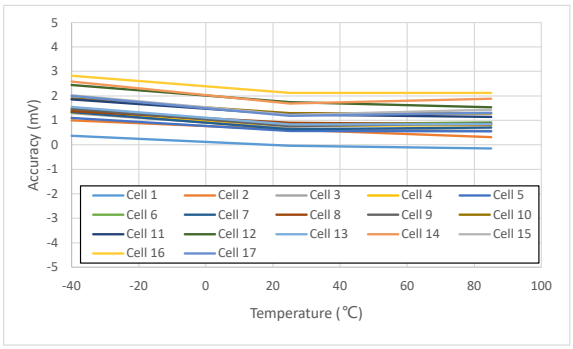


Figure 2. Cell Voltage Measurement Error vs. Temperature with Cell Voltage = 2.3 V

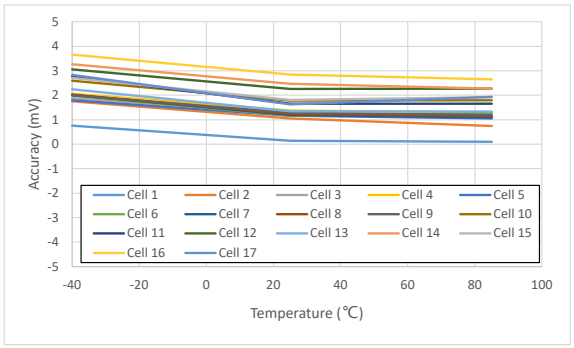


Figure 3. Cell Voltage Measurement Error vs. Temperature with Cell Voltage = 3.1 V

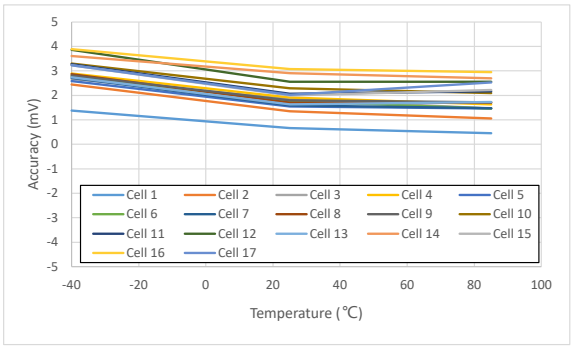


Figure 4. Cell Voltage Measurement Error vs. Temperature with Cell Voltage = 3.9 V

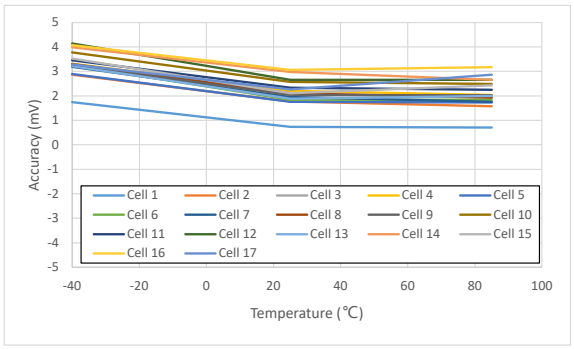


Figure 5. Cell Voltage Measurement Error vs. Temperature with Cell Voltage = 4.5 V

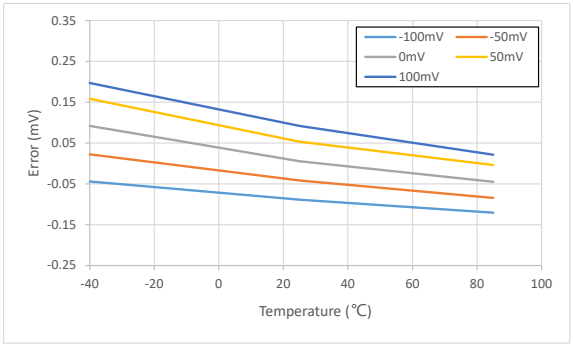


Figure 6. Current Measurement Error vs. Temperature

Detailed Description

Overview

The TPB76016 is a multicell battery stack monitor that measures up to 17 series battery cells with a total measurement error of less than 5mV typical. The cell measurement range is from 0V to 5V, with supporting Li-ion, Li-Polymer, and LiFePO4 battery types. All 17 cells can be measured within 50ms. The TPB76016 also integrates an ADC to measure charge/discharge current with a coulomb counter, which provides data for host-based algorithms and control. The TPB76016 integrates a safety engine that provides reliability protection for OV, UV, OTC, UTC, OTD, UTD, COC, DOC, SCD, and SOV with programmable detection threshold and delay time. The COC, DOC, and SCD use a hardware comparator for fast protection. The TPB76016 provides internal cell balance, the cell balance current is 50 mA, for a higher cell balance current, an external cell balance circuit may be used.

The TPB76016 has a host communication peripheral supporting 1Mbps SPI, multiple digital control and status data are available through SPI. The device includes an interrupt to the host and independent control for host override of each low-side protection NFET. There are four GPIO pins which can be used for temperature measurements using external thermistors, and a FUSE drive to control external fuse to achieve secondary protection. The one-time-programmable (OTP) memory is available for customers to set up device operation on their own side.

Functional Block Diagram

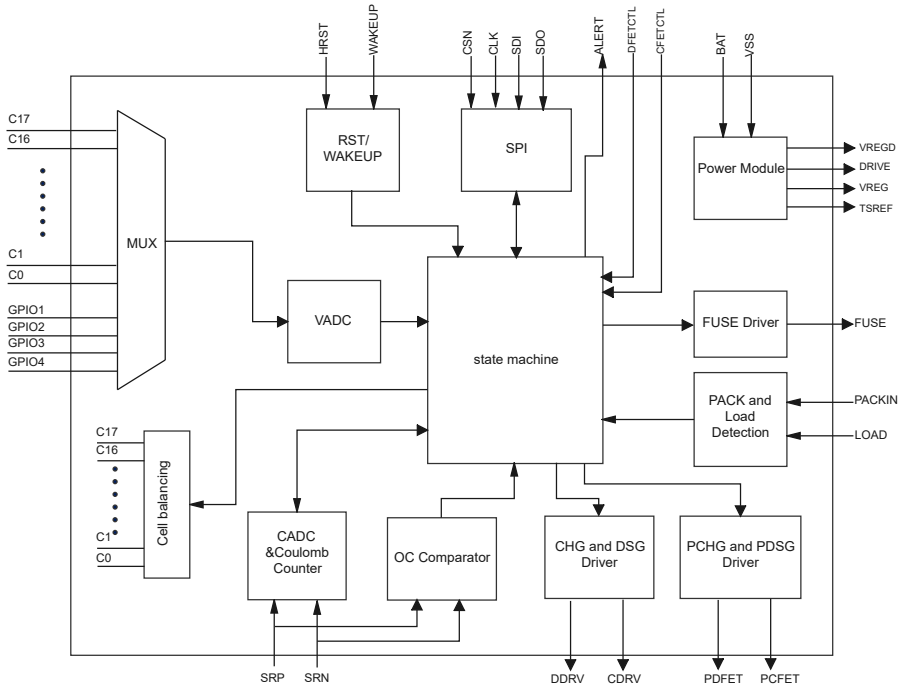


Figure 7. Functional Block Diagram

Feature Description

Operation Modes

The TPB76016 supports two operation modes, one is standalone mode, another is host mode. In standalone mode, the TPB76016 can operate independently to fulfill the measurement and protection, while it also provides the flexibility of cooperation with the host through the SPI interface, external host can access the internal registers of the TPB76016 to get ADC measurement results and protection state, and etc. In host mode, TPB76016 doesn't implement measurement without host control, and the protection should be implemented by the host to control and charge FET and discharge FET, while the over-current protection is operated by the device independently. After power-on reset, TPB76016 enters standalone mode by default, host mode is available by factory trim.

In standalone mode, the TPB76016 has four power modes to support optimized features and power consumption, the device is able to transit between modes either automatically or controlled by the host.

- Norma mode: in this mode, the device performs frequent measurements of cell voltages, current, thermistor temperature and various other voltages, operates protection, and provides data and status updates.
- Sleep mode: there are wake period and quiet period in this mode. In the wake period, the operation is the same as normal mode. In the quiet period, the ADC measurement is disabled, the REF voltage is off, the TSREF voltage can be set on or off, the cell balance and load detection function are disabled either, the power consumption is reduced, and the current hardware protections are still enabled. The wake period and quiet period are adjustable in registers 0X45 and 0X46. In sleep mode, the device total average current consumption of the device is reduced.
- Deep sleep mode: in this mode, the operation is the same as the quiet period of sleep mode, the device total current consumption of the device is reduced further.
- Shutdown mode: in this mode, the device is completely disabled, all measurement and protection are disabled, and the CHG, PCHG, DSG, and PDSG FETs are all disabled, while the WAKEUP and charger in detection are still enabled. This is the lowest power state of the device, which may be used for shipment or long-term storage. After powering on, the TPB76016 enters this mode.

The power mode transition is shown below.

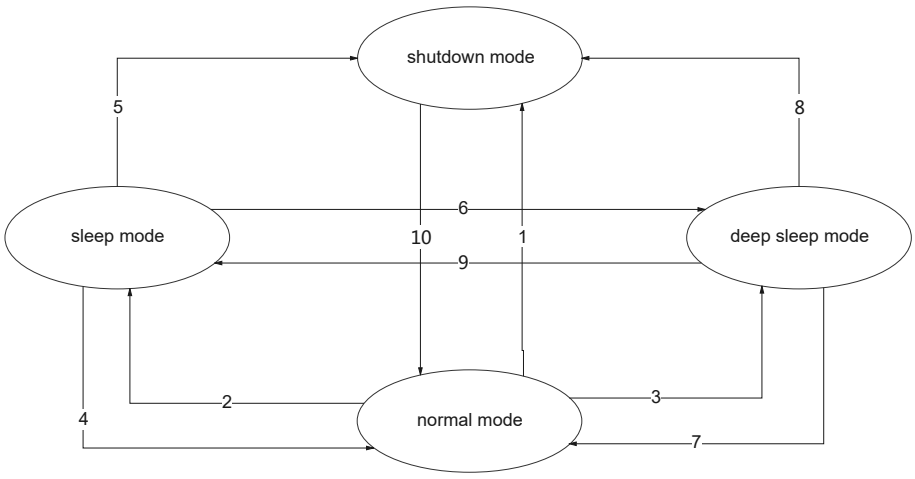


Figure 8. Power Mode Transition

The power mode transition table is as below.

Transition	Initial Mode	Condition	Final Mode
1	Normal Mode	SPI SHUTDOWN command	SHUTDOWN Mode
		HRST high pulse > 8 ms	

Transition	Initial Mode	Condition	Final Mode
		SUV shutdown	
		Low BAT voltage	
		Thermal shutdown	
2		SPI SLEEP command (configurable) **AND** Enter sleep mode is enabled **AND** No fault **AND** Standalone **AND** charge/discharge current lower than sleep current threshold	SLEEP Mode
3		SPI DEEPSLEEP command	DEEPSLEEP Mode
4	SLEEP Mode	SPI Exit_SLEEP command	Normal Mode
		Fault occurs	
		Charge/Discharge Current larger than sleep current threshold	
5		HRST high pulse>8ms	SHUTDOWN Mode
		Low BAT voltage	
		SUV shutdown	
		SPI SHUTDOWN Command	
		Thermal shutdown	
6		SPI DEEPSLEEP command	DEEPSLEEP Mode
7	DEEPSLEEP Mode	SPI exit DEEPSLEEP command	Normal Mode
		Charger plug in detected	
8		SPI SHUTDWON Command	SHUTDOWN Mode
		HRST high pulse>8ms	
		Thermal shutdown	
		Low BAT voltage	
9		SPI SLEEP Command	SLEEP Mode
10	SHUTDOWN Mode	Charger plug in detected	Normal Mode
		WAKEUP high pulse>8ms	
		SPI bus active	

In host mode, the TPB76016 operates in normal power mode and waits for the host command to implement measurement, if the host sends the SPI SHUTDOWN command, the device enters shutdown mode. In power-up procedure of host mode device, the host should disable measurement firstly by configuring REG0x47H to 0xFF, REG0x48H to 0x7F, REG0x49H to 0xF0, then send a command to implement measurement.

Voltage Measurement ADC

The TPB76016 integrates a 16-bit Σ-Δ ADC with multiplex to measure cell voltages, up to four external thermistors, BAT voltage, VAO, BG, VDRIVE, LOAD pin, VREG, VREGD, and TSREF. The TPB76016 supports cells up to 17-series cell, each cell voltage is a differential measurement of Cn and Cn-1 (n=1 to 17), and each cell voltage measurement range is 0 to 5V with 100μV/LSB. All 17 cell voltages are measured in a cell measurement loop which consists of multiple measurement slots, each cell voltage takes a measurement slot. LOAD pin is measured in the load detection measurement loop, and

external thermistors, BAT voltage, VAO, and other voltages are measured in the aux measurement loop, each voltage takes a measurement slot. There is an open wire measurement loop dedicated to the open wire detection period.

Each measurement loop time can be set from 50ms to 10s through registers, while open wire measurement loop time is set from 1s to 80s, see more detail in REG0x47H and REG0x48H. Take the cell voltage measurement loop and aux measurement loop for example, the measurement slot in each measurement loop is arranged as in Figure 9, the measurement slots take a small section of measurement loop time, and the remaining is injected with idle slots. Customers can get more accurate ADC results by setting higher OSR in CELL_OSR, AUX_OSR, and LD_OSR bits.

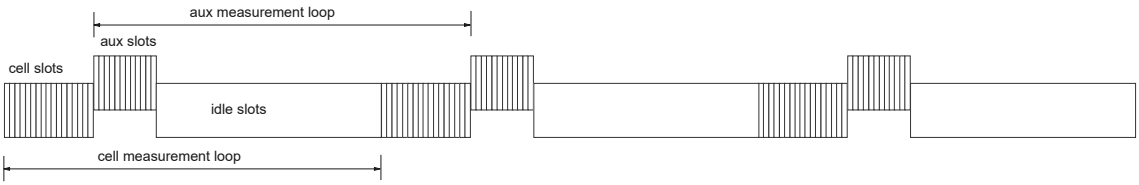


Figure 9. Measurement Slot Timing

The voltage measurement ADC results are stored in 16-bit registers, from register 0XC0 to 0XFD.

Current Measurement ADC

The TPB76016 implements another 16-bit Σ-Δ ADC to measure the charge/discharge current, the current is sensed via the sense resistor between the SRP and SRN pins through an external RC filter. The current ADC input voltage range is −0.1 V to 0.1 V with 4 μV/LSB. The current is measured in the current measurement loop, the loop time can be set from 50 ms to 10 s through the register, see more detail in REG0x49H. Customers can get more accurate ADC results by setting higher OSR in the CADC_OSR bit.

The current measurement ADC result is a 16-bit signed number, stored in registers 0XFE and 0XFF, the 1 in signed bit means discharge current, and 0 means charge current.

The TPB76016 also provides a coulomb counter in 32-bit format stored in registers 0XAB to 0XAE, the MSB is the sign bit, 1 means discharge current, and 0 means charge current. The coulomb counter is updated every 10 ms. If the registers 0XAB to 0XAE are full, the CCUF_FLG or CCOF_FLG bit will be set.

Measurement in Host Mode

In host mode, TPB76016 waits for the host poll command to implement ADC measurement, when the measurement is done, the TPB76016 provides the done indication in the POLL_STAT bit, and the host should implement the read command to get the measurement results. Refer to the SPI Interface section for more information about poll command and read command.

Protection

The TPB76016 integrates a safety engine that provides reliability protection for OV, UV, OTC, UTC, OTD, UTD, COC, DOC, SCD, and SOV with a programmable detection threshold and delay time.

1. Over Voltage Protection
   The TPB76016 monitors the voltages of every cell using voltage measurement ADC, if any cell voltage is higher than the over-voltage threshold for a deglitch time, the over-voltage protection is triggered. The over-voltage threshold is set in OV_TH_SEL bits, the deglitch time is set in OV_DLY_SEL bits.
   In over voltage state, the TPB76016 turns off CHG FET, enable charger removal detection and load insert detection, sets the corresponding bit in the over-voltage status register and over-voltage flag register, and triggers an alert signal to the host if OV_ALT_EN is enabled.
   The over-voltage protection is released if all cell voltages decrease to less than the over voltage release threshold, which is set in OV_RCV_SEL bits. The corresponding bit in over voltage status is cleared, while the flag bit needs the host to clear.
2. Under Voltage Protection

The TPB76016 monitors the voltages of every cell using voltage measurement ADC, if any cell voltage is lower than under-voltage threshold for a deglitch time, the under-voltage protection is triggered. The under-voltage threshold is set in UV_TH_SEL bits, the deglitch time is set in UV_DLY_SEL bits.
In the under voltage state, the TPB76016 turns off discharge FET, enables load removal detection, sets the corresponding bit in under the voltage status register and under the voltage flag register, and triggers an alert signal to host if UV_ALT_EN is enabled.
The under-voltage protection is released if all cell voltages rise higher than the under voltage release threshold, which is set in UV_RCV_SEL bits. The corresponding bit in under voltage status is cleared, while the flag bit needs the host to clear.

3. Super Under Voltage Protection
   In the under voltage state, if any cell voltage still decreases to lower than the super under voltage threshold for a deglitch time, the super under voltage protection is triggered, the super under voltage threshold is set in SUV_TH_SEL bits, the deglitch time is set in SUV_DLY_SEL bits.
   When super under voltage protection is triggered, the device enters shutdown mode.
4. Over Temperature Charge
   The TPB76016 monitors the temperature of the NTC thermistor via the voltage of the GPIO pin where the NTC thermistor is connected, if the GPIO voltage is lower than over-temperature charger threshold, for a deglitch time, the over-temperature charge protection is triggered. The over-temperature charge threshold is set in OTC_TH_SEL bits, the deglitch time is set in OTC_DLY_SEL bits.
   In over temperature charge state, the CHG FET and DSG FET are turned off, the corresponding bit in GPIOn_OTC_STAT register and GPIOn_OTC_STAT flag register are set, and an alert signal is triggered if OTC_ALT_EN is enabled.
   The over-temperature charge protection is released if GPIOn voltage is higher than over temperature charge recovery threshold, set in OTC_RCV_SEL bits, for deglitch time, set in OTC_RCV_DLY_SEL, the corresponding status bit is cleared, while the flag bit needs a host to clear.
5. Under Temperature Charge
   The TPB76016 monitors the temperature of the NTC thermistor via the voltage of the GPIO pin where the NTC thermistor is connected, if GPIO voltage is higher than the under-temperature charger threshold, set in UTC_TH_SEL bits, for a deglitch time, set in UTC_DLY_SEL bits, the under temperature charge protection is triggered.
   In under temperature charge state, the CHG FET and DSG FET are turned off, the corresponding bit in GPIOn_UTC_STAT register and GPIOn_UTC_STAT flag register are set, and an alert signal is triggered if UTC_ALT_EN is enabled.
   The under-temperature charge protection is released if GPIOn voltage is lower than under temperature charge recovery threshold, set in UTC_RCV_SEL bits, for deglitch time, set in UTC_RCV_DLY_SEL bits, the corresponding status bit is cleared, while the flag bit needs a host to clear.
6. Over Temperature Discharge
   The TPB76016 monitors the temperature of the NTC thermistor via the voltage of the GPIO pin where the NTC thermistor is connected, if the GPIO voltage is lower than over temperature discharger threshold, set in OTD_TH_SEL bits, for a deglitch time, set in OTD_DLY_SEL bits, the over temperature discharge protection is triggered.
   In over temperature discharge state, the DSG FET is turned off, the corresponding bit in GPIOn_OTD_STAT register and GPIOn_OTD_STAT flag register are set, and an alert signal is triggered if OTD_ALT_EN is enabled.
   The over-temperature discharge protection is released if the GPIOn voltage is higher than over temperature discharge recovery threshold, set in OTD_RCV_SEL bits, for deglitch time, set in OTD_RCV_DLY_SEL bits, the corresponding status bit is cleared, while the flag bit needs the host to clear.
7. Under Temperature Discharge
   The TPB76016 monitors the temperature of the NTC thermistor via the voltage of the GPIO pin where the NTC thermistor is connected, if the GPIO voltage is higher than under temperature discharger threshold, set in UTD_TH_SEL bits, for a deglitch time, set in UTD_DLY_SEL bits, the under-temperature discharge protection is triggered.
   In under temperature discharge state, the DSG FET is turned off, the corresponding bit in GPIOn_UTD_STAT register and GPIOn_UTD_STAT flag register are set, and an alert signal is triggered if UTD_ALT_EN is enabled.
   The under-temperature discharge protection is released if GPIOn voltage is lower than under temperature discharge recovery threshold, set in UTD_RCV_SEL bits, for deglitch time, set in UTD_RCV_DLY_SEL bits, the corresponding status bit is cleared, while the flag bit needs the host to clear.
8. Charge Over Current

The TPB76016 detects the charge current via the hardware comparator, if the charge current is larger than the charge over the current threshold for a deglitch time, the charge over current protection is triggered. The charge over the current threshold is set in COC_SEL bits, the deglitch time is set in COC_DLY_SEL bits.
In charge over current state, the TPB76016 turns off the CHG FET, enables charger removal detection, sets COC_STAT bit and COC_FLG bit, and triggers an alert signal to the host if OCC_ALT_EN is enabled.
The charge over current protection is released in either of the three ways below, which can be selected in COC_RCV_SEL bits.

- Charger removal is detected
- After the recovery delay time, which is set in COC_RCV_DLY_SEL bits.
- After recovery delay time for three times, if over current is still there, the state is latched, needs the host to release the latch by setting CLR_CUR bit.

9. Discharge Over Current
   The TPB76016 detects the discharge current via the hardware comparator, if the discharge current is larger than the discharge over current threshold for a deglitch time, the discharge over current protection is triggered. The discharge over current is set in DOC_SEL bits, the deglitch time is set in DOC_DLY_SEL bits.
   In discharge over current state, the TPB76016 turns off the DSG FET, enables charger insert detection and load removal detection, sets DOC_STAT bit and DOC_FLG bit, and triggers an alert signal to host if DOC_ALT_EN is enabled.
   The discharge over current protection is released in either one of below three ways below, which can be selected in DOC_RCV_SEL bits.
   - Load removal is detected
   - After the recovery delay time, which is set in DOC_RCV_DLY_SEL bits.
   - After recovery delay time for three times, if over current is still there, the state is latched, and need a host to release the latch by setting CLR_CUR bit.
10. Discharge Short Current
    The TPB76016 detects the discharge current via the hardware comparator, if the discharge current is larger than the discharge short current threshold for a deglitch time, the discharge short current protection is triggered. The discharge short current is set in SCD_SEL bits, the deglitch time is set in SCD_DLY_SEL bits.
    In the discharge short current state, the TPB76016 turns off the DSG FET, enables charger insert detection and load removal detection, sets SCD_STAT bit and SCD_FLG bit, and triggers an alert signal to host if SCD_ALT_EN is enabled. The state is latched.
    The discharge short current protection is released in either one of below two ways below, which can be selected in SCD_RCV_SEL bits.
    - Host releases the latch by setting CLR_CUR bit
    - load removal is detected

In host mode, the charge over current protection, discharge over current protection, and discharge short current protection are implemented by the TPB76016 itself, the voltage protection and temperature protection need a host to implement.

Open Wire Detection

The TPB76016 integrates open wire detection. The open wire detection is configured by OW_PERIOD bits, if these bits are set to 111, the open wire detection is disabled, otherwise, the open wire detection is enabled, and the detection period is fixed by the configuration. The open wire detection depends on the ADC to measure each cell voltage, during each cell detection slot, the cell voltage is measured by ADC for the first time, then the cell balance FET is turned on for a short time, after that, the cell voltage is measured by ADC for the second time, the open wire for that cell is detected if the one of below condition is met

- ADC measurement result each time is lower than 0.5 V.
- The difference between the two ADC measurement results is larger than the open wire threshold, set in OW_TH_SEL bits.

If the open wire is detected, the OW_STAT and OW_FLG bit are set, and an alert is triggered if OW_ALT_EN is enabled, the OW_FLG bit needs a host to write CLR_OW bit to clear. The corresponding cell of open wire is shown in OW_CH_STAT bits, and the voltage difference of twice ADC measurement result is shown in OW_SUB bits.

The open wire detection is checked on each cell one by one from the highest number cell to the lowest.

FET SYNC

In UV, DOC, and SCD protection, the DSG FET is turned off, if the charger is inserted, charging is allowed, and the charging current flows through the body diode of the DSG FET. While DSG FET can be turned on by the FET SYNC function regardless of UV, DOC, and SCD protection. DSG FET SYNC function should be enabled in DFET_SYNC_EN bit first, then configure the DFET in DFETSYNC_ON bit, when the device detects the charging current larger than the threshold of charging wake current for a deglitch time, the DSGFET is turned on. The charging wake current is set in CWAKED_SEL bits, and the deglitch time is set in CWAKED_DLY_SEL bits.

Similarly, in OV, COC protection, the CHG FET is turned off, if the load is inserted, discharging is allowed, and the discharging current flows through the body diode of CHG FET. While CHG FET can be turned on by the FET SYNC function regardless of OV and COC protection. CHG FET SYNC function should be enabled in the CFET_SYNC_EN bit first, then configure the CFET in the CFETSYNC_ON bit, when the device detects the discharging current larger than the threshold of discharging wake current for a deglitch time, the CHGFET is turned on. The discharging wake current is set in CWAKEC_SEL bits, and the deglitch time is set in CWAKEC_DLY_SEL bits.

FET Driver and Control

The TPB76016 integrates the NMOSFET driver, including the CHG FET driver, DSG FET driver, PreCHG FET driver, and PreDSG FET driver, in corresponding to the pins of CDRV, DDRV, PCFET, and PDFET. The DDRV and PDFET are push-pull output, while CDRV and PCFET are current source outputs, the source current capability is set in CDRV_20U and PCDRV_20U bit. The FET driver is controlled by the state machine.

CHG FET Driver

The condition of controlling the CHG FET Driver is as below, with priority descending.

- CFETCTL pin control. If the CFETCTL pin detects a high input, the CHG FET is turned off, otherwise, the CHG FET control depends on the below controls. This pin can be configured to low active by the FET_CTL_INV bit.
- FET SYNC function control, as described in the FET SYNC section.
- Register control. CHG FET driver controlled by the register is enabled by setting REG_CTRL bit to 1, then configuring CFET_CTL bit to turn on or turn off the CHG FET.
- State machine control. During the power-on initiation procedure, the CHG FET is turned off, then depends on the state machine after the initiation procedure. In deep sleep mode or shutdown mode, the CHG FET is turned off. In normal mode or sleep mode, the CHG FET control depends on the protection state.
- In the case that CHG FET is controlled by the register, if COC occurs, CHG FET will be turned off.

DSG FET Driver

The condition of controlling the DSG FET Driver is as below, with priority descending.

- DFETCTL pin control. If the DFETCTL pin detects a high input, the DSG FET is turned off, otherwise, the DSG FET control depends on the below controls. This pin can be configured to low active by the FET_CTL_INV bit.
- FET SYNC function control, as described in the FET SYNC section.
- Register control. DSG FET driver controlled by register is enabled by setting REG_CTRL bit to 1, then configure DFET_CTL bit to turn on or turn off the DSG FET.
- State machine control. During the power-on initiation procedure, the DSG FET is turned off, then depends on the state machine after the initiation procedure. In deep sleep mode or shutdown mode, the DSG FET is turned off. In normal mode or sleep mode, the DSG FET control depends on the protection state.

- In the case that DSG FET is controlled by the register, if DOC or SCD occurs, DSG FET will be turned off.

PRECHG FET Driver

The TPB76016 integrates pre CHG FET driver, the condition of controlling pre CHG FET Driver is as below, with priority descending.

- Register control. Pre CHG FET driver controlled by register is enabled by setting the REG_CTRL bit to 1, then configure the PCFET_CTL bit to turn on or turn off the Pre CHG FET.
- State machine control. During power-on initiation procedure, the Pre CHG FET is turned off, then depends on state machine after initiation procedure. In deepsleep mode or shutdown mode, the Pre CHG FET is turned off. In normal mode or sleep mode, the device detects the battery voltage to decide, if the battery voltage is lower than the pre charge threshold, set in PCHG_SEL bits, the pre CHG FET is turned on, if the battery voltage is higher than the pre charge recovery threshold, set in PCHG_RCV_SEL bits, the pre CHG FET is off. In other conditions, the pre CHG FET is off. The CHG FET is off during pre charging.

PREDSG FET Driver

The TPB76016 integrates pre DSG FET driver. During power-on initiation procedure, the Pre DSG FET is turned off, then depends on state machine after initiation procedure. In deepsleep mode or shutdown mode, the Pre DSG FET is turned off. In normal mode or sleep mode, the pre DSG FET driver is turned off in protection state, or cell balancing is on going, or cell open wire is detected, otherwise, the pre DSG FET is controlled by register. Pre DSG FET driver controlled by register is enabled by setting the REG_CTRL bit to 1, then configure the PDFET_CTL bit to turn on or turn off the Pre DSG FET.

Cell Balance

The TPB76016 integrates internal passive cell balance function, and supports odd or even channel cell balance, it is enabled under the conditions that,

1. RLX_BAL_EN is set to 1, which enables cell balance
2. No faults occur, except OV, UV and UTC
3. Cell balance timer is enabled, which is set in BAL_TIMER_DIS bit, and the balance timer is set in BAL_TO_SEL and BAL_RANGE_SEL bits.

When the cell balance function is enabled, the device monitors each cell voltage in each cell voltage measurement loop, and finds the max voltage cell and min voltage cell. If the max voltage is higher than the balance start threshold, set in VCB_START_SEL bits, and the difference voltage between the max cell voltage and min cell voltage is higher than the difference threshold, set in VCB_TH_SEL bits, the cell balance conditions are met. If the max voltage cell is odd channel cell, then all the odd channel cells that meet cell balance conditions start balancing, the internal cell balance FET are turned on. So is the same if the max voltage cell is even channel cell.

The balance timer is normally set longer than the cell voltage measurement loop period, if cell voltage measurement is required when cell balancing is on going, the cell balancing suspends, and after a delay time, set in BAL_RLS_TIMER_SEL bits, the cell voltage measurement loop starts, during the cell voltage measurement, the balance timer still counts.

The cell balance stops if the voltage difference between the max cell voltage and min cell voltage is lower than VCB_TH_SEL, or if balance timer is out, the balance timeout sets BAL_TO_FLG bit, which needs host to clear it, then next cell balance can start.

The internal passive cell balance limits the max cell balancing current due to IC thermal consideration. An external circuit is needed when larger cell balancing current is required, the external cell balancing circuit is as below Figure 10. The external balance current is determined by cell voltage, the gate-source voltage of Qn and the value of resistor RCn.

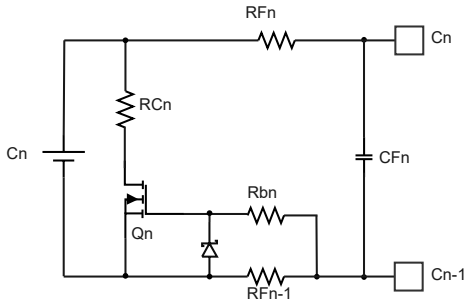


Figure 10. External Balance Circuit

In host mode, the host can control any channel balance to implement a flexible balance strategy. The host can select the channel for balance in REG0x45H, REG0x46H, and REG0x47H. The 8 bits in REG0x45H are used to select cell 1 to cell 8, with LSB for cell 1 and MSB for cell 8. The 8 bits in REG0x46H are used to select cell 9 to cell 16, with LSB for cell 9 and MSB for cell 16. The bit0 in REG0x47H is used to select cell 17. The start and stop of cell balance in host mode are controlled by poll command, refer SPI Interface section for more information.

Load Detection

The TPB76016 implements load removal detection by monitoring LOAD voltage by ADC, the monitor period is set in LD_PERIOD bits, if the bits are set to 1111, the load detection is disabled, otherwise, load detection is enabled. The load removal function is valid under the condition that DOC occurs and DSG FET is off, under which condition, the LOAD pin is pulled high due to external loading. If the TPB76016 monitors the load pin is lower than the load out threshold set in the LD_TH_SEL, the load removal is detected, the LOAD_STAT bit will be set and an alert signal is triggered if LOAD_ALT_EN is enabled. There is pull down resistor within the LOAD pin to pull low LOAD pin voltage when load detection is enabled, in order to detect load removal effectively, customers can adjust the pull-down resistor by setting VM_PD_SEL bits, if choosing a small pull-down resistor, load removal can be detected more effectively, but the current consumption will be higher.

Charger In Detection

The TPB76016 implements charger insertion detection by detecting the PACKIN voltage. The charger insert function is valid under the condition that CHG FET is off. If the TPB76016 detects PACKIN voltage lower than V_{PACKIN_TH} for 32 ms, the charger insert is detected, and an alert signal is triggered if CHG_ALT_EN is enabled. If the PACKIN voltage is higher than V_{PACKIN_RM} for 32ms, the charger removal is detected. In sleep mode, deep sleep mode, or shutdown mode, if charger insert is detected, the power mode transits to normal mode.

GPIO

There are four GPIO pins in the TPB76016, which are configured as input. GPIO can be used to sense the voltage of the NTC thermistor, the circuit is as below. The GPIO voltage is sensed by voltage ADC, the sense can be disabled by GPIO_EN bits, if disabled, the OTC, UTC, OTD, and UTD protection will be disabled either. In order to improve the NTC temperature sense accuracy, the voltage ADC reference voltage can be selected as TSREF when measuring GPIO voltage, which reduces the common variable factor of TSREF.

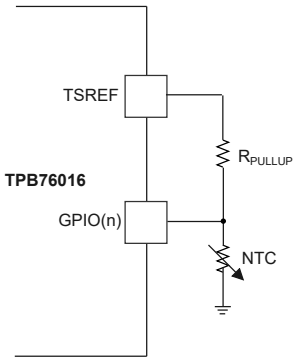


Figure 11. Temperature Sensor Circuit

FUSE Drive

The TPB76016 integrates secondary protection if conditions are considered so serious that the pack should be permanently disabled. The secondary protection only checks the battery voltage and temperature.

The secondary protection can be configured enabled or disabled by PF_EN bit, the secondary protection is triggered if

- The monitored battery voltage is higher than the secondary over voltage threshold, set in SOV_TH_CFG bits, for deglitch time, set in SOV_DLY_CFG bit
- Or, if the monitored NTC voltage during charging is lower than the secondary over temperature charging threshold, set in SOTC_TH_SEL bits, for deglitch time, set in SOTC_DLY_CFG bits
- Or, if the monitored NTC voltage during discharge is lower than the secondary over temperature discharging threshold, set in SOTD_TH_SEL bits, for deglitch time, set in SOTD_DLY_CFG bits

In the secondary protection state, the TPB76016 turns off CHG FET and DSG FET, sets the corresponding bit in the PFAIL status register, triggers an alert signal, and after a deglitch time, sets in PF2FUSE_DLY_CFG bits, and drives FUSE pin high for a time, set in FUSE_DLY_CFG bits, to burn the external fuse. The power state can be configured in PF_DPSLP_EN bit to enter deepsleep mode to save power consumption.

CWAKEC and CWAKED

The device has a current hardware comparator to detect the charging status and discharging status. If the CWAKEC_EN bit is enabled and charging current is higher than the threshold set in CWAKEC_SEL bits for a deglitch time that set in CWAKEC_DLY_SEL bits, the device detects there is charging current, then the CWAKEC_STAT and CWAKEC_FLG bit are set, and an alert signal is triggered if CWAKEC_ALT_EN bit is set. The CWAKEC function can be used for sleep mode transition to normal mode, or the CFETSYNC function as described in the FET SYNC section. If the CWAKED_EN bit is enabled and the discharging current is higher than the threshold set in CWAKED_SEL bits for a deglitch time that set in CWAKED_DLY_SEL bits, the device detects there is discharging current, then the CWAKED_STAT and CWAKED_FLG bit are set, and an alert signal is triggered if CWAKED_ALT_EN bit is set. The CWAKED function can be used for sleep mode transition to normal mode, or the DFETSYNC function as described in the FET SYNC section.

Status and Flag

The TPB76016 provides status and flag indication in status registers that allows the host to get access through the SPI interface. Status shows the real status of the device, no matter protection or operation, while the flag indicates that an event happens ever, needs the host to write the corresponding clear bit to clear.

If the status bit is set, and the corresponding flag bit is set, an alert signal of 10-ms low pulse will be triggered to host if the corresponding alert allows bit is set. Refer to the register section for more details about status and flag information.

SPI Interface

The TPB76016 supports a 4-wire SPI interface to communicate with the host, the TPB76016 acts as a slaver, host acts as a master. The TPB76016 supports SPI mode 3 (CPOL=1, CPHA=1), the SCLK is high during idle, and the data outputs at the falling edge of the SCLK, sampled at the rising edge of the SCLK. The max frequency of the SCLK is 1MHz, the timing of SPI is as below. Refer to the EC table for the timing spec.

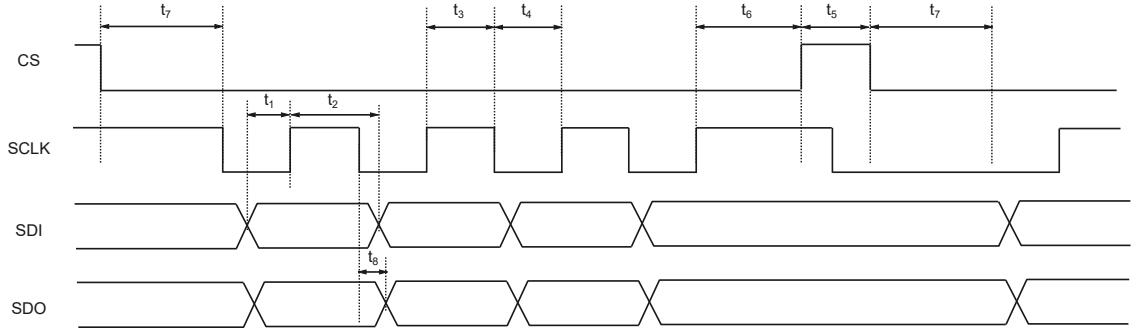


Figure 12. SPI Timing

The protocol formats is as below table.

Table 2. Protocol Format

CMD0	Command byte 0
CMD1	Command byte 1
PEC0	Packet error code byte 0
PEC1	Packet error code byte 1
N	Number of bytes
.....	Continuation of protocol
	Master to slave
	Salve to master

The command code consists of CMD0 and CMD1, each byte is sent to MSB first. The TPB76016 supports single register read command, single register write command, block read command, and poll command. The poll command is only available in host mode, other commands are available in both standalone and host mode. Each command code is listed in the table below.

Table 3. Single Write/Read Register Command Code

NAME	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CMD0	1	1/0	0	0	0	0	0	0
CMD1	Addr[7]	Addr[6]	Addr[5]	Addr[4]	Addr[3]	Addr[2]	Addr[1]	Addr[0]

Table 4. Poll & Block Read Command Code

NAME	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CMD0	0	0	0	0	0	CC[10]	CC[9]	CC[8]
CMD1	CC[7]	CC[6]	CC[5]	CC[4]	CC[3]	CC[2]	CC[1]	CC[0]

The TPB76016 supports 11 poll command and 12 read block command as below.

Table 5. Poll Command Code

Command	CC[10]	CC[9]	CC[8]	CC[7]	CC[6]	CC[5]	CC[4]	CC[3]	CC[2]	CC[1]	CC[0]	Description
ADCV	0	1	1	0	0	0	0	0	0	0	1	Run Cell1-17 Voltage ADC Conversion once
ADAX	0	1	1	0	0	0	0	0	0	1	0	Run Aux Voltage ADC Conversion once
ADLD	0	1	1	0	0	0	0	0	0	1	1	Run Load and BAT Voltage ADC Conversion once
ADCVAX	0	1	1	0	0	0	0	0	1	0	0	Run Cell1-17 and Aux Voltage ADC Conversion once
ADCC	0	1	1	0	0	0	0	0	1	0	1	Run Current ADC Conversion once
ADCVC	0	1	1	0	0	0	0	0	1	1	0	Run Cell1-17 Voltage and Current ADC Conversion once
ADCALL	0	1	1	0	0	0	0	0	1	1	1	Run Cell1-17 Voltage, Aux Voltage and Current ADC Conversion once
ADOW	0	1	1	0	0	0	0	1	0	0	0	Run Open Wire Detection once
SHUT	0	1	1	0	0	0	0	1	1	1	0	Enter Shutdown Mode
BALST	0	1	1	0	0	0	0	1	1	1	1	Start Cell Balance
BALEND	0	1	1	0	0	0	1	0	0	0	0	Stop Cell Balance

Table 6. Read Block Command Code

Command	CC[10]	CC[9]	CC[8]	CC[7]	CC[6]	CC[5]	CC[4]	CC[3]	CC[2]	CC[1]	CC[0]	Description
RDCVA	1	0	0	0	0	0	0	0	0	0	0	Read cell3, cell2, cell1
RDCVB	1	0	0	0	0	0	0	0	0	0	1	Read cell6, cell5, cell4
RDCVC	1	0	0	0	0	0	0	0	0	1	0	Read cell9, cell8, cell7
RDCVD	1	0	0	0	0	0	0	0	0	1	1	Read cell12, cell11, cell10
RDCVE	1	0	0	0	0	0	0	0	1	0	0	Read cell15, cell14, cell13
RDCVF	1	0	0	0	0	0	0	0	1	0	1	Read cell17, cell16
RDAUXA	1	0	0	0	0	0	0	0	1	0	1	Read GPIO3, GPIO2, GPIO1

Command	CC[10]	CC[9]	CC[8]	CC[7]	CC[6]	CC[5]	CC[4]	CC[3]	CC[2]	CC[1]	CC[0]	Description
RDAUXB	1	0	0	0	0	0	0	0	1	1	1	Read CADC, FUSE, GPIO4
RDAUXC	1	0	0	0	0	0	0	1	0	0	0	Read PTAT, VAO, BAT
RDAUXD	1	0	0	0	0	0	0	1	0	0	1	Read LOAD, DRIVE
RDAUXE	1	0	0	0	0	0	0	1	0	1	0	Read TSREF, VREGD，VREG
RDAUXF	1	0	0	0	0	0	0	1	0	1	1	Read CADC, Coulomb counter

The PEC (packet error code) consists of PEC0 and PEC, each byte is sent MSB firstly. The command code and data code need PEC separately. The PEC adopts 15 bits CRC, the polynomial of CRC is $X^{15} + X^{14} + X^{10} + X^8 + X^7 + X^4 + X^3 + 1$ The final PEC code consists of 15 bits CRC and 0 compensated at LSB, as below.

Table 7. PEC Format

NAME	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PEC0	PEC[14]	PEC[13]	PEC[12]	PEC[11]	PEC[10]	PEC[9]	PEC[8]	PEC[7]
PEC1	PEC[6]	PEC[5]	PEC[4]	PEC[3]	PEC[2]	PEC[1]	PEC[0]	0

The default value of PEC is 0X0010.

The detail format of single register read command, single register write command, block read command and poll command are as below.

Table 8. Single Read Command Format

8bit	8bit	8bit	8bit	8bit	8bit	8bit	8bit	N byte
CMD0	CMD1	PEC0	PEC1	Data0	Data1	PEC0	PEC1	Shift byte

In single read command format, master sends the register address and address PEC, slave returns 16 bit data and data PEC. After that, if CSN is still low, the device will return SDI data to SDO.

Table 9. Single Write Command Format

8bit	8bit	8bit	8bit	8bit	8bit	8bit	8bit	N byte
CMD0	CMD1	PEC0	PEC1	Data0	Data1	PEC0	PEC1	Shift byte

In single write command format, master sends the register address, address PEC, data and data PEC.After that, if CSN is still low, the device will return SDI data to SDO.

Table 10. Poll Command Format

8bit	8bit	8bit	8bit	N byte
CMD0	CMD1	PEC0	PEC1	Poll data

In poll command format, master sends the command and command PEC, slave returns poll data to indicate if the command execution is done.

Table 11. Read Block Command Format

8bit	8bit	8bit	8bit	8bit	8bit	8bit	8bit	8bit	N byte
CMD0	CMD1	PEC0	PEC1	Data0	.....	Data5	PEC0	PEC1	Shift byte

In read block command format, master sends the block address and address PEC, slave returns 6 bytes block data and data PEC to master. After that, if the CSN is still low, the device will return SDI data to SDO.

Register Maps

TPB76016 integrates registers to store the protection threshold, delay times, and other parameters selected by system designers, device reset will put these registers value to the reset value. TPB76016 provides a non-volatile one-time programmable (OTP) memory addressing from 0x40 to 0x7F that allows the customer to program the OTP to store different reset values that the customer desires. The following table lists all the registers and describes each in detail. All register addresses not listed in this table should be considered as reserved locations.

Address	Register Name	Description
40H	Analog Timer Control 1	Balance time, open wire detection time, and load detection configuration
41H	Analog Timer Control 2	ADC start time configuration
42H	CADC Calibration	CADC Calibration
43H	FET SYNC	CHG FET and DSG FET SYNC function configuration
44H	Mode and Driver Control	Power mode, CHG FET driver and DSG FET driver control
45H	SLEEP Mode Quiet Period	Sleep mode quiet stage period configuration
46H	SLEEP Mode Wake Period	Sleep mode wake stage period configuration
47H	Cell and Aux Measurement Loop Period	Cell and Aux Measurement Loop Period
48H	Load Detection and Open Wire Detection Period	Load Detection and Open Wire Detection Period
49H	Open Wire Detection Configuration and CADC Period	Open Wire Detection Configuration and CADC Period
4AH	Cell Over Voltage Threshold	Cell Over Voltage Threshold
4BH	Cell Over Voltage Recovery Threshold	Cell Over Voltage Recovery Threshold
4CH	Cell Under Voltage Threshold	Cell Under Voltage Threshold
4DH	Cell Under Voltage Recovery Threshold	Cell Under Voltage Recovery Threshold
4EH	Cell Super Under Voltage Threshold	Cell Super Under Voltage Threshold
4FH	Cell Super Under Voltage Recovery Threshold	Cell Super Under Voltage Recovery Threshold
50H	GPIO Voltage Threshold for Charge Over Temperature	GPIO Voltage Threshold for Charge Over Temperature
51H	GPIO Voltage Threshold for Charge Over Temperature Recovery	GPIO Voltage Threshold for Charge Over Temperature Recovery
52H	GPIO Voltage Threshold for Charge Under Temperature	GPIO Voltage Threshold for Charge Under Temperature
53H	GPIO Voltage Threshold for Charge Under Temperature Recovery	GPIO Voltage Threshold for Charge Under Temperature Recovery
54H	GPIO Voltage Threshold for Discharge Over Temperature	GPIO Voltage Threshold for Discharge Over Temperature

Address	Register Name	Description
55H	GPIO Voltage Threshold for Discharge Over Temperature Recovery	GPIO Voltage Threshold for Discharge Over Temperature Recovery
56H	GPIO Voltage Threshold for Discharge Under Temperature	GPIO Voltage Threshold for Discharge Under Temperature
57H	GPIO Voltage Threshold for Discharge Under Temperature Recovery	GPIO Voltage Threshold for Discharge Under Temperature Recovery
5DH	Charge Over Current and Low Current Threshold	Current Comparator Detect Charge Over Current and Current CADC Detect Low Current Threshold
5EH	Discharge Over Current Threshold	Discharge Over Current Threshold
5FH	Wake Current Threshold	Current Comparator Detect Charge Current or Discharge Current Wake Threshold
60H	Over Current Comparator Configuration	Over Current and Wake Current Detect Enable
61H	OVUV Delay Time Configuration	Cell Over Voltage and Under Voltage Detection Delay Time
62H	SUV Delay Time and DOC Recovery Way Configuration	Cell Super Under Voltage Protection Delay Time and Dsicharge Over Current Protection Recovery Ways
63H	OTC and UTC Delay Time Configuration	Charge Over Temperature and Under Temperature Delay Time
64H	UTD and OTD Delay Time Configuration	Discharge Over Temperature and Under Temperature Delay Time
65H	Over and Under Temperature Recovery Delay Time Configuration	Over and Under Temperature Recovery Delay Time Configuration
66H	Charge Over Current Delay Time Configuration	Charge Over Current Delay Time Configuration
67H	Discharge Over Current Delay Time Configuration	Discharge Over Current Delay Time Configuration
68H	Low Current and SCD Delay Time Configuration	Low Current and SCD Delay Time Configuration
69H	Over Current Recovery Configuration	Charge Over Current Recovery Threshold and Delay Time, Discharge Over Current Recovery Delay Time
6AH	Precharge and Precharge Recovery Voltage Threshold	Precharge and Precharge Recovery Voltage Threshold
6BH	Cell Voltage Measurement Enable Configuration	Cell Voltage Measurement Enable Configuration
6CH	Cell Voltage Measurement Enable Configuration	Cell Voltage Measurement Enable Configuration
6DH	GPIO and REF Voltage Measurement Enable Configuration	GPIO and REF Voltage Measurement Enable Configuration

Address	Register Name	Description
6EH	AUX Voltage Measurement Enable Configuration	AUX Voltage Measurement Enable Configuration
6FH	Alert Enable Configuration 1	Alert Enable Configuration 1
70H	Alert Enable Configuration 2	Alert Enable Configuration 2
71H	EOC and Balance Configuration	End of Charge and Cell balance Configuration
72H	EOC Threshold Configuration	EOC Threshold Configuration
73H	Balance Start Configuration	Balance Start Condition Configuration
74H	Balance Time Configuration	Balance Time Configuration
75H	Sleep Mode Configuration	Enter Sleep Mode Condition Configuration
77H	Wake Current and EOC Delay Time Configuration	Wake Current and EOC Delay Time Configuration
78H	Alert Enable Configuration 3	Alert Enable Configuration 3
79H	FET Driver Configuration	CHG FET and DSG FET Driver Control
7AH	Secondary Protection Enable Configuration	Secondary Protection Enable Configuration
7BH	Secondary Protection Threshold Configuration	Secondary Protection Threshold Configuration
7CH	Secondary Protection Threshold Configuration 2	Secondary Protection Threshold Configuration 2
7DH	FUSE Output Configuration	Fuse pin output configuration
80H	FET Driver Configuration 2	CHG FET and DSG FET Driver Control
87H	ADC Configuration	ADC Over Sample Rate Configuration
8AH	Flag Clear Configuration	Flag bit Clear Configuration
90H	GPO_EN	GPIO Output Enable
91H	Power Mode Status	Power Mode Status
92H	FET Driver Status	FET Driver Status
93H	SPI Status	SPI Status
97H	Open Wire Detection Result	Open Wire Detection Result
98H	Open Wire Channel	Open Wire Channel
99H	Cell Over Voltage Flag 1	Cell Over Voltage Flag 1
9AH	Cell Over Voltage Flag 2	Cell Over Voltage Flag 2
9BH	Cell Under Voltage Flag 1	Cell Under Voltage Flag 1
9CH	Cell Under Voltage Flag 2	Cell Under Voltage Flag 2
9DH	Over Temperature Flag	Over Temperature Flag
9EH	Under Temperature Flag	Under Temperature Flag
9FH	Over Current and Current Wake Flag	Over Current and Current Wake Flag
A0H	BAT Voltage Flag	BAT Voltage, EOC, OW, OV17, UV17 Flag
A1H	Other Flag	Balance Timeout, Coulomb Counter overflow flag

Address	Register Name	Description
A2H	Cell Over Voltage Status 1	Cell Over Voltage Status 1
A3H	Cell Over Voltage Status 2	Cell Over Voltage Status 2
A4H	Cell Under Voltage Status 1	Cell Under Voltage Status 1
A5H	Cell Under Voltage Status 2	Cell Under Voltage Status 2
A6H	Over Temperature Status	Over Temperature Status
A7H	Under Temperature Status	Under Temperature Status
A8H	Over Current and Current Wake Status	Over Current and Current Wake Status
A9H	BAT Voltage Status	BAT Voltage, EOC, OW, OV17, UV17 Status
AAH	Load Detection Status	Load Detection Status
ABH	Coulomb Counter bit 31-24	Coulomb Counter bit 31-24
ACH	Coulomb Counter bit 23-16	Coulomb Counter bit 23-16
ADH	Coulomb Counter bit 15-8	Coulomb Counter bit 15-8
AEH	Coulomb Counter bit 7-0	Coulomb Counter bit 7-0
B2H	Secondary Charge Over Temperature Threshold Configuration	Secondary Charge Over Temperature Threshold Configuration
B3H	Secondary Charge Over Temperature Recovery Threshold Configuration	Secondary Charge Over Temperature Recovery Threshold Configuration
B4H	Secondary Discharge Over Temperature Threshold Configuration	Secondary Discharge Over Temperature Threshold Configuration
B5H	Secondary Discharge Over Temperature Recovery Threshold Configuration	Secondary Discharge Over Temperature Recovery Threshold Configuration
B6H	Secondary Over Temperature Threshold Configuration	Secondary Over Temperature Threshold Configuration
B7H	Secondary Over Temperature Delay Time Configuration	Secondary Over Temperature Delay Time Configuration
B8H	Secondary Over Temperature Recovery Delay Time Configuration	Secondary Over Temperature Recovery Delay Time Configuration
B9H	Secondary Protection Status and Flag	Secondary Protection Status and Flag
C0H	Cell1 Voltage ADC Measurement Result	Cell1 Voltage ADC Measurement Result
C1H	Cell1 Voltage ADC Measurement Result	Cell1 Voltage ADC Measurement Result
C2H	Cell2 Voltage ADC Measurement Result	Cell2 Voltage ADC Measurement Result

Address	Register Name	Description
C3H	Cell2 Voltage ADC Measurement Result	Cell2 Voltage ADC Measurement Result
C4H	Cell3 Voltage ADC Measurement Result	Cell3 Voltage ADC Measurement Result
C5H	Cell3 Voltage ADC Measurement Result	Cell3 Voltage ADC Measurement Result
C6H	Cell4 Voltage ADC Measurement Result	Cell4 Voltage ADC Measurement Result
C7H	Cell4 Voltage ADC Measurement Result	Cell4 Voltage ADC Measurement Result
C8H	Cell5 Voltage ADC Measurement Result	Cell5 Voltage ADC Measurement Result
C9H	Cell5 Voltage ADC Measurement Result	Cell5 Voltage ADC Measurement Result
CAH	Cell6 Voltage ADC Measurement Result	Cell6 Voltage ADC Measurement Result
CBH	Cell6 Voltage ADC Measurement Result	Cell6 Voltage ADC Measurement Result
CCH	Cell7 Voltage ADC Measurement Result	Cell7 Voltage ADC Measurement Result
CDH	Cell7 Voltage ADC Measurement Result	Cell7 Voltage ADC Measurement Result
CEH	Cell8 Voltage ADC Measurement Result	Cell8 Voltage ADC Measurement Result
CFH	Cell8 Voltage ADC Measurement Result	Cell8 Voltage ADC Measurement Result
D0H	Cell9 Voltage ADC Measurement Result	Cell9 Voltage ADC Measurement Result
D1H	Cell9 Voltage ADC Measurement Result	Cell9 Voltage ADC Measurement Result
D2H	Cell10 Voltage ADC Measurement Result	Cell10 Voltage ADC Measurement Result
D3H	Cell10 Voltage ADC Measurement Result	Cell10 Voltage ADC Measurement Result
D4H	Cell11 Voltage ADC Measurement Result	Cell11 Voltage ADC Measurement Result
D5H	Cell11 Voltage ADC Measurement Result	Cell11 Voltage ADC Measurement Result
D6H	Cell12 Voltage ADC Measurement Result	Cell12 Voltage ADC Measurement Result

Address	Register Name	Description
D7H	Cell12 Voltage ADC Measurement Result	Cell12 Voltage ADC Measurement Result
D8H	Cell13 Voltage ADC Measurement Result	Cell13 Voltage ADC Measurement Result
D9H	Cell13 Voltage ADC Measurement Result	Cell13 Voltage ADC Measurement Result
DAH	Cell14 Voltage ADC Measurement Result	Cell14 Voltage ADC Measurement Result
DBH	Cell14 Voltage ADC Measurement Result	Cell14 Voltage ADC Measurement Result
DCH	Cell15 Voltage ADC Measurement Result	Cell15 Voltage ADC Measurement Result
DDH	Cell15 Voltage ADC Measurement Result	Cell15 Voltage ADC Measurement Result
DEH	Cell16 Voltage ADC Measurement Result	Cell16 Voltage ADC Measurement Result
DFH	Cell16 Voltage ADC Measurement Result	Cell16 Voltage ADC Measurement Result
E0H	Cell17 Voltage ADC Measurement Result	Cell17 Voltage ADC Measurement Result
E1H	Cell17 Voltage ADC Measurement Result	Cell17 Voltage ADC Measurement Result
E2H	GPIO1 Voltage ADC Measurement Result	GPIO1 Voltage ADC Measurement Result
E3H	GPIO1 Voltage ADC Measurement Result	GPIO1 Voltage ADC Measurement Result
E4H	GPIO2 Voltage ADC Measurement Result	GPIO2 Voltage ADC Measurement Result
E5H	GPIO2 Voltage ADC Measurement Result	GPIO2 Voltage ADC Measurement Result
E6H	GPIO3 Voltage ADC Measurement Result	GPIO3 Voltage ADC Measurement Result
E7H	GPIO3 Voltage ADC Measurement Result	GPIO3 Voltage ADC Measurement Result
E8H	GPIO4 Voltage ADC Measurement Result	GPIO4 Voltage ADC Measurement Result
E9H	GPIO4 Voltage ADC Measurement Result	GPIO4 Voltage ADC Measurement Result
ECH	BAT Voltage ADC Measurement Result	BAT Voltage ADC Measurement Result

Address	Register Name	Description
EDH	BAT Voltage ADC Measurement Result	BAT Voltage ADC Measurement Result
EEH	VAO Voltage ADC Measurement Result	VAO Voltage ADC Measurement Result
EFH	VAO Voltage ADC Measurement Result	VAO Voltage ADC Measurement Result
F0H	VBG Voltage ADC Measurement Result	VBG Voltage ADC Measurement Result
F1H	VBG Voltage ADC Measurement Result	VBG Voltage ADC Measurement Result
F2H	VDRIVE Voltage ADC Measurement Result	VDRIVE Voltage ADC Measurement Result
F3H	VDRIVE Voltage ADC Measurement Result	VDRIVE Voltage ADC Measurement Result
F4H	C0 Voltage ADC Measurement Result	C0 Voltage ADC Measurement Result
F5H	C0 Voltage ADC Measurement Result	C0 Voltage ADC Measurement Result
F6H	LOAD Voltage ADC Measurement Result	LOAD Voltage ADC Measurement Result
F7H	LOAD Voltage ADC Measurement Result	LOAD Voltage ADC Measurement Result
F8H	VREG Voltage ADC Measurement Result	VREG Voltage ADC Measurement Result
F9H	VREG Voltage ADC Measurement Result	VREG Voltage ADC Measurement Result
FAH	VREGD Voltage ADC Measurement Result	VREGD Voltage ADC Measurement Result
FBH	VREGD Voltage ADC Measurement Result	VREGD Voltage ADC Measurement Result
FCH	VTSREF Voltage ADC Measurement Result	VTSREF Voltage ADC Measurement Result
FDH	VTSREF Voltage ADC Measurement Result	VTSREF Voltage ADC Measurement Result
FEH	Current ADC Measurement Result	Current ADC Measurement Result
FFH	Current ADC Measurement Result	Current ADC Measurement Result

Analog Timer Control 1 (Address = 40H)

Bit	Field	Type	Reset	Description
7:6	BAL_RLS_TIMER_SEL	R/W	0x00	Balance release timer selection When ADC measurement is required during cell balance, balancing suspends, and after the release time, ADC measurement starts. 00: 100μs 01: 1ms 10: 2ms 11: 20ms
5:4	OW_RLS_CFG	R/W	0x02	Open wire release time configuration Cell balance FET off time in open wire detection 00: 40μs 01: 200μs 10: 1ms 11: 4ms
3:2	TSREF_TIMER_SEL	R/W	0x01	TSREF on delay time selection 00: 2ms 01: 4ms 10: 6ms 11: 8ms
1:0	VM_PD_SEL	R/W	0x00	Load detect pull down resistor configuration 00: 1900kΩ 01: 300kΩ 10: 100kΩ 11: 45kΩ

Analog Timer Control 2 (Address = 41H)

Bit	Field	Type	Reset	Description
7:5	LS_TIMER_SEL	R/W	0x00	**Delay Time before ADC DSM Start** 000: 25μs 001: 50μs 010: 100μs 011: 200μs 100: 1ms 101: 4ms 110: 8ms others: 25μs
4	VREGD_5V_EN	R/W	0x00	VREGD voltage configuration 0: VREGD=3.3V 1: VREGD=VREG
3:0	OFST_CADC_EXT_H	R/W	0x00	**CADC Offset Calibration high 4 bits**

Bit	Field	Type	Reset	Description
				If OFST_CADC_EXT_H[3]=0, CADC offset calibration is (OFST_CADC_EXT_H*256+OFST_CADC_EXT_L)*4μV If OFST_CADC_EXT_H[3]=1, CADC offset calibration is -(4096-OFST_CADC_EXT_H*256-OFST_CADC_EXT_L)*4μV

CADC Calibration 1 (Address = 42H)

Bit	Field	Type	Reset	Description
7:0	OFST_CADC_EXT_L	R/W	0x00	**CADC Offset Calibration low 8 bits** If OFST_CADC_EXT_H[3]=0, CADC offset calibration is (OFST_CADC_EXT_H*256+OFST_CADC_EXT_L)*4μV If OFST_CADC_EXT_H[3]=1, CADC offset calibration is -(4096-OFST_CADC_EXT_H*256-OFST_CADC_EXT_L)*4μV

FET SYNC (Address = 43H)

Bit	Field	Type	Reset	Description
7	DFETSYNC_ON	R/W	0x01	DSG FET Sync Configuration When DSG FET Sync is enabled by REG79[5], DSG FET is controlled by DFETSYNC when charge current is larger than CWAKEC 0: off 1: on
6	CFETSYNC_ON	R/W	0x01	DSG FET Sync Configuration When CHG FET Sync is enabled by REG79[6], CHG FET is controlled by CFETSYNC when discharge current is larger than CWAKED 0: off 1: on
5:0	VADC_GAINERR_CALIB	R/W	0x00	VADC Gain Error Calibration The LSB is 0.0015%, the max calibration capability is 0.096%

Mode and Driver Control (Address = 44H)

Bit	Field	Type	Reset	Description
7	PCDRV_20U	R/W	0x00	Precharge FET driver current 0: 10μA 1: 20μA
6	CDRV_20U	R/W	0x00	Charge FET driver current 0: 10μA 1: 20μA

Bit	Field	Type	Reset	Description
5	REG_CTRL	R/W	0x00	CHG FET and DSG FET driver controlled by register 0: not controlled by register 1: controlled by register
4:3	Reversed	R/W	0x01	Reversed
2	DPSLP_MODE_DIS	R/W	0x00	Deep sleep mode enter configuration 0: Enter deep sleep mode is allowed 1: Enter deep sleep mode is not allowed
1	SLP_MODE_DIS	R/W	0x00	Sleep mode enter configuration 0: Enter sleep mode is allowed 1: Enter sleep mode is not allowed
0	Reversed	R/W	0x01	Reversed

Sleep Mode Quiet Period (Address = 45H)

Bit	Field	Type	Reset	Description
7:0	SLEEP_PERIOD	R/W	0x1E	Sleep mode quiet stage period Quiet stage period time is SLEEP_PERIOD*100ms.

Sleep Mode Wake Period (Address = 46H)

Bit	Field	Type	Reset	Description
7:0	WAKE_PERIOD	R/W	0x05	Sleep mode wake stage period Wake stage period time is WAKE_PERIOD*100ms.

Cell and Aux Measurement Loop Period (Address = 47H)

Bit	Field	Type	Reset	Description
7:4	CELL_PERIOD	R/W	0x01	Cell measurement loop period 0000: 50ms 0001: 100ms 0010: 250ms 0011: 500ms 0100: 1s 0101: 2s 0110: 3s 0111: 4s 1000: 5s 1001: 8s 1010: 10s 1111: Cell measurement disabled others: 100ms

Bit	Field	Type	Reset	Description
3:0	AUX_PERIOD	R/W	0x03	Aux measurement loop period 0000: 50ms 0001: 100ms 0010: 250ms 0011: 500ms 0100: 1s 0101: 2s 0110: 3s 0111: 4s 1000: 5s 1001: 8s 1010: 10s 1111: Aux measurement disabled others: 1s

Load Detection and Open Wire Detection Period (Address = 48H)

Bit	Field	Type	Reset	Description
6:4	OW_PERIOD	R/W	0x01	Open wire detection period 000: 1s 001: 5s 010: 10s 011: 20s 100: 50s 101: 80s 111：OW detection disabled others: 80s
3:0	LD_PERIOD	R/W	0x04	Load detection period selection 0000: 50ms 0001: 100ms 0010: 250ms 0011: 500ms 0100: 1s 0101: 2s 0110: 3s 0111: 4s 1000: 5s 1001: 8s 1010: 10s 1111: load detect disabled others: 2s

Open Wire Detection Configuration and CADC Period (Address = 49H)

Bit	Field	Type	Reset	Description
7:4	CADC_PERIOD	R/W	0x04	Current ADC measurement loop period 0000: 50ms 0001: 100ms 0010: 250ms 0011: 500ms 0100: 1s 0101: 2s 0110: 3s 0111: 4s 1000: 5s 1001: 8s 1010: 10s 1111: CADC measurement disabled others: 10s
3:2	OW_TH_SEL	R/W	0x00	Open wire detection threshold 00: 0.4864V 01: 0.9984V 10: 1.5104V 11: 1.9968V
1	LD_TH_SEL	R/W	0x00	Load removal detection threshold 0: If LOAD voltage < 1V is detected, load removal is detected 1: If LOAD voltage < 0.5V is detected, load removal is detected
0	VCELL_RANGE	R/W	0x00	Cell OV/UV Threshold Range Selection 0: 3.3V 1: 4V

Cell Over Voltage Threshold (Address = 4AH)

Bit	Field	Type	Reset	Description
7:0	OV_TH_SEL	R/W	0x18	Cell Over Voltage Threshold If VCELL_RANGE=0, OV threshold is 3398.4+OV_TH_SEL*6.4 (mV) If VCELL_RANGE=1, OV threshold is 4096+OV_TH_SEL*6.4 (mV)

Cell Over Voltage Recovery Threshold (Address = 4BH)

Bit	Field	Type	Reset	Description
7:0	OV_RCV_SEL	R/W	0x75	Cell Over Voltage Recovery Threshold

Bit	Field	Type	Reset	Description
				If VCELL_RANGE=0, OV recovery threshold is 2598.4+OV_RCV_SEL*6.4 (mV) If VCELL_RANGE=1, OV recovery threshold is 3296+OV_RCV_SEL*6.4 (mV)

Cell Under Voltage Threshold (Address = 4CH)

Bit	Field	Type	Reset	Description
7:0	UV_TH_SEL	R/W	0x08	Cell Under Voltage Threshold If VCELL_RANGE=0, UV threshold is 1798.4+UV_TH_SEL*6.4 (mV) If VCELL_RANGE=1, UV threshold is 2796.8+UV_TH_SEL*6.4 (mV)

Cell Under Voltage Recovery Threshold (Address = 4DH)

Bit	Field	Type	Reset	Description
7:0	UV_RCV_SEL	R/W	0x27	Cell Under Voltage Recovery Threshold If VCELL_RANGE=0, UV recovery threshold is 1798.4+UV_RCV_SEL*12.8 (mV) If VCELL_RANGE=1, UV recovery threshold is 2796.8+UV_RCV_SEL*12.8 (mV)

Cell Super Under Voltage Threshold (Address = 4EH)

Bit	Field	Type	Reset	Description
7:0	SUV_TH_SEL	R/W	0x6D	Cell Super Under Voltage Threshold Super UV threshold is 499.2+SUV_TH_SEL*6.4 (mV)

Cell Super Under Voltage Recovery Threshold (Address = 4FH)

Bit	Field	Type	Reset	Description
7:0	SUV_RCV_SEL	R/W	0x85	Cell Super Under Voltage Recovery Threshold Super UV recovery threshold is 499.2+SUV_RCV_SEL*12.8 (mV)

GPIO Voltage Threshold for Charge Over Temperature (Address = 50H)

Bit	Field	Type	Reset	Description
7:0	OTC_TH_SEL	R/W	0x56	GPIO Voltage Threshold for Charge Over Temperature OTC threshold is 198.4+OTC_TH_SEL*6.4 (mV)

GPIO Voltage Threshold for Charge Over Temperature Recovery (Address = 51H)

Bit	Field	Type	Reset	Description
7:0	OTC_RCV_SEL	R/W	0x94	GPIO Voltage Threshold for Charge Over Temperature Recovery OTC recovery threshold is 198.4+OTC_RCV_SEL*6.4 (mV)

GPIO Voltage Threshold for Charge Under Temperature (Address = 52H)

Bit	Field	Type	Reset	Description
7:0	UTC_TH_SEL	R/W	0x7D	GPIO Voltage Threshold for Charge Under Temperature UTC threshold is 1798.4+UTC_TH_SEL*6.4 (mV)

GPIO Voltage Threshold for Charge Under Temperature Recovery (Address = 53H)

Bit	Field	Type	Reset	Description
7:0	UTC_RCV_SEL	R/W	0xA5	GPIO Voltage Threshold for Charge Under Temperature Recovery UTC recovery threshold is 1344+OTC_RCV_SEL*6.4 (mV)

GPIO Voltage Threshold for Discharge Over Temperature (Address = 54H)

Bit	Field	Type	Reset	Description
7:0	OTD_TH_SEL	R/W	0x26	GPIO Voltage Threshold for Discharge Over Temperature OTD threshold is 198.4+OTD_TH_SEL*6.4 (mV)

GPIO Voltage Threshold for Discharge Over Temperature Recovery (Address = 55H)

Bit	Field	Type	Reset	Description
7:0	OTD_RCV_SEL	R/W	0x45	GPIO Voltage Threshold for Discharge Over Temperature Recovery OTD recovery threshold is 198.4+OTD_RCV_SEL*6.4 (mV)

GPIO Voltage Threshold for Discharge Under Temperature (Address = 56H)

Bit	Field	Type	Reset	Description
7:0	UTD_TH_SEL	R/W	0x9C	GPIO Voltage Threshold for Discharge Under Temperature UTD threshold is 1798.4+UTD_TH_SEL*6.4 (mV)

GPIO Voltage Threshold for Discharge Under Temperature Recovery (Address = 57H)

Bit	Field	Type	Reset	Description
7:0	UTD_RCV_SEL	R/W	0xC4	GPIO Voltage Threshold for Discharge Under Temperature Recovery UTD recovery threshold is 1344+UTC_RCV_SEL*6.4 (mV)

Charge Over Current and Low Current Threshold (Address = 5DH)

Bit	Field	Type	Reset	Description
7:3	COC_SEL	R/W	0x03	Charge Over Current Threshold 00000: 4mV 00001: 8mV 00010: 12mV 11111: 128mV
2:0	LCURR_TH_SEL	R/W	0x01	Low Current Threshold The device can enter sleep mode if Current ADC detect low current 000: 50μV 001: 100μV 010: 150μV 011: 200μV 100: 500μV

Discharge Over Current Threshold (Address = 5EH)

Bit	Field	Type	Reset	Description
7:3	DOC_SEL	R/W	0x06	Discharge Over Current Threshold 00000: 12mV 00001: 18mV 00010: 24mV 11111: 198mV
2:0	SCD_SEL	R/W	0x04	Discharge Short Current Threshold

Bit	Field	Type	Reset	Description
				000: 16mV 001: 32mV 010: 48mV 011: 64mV 100: 144mV 101: 224mV 110: 304mV 111: 384mV

Wake Current Threshold (Address = 5FH)

Bit	Field	Type	Reset	Description
7:4	CWAKED_SEL	R/W	0x04	Discharge Current Wake Threshold 0000: 0.25mV 0001: 0.5mV 0010: 0.75mV 1111: 4mV
3:0	CWAKEC_SEL	R/W	0x04	Charge Current Wake Threshold 0000: 0.25mV 0001: 0.5mV 0010: 0.75mV 1111: 4mV

Over Current Comparator Configuration (Address = 60H)

Bit	Field	Type	Reset	Description
7	SUV_VALID	R/W	0x00	SUV trigger shutdown enable configuration 0: disable 1: enable
6	TSREF_ON	R/W	0x00	TSREF always on in sleep mode enable configuration 0: disable 1: enable
5	CWAKEC_EN	R/W	0x01	Charge Current WAKE Enable 0: disable 1: enable
4	COC_EN	R/W	0x01	Charge Over Current Enable 0: disable 1: enable
3	CWAKED_EN	R/W	0x01	Discharge Current WAKE Enable 0: disable

Bit	Field	Type	Reset	Description
				1: enable
2	SCD_EN	R/W	0x01	Discharge Short Current Enable 0: disable 1: enable
1	DOC_EN	R/W	0x01	Discharge Over Current Enable 0: disable 1: enable
0	reserved	R/W	0x00	reserved

OVUV Delay Time Configuration (Address = 61H)

Bit	Field	Type	Reset	Description
7:4	OV_DLY_SEL	R/W	0x06	Cell Over Voltage Delay Time Selection 0000: 50ms 0001: 120ms 0010: 250ms 0011: 500ms 0100: 1s 0101: 1.5s 0110: 2s 0111: 4s 1000: 6s 1001: 8s 1010: 10s others: 100ms
3:0	UV_DLY_SEL	R/W	0x07	Cell Under Voltage Delay Time Selection 0000: 50ms 0001: 120ms 0010: 250ms 0011: 500ms 0100: 1s 0101: 1.5s 0110: 2s 0111: 4s 1000: 6s 1001: 8s 1010: 10s others: 100ms

SUV Delay Time and DOC Recovery Way Configuration (Address = 62H)

Bit	Field	Type	Reset	Description
7:4	reserved	R/W	0x05	reserved

Bit	Field	Type	Reset	Description
3:2	DOC_RCV_SEL	R/W	0x01	Discharge Over Current Recovery Ways Selection 00: recover when load removal is detected 01: recover after DOC_RCV_DLY_SEL 10/11: recover after DOC_RCV_DLY_SEL, if retry 3 times, DOC protection is latched.
1:0	SUV_DLY_SEL	R/W	0x01	Cell Super Under Voltage Delay Time Selection 00: 2s 01: 4s 10: 8s 11: 20s

UTC and OTC Delay Time Configuration (Address = 63H)

Bit	Field	Type	Reset	Description
7:4	UTC_DLY_SEL	R/W	0x06	Charge Under Temperature Delay Time Selection 0000: 50ms 0001: 120ms 0010: 250ms 0011: 500ms 0100: 1s 0101: 1.5s 0110: 2s 0111: 4s 1000: 6s 1001: 8s 1010: 10s others: 100ms
3:0	OTC_DLY_SEL	R/W	0x06	Charge Over Temperature Delay Time Selection 0000: 50ms 0001: 120ms 0010: 250ms 0011: 500ms 0100: 1s 0101: 1.5s 0110: 2s 0111: 4s 1000: 6s 1001: 8s 1010: 10s others: 100ms

UTD and OTD Delay Time Configuration (Address = 64H)

Bit	Field	Type	Reset	Description
7:4	UTD_DLY_SEL	R/W	0x06	Discharge Under Temperature Delay Time Selection 0000: 50ms 0001: 120ms 0010: 250ms 0011: 500ms 0100: 1s 0101: 1.5s 0110: 2s 0111: 4s 1000: 6s 1001: 8s 1010: 10s others: 100ms
3:0	OTD_DLY_SEL	R/W	0x04	Discharge Over Temperature Delay Time Selection 0000: 50ms 0001: 120ms 0010: 250ms 0011: 500ms 0100: 1s 0101: 1.5s 0110: 2s 0111: 4s 1000: 6s 1001: 8s 1010: 10s others: 100ms

Over and Under Temperature Recovery Delay Time Configuration (Address = 65H)

Bit	Field	Type	Reset	Description
7:6	UTD_RCV_DLY_SEL	R/W	0x03	Discharge Under Temperature Recovery Delay Time Selection 00: 0ms 01: 200ms 10: 1s 11: 2s
5:4	OTD_RCV_DLY_SEL	R/W	0x03	Discharge Over Temperature Recovery Delay Time Selection 00: 0ms 01: 200ms 10: 1s 11: 2s

Bit	Field	Type	Reset	Description
3:2	UTC_RCV_DLY_SEL	R/W	0x03	Charge Under Temperature Recovery Delay Time Selection 00: 0ms 01: 200ms 10: 1s 11: 2s
1:0	OTC_RCV_DLY_SEL	R/W	0x03	Charge Over Temperature Recovery Delay Time Selection 00: 0ms 01: 200ms 10: 1s 11: 2s

Charge Over Current Delay Time Configuration (Address = 66H)

Bit	Field	Type	Reset	Description
7:5	reserved	R/W	0x02	reserved
4:0	COC_DLY_SEL	R/W	0x01	Charge Over Current Delay Time Selection COC delay time is 40*COC_DLY_SEL+10 (ms)

Discharge Over Current Delay Time Configuration (Address = 67H)

Bit	Field	Type	Reset	Description
7	INIT_ALT_EN	R/W	0x01	Initiation precedure error trigger Alert enable configuration 0: disable 1: enable
6	EOC_ALT_EN	R/W	0x01	EOC trigger Alert enable configuration 0: disable 1: enable
5	SCD_RCV_SEL	R/W	0x01	SCD flag bit clear ways 0: write corresponding register bit to clear 1: self clear when load removal is detected
4:0	DOC_DLY_SEL	R/W	0x01	Discharge Over Current Delay Time Selection DOC delay time is 40*DOC_DLY_SEL+10 (ms)

Low Current and SCD Delay Time Configuration (Address = 68H)

Bit	Field	Type	Reset	Description
7:4	LCURR_DLY_SEL	R/W	0x03	CADC low current detection delay time

Bit	Field	Type	Reset	Description
				low current detection delay time is 20*LCURR_DLY_SEL+10 (ms)
3:0	SCD_DLY_SEL	R/W	0x03	Discharge Short Current Delay Time Selection SCD delay time is SCD_DLY_SEL*10 (μs)+5μs

Over Current Recovery Configuration (Address = 69H)

Bit	Field	Type	Reset	Description
7:6	COC_RCV_DLY_SEL	R/W	0x02	Charge over current recovery delay time 00: 0 01: 200ms 10: 1s 11: 2s
5:4	COC_RCV_SEL	R/W	0x01	Charge Over Current Recovery Ways Selection 00: recover when charger removal is detected 01: recover after COC_RCV_DLY_SEL 10/11: recover after COC_RCV_DLY_SEL , if try 3 times, COC protection is latched.
3:1	DOC_RCV_DLY_SEL	R/W	0x03	Discharge over current recovery delay time 000: 0ms 001: 100ms 010: 200ms 011: 500ms 100: 1s 101: 2s others: 500ms
0	reserved	R/W	0x00	reserved

Precharge and Precharge Recovery Voltage Threshold Configuration (Address = 6AH)

Bit	Field	Type	Reset	Description
7:4	PCHG_RCV_SEL	R/W	0x0C	Precharge Recovery Voltage Threshold 0000: 12V 0001: 14.5V 0010: 17V 1111: 49.5V
3:0	PCHG_SEL	R/W	0x0A	Precharge Voltage Threshold 0000: 6V 0001: 8.5V 0010: 11V .....

Bit	Field	Type	Reset	Description
				1111: 43.5V

Cell Voltage Measurement Enable Configuration (Address = 6BH)

Bit	Field	Type	Reset	Description
7	CELL16_EN	R/W	0x01	Cell 16 Voltage Measurement Enable Configuration 0: disable 1: enable
6	CELL15_EN	R/W	0x01	Cell 15 Voltage Measurement Enable Configuration 0: disable 1: enable
5	CELL14_EN	R/W	0x01	Cell 14 Voltage Measurement Enable Configuration 0: disable 1: enable
4	CELL13_EN	R/W	0x01	Cell 13 Voltage Measurement Enable Configuration 0: disable 1: enable
3	CELL12_EN	R/W	0x01	Cell 12 Voltage Measurement Enable Configuration 0: disable 1: enable
2	CELL11_EN	R/W	0x01	Cell 11 Voltage Measurement Enable Configuration 0: disable 1: enable
1	CELL10_EN	R/W	0x01	Cell 10 Voltage Measurement Enable Configuration 0: disable 1: enable
0	CELL9_EN	R/W	0x01	Cell 9 Voltage Measurement Enable Configuration 0: disable 1: enable

Cell Voltage Measurement Enable Configuration (Address = 6CH)

Bit	Field	Type	Reset	Description
7	CELL8_EN	R/W	0x01	Cell 8 Voltage Measurement Enable Configuration 0: disable 1: enable
6	CELL7_EN	R/W	0x01	Cell 7 Voltage Measurement Enable Configuration 0: disable 1: enable
5	CELL6_EN	R/W	0x01	Cell 6 Voltage Measurement Enable Configuration 0: disable

Bit	Field	Type	Reset	Description
				1: enable
4	CELL5_EN	R/W	0x01	Cell 5 Voltage Measurement Enable Configuration 0: disable 1: enable
3	CELL4_EN	R/W	0x01	Cell 4 Voltage Measurement Enable Configuration 0: disable 1: enable
2	CELL3_EN	R/W	0x01	Cell 3 Voltage Measurement Enable Configuration 0: disable 1: enable
1	CELL2_EN	R/W	0x01	Cell 2 Voltage Measurement Enable Configuration 0: disable 1: enable
0	CELL1_EN	R/W	0x01	Cell 1 Voltage Measurement Enable Configuration 0: disable 1: enable

GPIO and REF Voltage Measurement Enable Configuration (Address = 6DH)

Bit	Field	Type	Reset	Description
7	VREGD_EN	R/W	0x01	VREGD Voltage Measurement Enable Configuration 0: disable 1: enable
6	TSREF_EN	R/W	0x01	TSREF Voltage Measurement Enable Configuration 0: disable 1: enable
5	reserved	R/W	0x00	reserved
4	GPIO4_EN	R/W	0x01	GPIO 4 Voltage Measurement Enable Configuration 0: disable 1: enable
3	GPIO3_EN	R/W	0x01	GPIO 3 Voltage Measurement Enable Configuration 0: disable 1: enable
2	GPIO2_EN	R/W	0x01	GPIO 2 Voltage Measurement Enable Configuration 0: disable 1: enable
1	GPIO1_EN	R/W	0x01	GPIO 1 Voltage Measurement Enable Configuration 0: disable 1: enable
0	CELL17_EN	R/W	0x01	Cell 17 Voltage Measurement Enable Configuration 0: disable 1: enable

AUX Voltage Measurement Enable Configuration (Address = 6EH)

Bit	Field	Type	Reset	Description
7	reserved	R/W	0x00	reserved
6	VREG_EN	R/W	0x01	VREG Voltage Measurement Enable Configuration 0: disable 1: enable
5	LOAD_EN	R/W	0x01	Load pin Voltage Measurement Enable Configuration 0: disable 1: enable
4	C0_EN	R/W	0x01	C0 Voltage Measurement Enable Configuration 0: disable 1: enable
3	DRIVE_EN	R/W	0x01	DRIVE Voltage Measurement Enable Configuration 0: disable 1: enable
2	VBG_EN	R/W	0x01	VBG Voltage Measurement Enable Configuration 0: disable 1: enable
1	VAO_EN	R/W	0x01	VAO Voltage Measurement Enable Configuration 0: disable 1: enable
0	BAT_EN	R/W	0x01	BAT Voltage Measurement Enable Configuration 0: disable 1: enable

Alert Enable Configuration 1 (Address = 6FH)

Bit	Field	Type	Reset	Description
7	DOC_ALT_EN	R/W	0x01	DOC Trigger Alert Enable Configuration 0: disable 1: enable
6	UTD_ALT_EN	R/W	0x01	UTD Trigger Alert Enable Configuration 0: disable 1: enable
5	OTD_ALT_EN	R/W	0x01	OTD Trigger Alert Enable Configuration 0: disable 1: enable
4	UTC_ALT_EN	R/W	0x01	UTC Trigger Alert Enable Configuration 0: disable 1: enable
3	OTC_ALT_EN	R/W	0x01	OTC Trigger Alert Enable Configuration

Bit	Field	Type	Reset	Description
				0: disable 1: enable
2	OW_ALT_EN	R/W	0x01	OW Trigger Alert Enable Configuration 0: disable 1: enable
1	UV_ALT_EN	R/W	0x01	UV Trigger Alert Enable Configuration 0: disable 1: enable
0	OV_ALT_EN	R/W	0x01	OV Trigger Alert Enable Configuration 0: disable 1: enable

Alert Enable Configuration 2 (Address = 70H)

Bit	Field	Type	Reset	Description
7	reserved	R/W	0x00	reserved
6	CCOF_ALT_EN	R/W	0x00	Coulomb Counter Trigger Alert Enable Configuration 0: disable 1: enable
5	CWAKED_ALT_EN	R/W	0x00	Discharge Wake Current Trigger Alert Enable Configuration 0: disable 1: enable
4	CWAKEC_ALT_EN	R/W	0x00	Charge Wake Current Trigger Alert Enable Configuration 0: disable 1: enable
3	CHG_ALT_EN	R/W	0x00	Charger Plug in Trigger Alert Enable Configuration 0: disable 1: enable
2	LOAD_ALT_EN	R/W	0x00	LOAD detection Trigger Alert Enable Configuration 0: disable 1: enable
1	SCD_ALT_EN	R/W	0x01	SCD Trigger Alert Enable Configuration 0: disable 1: enable
0	COC_ALT_EN	R/W	0x01	COC Trigger Alert Enable Configuration 0: disable 1: enable

EOC and Balance Configuration (Address = 71H)

Bit	Field	Type	Reset	Description
7	FIFO_ALT_EN	R/W	0x01	FIFO full Trigger Alert Enable Configuration 0: disable 1: enable
6:4	VCB_HYS_SEL	R/W	0x01	Cell Voltage Difference Threshold to Stop Balancing 000: 5mV 001: 15mV 010: 20mV 011: 50mV 100: 80mV others: 5mV
3	EOC_EN	R/W	0x01	End of Charge Enable Configuration 0: disable 1: enable
2:0	IEOC_SEL	R/W	0x01	End of Charge Current Configuration 000: 200μV 001: 500μV 010: 800μV 011: 1200μV 100: 1.5mV 101: 2mV others: 200μV

EOC Threshold Configuration (Address = 72H)

Bit	Field	Type	Reset	Description
7:0	VEOC_SEL	R/W	0x17	End of Charge Threshold Configuration If VCELL_RANGE=0, EOC threshold is 3299.2+VEOC_SEL*6.4 (mV) If VCELL_RANGE=1, EOC threshold is 4000+VEOC_SEL*6.4 (mV)

Balance Start Configuration (Address = 73H)

Bit	Field	Type	Reset	Description
7				
6	RLX_BAL_EN	R/W	0x00	Cell Balance Enable Configuration 0: enable cell balance during charging 1: enable cell balance during charging or idle
5:4	VCB_TH_SEL	R/W	0x01	Cell Voltage Difference Threshold to Start Balancing 00: 15mV 01: 30mV

Bit	Field	Type	Reset	Description
				10: 50mV 11: 100mV
3:0	VCB_START_SEL	R/W	0x00	Balance Start Condition Configuration If VCELL_RANGE=0 0000: 3200mV 0001: 3250mV 0010: 3300mV 0011: 3350mV 0100: 3400mV 0101: 3450mV 0110: 3500mV 0111: 3550mV 1000: 3600mV others: 3200mV If VCELL_RANGE=1 0000: 3800mV 0001: 3850mV 0010: 3900mV 0011: 3950mV 0100: 4000mV 0101: 4050mV 0110: 4100mV 0111: 4150mV 1000: 4200mV others: 3800mV

Balance Time Configuration (Address = 74H)

Bit	Field	Type	Reset	Description
7	BAL_TO_RCV_SEL	R/W	0x00	Balance Timerout Auto Recovery Enable to Clear BAL_TIMER_OUT Flag after 1s delay 0: disable 1: enable
6	BAL_TIMER_DIS	R/W	0x00	Balance Timer Configuration 0: enable 1: disable
5:4	BAL_RANGE_SEL	R/W	0x00	Balance Time Configuration Combination with BAT_TO_SEL 00: small range 01: middle range 10: large range
3:0	BAL_TO_SEL	R/W	0x01	Balance Time Configuration If BAL_RANGE_SEL=0 0000: 200ms

Bit	Field	Type	Reset	Description
				0001: 1s 0010: 2s 0011: 3s 0100: 4s 0101: 5s 0110: 6s 0111: 7s 1000: 8s 1001: 9s 1010: 10s others: 2s If BAL_RANGE_SEL=1 0000: 20s 0001: 30s 0010: 40s 0011: 50s 0100: 60s 0101: 70s 0110: 80s 0111: 90s 1000: 100s 1001: 110s 1010: 120s others: 20s If BAL_RANGE_SEL=2 0000: 200s 0001: 800s 0010: 1400s 0011: 2000s 0100: 2600s 0101: 3200s 0110: 3800s 0111: 4400s 1000: 5000s 1001: 5600s 1010: 6200s others: 800s

Sleep Mode Configuration (Address = 75H)

Bit	Field	Type	Reset	Description
7	reserved	R/W	0x00	reserved
6	AUTO_SLP_DIS	R/W	0x01	Enter Sleep by CMD Enable Configuration 0: not need CMD to enter sleep mode 1: need CMD to enter sleep mode

Bit	Field	Type	Reset	Description
5:4	INIT_SLP_EN	R/W	0x02	Delay Time of First Enter Sleep Mode after Power on 00: 2s 01: 10s 10: 100s 11: 200s
3:2	CWAKED_DEC_SEL	R/W	0x00	Decimation Configuration for CWAKED 00: 64 01: 256 10: 256 11: 256
1:0	CWAKEC_DEC_SEL	R/W	0x00	Decimation Configuration for CWAKEC 00: 64 01: 256 10: 256 11: 256

Wake Current and EOC Delay Time Configuration (Address = 77H)

Bit	Field	Type	Reset	Description
7:6	EOC_DLY_SEL	R/W	0x03	EOC Delay Time Configuration 00: 16s 01: 32s 10: 64s 11: 128s
5:3	CWAKED_DLY_SEL	R/W	0x00	CWAKED Delay Time Configuration 000: 32ms 001: 64ms 010: 128ms 011: 256ms 100: 512ms others: 64ms
2:0	CWAKEC_DLY_SEL	R/W	0x02	CWAKEC Delay Time Configuration 000: 32ms 001: 64ms 010: 128ms 011: 256ms 100: 512ms others: 64ms

Alert Enable Configuration 3 (Address = 78H)

Bit	Field	Type	Reset	Description
7	INIT_OK_ALT_EN	R/W	0x00	Initiation ok Trigger ALERT Enable Configuration 0: disable 1: enable
6	OW_FET_CTL_EN	R/W	0x00	Open Wire Control CHG FET and DSG FET Configuration 0: enable 1: disable
5	OTHP_ALT_EN	R/W	0x00	Thermal Shutdown Trigger ALERT Enable Configuration 0: disable 1: enable
4:0	SPI_ALT_EN	R/W	0x00	SPI Trigger ALERT Enable Configuration

FET Driver Configuration (Address = 79H)

Bit	Field	Type	Reset	Description
7	FET_CTL_INV	R/W	0x00	DFETCTL and CFETCTL Input Invert Configuration 0: not INV 1: INV
6	CFET_SYNC_EN	R/W	0x00	CFET SYNC Function Enable Configuration 0: enable 1: disable
5	DFET_SYNC_EN	R/W	0x00	DFET SYNC Function Enable Configuration 0: enable 1: disable
4	FETCTL_GLITCH_EN	R/W	0x00	Glitch Enable Configuration for CFETCTL and DFETCTL Input 0: disable 1: enable
3	REG_PCFET_CTL_EN	R/W	0x00	Register Control PreCFET Enable Configuration 0: disable 1: enable
2	REG_PDFET_CTL_EN	R/W	0x00	Register Control PreDFET Enable Configuration 0: disable 1: enable
1	REG_CFET_CTL_EN	R/W	0x00	Register Control CFET Enable Configuration 0: disable 1: enable
0	REG_DFET_CTL_EN	R/W	0x00	Register Control DFET Enable Configuration 0: disable 1: enable

Secondary Protection Enable Configuration (Address = 7AH)

Bit	Field	Type	Reset	Description
7	PF_DPSLP_EN	R/W	0x00	Secondary Protection Trigger Device Enter Deepsleep Mode Enable Configuration 0: disable 1: enable
6	PF_EN	R/W	0x00	Secondary Protection Enable Configuration 0: disable 1: enable
5:0	SOV_DLY_CFG	R/W	0x01	Secondary Over Voltage Protection Delay Configuration Delay time is SOV_DLY_CFG*4s

Secondary Protection Threshold Configuration (Address = 7BH)

Bit	Field	Type	Reset	Description
7:0	SOV_TH_CFG	R/W	0x10	Secondary Over Voltage Protection Threshold Configuration If VCELL_RANGE=0, SOV threshold is 3795.2+SOV_DLY_CFG*6.4(mV) If VCELL_RANGE=1, SOV threshold is 4396.8+SOV_DLY_CFG*6.4(mV)

Secondary Protection Threshold Configuration 2 (Address = 7CH)

Bit	Field	Type	Reset	Description
7:6	FUSE_DLY_CFG_H	R/W	0x00	FUSE output high time configuration These two bits are the high MSB of FUSE_DLY_CFG Fuse output high time is FUSE_DLY_CFG*4s+100ms
5:0	SOV_RCV_TH_CFG	R/W	0x1F	Secondary Over Voltage Protection Recovery Threshold Configuration If VCELL_RANGE=0, SOV recovery threshold is 2995.2+SOV_DLY_CFG*25.6(mV) If VCELL_RANGE=1, SOV threshold is 3596.8+SOV_DLY_CFG*25.6(mV)

FUSE Output Configuration (Address = 7DH)

Bit	Field	Type	Reset	Description
7:4	FUSE_DLY_CFG_L	R/W	0x01	FUSE output high time configuration

Bit	Field	Type	Reset	Description
				These four bits are the low LSB of FUSE_DLY_CFG Fuse output high time is FUSE_DLY_CFG*4s+100ms
3:0	PF2FUSE_DLY_CFG	R/W	0x01	Delay Time from Secondary Protection to Fuse Output High Time is PF2FUSE_DLY_CFG*20ms+10ms

FET Driver Configuration 2 (Address = 80H)

Bit	Field	Type	Reset	Description
7: 6	reserved	R/W	0x00	reserved
5	FUSE_DRV_CTL	R/W	0x00	FUSE pin output controlled by host 0: output low 1: output high
4	FUSE_DRV_CFG	R/W	0x00	FUSE pin control ways 0: FUSE pin internal logic 1: host
3	PCFET_CTL	R/W	0x00	Register Control PreCFET Configuration 0: off 1: on
2	PDFET_CTL	R/W	0x00	Register Control PreDFET Configuration 0: off 1: on
1	CFET_CTL	R/W	0x00	Register Control CFET Configuration 0: off 1: on
0	DFET_CTL	R/W	0x00	Register Control DFET Configuration 0: off 1: on

ADC Configuration (Address = 87H)

Bit	Field	Type	Reset	Description
7:6	CADC_OSR	R/W	0x02	Current Measurement ADC OSR Configuration 00: 64 01: 128 10: 256 11: 512
5:4	LD_OSR	R/W	0x02	Load Detection Measurement ADC OSR Configuration 00: 64 01: 128 10: 256

Bit	Field	Type	Reset	Description
				11: 512
3:2	AUX_OSR	R/W	0x02	AUX Voltage Measurement ADC OSR Configuration 00: 64 01: 128 10: 256 11: 512
1: 0	CELL_OSR	R/W	0x02	Cell Voltage Measurement ADC OSR Configuration 00: 64 01: 128 10: 256 11: 512

Flag Clear Configuration 1 (Address = 8AH)

Bit	Field	Type	Reset	Description
7	reserved	R/W	0x00	reserved
6	CLR_ALL	R/W	0x00	Flag related to OTHP Clear Configuration 0: off 1: Clear
5	CLR_BAL	R/W	0x00	Flag related to Cell Balance Clear Configuration 0: off 1: Clear
4	CLR_CC	R/W	0x00	Flag related to Coulomb Counter Clear Configuration 0: off 1: Clear
3	CLR_OW	R/W	0x00	Flag related to Open Wire Detection Clear Configuration 0: off 1: Clear
2	CLR_CADC	R/W	0x00	Flag related to CADC Clear Configuration 0: off 1: Clear
1	CLR_CUR	R/W	0x00	Flag related to Current Clear Configuration 0: off 1: Clear
0	CLR_VOL	R/W	0x00	Flag related to Voltage Clear Configuration 0: off 1: Clear

GPIO Output Enable (Address = 90H)

Bit	Field	Type	Reset	Description
7:4	Reserved	R/W	0x00	Reserved
3	GPIO4_OUT_EN	R/W	0x00	GPIO4 Output Enable 0: GPIO4 as input 1: GPIO4 as output
2	GPIO3_OUT_EN	R/W	0x00	GPIO3 Output Enable 0: GPIO3 as input 1: GPIO3 as output
1	GPIO2_OUT_EN	R/W	0x00	GPIO2 Output Enable 0: GPIO2 as input 1: GPIO2 as output
0	GPIO1_OUT_EN	R/W	0x00	GPIO1 Output Enable 0: GPIO1 as input 1: GPIO1 as output

Power Mode Status (Address = 91H)

Bit	Field	Type	Reset	Description
7:5	reserved	R	0x00	reserved
4:2	MODE_STAT	R	0x00	Power Mode Status 000: shutdown mode 001: initiation mode 010: normal mode 011: sleep mode 100: deepsleep mode 101: initiation error mode 1 110: initiation error mode 2 111: initiation error mode 3
1	DSLP_STAT	R	0x00	Deep Sleep Mode Status 0: not in deep sleep mode 1: in deep sleep mode
0	SLP_STAT	R	0x00	Sleep Mode Status 0: not in sleep mode 1: in sleep mode

FET Driver Status (Address = 92H)

Bit	Field	Type	Reset	Description
7:4	reserved	R	0x00	reserved
3	PCFET_STAT	R	0x00	PreCFET Driver Status 0: off

Bit	Field	Type	Reset	Description
				1: on
2	CFET_STAT	R	0x00	CFET Driver Status 0: off 1: on
1	PDFET_STAT	R	0x00	PreDFET Driver Status 0: off 1: on
0	DFET_STAT	R	0x00	DFET Driver Status 0: off 1: on

SPI Status (Address = 93H)

Bit	Field	Type	Reset	Description
7	POLL_STAT	R	0x00	In host mode, the command implementation status 0: normal 1: command implement done
6:5	Reserved	R	0x00	reserved
4	Data CRC_STAT	R	0x00	Data CRC Status 0: normal 1: Data CRC error
3	COMMAND CRC_STAT	R	0x00	Command CRC Status 0: normal 1: Command CRC error
2	INVALID COMMAND_STAT	R	0x00	Invalid Command Status 0: normal 1: Receive invalid command
1	LONG COMMAND_STAT	R	0x00	Long Command Status 0: normal 1: Receive long command
0	COMMAND_STAT	R	0x00	SPI Command Status 0: normal 1: Not receive command

Open Wire Detection Result (Address = 97H)

Bit	Field	Type	Reset	Description
7:0	OW_SUB	R	0x00	Open wire channel voltage difference between twice ADC result 1LSB=1.024mV

Open Wire Channel (Address = 98H)

Bit	Field	Type	Reset	Description
4:0	OW_CH_STAT	R	0x00	Open Wire Channel 00000: no open wire 00001: channel 1 open wire 00010: channel 2 open wire 00011: channel 3 open wire ..... 10001: channel 17 open wire others: reserved

Cell Over Voltage Flag 1 (Address = 99H)

Bit	Field	Type	Reset	Description
7	OV16_FLG	R	0x00	Cell 16 Over Voltage Flag If cell 16 OV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
6	OV15_FLG	R	0x00	Cell 15 Over Voltage Flag If cell 15 OV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
5	OV14_FLG	R	0x00	Cell 14 Over Voltage Flag If cell 14 OV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
4	OV13_FLG	R	0x00	Cell 13 Over Voltage Flag If cell 13 OV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
3	OV12_FLG	R	0x00	Cell 12 Over Voltage Flag If cell 12 OV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
2	OV11_FLG	R	0x00	Cell 11 Over Voltage Flag If cell 11 OV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
1	OV10_FLG	R	0x00	Cell 10 Over Voltage Flag If cell 10 OV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
0	OV9_FLG	R	0x00	Cell 9 Over Voltage Flag If cell 9 OV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.

Cell Over Voltage Flag 2 (Address = 9AH)

Bit	Field	Type	Reset	Description
7	OV8_FLG	R	0x00	Cell 8 Over Voltage Flag If cell 8 OV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
6	OV7_FLG	R	0x00	Cell 7 Over Voltage Flag If cell 7 OV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
5	OV6_FLG	R	0x00	Cell 6 Over Voltage Flag If cell 6 OV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
4	OV5_FLG	R	0x00	Cell 5 Over Voltage Flag If cell 5 OV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
3	OV4_FLG	R	0x00	Cell 4 Over Voltage Flag If cell 4 OV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
2	OV3_FLG	R	0x00	Cell 3 Over Voltage Flag If cell 3 OV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
1	OV2_FLG	R	0x00	Cell 2 Over Voltage Flag If cell 2 OV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
0	OV1_FLG	R	0x00	Cell 1 Over Voltage Flag If cell 1 OV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.

Cell Under Voltage Flag 1 (Address = 9BH)

Bit	Field	Type	Reset	Description
7	UV16_FLG	R	0x00	Cell 16 Under Voltage Flag If cell 16 UV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
6	UV15_FLG	R	0x00	Cell 15 Under Voltage Flag If cell 15 UV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
5	UV14_FLG	R	0x00	Cell 14 Under Voltage Flag If cell 14 UV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
4	UV13_FLG	R	0x00	Cell 13 Under Voltage Flag If cell 13 UV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
3	UV12_FLG	R	0x00	Cell 12 Under Voltage Flag

Bit	Field	Type	Reset	Description
				If cell 12 UV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
2	UV11_FLG	R	0x00	Cell 11 Under Voltage Flag If cell 11 UV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
1	UV10_FLG	R	0x00	Cell 10 Under Voltage Flag If cell 10 UV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
0	UV9_FLG	R	0x00	Cell 9 Under Voltage Flag If cell 9 UV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.

Cell Under Voltage Flag 2 (Address = 9CH)

Bit	Field	Type	Reset	Description
7	UV8_FLG	R	0x00	Cell 8 Under Voltage Flag If cell 8 UV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
6	UV7_FLG	R	0x00	Cell 7 Under Voltage Flag If cell 7 UV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
5	UV6_FLG	R	0x00	Cell 6 Under Voltage Flag If cell 6 UV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
4	UV5_FLG	R	0x00	Cell 5 Under Voltage Flag If cell 5 UV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
3	UV4_FLG	R	0x00	Cell 4 Under Voltage Flag If cell 4 UV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
2	UV3_FLG	R	0x00	Cell 3 Under Voltage Flag If cell 3 UV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
1	UV2_FLG	R	0x00	Cell 2 Under Voltage Flag If cell 2 UV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
0	UV1_FLG	R	0x00	Cell 1 Under Voltage Flag If cell 1 UV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.

Over Temperature Flag (Address = 9DH)

Bit	Field	Type	Reset	Description
7	GPIO4_OTD_FLG	R	0x00	GPIO4 Over Temperature Discharge Flag If GPIO4 OTD occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
6	GPIO3_OTD_FLG	R	0x00	GPIO3 Over Temperature Discharge Flag If GPIO3 OTD occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
5	GPIO2_OTD_FLG	R	0x00	GPIO2 Over Temperature Discharge Flag If GPIO2 OTD occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
4	GPIO1_OTD_FLG	R	0x00	GPIO1 Over Temperature Discharge Flag If GPIO1 OTD occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
3	GPIO4_OTC_FLG	R	0x00	GPIO4 Over Temperature Charge Flag If GPIO4 OTC occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
2	GPIO3_OTC_FLG	R	0x00	GPIO3 Over Temperature Charge Flag If GPIO3 OTC occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
1	GPIO2_OTC_FLG	R	0x00	GPIO2 Over Temperature Charge Flag If GPIO2 OTC occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
0	GPIO1_OTC_FLG	R	0x00	GPIO1 Over Temperature Charge Flag If GPIO1 OTC occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.

Under Temperature Flag (Address = 9EH)

Bit	Field	Type	Reset	Description
7	GPIO4_UTD_FLG	R	0x00	GPIO4 Under Temperature Discharge Flag If GPIO4 UTD occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
6	GPIO3_UTD_FLG	R	0x00	GPIO3 Under Temperature Discharge Flag If GPIO3 UTD occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
5	GPIO2_UTD_FLG	R	0x00	GPIO2 Under Temperature Discharge Flag If GPIO2 UTD occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
4	GPIO1_UTD_FLG	R	0x00	GPIO1 Under Temperature Discharge Flag If GPIO1 UTD occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
3	GPIO4_UTC_FLG	R	0x00	GPIO4 Under Temperature Charge Flag

Bit	Field	Type	Reset	Description
				If GPIO4 UTC occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
2	GPIO3_UTC_FLG	R	0x00	GPIO3 Under Temperature Charge Flag If GPIO3 UTC occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
1	GPIO2_UTC_FLG	R	0x00	GPIO2 Under Temperature Charge Flag If GPIO2 UTC occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
0	GPIO1_UTC_FLG	R	0x00	GPIO1 Under Temperature Charge Flag If GPIO1 UTC occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.

Over Current and Current Wake Flag (Address = 9FH)

Bit	Field	Type	Reset	Description
7:5	reserved	R	0x00	reserved
4	DOC_FLG	R	0x00	Discharge over current Flag If discharge over current occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
3	SCD_FLG	R	0x00	Discharge short current Flag If discharge short current occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
2	COC_FLG	R	0x00	Charge over current Flag If charge over current occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
1	CWAKED_FLG	R	0x00	CWAKED Flag If discharge current is higher than CWAKED threshold, this bit is set to 1, otherwise 0. This bit needs host to clear it.
0	CWAKEC_FLG	R	0x00	CWAKEC Flag If charge current is higher than CWAKEC threshold, this bit is set to 1, otherwise 0. This bit needs host to clear it.

BAT Voltage Flag (Address = A0H)

Bit	Field	Type	Reset	Description
7	MUX_ERR_FLG	R	0x00	MUX Error Flag If channel mux has error, this bit is set to 1, otherwise 0. This bit needs host to clear it.
6	EOC_FLG	R	0x00	EOC Flag

Bit	Field	Type	Reset	Description
				If EOC is detected, this bit is set to 1, otherwise 0. This bit needs host to clear it.
5	OW_FLG	R	0x00	Open Wire Detection Flag If open wire is detected, this bit is set to 1, otherwise 0. This bit needs host to clear it.
4	BAT_OV_FLG	R	0x00	Bat Over Voltage Flag If Bat OV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
3	BAT_UV_FLG	R	0x00	Bat Under Voltage Flag If bat UV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
2	OV17_FLG	R	0x00	Cell 17 Over Voltage Flag If cell 17 OV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
1	UV17_FLG	R	0x00	Cell 17 Under Voltage Flag If cell 17 UV occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
0	reserved	R	0x00	reserved

Other Flag (Address = A1H)

Bit	Field	Type	Reset	Description
7:4	reserved	R	0x00	reserved
3	BAL_TO_FLG	R	0x00	Balance Timeout Flag If Balance timeout occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
2	CCOF_FLG	R	0x00	Coulomb Counter Overflow Flag If coulomb counter over flow occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
1	CCUF_FLG	R	0x00	Coulomb Counter Under flow Flag If coulomb counter under flow occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.
0	OTHP_FLG	R	0x00	Die Over Temperature Flag If die over temperature occurs, this bit is set to 1, otherwise 0. This bit needs host to clear it.

Cell Over Voltage Status 1 (Address = A2H)

Bit	Field	Type	Reset	Description
7	OV16_STAT	R	0x00	Cell 16 Over Voltage Status If cell 16 OV occurs, this bit is set to 1, otherwise 0

Bit	Field	Type	Reset	Description
6	OV15_STAT	R	0x00	Cell 15 Over Voltage Status If cell 15 OV occurs, this bit is set to 1, otherwise 0
5	OV14_STAT	R	0x00	Cell 14 Over Voltage Status If cell 14 OV occurs, this bit is set to 1, otherwise 0
4	OV13_STAT	R	0x00	Cell 13 Over Voltage Status If cell 13 OV occurs, this bit is set to 1, otherwise 0
3	OV12_STAT	R	0x00	Cell 12 Over Voltage Status If cell 12 OV occurs, this bit is set to 1, otherwise 0
2	OV11_STAT	R	0x00	Cell 11 Over Voltage Status If cell 11 OV occurs, this bit is set to 1, otherwise 0
1	OV10_STAT	R	0x00	Cell 10 Over Voltage Status If cell 10 OV occurs, this bit is set to 1, otherwise 0
0	OV9_STAT	R	0x00	Cell 9 Over Voltage Status If cell 9 OV occurs, this bit is set to 1, otherwise 0

Cell Over Voltage Status 2 (Address = A3H)

Bit	Field	Type	Reset	Description
7	OV8_STAT	R	0x00	Cell 8 Over Voltage Status If cell 8 OV occurs, this bit is set to 1, otherwise 0
6	OV7_STAT	R	0x00	Cell 7 Over Voltage Status If cell 7 OV occurs, this bit is set to 1, otherwise 0
5	OV6_STAT	R	0x00	Cell 6 Over Voltage Status If cell 6 OV occurs, this bit is set to 1, otherwise 0
4	OV5_STAT	R	0x00	Cell 5 Over Voltage Status If cell 5 OV occurs, this bit is set to 1, otherwise 0
3	OV4_STAT	R	0x00	Cell 4 Over Voltage Status If cell 4 OV occurs, this bit is set to 1, otherwise 0
2	OV3_STAT	R	0x00	Cell 3 Over Voltage Status If cell 3 OV occurs, this bit is set to 1, otherwise 0
1	OV2_STAT	R	0x00	Cell 2 Over Voltage Status If cell 2 OV occurs, this bit is set to 1, otherwise 0
0	OV1_STAT	R	0x00	Cell 1 Over Voltage Status If cell 1 OV occurs, this bit is set to 1, otherwise 0

Cell Under Voltage Status 1 (Address = A4H)

Bit	Field	Type	Reset	Description
7	UV16_STAT	R	0x00	Cell 16 Under Voltage Status If cell 16 UV occurs, this bit is set to 1, otherwise 0

Bit	Field	Type	Reset	Description
6	UV15_STAT	R	0x00	Cell 15 Under Voltage Status If cell 15 UV occurs, this bit is set to 1, otherwise 0
5	UV14_STAT	R	0x00	Cell 14 Under Voltage Status If cell 14 UV occurs, this bit is set to 1, otherwise 0
4	UV13_STAT	R	0x00	Cell 13 Under Voltage Status If cell 13 UV occurs, this bit is set to 1, otherwise 0
3	UV12_STAT	R	0x00	Cell 12 Under Voltage Status If cell 12 UV occurs, this bit is set to 1, otherwise 0
2	UV11_STAT	R	0x00	Cell 11 Under Voltage Status If cell 11 UV occurs, this bit is set to 1, otherwise 0
1	UV10_STAT	R	0x00	Cell 10 Under Voltage Status If cell 10 UV occurs, this bit is set to 1, otherwise 0
0	UV9_STAT	R	0x00	Cell 9 Under Voltage Status If cell 9 UV occurs, this bit is set to 1, otherwise 0

Cell Under Voltage Status 2 (Address = A5H)

Bit	Field	Type	Reset	Description
7	UV8_STAT	R	0x00	Cell 8 Under Voltage Status If cell 8 UV occurs, this bit is set to 1, otherwise 0
6	UV7_STAT	R	0x00	Cell 7 Under Voltage Status If cell 7 UV occurs, this bit is set to 1, otherwise 0
5	UV6_STAT	R	0x00	Cell 6 Under Voltage Status If cell 6 UV occurs, this bit is set to 1, otherwise 0
4	UV5_STAT	R	0x00	Cell 5 Under Voltage Status If cell 5 UV occurs, this bit is set to 1, otherwise 0
3	UV4_STAT	R	0x00	Cell 4 Under Voltage Status If cell 4 UV occurs, this bit is set to 1, otherwise 0
2	UV3_STAT	R	0x00	Cell 3 Under Voltage Status If cell 3 UV occurs, this bit is set to 1, otherwise 0
1	UV2_STAT	R	0x00	Cell 2 Under Voltage Status If cell 2 UV occurs, this bit is set to 1, otherwise 0
0	UV1_STAT	R	0x00	Cell 1 Under Voltage Status If cell 1 UV occurs, this bit is set to 1, otherwise 0

Over Temperature Status (Address = A6H)

Bit	Field	Type	Reset	Description
7	GPIO4_OTD_STAT	R	0x00	GPIO4 Over Temperature Discharge Status If GPIO4 OTD occurs, this bit is set to 1, otherwise 0.

Bit	Field	Type	Reset	Description
6	GPIO3_OTD_STAT	R	0x00	GPIO3 Over Temperature Discharge Status If GPIO3 OTD occurs, this bit is set to 1, otherwise 0.
5	GPIO2_OTD_STAT	R	0x00	GPIO2 Over Temperature Discharge Status If GPIO2 OTD occurs, this bit is set to 1, otherwise 0.
4	GPIO1_OTD_STAT	R	0x00	GPIO1 Over Temperature Discharge Status If GPIO1 OTD occurs, this bit is set to 1, otherwise 0.
3	GPIO4_OTC_STAT	R	0x00	GPIO4 Over Temperature Charge Status If GPIO4 OTC occurs, this bit is set to 1, otherwise 0.
2	GPIO3_OTC_STAT	R	0x00	GPIO3 Over Temperature Charge Status If GPIO3 OTC occurs, this bit is set to 1, otherwise 0.
1	GPIO2_OTC_STAT	R	0x00	GPIO2 Over Temperature Charge Status If GPIO2 OTC occurs, this bit is set to 1, otherwise 0.
0	GPIO1_OTC_STAT	R	0x00	GPIO1 Over Temperature Charge Status If GPIO1 OTC occurs, this bit is set to 1, otherwise 0.

Under Temperature Status (Address = A7H)

Bit	Field	Type	Reset	Description
7	GPIO4_UTD_STAT	R	0x00	GPIO4 Under Temperature Discharge Status If GPIO4 UTD occurs, this bit is set to 1, otherwise 0.
6	GPIO3_UTD_STAT	R	0x00	GPIO3 Under Temperature Discharge Status If GPIO3 UTD occurs, this bit is set to 1, otherwise 0.
5	GPIO2_UTD_STAT	R	0x00	GPIO2 Under Temperature Discharge Status If GPIO2 UTD occurs, this bit is set to 1, otherwise 0.
4	GPIO1_UTD_STAT	R	0x00	GPIO1 Under Temperature Discharge Status If GPIO1 UTD occurs, this bit is set to 1, otherwise 0.
3	GPIO4_UTC_STAT	R	0x00	GPIO4 Under Temperature Charge Status If GPIO4 UTC occurs, this bit is set to 1, otherwise 0.
2	GPIO3_UTC_STAT	R	0x00	GPIO3 Under Temperature Charge Status If GPIO3 UTC occurs, this bit is set to 1, otherwise 0.
1	GPIO2_UTC_STAT	R	0x00	GPIO2 Under Temperature Charge Status If GPIO2 UTC occurs, this bit is set to 1, otherwise 0.
0	GPIO1_UTC_STAT	R	0x00	GPIO1 Under Temperature Charge Status If GPIO1 UTC occurs, this bit is set to 1, otherwise 0.

Over Current and Current Wake Status (Address = A8H)

Bit	Field	Type	Reset	Description
7:5	reserved	R	0x00	reserved
4	DOC_STAT	R	0x00	Discharge over current Status

Bit	Field	Type	Reset	Description
				If discharge over current occurs, this bit is set to 1, otherwise 0.
3	SCD_STAT	R	0x00	Discharge short current Status If discharge short current occurs, this bit is set to 1, otherwise 0.
2	COC_STAT	R	0x00	Charge over current Status If charge over current occurs, this bit is set to 1, otherwise 0.
1	CWAKED_STAT	R	0x00	CWAKED Status If discharge current is higher than CWAKED threshold, this bit is set to 1, otherwise 0.
0	CWAKEC_STAT	R	0x00	CWAKEC Status If charge current is higher than CWAKEC threshold, this bit is set to 1, otherwise 0.

BAT Voltage Status (Address = A9H)

Bit	Field	Type	Reset	Description
7	MUX_ERR_STAT	R	0x00	MUX Error Status If channel mux has error, this bit is set to 1, otherwise 0.
6	EOC_STAT	R	0x00	EOC Status If EOC is detected, this bit is set to 1, otherwise 0.
5	OW_STAT	R	0x00	Open Wire Detection Status If open wire is detected, this bit is set to 1, otherwise 0.
4	BAT_OV_STAT	R	0x00	Bat Over Voltage Status If Bat OV occurs, this bit is set to 1, otherwise 0.
3	BAT_UV_STAT	R	0x00	Bat Under Voltage Status If bat UV occurs, this bit is set to 1, otherwise 0.
2	OV17_STAT	R	0x00	Cell 17 Over Voltage Status If cell 17 OV occurs, this bit is set to 1, otherwise 0.
1	UV17_STAT	R	0x00	Cell 17 Under Voltage Status If cell 17 UV occurs, this bit is set to 1, otherwise 0.
0	reserved	R	0x00	reserved

Load Detection Status (Address = AAH)

Bit	Field	Type	Reset	Description
7:3	reserved	R	0x00	reserved
2	LOAD_VLD	R	0x00	Load detect valid status

Bit	Field	Type	Reset	Description
				0: invalid 1: valid
1	LOAD_STAT	R	0x00	Load Detect Status If load insert is detected, this bit is set to 1, otherwise 0.
0	LOW_CURR_STAT	R	0x00	Load Current Detect Status If low current is detected, this bit is set to 1, otherwise 0.

Coulomb Counter bit 31-24 (Address = ABH)

Bit	Field	Type	Reset	Description
7:0	CC1	R	0x00	Coulomb Counter Bit 31-24

Coulomb Counter bit 23-16 (Address = ACH)

Bit	Field	Type	Reset	Description
7:0	CC2	R	0x00	Coulomb Counter Bit 23-16

Coulomb Counter bit 15-8 (Address = ADH)

Bit	Field	Type	Reset	Description
7:0	CC3	R	0x00	Coulomb Counter Bit 15-8

Coulomb Counter bit 7-0 (Address = AEH)

Bit	Field	Type	Reset	Description
7:0	CC4	R	0x00	Coulomb Counter Bit 7-0 1LSB=1.11*10^(-8)/Rsns, where, the unit of LSB is Ah, the unit of Rsns is mΩ.

Secondary Charge Over Temperature Threshold Configuration (Address = B2H)

Bit	Field	Type	Reset	Description
7:0	SOTC_TH_SEL_L	R/W	0x4B	Secondary Protection for charge over Temperature Threshold Low 8 bits of SOT_TH_SEL SOTC threshold is 198.4+SOTC_TH_SEL*6.4 (mV)

Secondary Charge Over Temperature Recovery Threshold Configuration (Address = B3H)

Bit	Field	Type	Reset	Description
7:0	SOTC_RCV_TH_SEL_L	R/W	0x89	Secondary Protection for charge over Temperature Recovery Threshold Low 8 bits of SOTC_RCV_TH_SEL SOTC recovery threshold is 198.4+SOTC_RCV_TH_SEL*6.4 (mV)

Secondary Discharge Over Temperature Threshold Configuration (Address = B4H)

Bit	Field	Type	Reset	Description
7:0	SOTD_TH_SEL_L	R/W	0x36	Secondary Protection for Discharge over Temperature Threshold Low 8 bits of SOTD_TH_SEL SOTD threshold is 198.4+SOTD_TH_SEL*6.4 (mV)

Secondary Discharge Over Temperature Recovery Threshold Configuration (Address = B5H)

Bit	Field	Type	Reset	Description
7:0	SOTD_RCV_TH_SEL_L	R/W	0x89	Secondary Protection for Discharge over Temperature Recovery Threshold Low 8 bits of SOTD_RCV_TH_SEL SOTD recovery threshold is 198.4+SOTD_RCV_TH_SEL*6.4 (mV)

Secondary Over Temperature Threshold Configuration (Address = B6H)

Bit	Field	Type	Reset	Description
7:4	reserved	R/W	0x00	reserved
3	SOTC_TH_SEL_H	R/W	0x00	Secondary Protection for charge over Temperature Threshold High 1 bit of SOT_TH_SEL SOTC threshold is 198.4+SOTC_TH_SEL*6.4 (mV)
2	SOTC_RCV_TH_SEL_H	R/W	0x00	Secondary Protection for charge over Temperature Recovery Threshold High 1 bit of SOTC_RCV_TH_SEL SOTC recovery threshold is 198.4+SOTC_RCV_TH_SEL*6.4 (mV)
1	SOTD_TH_SEL_H	R/W	0x00	Secondary Protection for Discharge over Temperature Threshold High 1 bit of SOTD_TH_SEL SOTD threshold is 198.4+SOTD_TH_SEL*6.4 (mV)

Bit	Field	Type	Reset	Description
0	SOTD_RCV_TH_SEL_H	R/W	0x00	Secondary Protection for Discharge over Temperature Recovery Threshold High 1 bit of SOTD_RCV_TH_SEL SOTD recovery threshold is 198.4+SOTD_RCV_TH_SEL*6.4 (mV)

Secondary Over Temperature Delay Time Configuration (Address = B7H)

Bit	Field	Type	Reset	Description
7:4	SOTD_DLY_CFG	R/W	0x00	Secondary Protection for Discharge over Temperature Delay Configuration SOTD delay time is 4+SOTD_DLY_CFG*8 (s)
3:0	SOTC_DLY_CFG	R/W	0x00	Secondary Protection for Charge over Temperature Delay Configuration SOTC delay time is 4+SOTC_DLY_CFG*8 (s)

Secondary Over Temperature Recovery Delay Time Configuration (Address = B8H)

Bit	Field	Type	Reset	Description
7:4	SOTD_RCV_DLY_CFG	R/W	0x00	Secondary Protection for Discharge over Temperature Delay Configuration SOTD delay time is 4+SOTD_RCV_DLY_CFG*8 (s)
3:0	SOTC_RCV_DLY_CFG	R/W	0x00	Secondary Protection for Charge over Temperature Delay Configuration SOTC delay time is 4+SOTC_RCV_DLY_CFG*8 (s)

Secondary Protection Status and Flag (Address = B9H)

Bit	Field	Type	Reset	Description
7	SOV_STAT	R	0x00	Secondary Over Voltage Detected Status If secondary over voltage is detected, this bit is set to 1, otherwise 0.
6	SOTC_STAT	R	0x00	Secondary Charge Over Temperature Detected Status If secondary charge over temperature is detected, this bit is set to 1, otherwise 0.
5	SOTD_STAT	R	0x00	Secondary Discharge Over Temperature Detected Status If secondary discharge over temperature is detected, this bit is set to 1, otherwise 0.
4	PFAIL_STAT	R	0x00	Secondary Detected Status

Bit	Field	Type	Reset	Description
				If secondary is detected, this bit is set to 1, otherwise 0.
3	SOV_FLG	R	0x00	Secondary Over Voltage Detected Flag If secondary over voltage is detected, this bit is set to 1, otherwise 0. This bit needs host to clear it.
2	SOTC_FLG	R	0x00	Secondary Charge Over Temperature Detected Flag If secondary charge over temperature is detected, this bit is set to 1, otherwise 0. This bit needs host to clear it.
1	SOTD_FLG	R	0x00	Secondary Discharge Over Temperature Detected Flag If secondary discharge over temperature is detected, this bit is set to 1, otherwise 0. This bit needs host to clear it.
0	PFAIL_FLG	R	0x00	Secondary Detected Flag If secondary is detected, this bit is set to 1, otherwise 0. This bit needs host to clear it.

Cell1 Voltage ADC Measurement Result (Address = C0H)

Bit	Field	Type	Reset	Description
7:0	C1_H	R	0x00	Cell1 Voltage ADC Measurement Result High 8 bits Cell1 voltage measurement result is (C1_H*256+C1_L)*100μV

Cell1 Voltage ADC Measurement Result (Address = C1H)

Bit	Field	Type	Reset	Description
7:0	C1_L	R	0x00	Cell1 Voltage ADC Measurement Result Low 8 bits

Cell2 Voltage ADC Measurement Result (Address = C2H)

Bit	Field	Type	Reset	Description
7:0	C2_H	R	0x00	Cell2 Voltage ADC Measurement Result High 8 bits Cell2 voltage measurement result is (C2_H*256+C2_L)*100μV

Cell2 Voltage ADC Measurement Result (Address = C3H)

Bit	Field	Type	Reset	Description
7:0	C2_L	R	0x00	Cell2 Voltage ADC Measurement Result Low 8 bits

Cell3 Voltage ADC Measurement Result (Address = C4H)

Bit	Field	Type	Reset	Description
7:0	C3_H	R	0x00	Cell3 Voltage ADC Measurement Result High 8 bits Cell3 voltage measurement result is (C3_H*256+C3_L)*100μV

Cell3 Voltage ADC Measurement Result (Address = C5H)

Bit	Field	Type	Reset	Description
7:0	C3_L	R	0x00	Cell3 Voltage ADC Measurement Result Low 8 bits

Cell4 Voltage ADC Measurement Result (Address = C6H)

Bit	Field	Type	Reset	Description
7:0	C4_H	R	0x00	Cell4 Voltage ADC Measurement Result High 8 bits Cell4 voltage measurement result is (C4_H*256+C4_L)*100μV

Cell4 Voltage ADC Measurement Result (Address = C7H)

Bit	Field	Type	Reset	Description
7:0	C4_L	R	0x00	Cell4 Voltage ADC Measurement Result Low 8 bits

Cell5 Voltage ADC Measurement Result (Address = C8H)

Bit	Field	Type	Reset	Description
7:0	C5_H	R	0x00	Cell5 Voltage ADC Measurement Result High 8 bits Cell5 voltage measurement result is (C5_H*256+C5_L)*100μV

Cell5 Voltage ADC Measurement Result (Address = C9H)

Bit	Field	Type	Reset	Description
7:0	C5_L	R	0x00	Cell5 Voltage ADC Measurement Result Low 8 bits

Cell6 Voltage ADC Measurement Result (Address = CAH)

Bit	Field	Type	Reset	Description
7:0	C6_H	R	0x00	Cell6 Voltage ADC Measurement Result High 8 bits Cell6 voltage measurement result is (C6_H*256+C6_L)*100μV

Cell6 Voltage ADC Measurement Result (Address = CBH)

Bit	Field	Type	Reset	Description
7:0	C6_L	R	0x00	Cell6 Voltage ADC Measurement Result Low 8 bits

Cell7 Voltage ADC Measurement Result (Address = CCH)

Bit	Field	Type	Reset	Description
7:0	C7_H	R	0x00	Cell7 Voltage ADC Measurement Result High 8 bits Cell7 voltage measurement result is (C7_H*256+C7_L)*100μV

Cell7 Voltage ADC Measurement Result (Address = CDH)

Bit	Field	Type	Reset	Description
7:0	C7_L	R	0x00	Cell7 Voltage ADC Measurement Result Low 8 bits

Cell8 Voltage ADC Measurement Result (Address = CEH)

Bit	Field	Type	Reset	Description
7:0	C8_H	R	0x00	Cell8 Voltage ADC Measurement Result High 8 bits

Bit	Field	Type	Reset	Description
				Cell8 voltage measurement result is (C8_H*256+C8_L)*100μV

Cell8 Voltage ADC Measurement Result (Address = CFH)

Bit	Field	Type	Reset	Description
7:0	C8_L	R	0x00	Cell8 Voltage ADC Measurement Result Low 8 bits

Cell9 Voltage ADC Measurement Result (Address = D0H)

Bit	Field	Type	Reset	Description
7:0	C9_H	R	0x00	Cell9 Voltage ADC Measurement Result High 8 bits Cell9 voltage measurement result is (C9_H*256+C9_L)*100μV

Cell9 Voltage ADC Measurement Result (Address = D1H)

Bit	Field	Type	Reset	Description
7:0	C9_L	R	0x00	Cell9 Voltage ADC Measurement Result Low 8 bits

Cell10 Voltage ADC Measurement Result (Address = D2H)

Bit	Field	Type	Reset	Description
7:0	C10_H	R	0x00	Cell10 Voltage ADC Measurement Result High 8 bits Cell10 voltage measurement result is (C10_H*256+C10_L)*100μV

Cell10 Voltage ADC Measurement Result (Address = D3H)

Bit	Field	Type	Reset	Description
7:0	C10_L	R	0x00	Cell10 Voltage ADC Measurement Result Low 8 bits

Cell11 Voltage ADC Measurement Result (Address = D4H)

Bit	Field	Type	Reset	Description
7:0	C11_H	R	0x00	Cell11 Voltage ADC Measurement Result High 8 bits Cell11 voltage measurement result is (C11_H*256+C11_L)*100μV

Cell11 Voltage ADC Measurement Result (Address = D5H)

Bit	Field	Type	Reset	Description
7:0	C11_L	R	0x00	Cell11 Voltage ADC Measurement Result Low 8 bits

Cell12 Voltage ADC Measurement Result (Address = D6H)

Bit	Field	Type	Reset	Description
7:0	C12_H	R	0x00	Cell12 Voltage ADC Measurement Result High 8 bits Cell12 voltage measurement result is (C12_H*256+C12_L)*100μV

Cell12 Voltage ADC Measurement Result (Address = D7H)

Bit	Field	Type	Reset	Description
7:0	C12_L	R	0x00	Cell12 Voltage ADC Measurement Result Low 8 bits

Cell13 Voltage ADC Measurement Result (Address = D8H)

Bit	Field	Type	Reset	Description
7:0	C13_H	R	0x00	Cell13 Voltage ADC Measurement Result High 8 bits Cell13 voltage measurement result is (C13_H*256+C13_L)*100μV

Cell13 Voltage ADC Measurement Result (Address = D9H)

Bit	Field	Type	Reset	Description
7:0	C13_L	R	0x00	Cell13 Voltage ADC Measurement Result Low 8 bits

Cell14 Voltage ADC Measurement Result (Address = DAH)

Bit	Field	Type	Reset	Description
7:0	C14_H	R	0x00	Cell14 Voltage ADC Measurement Result High 8 bits Cell14 voltage measurement result is (C14_H*256+C14_L)*100μV

Cell14 Voltage ADC Measurement Result (Address = DBH)

Bit	Field	Type	Reset	Description
7:0	C14_L	R	0x00	Cell14 Voltage ADC Measurement Result Low 8 bits

Cell15 Voltage ADC Measurement Result (Address = DCH)

Bit	Field	Type	Reset	Description
7:0	C15_H	R	0x00	Cell15 Voltage ADC Measurement Result High 8 bits Cell15 voltage measurement result is (C15_H*256+C15_L)*100μV

Cell15 Voltage ADC Measurement Result (Address = DDH)

Bit	Field	Type	Reset	Description
7:0	C15_L	R	0x00	Cell15 Voltage ADC Measurement Result Low 8 bits

Cell16 Voltage ADC Measurement Result (Address = DEH)

Bit	Field	Type	Reset	Description
7:0	C16_H	R	0x00	Cell16 Voltage ADC Measurement Result High 8 bits Cell16 voltage measurement result is (C16_H*256+C16_L)*100μV

Cell16 Voltage ADC Measurement Result (Address = DFH)

Bit	Field	Type	Reset	Description
7:0	C16_L	R	0x00	Cell16 Voltage ADC Measurement Result Low 8 bits

Cell17 Voltage ADC Measurement Result (Address = E0H)

Bit	Field	Type	Reset	Description
7:0	C17_H	R	0x00	Cell17 Voltage ADC Measurement Result High 8 bits Cell17 voltage measurement result is (C17_H*256+C17_L)*100μV

Cell17 Voltage ADC Measurement Result (Address = E1H)

Bit	Field	Type	Reset	Description
7:0	C17_L	R	0x00	Cell17 Voltage ADC Measurement Result Low 8 bits

GPIO1 Voltage ADC Measurement Result (Address = E2H)

Bit	Field	Type	Reset	Description
7:0	G1_H	R	0x00	GPIO1 Voltage ADC Measurement Result High 8 bits GPIO1 voltage measurement result is (G1_H*256+G1_L)*100μV

GPIO1 Voltage ADC Measurement Result (Address = E3H)

Bit	Field	Type	Reset	Description
7:0	G1_L	R	0x00	GPIO1 Voltage ADC Measurement Result Low 8 bits

GPIO2 Voltage ADC Measurement Result (Address = E4H)

Bit	Field	Type	Reset	Description
7:0	G2_H	R	0x00	GPIO2 Voltage ADC Measurement Result High 8 bits GPIO2 voltage measurement result is (G2_H*256+G2_L)*100μV

GPIO2 Voltage ADC Measurement Result (Address = E5H)

Bit	Field	Type	Reset	Description
7:0	G2_L	R	0x00	GPIO2 Voltage ADC Measurement Result Low 8 bits

GPIO3 Voltage ADC Measurement Result (Address = E6H)

Bit	Field	Type	Reset	Description
7:0	G3_H	R	0x00	GPIO3 Voltage ADC Measurement Result High 8 bits GPIO3 voltage measurement result is (G3_H*256+G3_L)*100μV

GPIO3 Voltage ADC Measurement Result (Address = E7H)

Bit	Field	Type	Reset	Description
7:0	G3_L	R	0x00	GPIO3 Voltage ADC Measurement Result Low 8 bits

GPIO4 Voltage ADC Measurement Result (Address = E8H)

Bit	Field	Type	Reset	Description
7:0	G4_H	R	0x00	GPIO4 Voltage ADC Measurement Result High 8 bits GPIO4 voltage measurement result is (G4_H*256+G4_L)*100μV

GPIO4 Voltage ADC Measurement Result (Address = E9H)

Bit	Field	Type	Reset	Description
7:0	G4_L	R	0x00	GPIO4 Voltage ADC Measurement Result Low 8 bits

BAT Voltage ADC Measurement Result (Address = ECH)

Bit	Field	Type	Reset	Description
7:0	BAT_H	R	0x00	BAT Voltage ADC Measurement Result High 8 bits BAT voltage measurement result is (BAT_H*256+BAT_L)*3.2mV

BAT Voltage ADC Measurement Result (Address = EDH)

Bit	Field	Type	Reset	Description
7:0	BAT_L	R	0x00	BAT Voltage ADC Measurement Result Low 8 bits

VAO Voltage ADC Measurement Result (Address = EEH)

Bit	Field	Type	Reset	Description
7:0	VAO_H	R	0x00	VAO Voltage ADC Measurement Result High 8 bits VAO voltage measurement result is (VAO_H*256+VAO_L)*100μV

VAO Voltage ADC Measurement Result (Address = EFH)

Bit	Field	Type	Reset	Description
7:0	VAO_L	R	0x00	VAO Voltage ADC Measurement Result Low 8 bits

VBG Voltage ADC Measurement Result (Address = F0H)

Bit	Field	Type	Reset	Description
7:0	VBG_H	R	0x00	VBG Voltage ADC Measurement Result High 8 bits VBG voltage measurement result is (VBG_H*256+VBG_L)*100μV

VBG Voltage ADC Measurement Result (Address = F1H)

Bit	Field	Type	Reset	Description
7:0	VBG_L	R	0x00	VBG Voltage ADC Measurement Result Low 8 bits

VDRIVE Voltage ADC Measurement Result (Address = F2H)

Bit	Field	Type	Reset	Description
7:0	VDRIVE_H	R	0x00	VDRIVE Voltage ADC Measurement Result High 8 bits

Bit	Field	Type	Reset	Description
				VDRIVE voltage measurement result is (VDRIVE_H*256+VDRIVE_L)*100μV

VDRIVE Voltage ADC Measurement Result (Address = F3H)

Bit	Field	Type	Reset	Description
7:0	VDRIVE_L	R	0x00	VDRIVE Voltage ADC Measurement Result Low 8 bits

C0 Voltage ADC Measurement Result (Address = F4H)

Bit	Field	Type	Reset	Description
7:0	C0_H	R	0x00	C0 Voltage ADC Measurement Result High 8 bits C0 voltage measurement result is (C0_H*256+C1_L)*100μV

C0 Voltage ADC Measurement Result (Address = F5H)

Bit	Field	Type	Reset	Description
7:0	C0_L	R	0x00	C0 Voltage ADC Measurement Result Low 8 bits

LOAD Voltage ADC Measurement Result (Address = F6H)

Bit	Field	Type	Reset	Description
7:0	VLOAD_H	R	0x00	VLOAD Voltage ADC Measurement Result High 8 bits LOAD voltage measurement result is (VLOAD_H*256+VLOAD_L)*100μV

LOAD Voltage ADC Measurement Result (Address = F7H)

Bit	Field	Type	Reset	Description
7:0	VLOAD_L	R	0x00	VLOAD Voltage ADC Measurement Result Low 8 bits

VREG Voltage ADC Measurement Result (Address = F8H)

Bit	Field	Type	Reset	Description
7:0	VREG_H	R	0x00	VREG Voltage ADC Measurement Result High 8 bits VREG voltage measurement result is (VREG_H*256+VREG_L)*100μV

VREG Voltage ADC Measurement Result (Address = F9H)

Bit	Field	Type	Reset	Description
7:0	VREG_L	R	0x00	VREG Voltage ADC Measurement Result Low 8 bits

VREGD Voltage ADC Measurement Result (Address = FAH)

Bit	Field	Type	Reset	Description
7:0	VREGD_H	R	0x00	VREGD Voltage ADC Measurement Result High 8 bits VREGD voltage measurement result is (VREGD_H*256+VREGD_L)*100μV

VREGD Voltage ADC Measurement Result (Address = FBH)

Bit	Field	Type	Reset	Description
7:0	VREGD_L	R	0x00	VREGD Voltage ADC Measurement Result Low 8 bits

VTSREF Voltage ADC Measurement Result (Address = FCH)

Bit	Field	Type	Reset	Description
7:0	VTSREF_H	R	0x00	VTSREF Voltage ADC Measurement Result High 8 bits VTSREF voltage measurement result is (VTSREF_H*256+VTSREF_L)*100μV

VTSREF Voltage ADC Measurement Result (Address = FDH)

Bit	Field	Type	Reset	Description
7:0	VTSREF_L	R	0x00	VTSREF Voltage ADC Measurement Result Low 8 bits

Current ADC Measurement Result (Address = FEH)

Bit	Field	Type	Reset	Description
7:0	CADC_H	R	0x00	Current ADC Measurement Result High 8 bits If CADC_H[7]=0, Current ADC result is (CADC_H*256+CADC_L)*4μV If CADC_H[7]=1, Current ADC result is -(65536-CADC_H*256-CADC_L)*4μV

Current ADC Measurement Result (Address = FFH)

Bit	Field	Type	Reset	Description
7:0	CADC_L	R	0x00	Current ADC Measurement Result Low 8 bits

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPB76016 supports 12-V to 75-V battery voltage range, so can be used with up to 17 series battery packs. The digital control and status data are available through SPI, customers can use the TPB76016 GUI with SPI interface to access TPB76016 for specific applications, such as reading monitor ADC results, setting cels numbers, protection threshold, delay time, etc.

Typical Application

Figure 13 shows the typical application schematic of the TPB76016, using the TPB76016 together with a host microcontroller. This configuration uses CHG and DSG FETs in series, together with the Pre FETs used to implement precharge and predischarge functions. Several points to consider in an implementation are included below:

- A series diode is recommended at the BAT pin with an RC filter at this pin to AGND. These components allow the device to continue to operate for a short time when a pack short circuit occurs. In this case, the diode prevents the BAT pin from being pulled low with the stack, and the device continues to operate until the device detects the short circuit events and disables the DSGFET. A Schottky diode is recommended if low-voltage pack operation is needed, otherwise, a general diode can be used.
- A diode is recommended at the Collector of external NPN. This diode prevents reverse current flowing from DRIVE to a collector in the event of a pack short circuit event. A Schottky diode is recommended if low-voltage pack operation is needed, otherwise, a general diode can be used.
- It is recommended to put an additional Schottky diode at the C0 pin to AGND and C1 pin to AGND, a resistor, for example, 51 Ω, can be put between AGND and the lowest battery cathode. These components prevent C0 and C1 pins from being pulled below ground too much in pack short-circuit events.
- It is recommended to insert resistors in series with the SRP pin and SRN pin, and a 100 nF to AGND with a 1 μF differential capacitor between the SRP pin and SRN pin for noise filtering. These components should be put on the same side of the PCB, and the routing of these components should be minimized and fully symmetric.

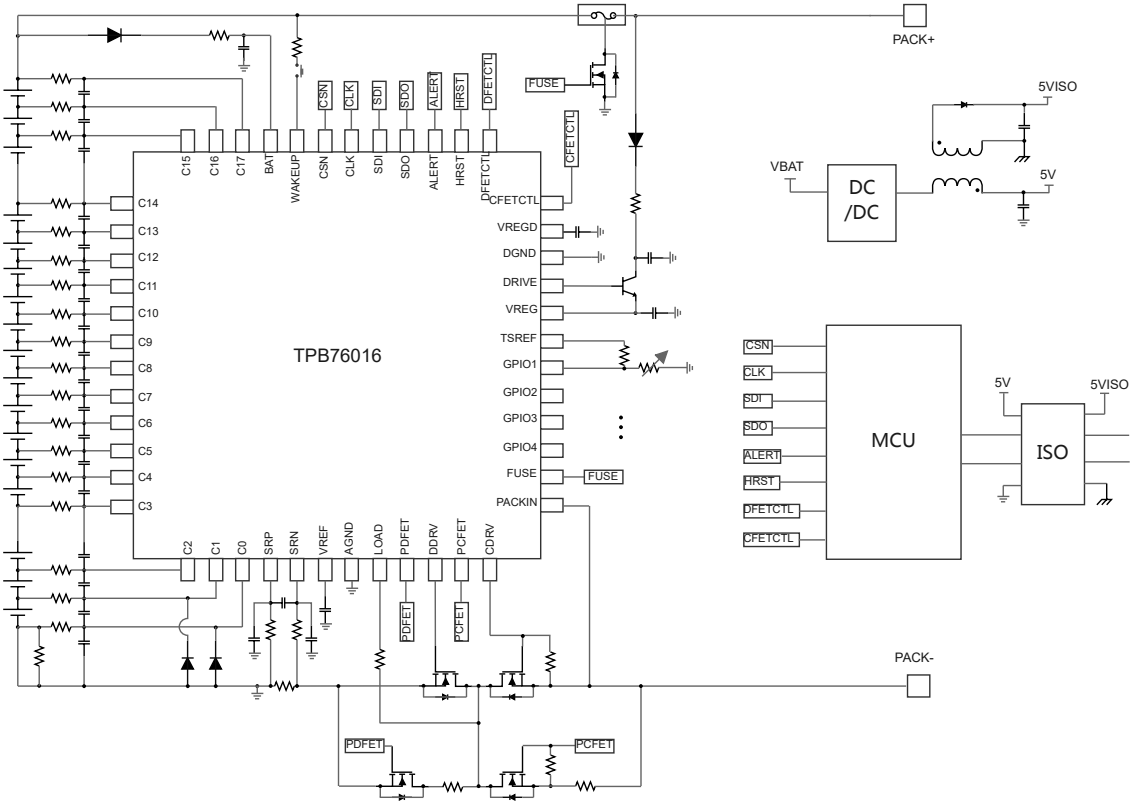


Figure 13. TPB76016 Typical Application Circuit

Reduced Cell Count Applications

The TPB76016 may be used in applications with less than 17 cells in series, it is necessary to short unused input together, and C17 is recommended to connect the positive pin of the highest cell, through the appropriate discrete component network. Figure 14 shows an example of application with less than 17 cells in series.

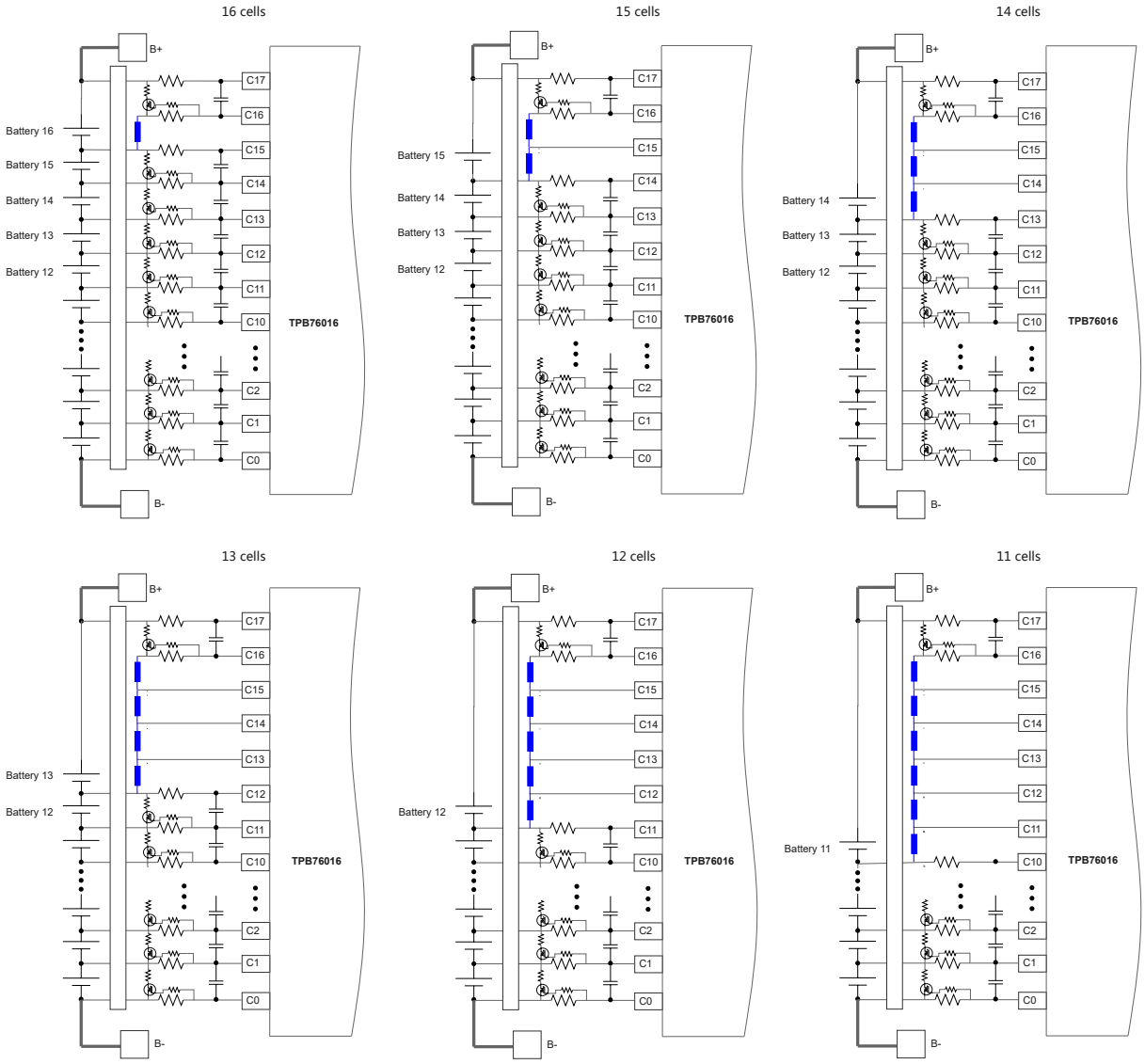


Figure 14. Reduced Cell Pins Connection

Unused Pins

Some device pins may not be used in the application. The unused pins connection is described below.

Table 12. Unused Pins Connection

Pin	Name	Recommendation
1-15, 46-48	C0-C17	Cell input 1, 2 and 17 are recommended to be connected to actual cells, with cell connected between C1 and C0, C2 and C1, and C17 and C16, C0 should be connected to AGND through a resistor and capacitor. Refer to **Reduced Cell Count Application** for other unused cell input pins.
16, 17	SRP, SRN	If not used, these pins should be connected together, and connected to AGND.
20	LOAD	If not used, this pin can be left floating.

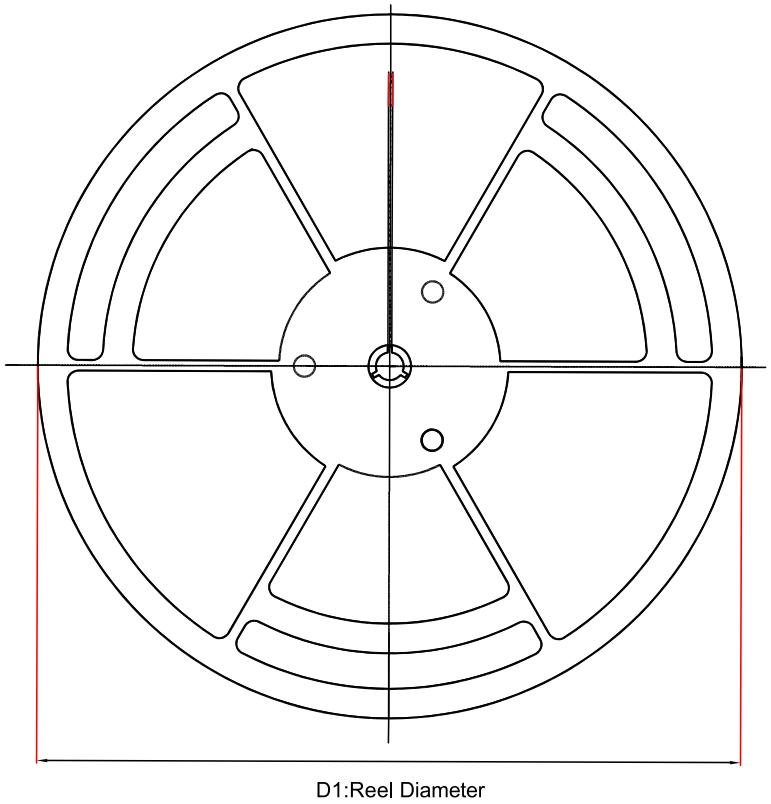
21, 22, 23, 24	PDFET, DDRV, PCFET, CDRV	If not used, these pins can be left floating.
25	PACKIN	If not used, this pin can be left floating.
26	FUSE	If not used, this pin is recommended to be connected to AGND.
27, 28, 29, 30	GPIO4, GPIO3, GPIO2, GPIO1	If not used, these pins can be left floating.
36, 37	CFETCTL, DFETCTL	If not used, this pin is recommended to be pulled to VREG if the FET_CTL_INV bit is 0, or be connected to AGND if the FET_CTL_INV bit is 1.
38	HRST	If not used, this pin is recommended to be connected to AGND.
39	ALERT	If not used, this pin is recommended to be connected to AGND.

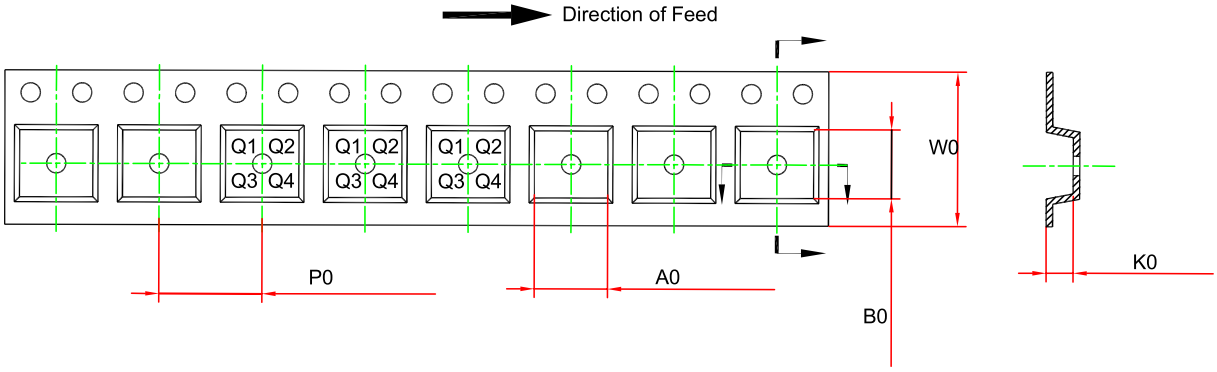
Layout

Layout Guideline

- Both input capacitors and output capacitors must be placed to the device pins as close as possible.
- The TPB76016 VREG requires an external decoupling capacitor, which should be placed as close to the VREG pin as possible, with minimized trace inductance, and connected to a ground plane.
- It is recommended to use wide and thick trace to minimize I×R drop and heat dissipation.
- For best current measurement performance, it is recommended to use kelvin connection at the sense resistor. 10 Ω resistors should be placed from the sense resistor terminals to the SRP and SRN pins, with a 1 μF filter capacitor placed across the SRP and SRN pins. All filter components should be placed as close as possible to the device, and the traces from the sense resistor routed in parallel to the filter circuit. A ground plane is recommended around the filter components for noise immunity.

Tape and Reel Information



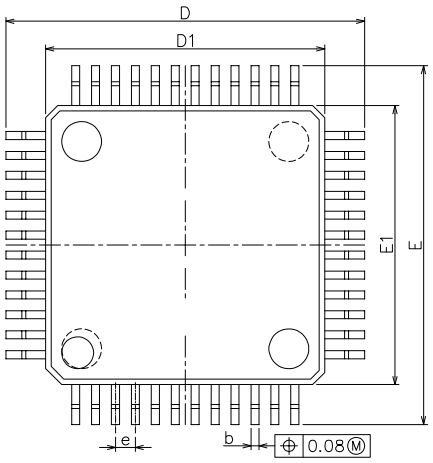


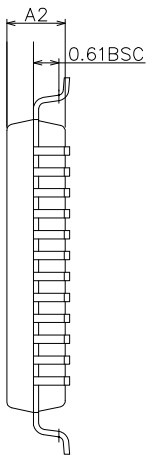
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPB76016-QP3R	LQFP-48	330	21.6	9.6	9.6	2	12	16	Q1

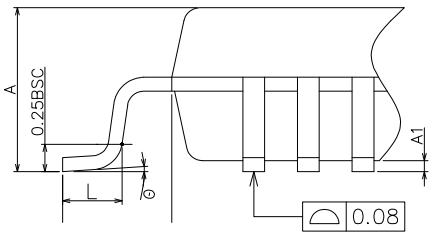
Package Outline Dimensions

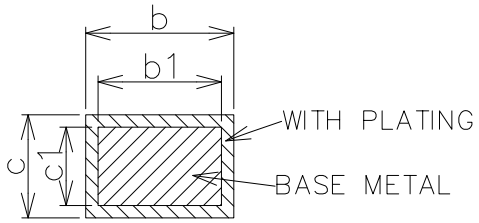
LQFP7x7-48

Package Outline Dimensions QP3(LQFP7X7-48-A)









NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.400	1.600	0.055	0.063
A1	0.050	0.150	0.002	0.006
A2	1.350	1.450	0.053	0.057
b	0.170	0.230	0.007	0.009
c	0.130	0.180	0.005	0.007
D	8.800	9.200	0.346	0.362
D1	6.900	7.100	0.272	0.280
E	8.800	9.200	0.346	0.362
E1	6.900	7.100	0.272	0.280
e	0.500 BSC		0.020 BSC	
L	0.450	0.750	0.018	0.030
θ	0	7°	0	7°

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPB76016-QP3R	−40 to 125°C	LQFP-48	76016	3	Tape and Reel, 2000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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