16-Bit, 16-Channel, Dual Simultaneous Sampling Bipolar Input ADC

Features

- 16-Bit, 16-Channel ADC with Integrated Analog Front-End
- Dual Simultaneous Sampling with 2x1 MSPS throughput Rate
- Independently Programmable Channel Input Ranges
  - True Bipolar: ±10 V, ±5 V, ±2.5 V
- Power Supply
  - Single Analog Supply 5 V
  - V_{DRIVE} Supply 1.71 V to V_{CC}
- Highly Integrated Analog Front-End
  - 1-MΩ Analog Input Impedance
  - Programmable Gain Amplifier
  - Analog Low-Pass Filter
  - Internal Accurate Reference and Reference Buffer
  - Dual 16-Bit 1 MPS SAR ADC
  - ±30 V Analog Input Overvoltage Clamp Protection with 7-kV ESD
- Flexible Digital and Interface
  - On-Chip Oversampling with Digital Filter
  - Sequencer with Burst Mode
  - Parallel and Serial Interface Compatible with SPI
  - Optional Cyclic Redundancy Check (CRC) Error Checking
  - Self-Diagnostic Function
  - Hardware/software Configuration
- Performance
  - SNR: 89 dB at 1 MSPS Typical
  - SINAD: 88.7 dB Typical
  - THD: −102 dB Typical
- Package: LQFP 80-pin 14 mm x 14 mm
- Wide Operating Temperature Range: −40°C to +125°C

Applications

- Relay Protection
- Power Line Monitoring
- Motor Control
- Multi-channel Data Acquisition

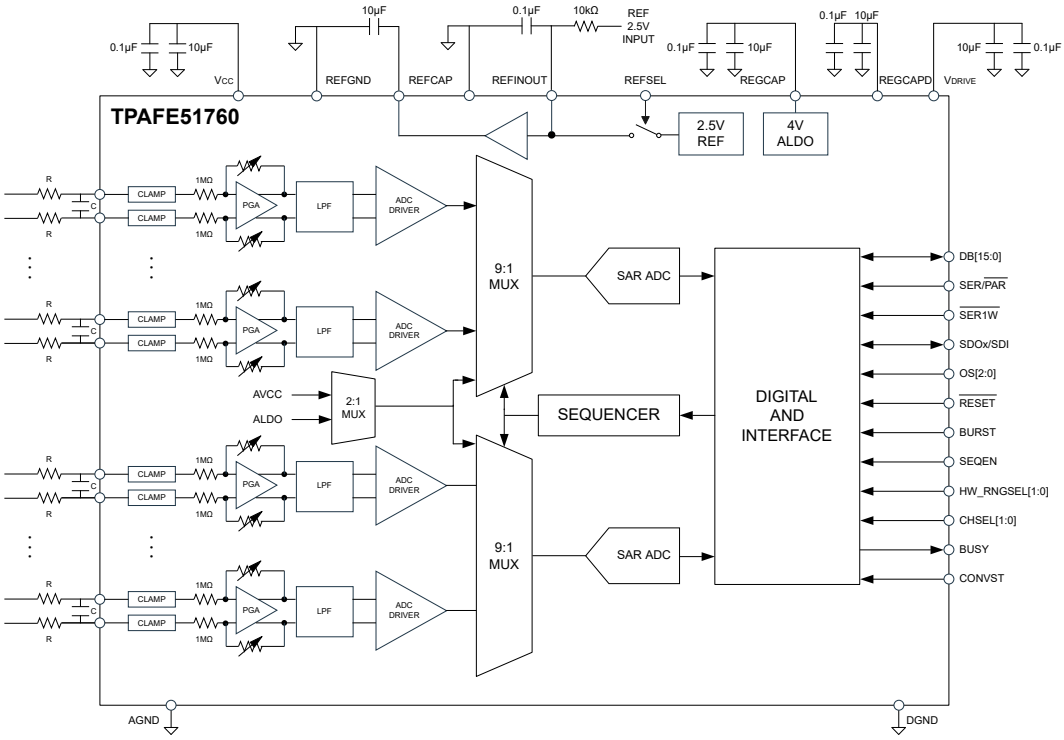
Description

The TPAFE51760 is a 16-channel, 16-bit, dual simultaneous 2 x 1 MSPS sampling system based on successive approximation register (SAR) analog-to-digital converter (ADC). The TPAFE51760 is highly integrated with an analog front-end for each channel, including an input overvoltage clamp, 1 MΩ input impedance, programmable gain amplifier (PGA), active low-pass filter, and ADC driver. Internal precision and low-drift reference with buffer make the device feasible for compact data acquisition solutions. The digital interface supports communication with various host controllers with SPI-compatible serial and parallel interfaces.

The TPAFE51760 can process true bipolar ± 10 V, ±5 V, and ±2.5 V input signals, with a single 5 V analog power supply. The 1 MΩ high input impedance simplified analog input design and the device can be connected directly with sensors. The analog input overvoltage could protect the device up to ±30 V. The device offers a flexible sequencer that allows it to be configured and burst mode is also supported. On-chip oversampling digital filters can be used to improve SNR and reduce throughput rates. Integrated chip self-detect function and optional CRC make the device robust in the application.

The TPAFE51760 is available in the LQFP14x14-80 package and operates from −40°C to +125°C.

Typical Application Circuit



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Product Family Table

Order Number	Channels	Resolution	Throughput	Package
TPAFE51760-QL6T	16	16 Bits	2 x 1 MSPS	LQFP14X14-80

Revision History

Date	Revision	Notes
2024-06-26	Rev.A.0	Initial released version

Pin Configuration and Functions

TPAFE51760
LQFP14X14-80 Package
Top View

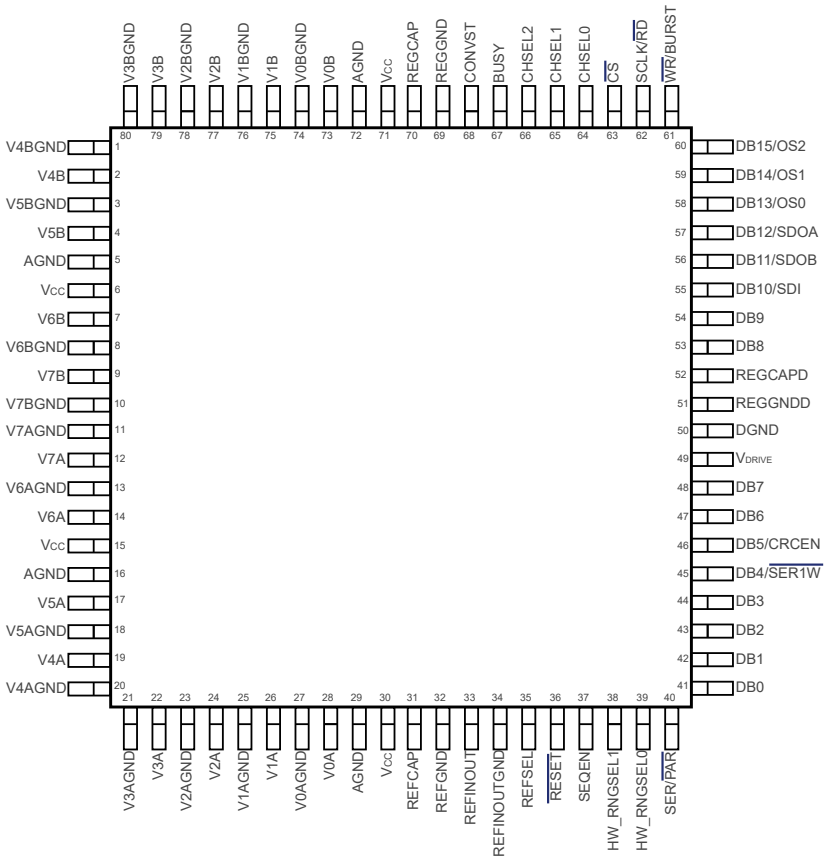


Table 1. Pin Functions: TPAFE51760

Pin		Type(1)	Description
No.	Name		
1	V4BGND	AIGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V4B.
2	V4B	AI	Analog Input for Channel 4, ADC B.
3	V5BGND	AIGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V5B.
4	V5B	AI	Analog Input for Channel 5, ADC B.
5, 16, 29,72	AGND	P	Analog Supply Ground Pins.
6, 15, 30, 71	V_{CC}	P	Analog Supply Voltage, 4.7 V to 5.25 V. Decouple these pins to AGND using capacitors.
7	V6B	AI	Analog Input for Channel 6, ADC B.
8	V6BGND	AIGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V6B.
9	V7B	AI	Analog Input for Channel 7, ADC B.

Pin		Type(1)	Description
No.	Name		
10	V7BGND	AIGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V7B.
11	V7AGND	AIGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V7A.
12	V7A	AI	Analog Input for Channel 7, ADC A.
13	V6AGND	AIGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V6A.
14	V6A	AI	Analog Input for Channel 6, ADC A.
17	V5A	AI	Analog Input for Channel 5, ADC A.
18	V5AGND	AIGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V5A.
19	V4A	AI	Analog Input for Channel 4, ADC A.
20	V4AGND	AIGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V4A.
21	V3AGND	AIGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V3A.
22	V3A	AI	Analog Input for Channel 3, ADC A.
23	V2AGND	AIGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V2A.
24	V2A	AI	Analog Input for Channel 2, ADC A.
25	V1AGND	AIGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V1A.
26	V1A	AI	Analog Input for Channel 1, ADC A.
27	V0AGND	AIGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V0A.
28	V0A	AI	Analog Input for Channel 0, ADC A.
31	REFCAP	CAP	Reference Buffer Output Force/Sense Pin. Decouple this pin to AGND using a low effective series resistance capacitor, as close to the REFCAP pin as possible. The voltage on this pin is typically 4.096 V.
32	REFGND	CAP	Reference Ground pin. Connect this pin to AGND.
33	REFINOUT	REF	Reference Input/Reference Output. The on-chip reference of 2.5 V is available on this pin for external use when the REFSEL pin is set to logic high. Alternatively, the internal reference can be disabled by setting the REFSEL pin to logic low, and an external reference of 2.5 V can be applied to this input. Decoupling is required on this pin for both the internal and external reference options. Connect a 100 nF capacitor between the REFINOUT and REFINOUTGND pins, as close to the REFINOUT pin as possible. If using an external reference, connect a 10 kΩ series resistor to this pin to band limit the reference signal.
34	REFINOUTGND	CAP	Reference Input, Reference Output Ground Pin. Connect this pin to AGND.
35	REFSEL	DI	Internal/External Reference Selection Input. REFSEL is a logic input. If this pin is set to logic high, the internal reference is selected and enabled. If this pin is set to logic low, the internal reference is disabled and an external reference voltage must be applied to the REFINOUT pin. The signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure.
36	$\overline{\text{RESET}}$	DI	Reset Input. Full and partial reset options are available. The type of reset is determined by the length of the $\overline{\text{RESET}}$ pulse. Keeping $\overline{\text{RESET}}$ low places the device into shutdown mode.

Pin		Type(1)	Description
No.	Name		
37	SEQEN	DI	Channel Sequencer Enable Input (Hardware Mode Only). When SEQEN is tied low, the sequencer is disabled.When SEQEN is high, the sequencer is enabled (with restricted functionality in hardware mode). See the Sequencer section for further details. The signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure. In software mode, this pin must be connected to DGND.
38, 39	HW_RNGSEL1, HW_RNGSEL0	DI	Hardware/Software Mode Selection, Hardware Mode Range Select Inputs. Hardware/software mode selection is latched at full reset. Range selection in hardware mode is not latched. HW_RNGSELx = 00: software mode; the device is configured via the software registers. W_RNGSELx = 01: hardware mode; analog input range is ±2.5 V. HHW_RNGSELx = 10: hardware mode; analog input range is ±5 V. HW_RNGSELx = 11: hardware mode; analog input range is ±10 V.
40	SER/$\overline{\text{PAR}}$	DI	Serial/Parallel Interface Selection Input. Logic input. If this pin is tied to a logic low, the parallel interface is selected. If this pin is tied to logic high, the serial interface is selected. The signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure.
41, 42, 43, 44	DB0, DB1, DB2, DB3	DO/DI	Parallel Output/Input Data Bit 0 to Data Bit 3. In parallel mode, these pins are output/input parallel data bits, DB7 to DB0. In serial mode, these pins must be tied to DGND.
45	DB4/$\overline{\text{SER1W}}$	DO/DI	Parallel Output/Input Data Bit 4/Serial Output Selection. In parallel mode, this pin acts as a three-state parallel digital output/input pin. In serial mode, this pin determines whether the serial output operates over SDOA and SDOB or just SDOA. When $\overline{\text{SER1W}}$ is low, the serial output operates over SDOA only. When $\overline{\text{SER1W}}$ is high, the serial output operates over both SDOA and SDOB. The signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure.
46	DB5/CRCEN	DO/DI	Parallel Output/Input Data Bit 5/CRC Enable Input. In parallel mode, this pin acts as a three-state parallel digital input/output. While in serial mode, this pin acts as a CRC-enabled input. The CRCEN signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure. In serial mode, when CRCEN is low, there is no CRC word following the conversion results; when CRCEN is high, an extra CRC word follows the last conversion word configured by CHSELx. In software mode, this pin must be connected to DGND.
47, 48	DB6, DB7	DO/DI	Parallel Output/Input Data Bit 6 and Data Bit 7. When SER/$\overline{\text{PAR}}$ = 0, these pins act as three-state parallel digital inputs/outputs. In serial mode, when SER/$\overline{\text{PAR}}$ = 1 these pins must be tied to DGND.
49	V_{DRIVE}	P	Logic Power Supply Input. The voltage (1.7 V to 5.25 V) supplied at this pin determines the operating voltage of the interface. This pin is nominally at the same supply as the supply of the host interface. Decouple this pin with capacitors.

Pin		Type(1)	Description
No.	Name		
50	DGND	P	Digital Ground. This pin is the ground reference point for all digital circuitry on the device. The DGND pin must connect to the DGND plane of a system.
51	REGGNDD	CAP	Ground for the Low Dropout (LDO) Regulator Connected to REGCAPD (Pin 52).
52	REGCAPD	CAP	Decoupling Capacitor Pin for Voltage Output from Internal Regulator. Decouple this output pin separately to REGGNDD using capacitors. The voltage at this pin is 4 V typical.
53, 54	DB8, DB9	DO/DI	Parallel Output/Input Data Bit 8 and Data Bit 9. When SER/$\overline{\text{PAR}}$ = 0, these pins act as three-state parallel digital input/outputs. In serial mode, when SER/$\overline{\text{PAR}}$ = 1 these pins must be tied to DGND.
55	DB10/SDI	DO/DI	Parallel Output/Input Data Bit DB10/Serial Data Input. When SER/$\overline{\text{PAR}}$ = 0, these pins act as three-state parallel digital input/outputs. In hardware serial mode, tie this pin to DGND. In serial mode, when SER/$\overline{\text{PAR}}$ = 1, this pin acts as the data input of the SPI interface.
56	DB11/SDOB	DO/DI	Parallel Output/Input Data Bit DB11/Serial Data Input. When SER/$\overline{\text{PAR}}$ = 0, these pins act as three-state parallel digital input/outputs. In serial mode, when SER/$\overline{\text{PAR}}$ = 1, this pin functions as SDOB and outputs serial conversion data.
57	DB12/SDOA	DO/DI	Parallel Output/Input Data Bit DB12/Serial Data Input. When SER/$\overline{\text{PAR}}$ = 0, these pins act as three-state parallel digital input/outputs. In serial mode, when SER/$\overline{\text{PAR}}$ = 1, this pin functions as SDOA and outputs serial conversion data.
58, 59, 60	DB13/OS0, DB14/OS1, DB15/OS2	DO/DI	Parallel Output/Input Data Bit 13, Data Bit 14, and Data Bit 15/Oversampling Ratio Selection. When SER/$\overline{\text{PAR}}$ = 0, these pins act as three-state parallel digital input/outputs. In serial hardware mode, these pins control the oversampling settings. The signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure. See the Digital Filter section for further details. In software serial mode, these pins must be connected to DGND.
61	$\overline{\text{WR}}$ /BURST	DI	Write/Burst Mode Enable In software parallel mode, this pin acts as $\overline{\text{WR}}$ for a parallel interface. In hardware parallel or serial mode, this pin enables BURST mode. The signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure. In software serial mode, connect this pin to DGND.
62	SCLK/$\overline{\text{RD}}$	DI	Serial Clock Input/Parallel Data Read Control Input. In serial mode, this pin acts as the serial clock input for data transfers. The $\overline{\text{CS}}$ falling edge takes the SDOA and SDOB data output lines out of three states and clocks out the MSB of the conversion result. The rising edge of SCLK clocks all subsequent data bits onto the SDOA and SDOB serial data outputs. When both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are logic-low in parallel mode, the output bus is enabled.
63	$\overline{\text{CS}}$	DI	Chip Select. This active low-logic input frames the data transfer.

Pin		Type(1)	Description
No.	Name		
			RIn parallel mode, when both $\overline{CS}$ and $\overline{RD}$ are logic low, the DBx output bus is enabled and the conversion result is output on the parallel data bus lines. In serial mode, $\overline{CS}$ frames the serial read transfer and clocks out the MSB of the serial output data.
64, 65, 66	CHSEL0, CHSEL1, CHSEL2	DI	Channel Selection Input 0 to Input 2. In hardware mode, these inputs select the input channels for the next conversion in Channel Group A and Channel Group B. For example, CHSELx = 0x000 selects V0A and V0B for the next conversion; CHSELx = 0x001 selects V1A and V1B for the next conversion. In software mode, these pins must be connected to DGND.
67	BUSY	DO	Busy Output. This pin transitions to a logic high after a CONVST rising edge and indicates that the conversion process has started. The BUSY output remains high until the conversion process for the currently selected channels is complete. The falling edge of BUSY signals that the conversion data is being latched into the output data registers and is available to read. Data must be read after BUSY returns to low. Rising edges on CONVST have no effect while the BUSY signal is high.
68	CONVST	DI	Conversion Start Input for Channel Group A and Channel Group B. This logic input initiates conversions on the analog input channels. A conversion is initiated when CONVST transitions from low to high for the selected analog input pair. When burst mode and oversampling mode are disabled, every CONVST transition from low to high converts one channel pair. In sequencer mode, when burst mode or oversampling is enabled, a single CONVST transition from low to high is necessary to perform the required number of conversions
69	REGGND	CAP	Internal Analog Regulator Ground. This pin must connect to the AGND plane of a system.
70	REGCAP	CAP	Decoupling Capacitor Pin for Voltage Output from Internal Analog Regulator. Decouple this output pin separately to REGGND using capacitors. The voltage at this pin is typically 4 V.
73	V0B	AI	Analog Input for Channel 0, ADC B.
74	V0BGND	AIGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V0B.
75	V1B	AI	Analog Input for Channel 1, ADC B.
76	V1BGND	AIGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V1B.
77	V2B	AI	Analog Input for Channel 2, ADC B.
78	V2BGND	AIGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V2B.
79	V3B	AI	Analog Input for Channel 3, ADC B.
80	V3BGND	AIGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V3B.

(1) AI is analog input, GND is ground, P is power supply, REF is reference input/output, DI is digital input, DO is digital output, and CAP is decoupling capacitor pin.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Analog Voltage	Analog Input Voltage to AGND	−30	+30	V
	REFINOUT to AGND	−0.3	V_{CC} + 0.3 V	V
Digital Voltage	Digital Input Voltage to AGND	−0.3	V_{DRIVE} + 0.3 V	V
	Digital Output Voltage to AGND	−0.3	V_{DRIVE} + 0.3 V	V
Supply Voltage	V_{CC} to AGND	−0.3	7	V
	$V_{DRIVE}$to AGND	−0.3	V_{CC} + 0.3 V	V
T_J	Maximum Junction Temperature		150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD All Pins Except Analog Input Pins	ANSI/ESDA/JEDEC JS-001 (1)	±5	kV
HBM	Human Body Model ESD Analog Input Pins Only	ANSI/ESDA/JEDEC JS-001 (1)	±8	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
V_{CC}	4.75	5	5.25	V
V_{DRIVE}	1.71	3.3	V_{CC}	V

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
QFP14X14-80	36.7	8.2	°C/W

Electrical Characteristics

All test conditions: V_{CC} = 5 V, V_{REF} = 2.5 V (internal/external), V_{DRIVE} = 3.3 V, f_{SAMPLE} = 1 MSPS, T_A = −40 °C to 125 °C, unless otherwise noted.

Parameter	Test Conditions		Min	Typ	Max	Unit
AC Accuracy						
SNR	fin = 1 kHz, ±10 V input range, no oversampling		84.5	89		dB
	fin = 1 kHz, ±5 V input range, no oversampling		84	88		dB
	fin = 1 kHz, ±2.5 V input range, no oversampling		82.5	85.4		dB
SINAD	fin = 1 kHz, ±10 V input range, no oversampling		84	88.7		dB
	fin = 1 kHz, ±5 V input range, no oversampling		84	87.8		dB
	fin = 1 kHz, ±2.5 V input range, no oversampling		82	85.3		dB
Dynamic Range	fin = 1 kHz, ±10 V input range, no oversampling			89.1		dB
	fin = 1 kHz, ±5 V input range, no oversampling			88.1		dB
	fin = 1 kHz, ±2.5 V input range, no oversampling			85.5		dB
THD	fin = 1 kHz, ±10 V input range, no oversampling			−102	−95	dB
	fin = 1 kHz, ±5 V input range, no oversampling			−102		dB
	fin = 1 kHz, ±2.5 V input range, no oversampling			−102		dB
Channel to Channel Isolation	f_{IN} on unselected channels up to 5 kHz			−141		dB
DC Accuracy						
Resolution	NO missing code		16			Bits
DNL			−0.99	±0.5	0.99	LSB
INL			−3	±1	3	LSB
Positive Full-Scale Error	External reference	±10 V input range	−60	±5	60	LSB
		±5 V input range		±6		LSB
		±2.5 V input range		±6		LSB
	Internal reference	±10 V input range		±5		LSB

Parameter	Test Conditions		Min	Typ	Max	Unit
Positive Full-Scale (PFS) Error Drift	External reference			±3.7		ppm/℃
	Internal reference			±7.8		ppm/℃
Positive Full-Scale Error Matching	±10 V input range			8	25	LSB
	±5 V input range			10.6		LSB
	±2.5 V input range			8.2		LSB
Negative Full-Scale Error	External reference	±10 V input range	−60	±4.2	60	LSB
		±5 V input range		±12.4		LSB
		±2.5 V input range		±10.2		LSB
	Internal reference	±10 V input range		±4.2		LSB
Negative Full-Scale (NFS) Error Drift	External reference			±2.7		ppm/℃
	Internal reference			±6.6		ppm/℃
Negative Full-Scale Error Matching	±10 V input range			7.6		LSB
	±5 V input range			21.9		LSB
	±2.5 V input range			17		LSB
Bipolar Zero Code Error	±10 V input range		−10	±1	10	LSB
	±5 V input range		−25	±5	25	LSB
	±2.5 V input range		−26	±5	26	LSB
Bipolar Zero Code Error Drift	±10 V input range			±8		μV/℃
	±5 V input range			±5		μV/℃
	±2.5 V input range			±3		μV/℃
Bipolar Zero Code Error Matching	±10 V input range			1.6	12	LSB
	±5 V input range			8.4		LSB
	±2.5 V input range			8.4		LSB
Analog Input						
Input Voltage Ranges	Software/hardware Configurable				±10	V
	Software/hardware selectable				±5	V
	Software/hardware selectable				±2.5	V
Analog Input Current	±10 V input range			±8.4		μA
	±5 V input range			±3.2		μA
	±2.5 V input range			±1		μA
Input Impedance				1		MΩ
Input Impedance Drift				12		ppm/℃
Analog Filter						
Full Power Bandwidth	−3 dB, ±10 V input range			35		kHz
	−3 dB, ±5 V/±2.5 V input range			31		kHz
Reference						
Reference Input Voltage Range			2.495	2.5	2.505	V

Parameter	Test Conditions	Min	Typ	Max	Unit
DC Leakage Current			1		µA
Input Capacitance	REFSEL = 1		3		pF
Reference Output Voltage (1)	REFINOUT	2.495	2.5	2.505	V
Reference Temperature Coefficient (2)			±3	±10	ppm/℃
Digital Input					
V_{IH}	High-level input voltage	0.7 x V_{DRIVE}		V_{DRIVE} + 0.3	V
V_{IL}	Low-level input voltage	−0.3		0.3 x V_{DRIVE}	V
Input Current			±1		uA
Digital Output					
Data Format			Twos complement		
V_{OH}	I_{SOURCE} = 100 µA	0.8 x V_{DRIVE}		V_{DRIVE}	V
V_{OL}	I_{SINK} = 100 µA	0		0.2 x V_{DRIVE}	V
Floating State Leakage Current			±1		uA
Conversion Rate					
Conversion Time	Per channel pair		750		ns
Acquisition Time	Per channel pair		250		ns
Throughput Rate	Per channel pair			1	MSPS
Power Supply					
V_{CC}[2]	Specified performance	4.75		5.25	V
V_{DRIVE}[2]	Specified performance	1.71		V_{CC}	V
I_{VCC}					
Static			43.2	50	mA
Operational	f_{SAMPLE} = 1 MSPS		47.6	53	mA
Shutdown Mode			11.6		uA
I_{DRIVE}	Digital inputs = 0 V or V_{DRIVE}				
Static			0.2		uA
Operational	f_{SAMPLE} = 1 MSPS		1.6		mA
Shutdown Mode			0.2		uA
Power Dissipation					
Static			216		mW
Operational	f_{SAMPLE} = 1 MSPS		244		mW
Shutdown Mode			0.06		mW
Temperature Range	Specified performance	−40		+125	℃

(1) Does not include the variation in voltage resulting from solder shift effects.
(2) Not production tested. Sample tested during initial release to ensure compliance.

Timing Requirements (1)

Universal Timing Specifications

V_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 1.71 V to 5.25 V, V_{REF} = 2.5 V external reference/internal reference.

T_A = −40°C to +125°C, unless otherwise noted. Interface timing tested using a load capacitance of 30 pF, dependent on V_{DRIVE} and load capacitance for the serial interface.

Table 2. Universal Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
t_{CYCLE}	Minimum time between consecutive CONVST rising edges (excluding burst and oversampling modes)	1			µs
t_{CONV_LOW}	CONVST low pulse width	50			ns
t_{CONV_HIGH}	CONVST high pulse width	50			ns
t_{BUSY_DELAY}	CONVST high to BUSY high (manual mode)			32	ns
t_{CS_SETUP}	BUSY falling edge to $\overline{CS}$ falling edge setup time	20			ns
t_{CH_SETUP}	Channel select setup time in hardware mode for CHSELx	50			ns
t_{CH_HOLD}	Channel select hold time in hardware mode for CHSELx	20			ns
t_{CONV}	Conversion time for the selected channel pair		700	800	ns
t_{ACQ}	Acquisition time for the selected channel pair	200			ns
t_{ACQ_BURST}	Acquisition time for the selected channel pair in burst mode	550	600		ns
t_{QUIET}	$\overline{CS}$ rising edge to next CONVST rising edge	50			ns
$t_{\overline{RESET}\_LOW}$					
Partial Reset	Partial $\overline{RESET}$ low pulse width	100		500	ns
Full Reset	Full $\overline{RESET}$ low pulse width	1.2			µs
t_{DEVICE_SETUP}					
Partial Reset	Time between partial $\overline{RESET}$ high and CONVST rising edge	70			ns
Full Reset	Time between full $\overline{RESET}$ high and CONVST rising edge	15			ms
t_{WRITE}					
Partial Reset	Time between partial $\overline{RESET}$ high and $\overline{CS}$ for write operation	70			ns
Full Reset	Time between full $\overline{RESET}$ high and $\overline{CS}$ for write operation	240			µs
$t_{\overline{RESET}\_WAIT}$	Time between stable V_{CC}/V_{DRIVE} and the release of $\overline{RESET}$	1			ms
$t_{\overline{RESET}\_SETUP}$					
Partial Reset	Time prior to the release of $\overline{RESET}$ that queried hardware inputs must be stable for	10			ns
Full Reset		0.05			ms
$t_{\overline{RESET}\_HOLD}$					
Partial Reset	Time after the release of $\overline{RESET}$ that queried hardware inputs must be stable for	10			ns
Full Reset		0.24			ms

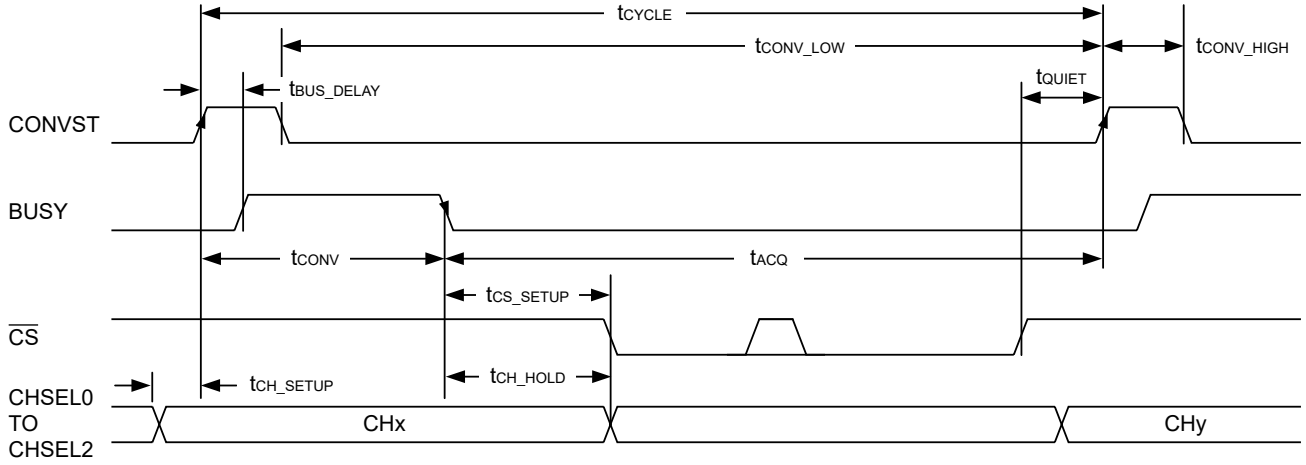


Figure 1. Universal Timing Diagram Across All Interfaces

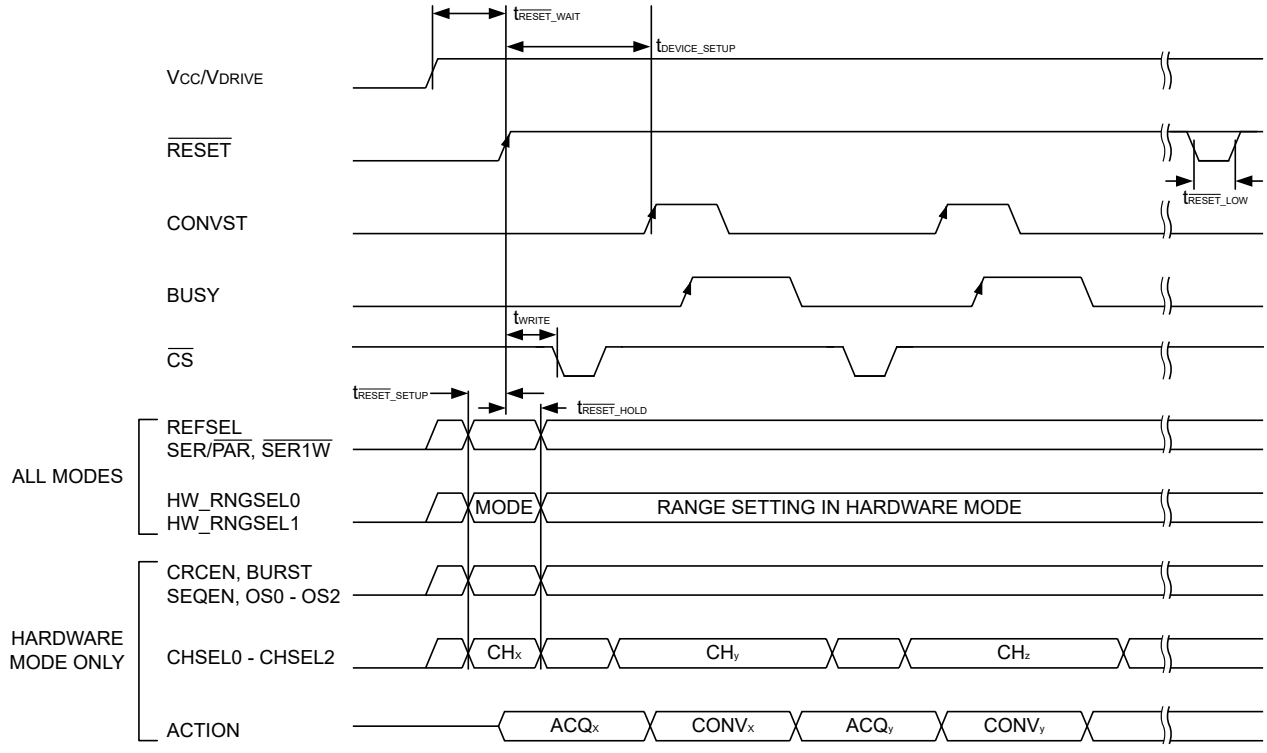


Figure 2. Reset Timing

Parallel Mode Timing Specifications

Table 3. Parallel Mode Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{RD}\_SETUP}$	$\overline{CS}$ falling edge to $\overline{RD}$ falling edge setup time	10			ns
$t_{\overline{RD}\_HOLD}$	$\overline{RD}$ rising edge to $\overline{CS}$ rising edge hold time	10			ns
$t_{\overline{RD}\_HIGH}$	$\overline{RD}$ high pulse width	10			ns
$t_{\overline{RD}\_LOW}$	$\overline{RD}$ low pulse width	30			ns
t_{DOUT_SETUP}	Data access time after the falling edge of $\overline{RD}$			30	ns
t_{DOUT_3STATE}	$\overline{CS}$ rising edge to DBx high impedance			11	ns
$t_{\overline{WR}\_HIGH}$	$\overline{CS}$ to $\overline{WR}$ setup time	10			ns
t_{WR_HIGH}	$\overline{WR}$ high pulse width	20			ns
$t_{\overline{WR}\_LOW}$	$\overline{WR}$ low pulse width	30			ns
$t_{\overline{WR}\_HOLD}$	$\overline{WR}$ hold time	10			ns
t_{DIN_SETUP}	Configuration data to $\overline{WR}$ setup time	30			ns
t_{DIN_HOLD}	Configuration data to $\overline{WR}$ hold time	10			ns
t_{CONF_SETTLE}	Configuration data settle time, $\overline{WR}$ rising edge to CONVST rising edge	20			ns

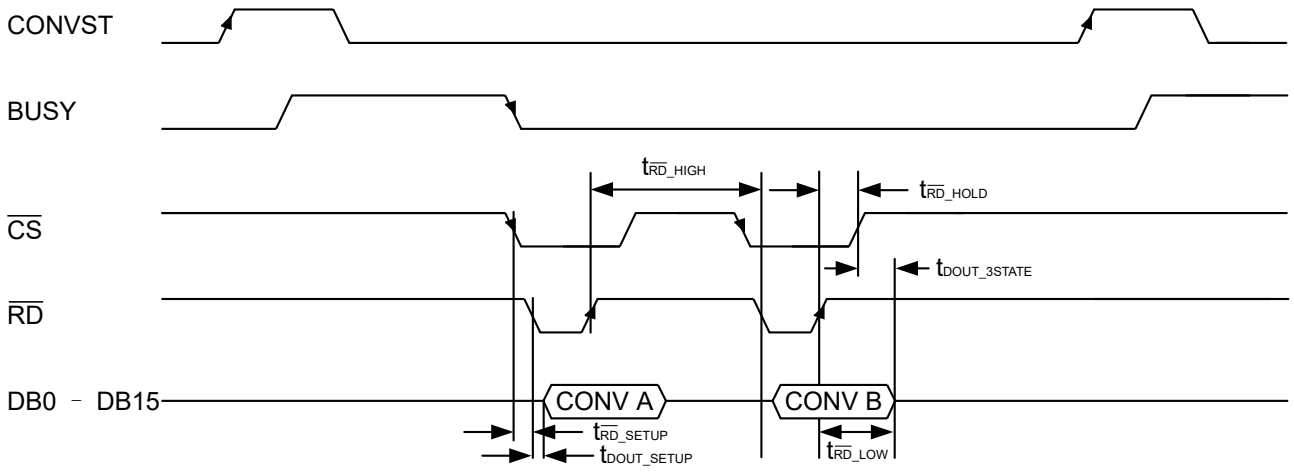


Figure 3. Parallel Read Timing Diagram

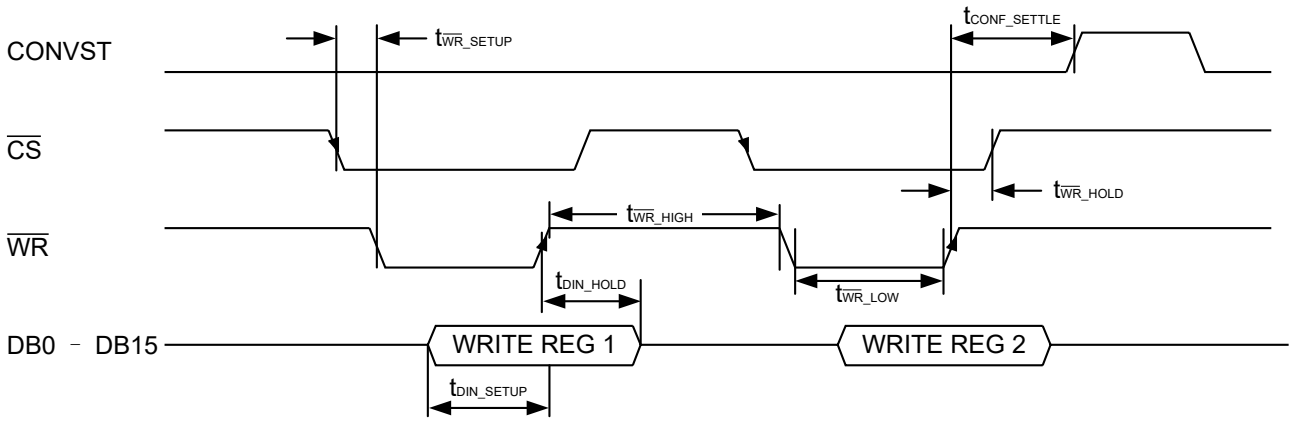


Figure 4. Parallel Write Timing Diagram

Serial Mode Timing Specifications

Table 4. Serial Mode Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
f_{SCLK}	SCLK frequency			40/50	MHz
t_{SCLK}	Minimum SCLK period	$1/f_{SCLK}$			
t_{SCLK_SETUP}	$\overline{CS}$ to SCLK falling edge setup time, V_{DRIVE} above 3 V	10.5			ns
	$\overline{CS}$ to SCLK falling edge setup time, V_{DRIVE} above 1.8 V	30			ns
t_{SCLK_HOLD}	SCLK to $\overline{CS}$ rising edge hold time	10			ns
t_{SCLK_LOW}	SCLK low pulse width	8			ns
t_{SCLK_HIGH}	SCLK high pulse width	9			ns
t_{DOUT_SETUP}	Data out access time after SCLK rising edge, V_{DRIVE} above 3 V			12	ns
	Data out access time after SCLK rising edge, V_{DRIVE} above 1.8 V			16	ns
t_{DOUT_HOLD}	Data out hold time after SCLK rising edge	4			ns
t_{DIN_SETUP}	Data in setup time before SCLK falling edge	10			ns
t_{DIN_HOLD}	Data in hold time after SCLK falling edge	8			ns
t_{DOUT_3STATE}	$\overline{CS}$ rising edge to SDOx high impedance			10	ns

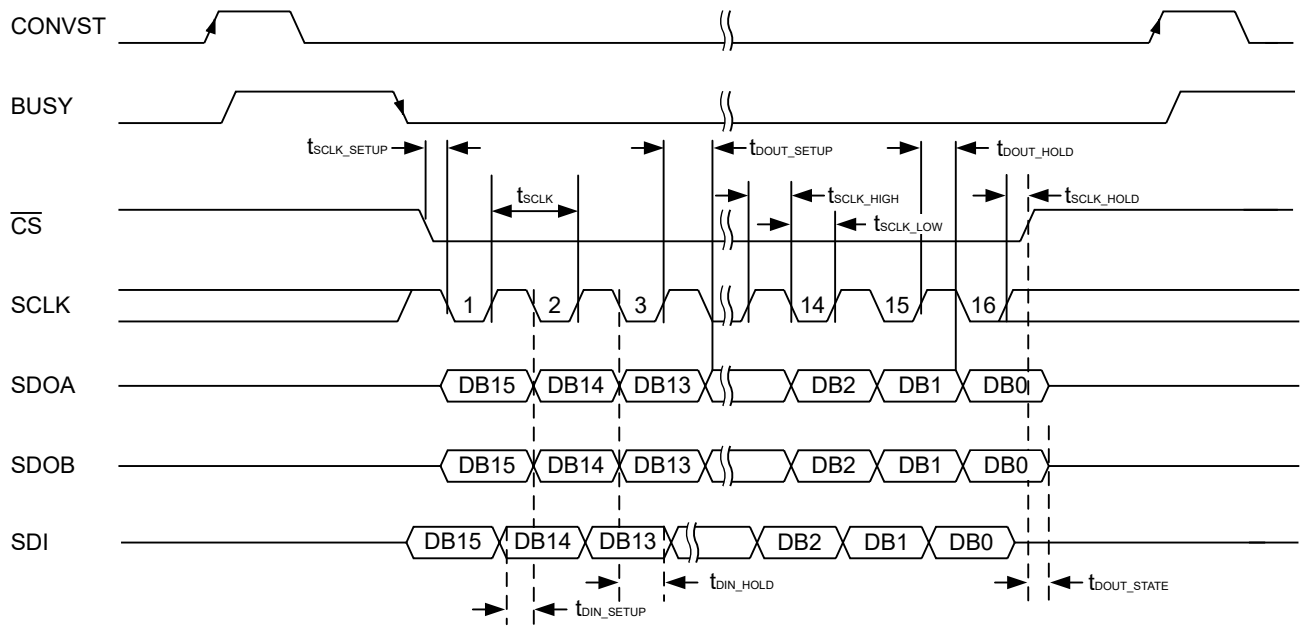


Figure 5. Serial Timing Diagram

(1) Parameters are guaranteed by design.

Typical Performance Characteristics

All test conditions: V_{REF} = 2.5 V internal, V_{CC} = 5 V, V_{DRIVE} = 3.3 V, f_{SAMPLE} = 1 MSPS, f_{IN} = 1 kHz T_A = 25°C, unless otherwise noted.

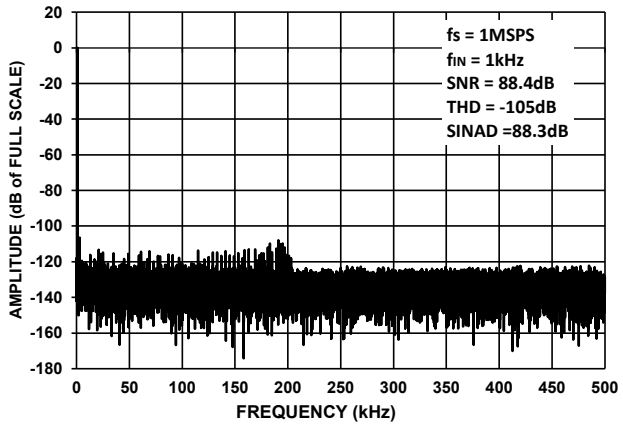


Figure 6. FFT, ±10 V Range

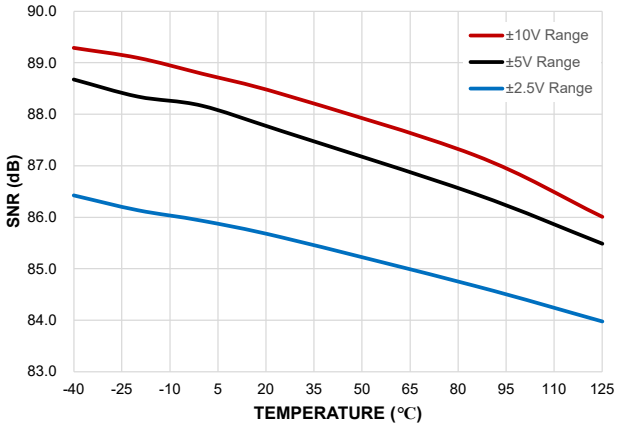


Figure 7. SNR vs. Temperature

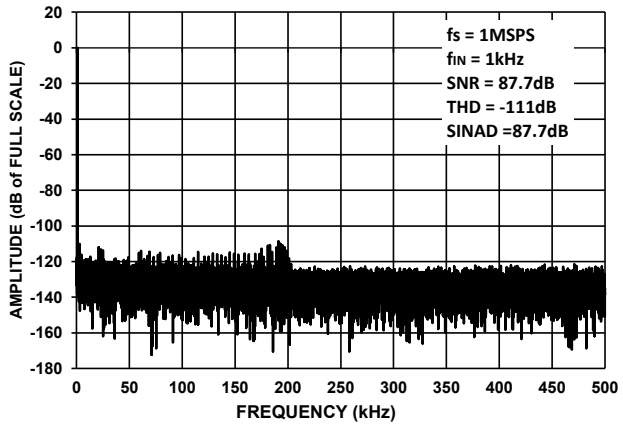


Figure 8. FFT, ±5 V Range

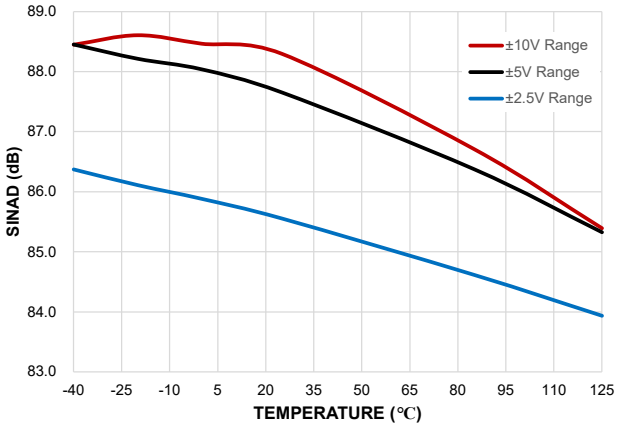


Figure 9. SINAD vs. Temperature

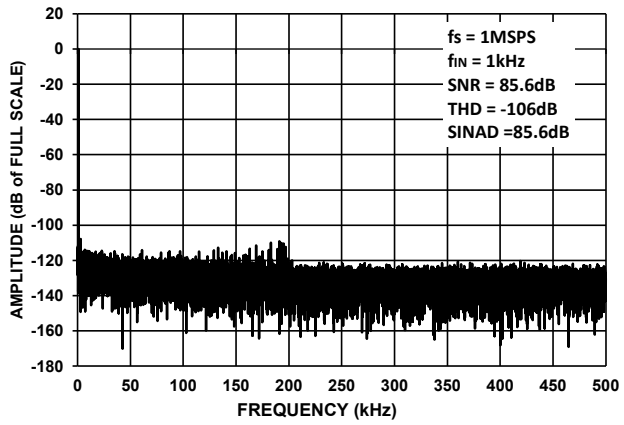


Figure 10. FFT, ±2.5 V Range

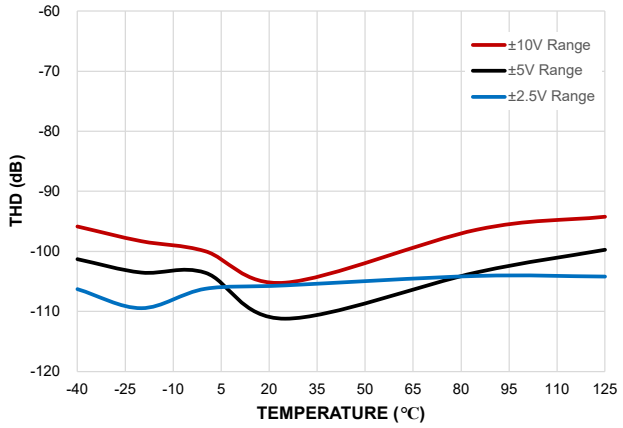


Figure 11. THD vs. Temperature

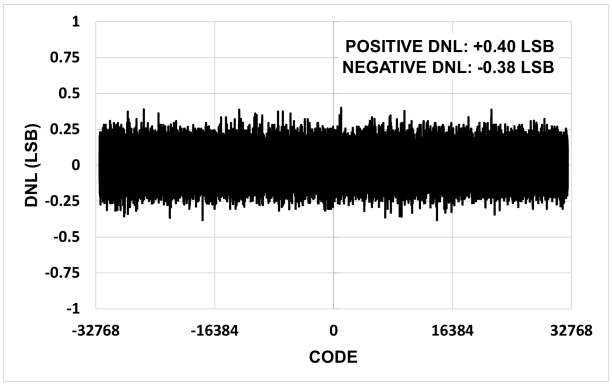


Figure 12. DNL, ±10 V Range

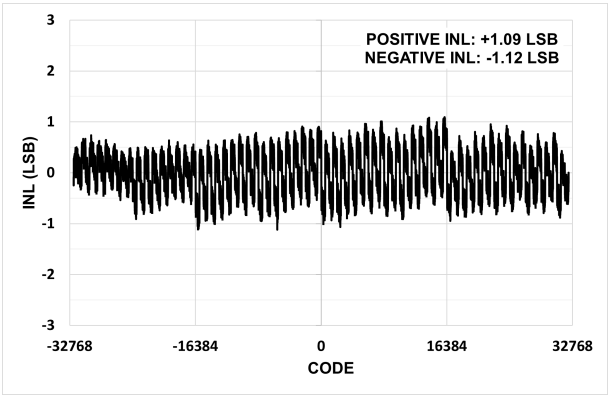


Figure 13. INL, ±10 V Range

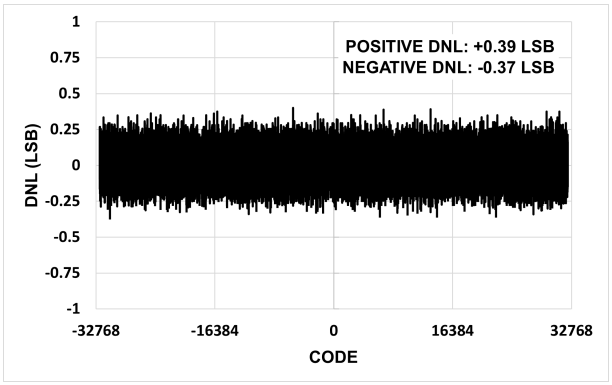


Figure 14. DNL, ±5 V Range

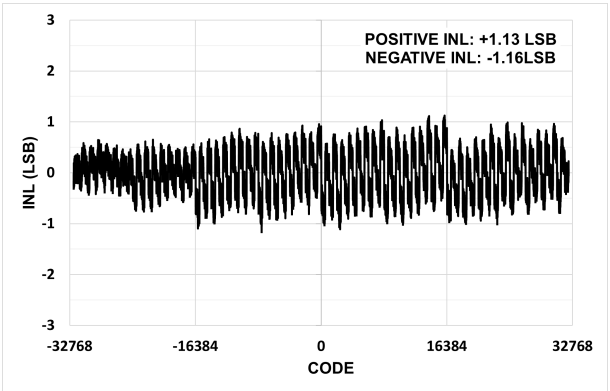


Figure 15. INL, ±5 V Range

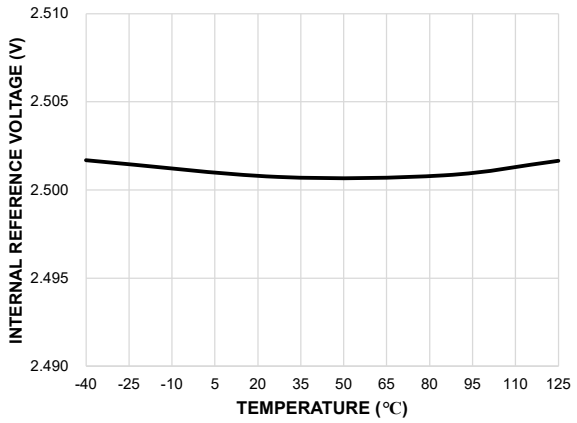


Figure 16. Internal Reference Voltage vs. Temperature

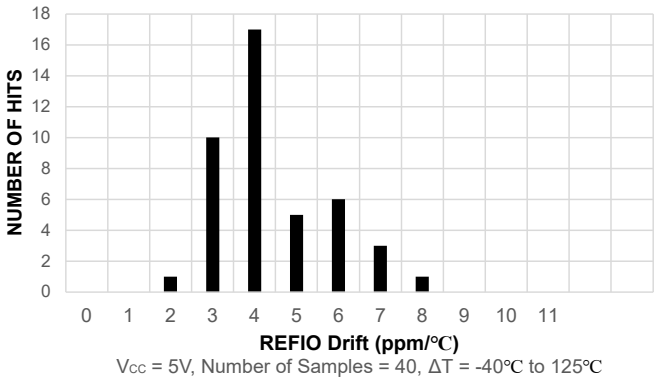


Figure 17. Internal Reference Temperature Drift Histogram

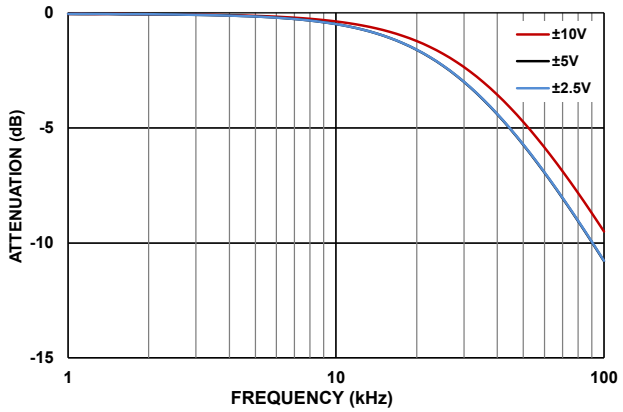


Figure 18. Analog Antialiasing Filter Frequency Response

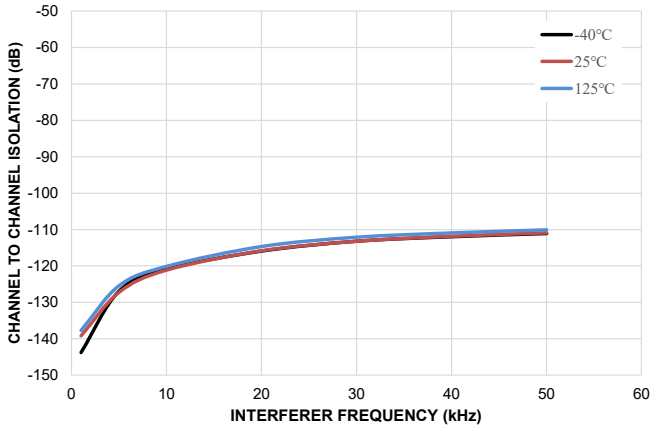


Figure 19. Channel to Channel Isolation

Detailed Description

Overview

The TPAFE51760 is a 16-bit data acquisition system with 16 analog input channels. Each input channel includes input protection circuitry, a programmable gain amplifier (PGA), an analog low-pass filter, and an analog-to-digital converter (ADC) driver. These channels feed into two simultaneous sampling 16-bit ADCs with 1 MSPS throughput rate. The device incorporates a 2.5-V internal reference with a fast-settling buffer, a programmable digital averaging filter to reduce noise, and a flexible channel sequencer. It also provides high-speed parallel and serial interfaces for communication with various digital hosts, making it suitable for a wide range of data acquisition applications.

The device operates with a single 5-V analog supply and can process true bipolar input signals. It provides a programmable analog signal range, including options for ±10 V, ±5 V, and ±2.5 V. The input clamp protection circuitry can protect the device from being damaged by voltages as high as ±30 V. The device features a constant 1-MΩ resistive input impedance.

The device offers both hardware and software operating modes, selectable through the HW_RNGSELx pins. In hardware mode, the device's configuration is determined by external pin settings. In contrast, software mode allows the device to be configured and controlled using control registers accessed through the parallel or serial interface.

Functional Block Diagram

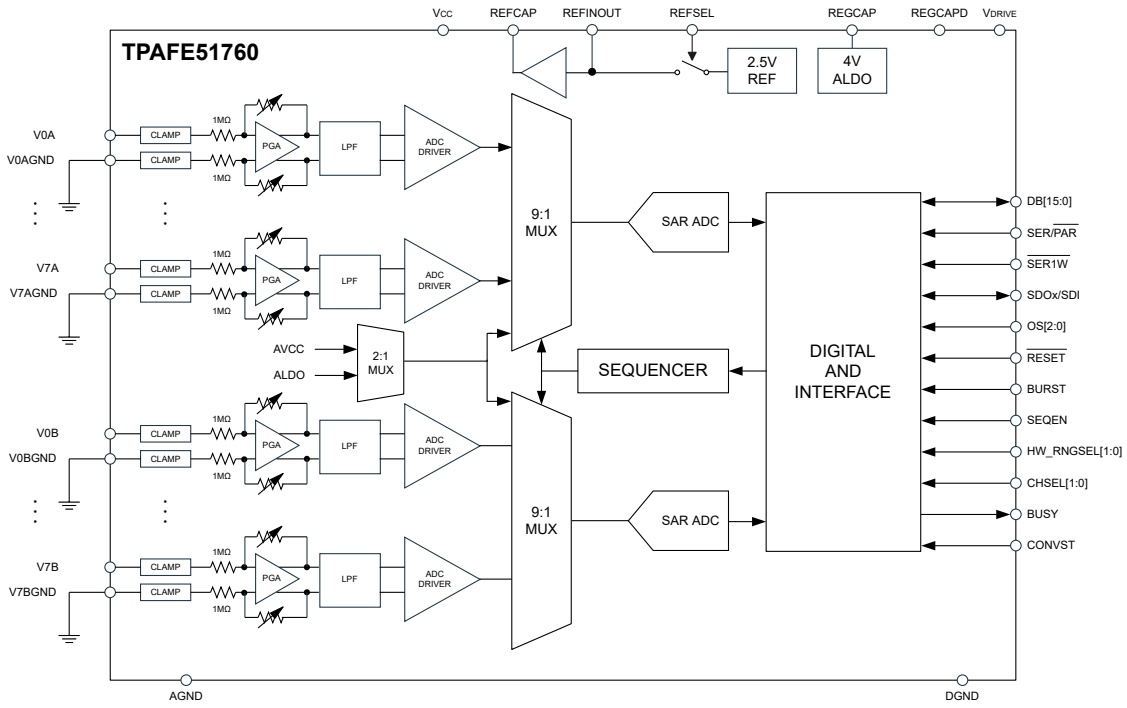


Figure 20. TPAFE51760 Block Diagram

Feature Description

Analog Input

Analog Input Channel Selection

The TPAFE51760 incorporates dual 16-bit ADCs that support simultaneous sampling of 16 analog input channels. It also features built-in diagnostic channels for V_{CC} supply monitoring and includes an internal LDO. Channel selection for conversion can be performed in two modes:

- **Hardware Mode:** Channels are chosen for conversion by setting external CHSELx pins. In this mode, simultaneous sampling is restricted to corresponding A and B channels (e.g., Channel V0A is paired with Channel V0B).
- **Software Mode:** Channel selection and configuration occur through control registers accessible via the parallel and serial interface. Software mode is necessary for sampling diagnostic channels and offers the flexibility to dynamically select any A channel alongside any B channel for simultaneous sampling. The device also features an on-chip sequencer for preprogramming channel conversion sequences.

Analog Input Ranges

The TPAFE51760 can process true bipolar, single-ended input voltages. The selection of analog input range for all analog input channels is determined by the logic levels applied to the range select pins, specifically HW_RNGSEL0 and HW_RNGSEL1:

- **Hardware Mode Range Selection:** The analog input range for all channels is determined by the logic levels on the range select pins. If both range-select pins are connected to a logic low (ground), the analog input range is configured in software mode using the input range registers. In hardware mode, any change in logic levels on the range select pins (HW_RNGSEL0 and HW_RNGSEL1) directly affects the analog input range. However, it's important to note that there is typically a settling time of approximately 120 µs required in addition to the normal acquisition time. To ensure proper operation and avoid issues related to settling time, the recommended practice is to hardwire (permanently set) the range select pins according to the desired input range for the system's signals.
- **Software Mode Range Selection:** In software mode, users have the flexibility to configure individual analog input ranges for each channel. This means that different channels can have its individual input ranges.

Table 5. Analog Input Range Selection

Analog Input Range	HW_RNGSEL1	HW_RNGSEL0
Configured via the Input Range Registers	0	0
±2.5 V	0	1
±5 V	1	0
±10 V	1	1

Analog Input Impedance

The TPAFE51760 features a fixed high analog input impedance of 1 MΩ, which is nearly constant at different sampling frequencies. It eliminates the need for an external driver amplifier, allowing direct connection to the source or sensor.

Analog Input Clamp Protection

Each analog input of the TPAFE51760 incorporates a clamp protection circuitry. Though the device's single 5 V supply operation, it provides robust protection against input overvoltages up to ±30 V. For source voltages within the range of -30 V to +30 V, there is no current flow through the clamp circuit. In this voltage range, the clamp circuit remains inactive. When input voltages exceed +30 V or fall below -30 V, the clamp circuitry activates. This activation occurs to protect the device and prevent damage from input voltages that exceed its specified operating range

It is recommended to add a series resistor for current limiting. This resistor limits the current to a safe ±10 mA level. When adding a series resistor to an analog input channel like VxA or VxB, it's crucial to also incorporate a corresponding resistor

on the analog input ground channel (VxAGND or VxBGND) to maintain proper signal referencing and prevent offset errors. However, it's advisable to avoid prolonged activation of the clamp protection circuitry during normal or power-down conditions for optimal device performance.

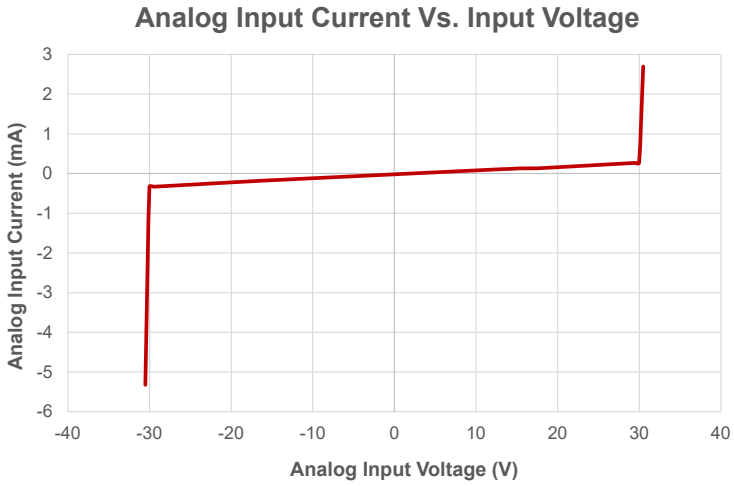


Figure 21. Input Protection Clamp Profile, Input Clamp Current vs. Source Voltage

Analog Input Filter

The TPAFE51760 integrates a first-order Butterworth analog anti-aliasing filter, which is designed to prevent aliasing and filter noise. The filter's typical corner frequency is approximately 35 kHz for the ±10 V input range and approximately 31 kHz for the ±5 V and ±2.5 V input range.

ADC Transfer Function

The TPAFE51760 outputs 16 bits of conversion data in binary twos complement format for all ranges. The code transitions are positioned at the midpoint between successive integer LSB values. Specifically, these transitions occur at 1/2 LSB and 3/2 LSB intervals. The size of the LSB is determined by the full-scale range divided by 65,536. It should be noted that the actual LSB size depends on the selected analog input range.

$$CODE = \frac{V_{IN}}{FULL\ SCALE\ RANGE} \times 65536 \times \frac{2.5V}{REFINOUT} \quad (1)$$

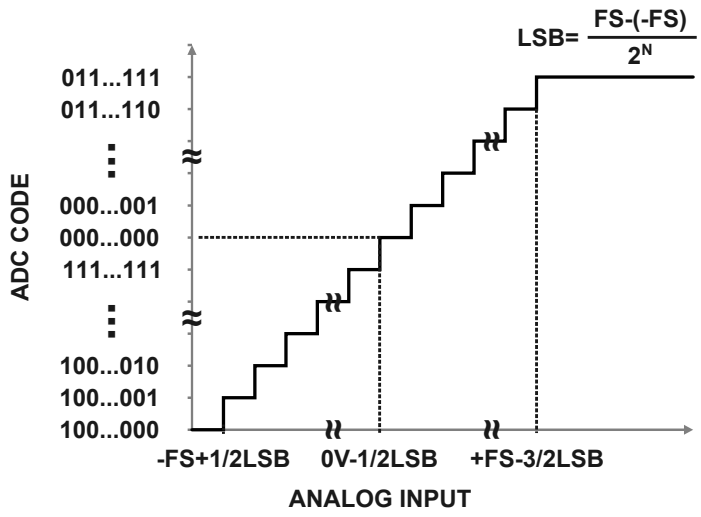


Table 6. Transfer Characteristics

	+FS	MIDSCALE	−FS	LSB
±10 V RANGE	+10 V	0 V	−10 V	305 µV
±5 V RANGE	+5 V	0 V	−5 V	152 µV
±2.5 V RANGE	+2.5 V	0 V	−2.5 V	76 µV

Internal/External Reference

The TPAFE51760 offers flexibility in its reference voltage configuration, allowing it to operate with either an internal or external reference:

- **Internal Reference:** The device includes an on-chip 2.5 V band-gap reference which can be accessed through the REFINOUT pin. This on-chip reference is used to generate an internal 4.096 V reference voltage. The SAR ADC utilizes this internally generated and buffered 4.096 V reference for its conversions.
- **External Reference:** Alternatively, the device can accept an external reference voltage of 2.5 V applied to the REFINOUT pin. When an external 2.5 V reference is provided, the device internally amplifies it to create the 4.096 V buffered reference used by the SAR ADC.

The device simplifies reference voltage selection through the REFSEL pin. When set to logic high (1), it activates the internal reference, utilizing the on-chip 2.5 V band-gap reference to generate a 4.096 V internal reference voltage. Conversely, when set to logic low (0), it deactivates the internal reference, necessitating the application of an external reference voltage to the REFINOUT pin, which is then internally amplified to create the 4.096 V reference.

The TPAFE51760 features an always-enabled internal reference buffer. Following a complete reset, the device operates in the reference mode determined by the REFSEL pin.

The device includes a reference buffer designed to amplify the reference voltage to approximately 4.096 V. The reference voltage is initially available at the REFINOUT pin as 2.5 V. In external reference mode, the REFINOUT pin functions as a high input impedance pin. If the user intends to use the internal reference voltage elsewhere in the system, it must be externally buffered before being applied to other components or circuits.

Shutdown Mode

The TPAFE51760 can be configured into shutdown mode by holding the RESET pin low for a duration greater than 1.2 µs. To exit shutdown mode and return to normal operation, set the RESET pin from low to high. During shutdown mode, the device exhibits a typical low current consumption and the power-up time is approximately 240 ms. For initiating a conversion, the power-up time is extended to 15 milliseconds. It's important to note that in shutdown mode, all internal circuitry is powered down, and all registers are cleared and reset to their default values, ensuring a controlled and consistent restart when exiting this mode.

Digital Filter

The TPAFE51760 has an optional digital averaging filter that can be used in slower throughput applications requiring lower noise and higher dynamic range. In oversampling mode, the samples are averaged to reduce the noise of the signal chain as well as to improve the SNR of the ADC. The final output is also decimated to provide data for each channel.

The Oversampling Ratio (OSR) of the digital filter in the device can be configured either in hardware or software mode. In software mode, the user can enable oversampling for all channels by setting the OS bits within the configuration register. In hardware mode, the OSR is determined by the state of the oversampling pins (OS2 to OS0) at the time of a full reset release.

Table 7. Oversampling Bit Decoding

OSx Pins/OS Bits	OSR
000	No oversampling

OSx Pins/OS Bits	OSR
001	2
010	4
011	8
100	16
101	32
110	64
111	128

Device Configuration
Operational Mode

The mode of operation (hardware mode or software mode) is determined when the TPAFE51760 exits from a full reset. This determination relies on the logic levels present on the HW_RNGSELx pins when the $\overline{\text{RESET}}$ pin transitions from a low to a high state. These pins have a dual function in this context.

If the HW_RNGSELx pins are set to 0b00 during the reset exit, the device enters software mode. In software mode, the logic levels of the HW_RNGSELx pins become irrelevant and are not considered. Subsequent device configuration in software mode is primarily achieved through register access.

Any other combination of the HW_RNGSELx pins configures the device for hardware mode. In hardware mode, all device configuration is controlled through pin settings. In this mode, access to on-chip registers is restricted.

Once an operational mode is configured, a full reset triggered by the $\overline{\text{RESET}}$ pin is necessary to exit that mode and switch to an alternative mode. In hardware mode, further device configuration is achieved through pin control, while in software mode, interface and reference configuration must be initially set through pin control, but the subsequent device configuration is primarily accomplished via register access.

Internal/External Reference

The configuration of the internal reference in the TPAFE51760 is determined upon exiting from a full reset. Specifically, the logic level of the REFSEL signal at the moment when the $\overline{\text{RESET}}$ pin transitions from a low to a high state sets the reference mode. Once the reference is configured, any subsequent changes to the logic level of the REFSEL signal are disregarded. If the REFSEL signal is set to 1, it enables the internal reference. If the REFSEL signal is set to Logic 0, it disables the internal reference, necessitating the provision of an external reference to the REFINOUT pin for the proper operation of the device. To transition to an alternative operational mode, a full reset through the $\overline{\text{RESET}}$ pin is mandatory.

Digital Interface

The option between the digital interface modes, parallel or serial, is established upon the TPAFE51760 exiting from a full reset. This configuration depends on the logic level of the SER/$\overline{\text{PAR}}$ signal at the moment when the $\overline{\text{RESET}}$ pin undergoes a transition from a low to a high state. If the SER/PAR signal is set to 0, it activates the parallel interface. If the SER/$\overline{\text{PAR}}$ signal is set to 1, it selects the serial interface. Furthermore, when the serial interface is chosen, the $\overline{\text{SER1W}}$ signal is monitored as the $\overline{\text{RESET}}$ pin is released to determine whether serial 1-wire or 2-wire mode is selected. Once the interface is configured, any subsequent changes to the logic levels of the SER/$\overline{\text{PAR}}$ signal or the $\overline{\text{SER1W}}$ signal (if the serial interface is enabled) are not taken into account. To switch to an alternative operational mode, a full reset using the $\overline{\text{RESET}}$ pin is required.

Hardware Mode

In hardware mode, the functionality of the TPAFE51760 is limited, and all configuration settings are controlled via pin control. Upon the device exiting from a full reset, the logic levels of the following signals are checked to determine the device's functionality: CRC, BURST, SEQEN, and OSx. The table below provides an overview of the signals that are latched by the device upon the release of a full reset, based on the chosen mode of operation. Once the device is configured, a full reset using the $\overline{\text{RESET}}$ pin is necessary to exit the current configuration and establish an alternative one. The availability of functionality is constrained depending on the interface type selected, and refer to the summary for a comprehensive list of the functionality available in hardware parallel or serial mode.

The CHSELx pins are examined during the reset process to establish the initial analog input channel pair for conversion or to configure the initial settings for the hardware sequencer. During regular operation, it is possible to reconfigure the channel pair designated for conversion or the hardware sequencer by setting and maintaining the CHSELx signal level before the rising edge of the CONVST signal until the falling edge of the BUSY signal.

The HW_RNGSELx signals are responsible for controlling the analog input range for all 16 analog input channels. When there is a logic change on these pins, it directly impacts the analog input range. However, it's important to note that there is typically a settling time of around 120μs required in addition to the normal acquisition time. It is recommended to set the range select pins to the desired input range for the system signals and leave them in that configuration. In hardware mode, access to the on-chip registers of the device is not allowed.

Table 8. Summary of Latched Hardware Signals

Signal	Latched at Full Reset		Read at Reset		Read During Busy		Edge Driven	
	HW Mode	SW Mode	HW Mode	SW Mode	HW Mode	SW Mode	HW Mode	SW Mode
REFSEL	Yes	Yes	N/A	N/A	N/A	N/A	N/A	N/A
SEQEN	Yes	No	N/A	N/A	N/A	N/A	N/A	N/A
HW_RNGSELx (Range Change)	N/A	N/A	Yes	Yes	N/A	N/A	Yes	No
HW_RNGSELx (Hardware (HW) or Software (SW) Mode)	Yes	Yes	N/A	N/A	N/A	N/A	N/A	N/A
SER/$\overline{\text{PAR}}$	Yes	Yes	N/A	N/A	N/A	N/A	N/A	N/A
CRCEN	Yes	No	N/A	N/A	N/A	N/A	N/A	N/A
OSx	Yes	No	N/A	N/A	N/A	N/A	N/A	N/A
BURST	Yes	No	N/A	N/A	N/A	N/A	N/A	N/A
CHSELx	N/A	N/A	Yes	No	Yes	No	N/A	N/A
$\overline{\text{SER1W}}$	Yes	Yes	N/A	N/A	N/A	N/A	N/A	N/A

Software Mode

When software mode is selected for the TPAFE51760, all configuration settings and functionality are controlled via the on-chip registers of the device. This mode provides full access to the device's features and capabilities. The summary table provides a summary of the signals that are latched by the device on the release of a full reset, depending on the mode of operation chosen.

Reset Functionality

The TPAFE51760 offers two reset modes: full and partial, which are determined by the length of the low pulse applied to the RESET pin.

- **Partial Reset:** A partial reset is triggered by holding the $\overline{\text{RESET}}$ pin low for a duration between 40 ns (nanoseconds) and 500 ns. After a minimum of 50 ns from the release of the $\overline{\text{RESET}}$ pin, the device becomes fully functional and is ready for operation. The sequencer, digital filter, SPI, and both SAR ADC cores are reinitialized by partial reset.
- **Full Reset:** A full reset is initiated by holding the $\overline{\text{RESET}}$ pin low for a minimum of 1.2 µs. After approximately 15 ms from the release of the $\overline{\text{RESET}}$ pin, the device undergoes a complete reconfiguration process. Following the full reset, the device is reset to its default state, and all settings and registers are restored to their initial values. Only after this full reset and reconfiguration can a conversion be initiated. A full reset restores the device to its default power-on state and configures some features upon release from reset, including the operational mode (hardware or software), reference selection (internal or external), and interface type (serial or parallel).

A partial reset in the TPAFE51760 discards the current conversion result but does not affect the register values programmed in software mode or the user configuration settings stored in latches in both hardware and software modes. To ensure proper operation in software mode after a partial reset, it typically requires a dummy conversion.

Upon power-up of the TPAFE51760, it is recommended to release the $\overline{\text{RESET}}$ signal once both the V_{CC} and V_{DRIVE} supplies have stabilized. The configuration of the device is determined by the logic levels of various pins, including HW_RNGSELx, REFSEL, SER/$\overline{\text{PAR}}$, and DB4/$\overline{\text{SER1W}}$, at the moment when the $\overline{\text{RESET}}$ pin is released after a full reset.

In hardware mode, the configuration of the device is established during a full reset and remains fixed until another reset occurs. This configuration includes settings for functions CRC, BURSTEN, SEQEN, and OSx. Changes to these signals

after configuration is not ignored. Additionally, the analog input range (controlled by HW_RNGSELx signals) can be adjusted during a full or partial reset or during normal operation. However, switching between hardware and software modes requires a full reset, as this setting is latched.

In hardware mode, the CHSELx and HW_RNGSELx pins are examined when the device is released from both full and partial resets to perform the following functions:

- Determine the initial analog input channel pair to use for conversion.
- Configure the initial settings for the sequencer.
- Select the analog input voltage range.

The CHSELx and HW_RNGSELx signals are not latched, meaning that the channel pair chosen for conversion or the hardware sequencer can be reconfigured during normal operation. This is achieved by setting and maintaining the CHSELx signal level before the CONVST rising edge and ensuring that the signal level remains constant until BUSY transitions low again.

In software mode, all additional functionality of the TPAFE51760 is configured by controlling the on-chip registers.

It should be noted that the default conversion results after reset are all zeros, if the conversion is not initiated.

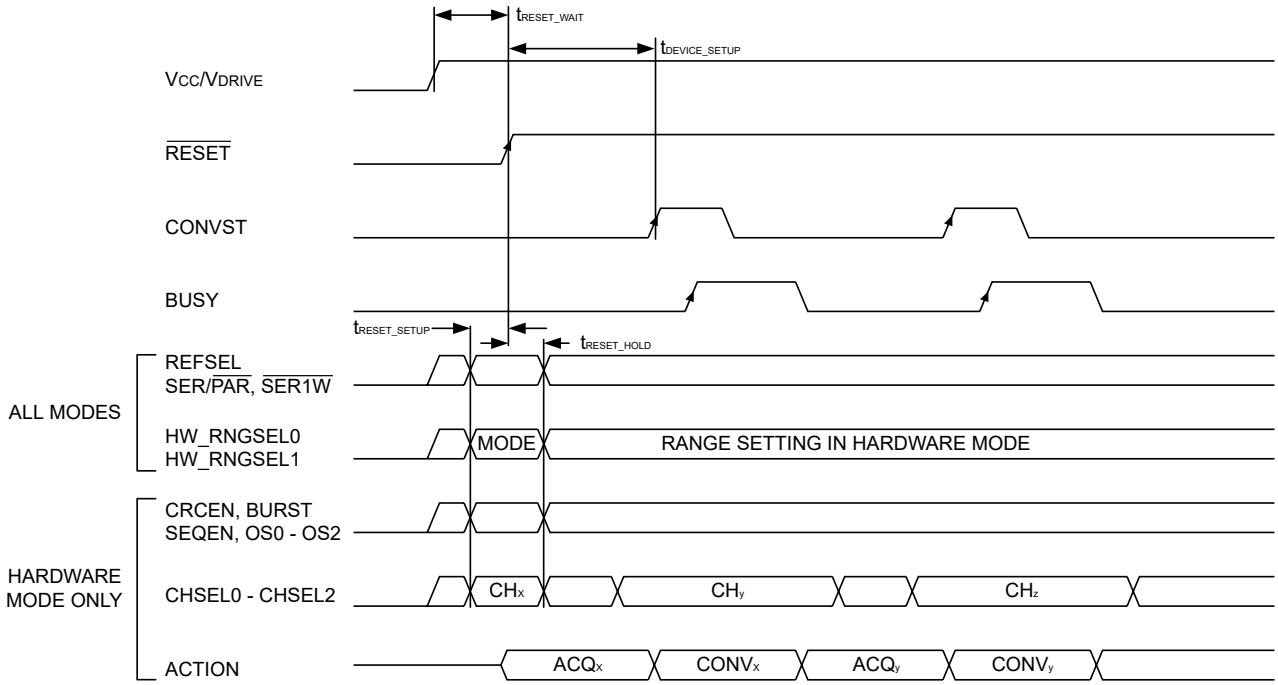


Figure 22. Configuration at Reset

Pin Function Overview

TPAFE51760 pin functionality in different modes of operation and interface modes is listed below, and it defines the dual function of these pins based on the configuration set by the HW_RNGSELx pins. These pins serve different purposes depending on whether the device is operating in hardware mode or software mode and whether the communication interface is parallel or serial.

Table 9. Pin Functionality Overview

Pins	Operation Mode			
	Software Mode, HW_RNGSELx = 00		Hardware Mode, HW_RNGSELx ≠ 00	
	Serial, SER/$\overline{PAR}$ = 1	Serial, SER/$\overline{PAR}$ = 0	Serial, SER/$\overline{PAR}$ = 1	Serial, SER/$\overline{PAR}$ = 0
CHSELx	No function, connect to DGND	No function, connect to DGND	CHSELx	CHSELx
SCLK/$\overline{RD}$	SCLK	$\overline{RD}$	SCLK	$\overline{RD}$
$\overline{WR}$/BURST	Connect to DGND	$\overline{WR}$	BURST	BURST
DB15/OS0 to DB13/OS2	Connect to DGND	DB15 to DB13	OSx	DB15 to DB13
DB12/SDOA	SDOA	DB12	SDOA	DB12
DB11/SDOB	SDOB, leave floating for serial 1-wire mode	DB11	SDOB	DB11
DB10/SDI	SDI	DB10	Connect to DGND	DB10
DB9 to DB6, DB3 to DB0	Connect to DGND	DB9 to DB6, DB3 to DB0	Connect to DGND	DB9 to DB6, DB3 to DB0
DB5/CRCEN	Connect to DGND	DB5	CRCEN	DB5
DB4/$\overline{SER1W}$	$\overline{SER1W}$	DB4	$\overline{SER1W}$	DB4
HW_RNGSELx	HW_RNGSELx, connect to DGND	HW_RNGSELx, connect to DGND	HW_RNGSELx, configure analog input range	HW_RNGSELx, configure analog input range
SEQEN	No function, connect to DGND	No function, connect to DGND	SEQEN	SEQEN
REFSEL	REFSEL	REFSEL	REFSEL	REFSEL

Digital Interface

Channel Selection
Hardware Mode

The CHSELx signals, which represent the channel selection, determine the channel pair for conversion in the TPAFE51760. During a full or partial reset, the logic levels of the CHSELx signals set the initial channel pair for sampling. Following a reset, the CHSELx signals' logic levels are examined while the BUSY signal is high to set the channel pair for the next conversion. It's essential to set the CHSELx signal level before the CONVST signal transitions from low to high and to maintain this level until BUSY goes from high to low, indicating the completion of a conversion.

Table 10. CHSELx Pin Decoding

Channel Selection Input Pin			Analog Input Channels for Conversion
CHSEL0	CHSEL1	CHSEL2	
0	0	0	V0A, V0B
0	0	1	V1A, V1B
0	1	0	V2A, V2B
0	1	1	V3A, V3B
1	0	0	V4A, V4B
1	0	1	V5A, V5B
1	1	0	V6A, V6B
1	1	1	V7A, V7B

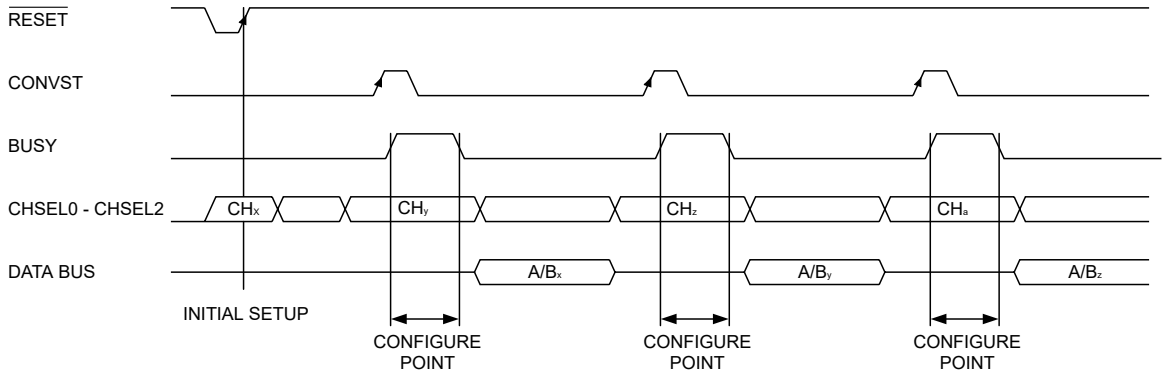


Figure 23. Hardware Mode Channel Conversion Setting

Software Mode

In software mode, the TPAFE51760 allows the selection of channels for conversion through control of the channel register. When the device is powered up or after a reset, the default channels chosen for conversion are Channel V0A and Channel V0B. Users can configure and change these channel selections as needed based on their application requirements.

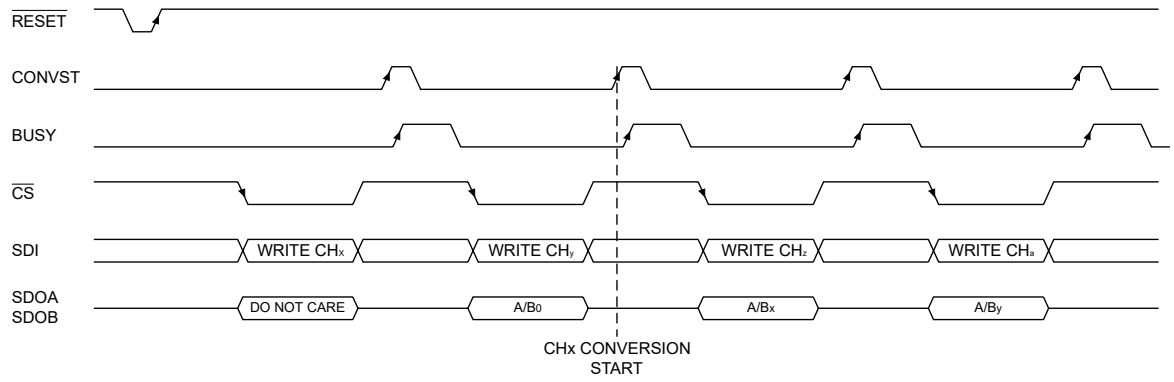


Figure 24. Software Serial Mode Channel Conversion Setting

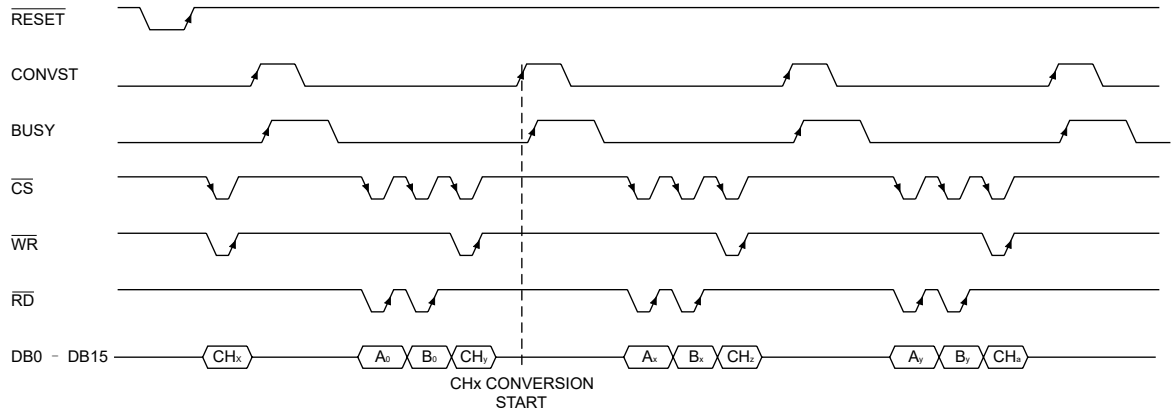


Figure 25. Software Parallel Mode Channel Conversion Setting

Parallel Interface

The parallel interface of the TPAFE51760 is used for reading conversion results and configuring and reading the on-chip registers. To read data from the device using the parallel bus, the SER/$\overline{PAR}$ pin should be tied low. The data is read through the parallel data bus, and controlled by $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$.

Reading Conversion Results

The CONVST signal is used to initiate the conversion process. When there is a low to high transition on the CONVST signal, it triggers the device to start converting the selected inputs. During the conversion process, the BUSY signal goes high to indicate that a conversion is in progress. Once the conversion is complete and the BUSY signal transitions from high to low, this indicates that a conversion result is available and can be read back through the parallel interface.

Data can be read through the parallel interface using the $\overline{CS}$ and $\overline{RD}$ signals. These input signals are internally gated to enable the conversion result to be placed on the data bus. When both $\overline{CS}$ and $\overline{RD}$ are at a logic low level, the data lines (DB15 to DB0) are out of a high-impedance state, allowing the data to be read from the device over the data bus.

The $\overline{CS}$ input signal is used to control the bus state during communication with the TPAFE51760. When the $\overline{CS}$ signal transitions from low to high (rising edge), it sets the data bus into a high-impedance state. Conversely, when the $\overline{CS}$ signal transitions from high to low (falling edge), it takes the data bus out of the high-impedance state. $\overline{CS}$ is a control signal that allows multiple devices to share the same parallel data bus, ensuring that only the selected device communicates on the bus when the $\overline{CS}$ signal is active.

The number of required read operations to read data from the TPAFE51760 depends on the device's configuration. At a minimum, two reads are needed to obtain the conversion results for the simultaneously sampled A and B channels. However, if additional functions like CRC checking, status information, or burst mode are enabled, the number of necessary readbacks will increase accordingly.

The $\overline{RD}$ pin is used to read data from the output conversion results register. When the user applies a sequence of $\overline{RD}$ pulses to the $\overline{RD}$ pin, it clocks the conversion results out from each channel onto the parallel bus, which consists of DB15 to DB0. The first $\overline{RD}$ falling edge after the BUSY signal goes low will clock out the conversion result from Channel A_X, and the subsequent RD falling edge will update the bus with the conversion result from Channel B_X.

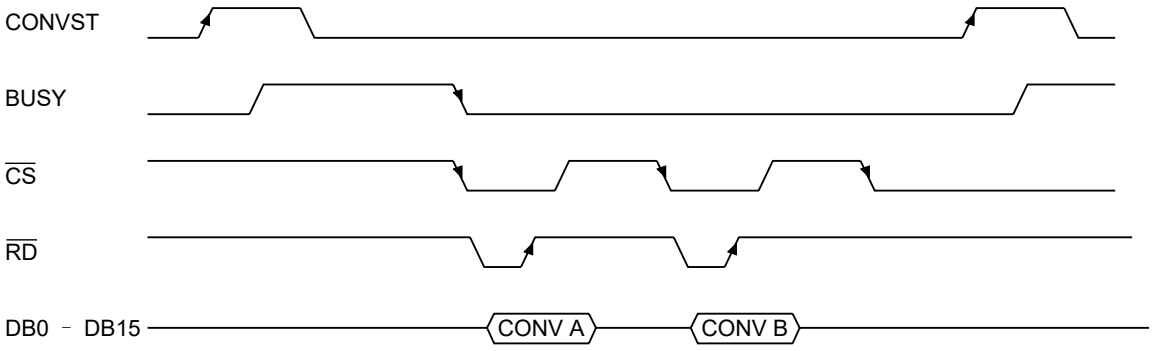


Figure 26. Parallel Interface Conversion Readback

Writing Register Data

In software mode, the user can write to all the read/write registers in the TPAFE51760 over the parallel interface using a register write command. The register writes command is performed by sending a single 16-bit parallel access via the parallel bus, DB15 to DB0 data lines, $\overline{CS}$, and $\overline{WR}$ signals. When writing data to the device, provide the data on DB15 to DB0 inputs, with DB0 being the LSB of the data word. The format for a write command is illustrated below. Bit D15 must be set to 1 to indicate a write command. Bits D14 to D9 contain the register address, and the subsequent nine bits (Bits D8 to D0) contain the data that should be written to the selected register. The data is latched into the device on the rising edge of the $\overline{WR}$ signal.

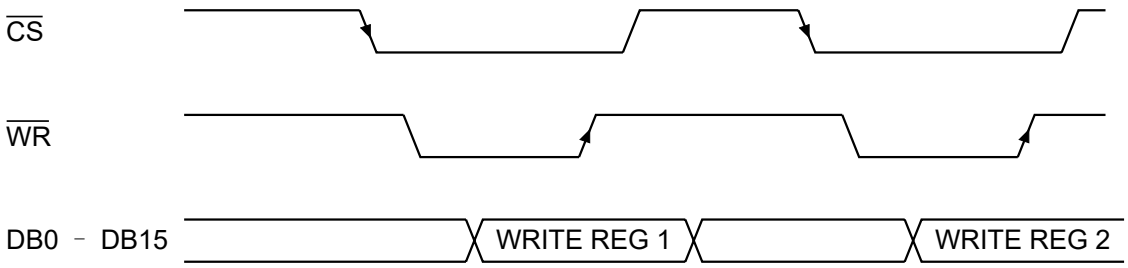


Figure 27. Parallel Interface Register Write

Reading Register Data

In software mode, all the registers in the TPAFE51760 can be read over the parallel interface. To perform a register read, the user first writes the address of the target register, with Bit D15 set to 0 to select a read command and Bits D14 to D9 containing the register address. The subsequent nine bits (Bits D8 to D0) are ignored. The read command is latched into the TPAFE51760 on the rising edge of the $\overline{WR}$ signal, and this latch operation transfers the register data to the output register. Subsequently, the user can read the register data from the device by using a standard read command, and this data will be available on the DB15 to DB0 pins.

Figure 28. Parallel Interface Register Read

Serial Interface

To interface with the TPAFE51760 using the SPI, the user should connect the SER/$\overline{PAR}$ pin to a high logic level. Data transfer is controlled by the $\overline{CS}$ and SCLK signals. The TPAFE51760 offers two serial data output pins, SDOA and SDOB.

When operating in serial 2-wire mode, conversion results from Channel V0A to Channel V7A are available on SDOA, while conversion results from Channel V0B to Channel V7B are present on SDOB. In contrast, in serial 1-wire mode, conversion results from Channel V0B to Channel V7B are interleaved with those from Channel V0A to Channel V7A. To achieve the highest throughput, it is recommended to use the 2-wire mode.

To read data from both SDOA and SDOB pins, the user should connect the $\overline{SER1W}$ pin to a high logic level. If the user wants to read data from SDOA only, tie the $\overline{SER1W}$ pin to a low logic level. The configuration for serial 1-wire or 2-wire mode is established when the device is released from a full reset.

Reading Conversion Results

The CONVST signal is used to initiate the conversion process. When there is a low to high transition on the CONVST signal, it triggers the device to start converting the selected inputs. During the conversion process, the BUSY signal goes high to indicate that a conversion is in progress. Once the conversion is complete and the BUSY signal transitions from high to low, this indicates that a conversion result is available and can be read back through the serial interface.

When the $\overline{CS}$ signal falls from high to low, it takes the data output lines, SDOA and SDOB, out of their three-state condition and allows the reading process to begin. The MSB of the conversion result is then clocked out on the rising edge of the SCLK signal. Subsequent data bits are clocked out on each subsequent rising edge of SCLK, completing the data transfer on both SDOA and SDOB lines. If additional data, such as the status register or data from the sequencer burst mode, is included with the conversion results where multiples of 16 SCLK transfers access data from the device, holding $\overline{CS}$ low throughout the entire data transfer process is necessary to frame the entire data. Alternatively, if only one SDOx line is used, it must be SDOA to access all conversion data. To access both Channel VxA and Channel VxB conversion results on one SDOx line, a total of 32 SCLK cycles is required. Users can frame these 32 SCLK cycles using one $\overline{CS}$ signal, or individually frame each group of 16 SCLK cycles using the $\overline{CS}$ signal. However, using just one SDOx line may reduce the throughput rate.

In serial 1-wire mode, the user should leave the unused SDOB line unconnected. When using SDOA as a single serial data output line, the channel results are output in the following order: VxA followed by VxB. The below figure illustrates a serial readback operation in this mode.

The speed at which data can be read back in serial interface mode depends on several factors, including the SPI frequency, V_{DRIVE} supply voltage, and the capacitance of the load on the SDO line (CLOAD). The spec table provides a summary of the maximum achievable speed under different conditions.

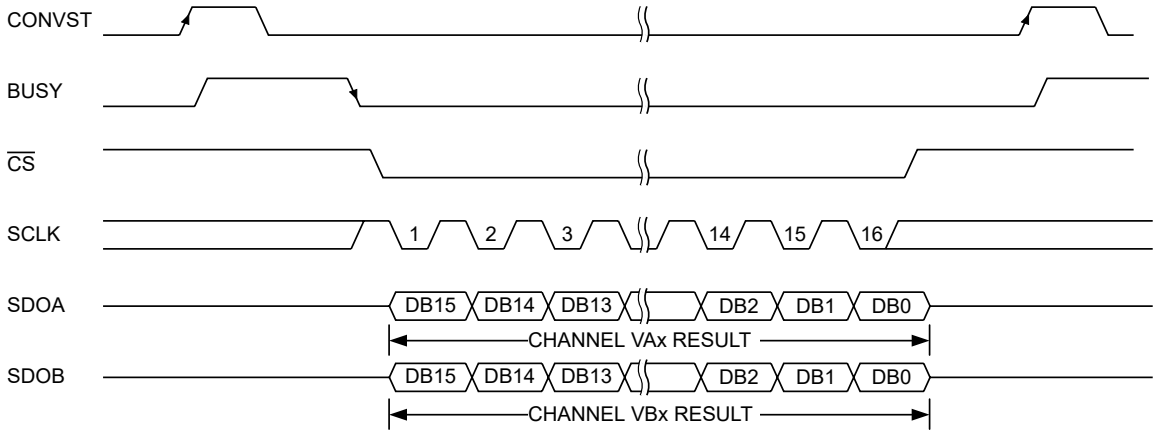


Figure 29. Serial Interface Conversion Results Read, 2-Wire Mode

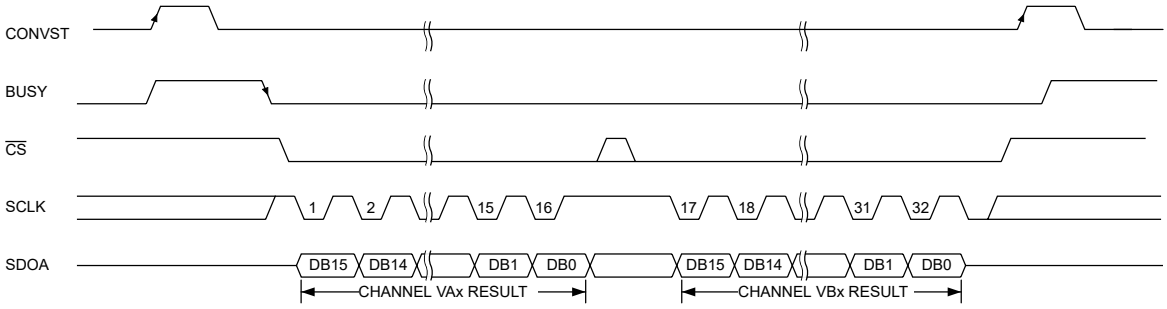


Figure 30. Serial Interface Conversion Results Read, 1-Wire Mode

Writing Register Data

Users can write to all the read/write registers in the TPAFE51760 using the serial interface. To perform a register write command, the user needs to use a single 16-bit SPI access. The format for a write command is shown below. Bit D15 should be set to 1 to select a write command. Bits D14 to D9 are the register address, and the following nine bits (Bits D8 to D0) should contain the data to be written to the selected register.

Table 11. Write Command Configuration

MSB															**LSB**
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W/R	REGADDR[5:0]						Data[8:0]								
1	Register address						Data to write								

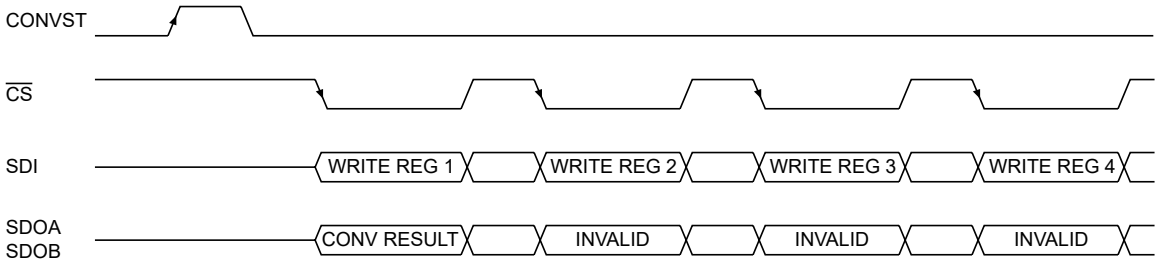


Figure 31. Serial Interface Register Write

Reading Register Data

All the registers in the TPAFE51760 can be read through the serial interface. To perform a register read, the user needs to issue a register read command followed by an additional SPI command, which can be either a valid command or a no operation (NOP). The format for a read command is outlined below. Bit D15 should be set to 0 to select a read command. Bits D14 to D9 are the registered address, and the following nine bits (Bits D8 to D0) are ignored.

Table 12. Read Command Configuration

MSB															**LSB**
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W/R	REGADDR[5:0]						Data[8:0]								
0	Register address						Data to write								

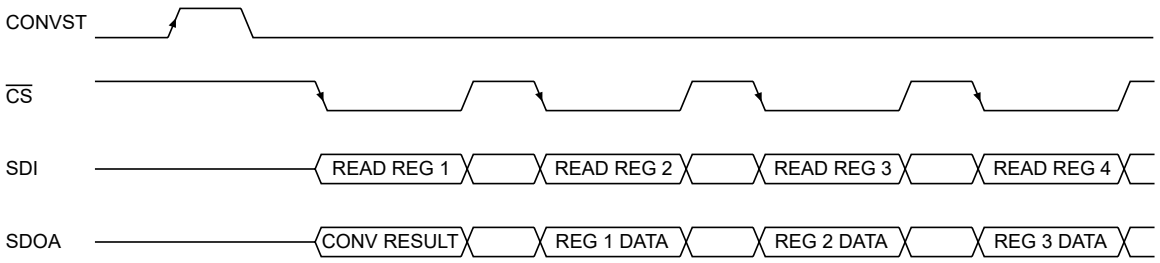


Figure 32. Serial Interface Register Read

Sequencer

The TPAFE51760 incorporates an internal sequencer, which is configurable by the user for different application requirements.

In hardware mode, the sequencer operates sequentially. It always begins the conversion process with Channel V0A and Channel V0B and then proceeds to convert each subsequent channel in sequence, up to the configured end channel.

In software mode, the sequencer offers more flexibility and configurability. It provides a sequencer stack with 32 uniquely configurable sequence steps, enabling the programming of any desired channel order. Moreover, it allows for the pairing of any Channel VxA input with any Channel VxB input or diagnostic channel, providing versatile configuration options.

The sequencer can operate with or without the burst function enabled. When the burst function is enabled, only one CONVST pulse is needed to convert every channel in a sequence. However, when the burst mode is disabled, one CONVST pulse is required for each conversion step in the sequence.

Hardware Mode Sequencer

In hardware mode, the operation of the sequencer is controlled by the SEQEN (Sequencer Enable) pin and the CHSELx pins. The sequencer can be enabled or disabled when the device is released from a full reset. The state of the SEQEN pin at the time when the $\overline{\text{RESET}}$ pin is released determines whether the sequencer is enabled or disabled. Once the $\overline{\text{RESET}}$ pin is released, the functionality is set, and a full reset via the $\overline{\text{RESET}}$ pin is necessary to exit this mode and configure an alternative setting.

Table 13. Hardware Mode Sequencer Configuration

SEQEN	Interface Mode
0	Sequencer disabled
1	Sequencer enabled

When the sequencer is enabled, the specific channels to be included in the conversion sequence are determined by the logic levels of the CHSELx pins. The initial channel configuration for the sequence is determined by the state of the CHSELx pins at the moment the $\overline{\text{RESET}}$ pin is released. To change the selection of channels for conversion during ongoing operation, the user must set the CHSELx pins to the desired configuration before the current conversion sequence is complete, and this configuration will take effect in the subsequent sequence.

Table 14. CHSELx Pin Decoding Sequencer

Channel Selection Input Pin			Analog Input Channels for Sequential Conversion
CHSEL0	CHSEL1	CHSEL2	
0	0	0	V0x only
0	0	1	V0x to V1x
0	1	0	V0x to V2x
0	1	1	V0x to V3x
1	0	0	V0x to V4x
1	0	1	V0x to V5x
1	1	0	V0x to V6x
1	1	1	V0x to V7x

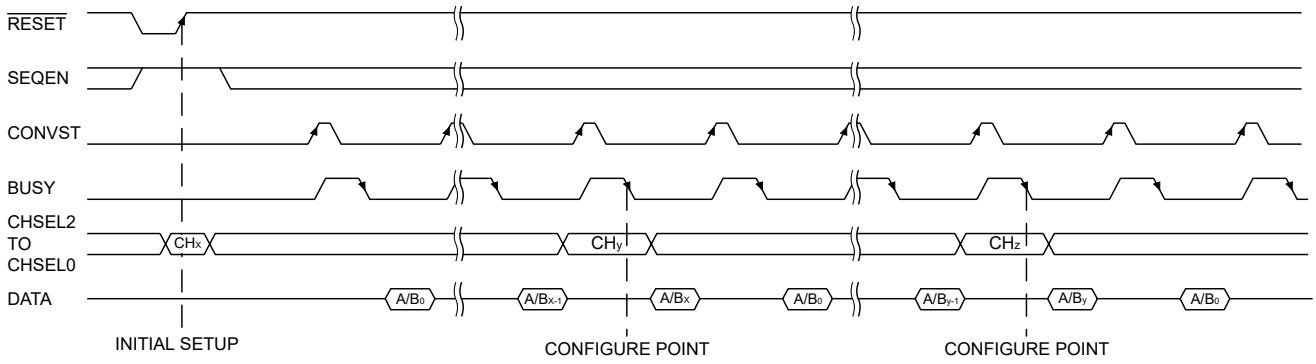


Figure 33. Hardware Mode Sequencer Configuration

Software Mode Sequencer

In software mode, the TPAFE51760 features a highly versatile 32-layer sequencer stack. Users can customize the behavior of the sequencer by programming the configuration register and sequencer stack registers through either the parallel or serial interface.

In software mode, each step in the sequencer stack can be fully customized. Users can pair any input from Channel VxA with any input from Channel VxB, or select any diagnostic channel for conversion. The sequencer depth, or the number of steps in the sequence, can be configured from 1 to 32 layers. To set the sequencer depth, set the SSRENx bit in the sequencer stack register corresponding to the last step configured. To select the channels for conversion in each step, users can program the ASELx and BSELx bits in the sequence stack registers according to the requirements. To activate the sequencer in software mode, set the SEQEN bit in the configuration register to 1.

To configure and enable the sequencer in software mode, follow the procedure outlined below:

1. Configure the analog input range for the required analog input channels.
2. Program the sequencer stack registers to select the channels for the sequence.
3. Set the SSRENx bit in the last required sequence step.
4. Set the SEQEN bit in the configuration register.
5. Provide a dummy CONVST pulse.
6. Cycle through CONVST pulses and conversion reads to step through each element of the sequencer stack.

The sequencer will automatically restart from the first element in the sequencer stack with the next CONVST pulse. After a partial reset, the sequencer pointer is repositioned to the first layer of the stack, but the register-programmed values remain unchanged.

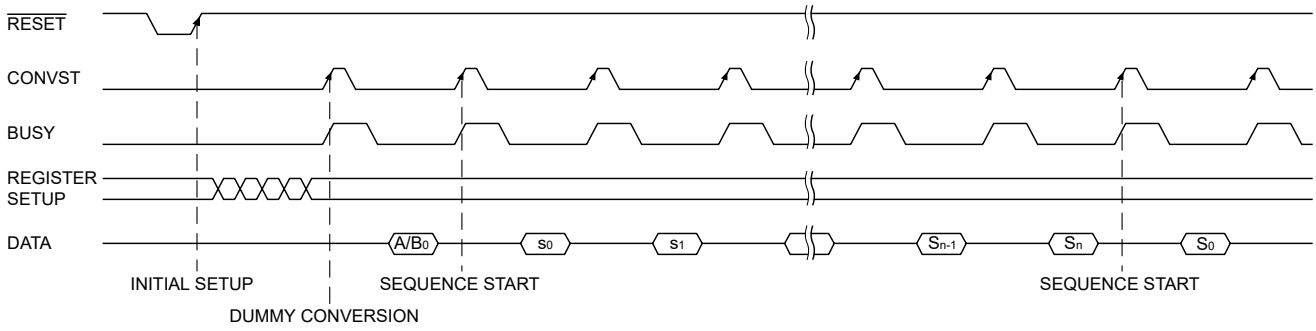


Figure 34. Software Mode Sequencer Configuration

Burst Sequencer

Burst mode in the TPAFE51760 allows user to convert multiple channels in a sequence without generating a CONVST pulse for each step. Instead, a single CONVST pulse initiates conversions for all the channels in the sequence.

The burst sequencer is an additional capability that operates alongside the standard sequencer. When the burst function is activated, a single CONVST pulse triggers the conversion of all the channels set in the sequencer. This eliminates the need to generate a separate CONVST pulse for each step in a sequence of conversions, which would be necessary if the burst function were disabled.

The setup for the burst function differs based on the chosen mode of operation, whether it's hardware or software mode. Once configured, the burst sequence starts when CONVST experiences a rising edge. The BUSY pin will go high to signal that a conversion is active. BUSY will stay high until all conversions in the sequence have finished. After BUSY transitions low, the conversion results can be accessed for readback.

The number of data reads needed to read all the data in the burst sequence depends on the length of the sequence that has been configured. The conversion results are presented on the data bus (whether parallel or serial) in the same order as they were programmed in the sequence.

The throughput rate of the TPAFE51760 is limited in burst mode and depends on the length of the sequence. Each channel pair in the sequence requires an acquisition, conversion, and readback time. The time taken to complete a sequence with a number of channel pairs, N, can be estimated using the following formula:

$$t_{BURST} = (t_{CONV} + 25\,ns) + (N - 1)\left(t_{ACQ\_BURST} + t_{CONV}\right) + N(t_{RB}) \quad (2)$$

t_{CONV} is the typical conversion time.

t_{ACQ_BURST} is burst mode typical acquisition time.

t_{RB} is the time required to read back the conversion results in either serial 1-wire, serial 2-wire, or parallel mode.

Hardware Mode Burst

In hardware mode, burst mode is enabled by setting the BURST pin to 1. Additionally, the SEQEN pin must also be set to 1 to enable the sequencer in burst mode. The burst sequencer is controlled by the BURST, SEQEN, and CHSELx pins. The burst sequencer can be enabled or disabled when the device is released from full reset. The logic levels of the SEQEN pin and the BURST pin when the $\overline{\text{RESET}}$ pin is released determine whether the burst sequencer is enabled or disabled. Once the $\overline{\text{RESET}}$ pin is released, the configuration is fixed, and to change it, a full reset via the $\overline{\text{RESET}}$ pin is necessary to exit the burst sequencer function and set up an alternative configuration.

When the burst sequencer is enabled in hardware mode, the channels selected for conversion in the burst sequence are determined by the logic levels of the CHSELx pins. The initial channel settings for the burst sequence are established based on the CHSELx pins' status at the time $\overline{\text{RESET}}$ is released. If the user needs to reconfigure the channels chosen for conversion after a reset, adjust the CHSELx pins to the desired settings during the next BUSY pulse.

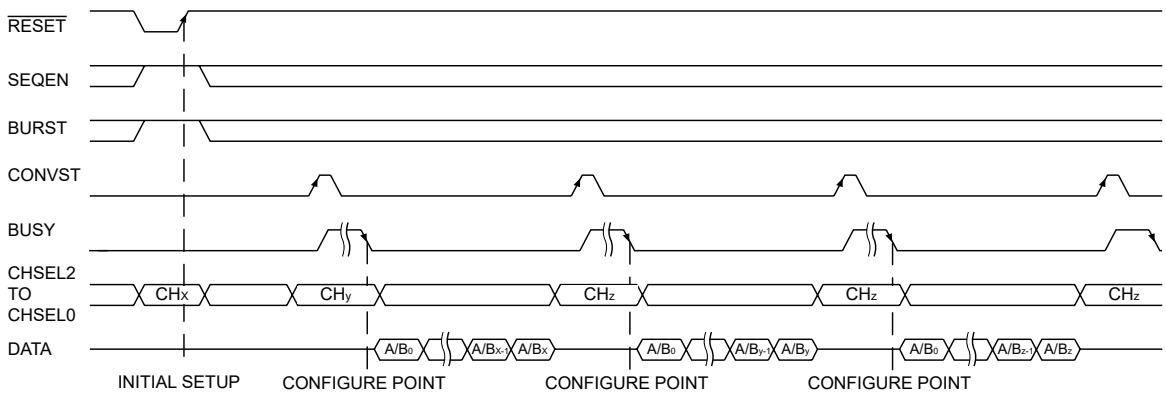


Figure 35. BURST Sequencer, Hardware Mode

Software Mode Burst

To enable the burst function in software mode, set the BURST bit in the configuration register to 1. This should be done in conjunction with configuring the sequencer using the SEQEN bit, as explained in the Software Mode Sequencer section.

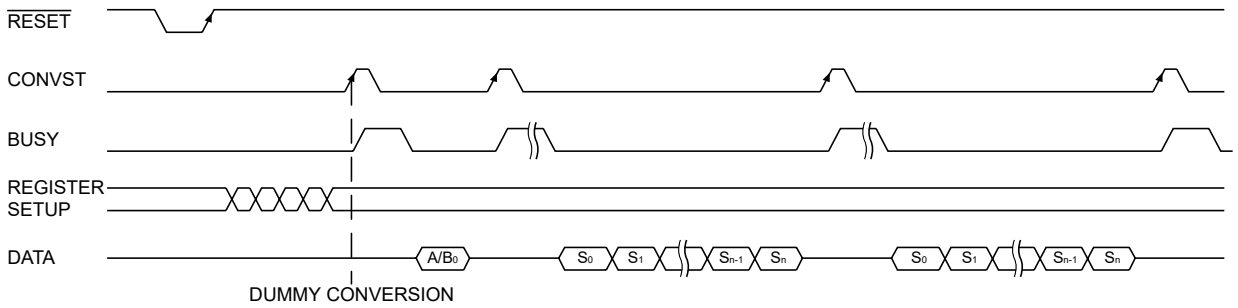


Figure 36. BURST Sequencer, Software Mode

Diagnostics

Diagnostic Channels

Besides the 16 analog inputs, VxA and VxB, the TPAFE51760 also can be used to diagnose $V_{CC}$and the analog ALDO voltage. To select diagnostic channels for conversion, the channel register needs to be programmed with the corresponding channel identifier. While diagnostic channels can be included in the sequencer stack in software mode, it's important to note that they offer accurate readings only at throughput rates below 250 kSPS.

The diagnostic results is measured as the following functions:

$$V_{CC}\,(CODE) = \frac{\frac{V_{CC}}{2} \times 65536}{V_{REF}} - 32768$$

$$V_{ALDO}\,(CODE) = \frac{\frac{V_{ALDO}}{2} \times 65536}{V_{REF}} - 32768$$

Interface Self Test

To test the integrity of the digital interface, the user can choose the communication self-test channel in the channel register.

By selecting the communication self-test for conversion, the conversion result register is set to a predetermined fixed output. When reading the conversion code, the output for ADC A is Code 0xAAAA, and for ADC B, it is Code 0x5555.

CRC

The TPAFE51760 ADC includes a cyclic redundancy check (CRC) checksum mode to enhance interface robustness by detecting data errors. This feature is applicable in both software (serial and parallel) mode and hardware (serial only) mode, but it is not available in hardware parallel mode. When the CRC feature is enabled, the status register becomes active, and the CRC result is stored within this status register. Enabling the status register will also activate the CRC feature.

In hardware mode, the CRC feature of the TPAFE51760 is controlled by the CRCEN pin. The CRC feature is enabled or disabled when the device is released from full reset. The logic level of the CRCEN pin at the time the $\overline{\text{RESET}}$ pin is released determines whether the CRC feature is enabled or disabled. To enable the CRC feature, set the CRCEN pin to high (1). Once the $\overline{\text{RESET}}$ pin is released, the function becomes fixed, and a full reset via the $\overline{\text{RESET}}$ pin is required to disable the function or set up an alternative configuration. For more details, refer to the Reset Functionality section. When the CRC feature is enabled, the CRC result is appended to the conversion result. This appended result consists of a 16-bit word: the first eight bits contain the channel ID of the last channel pair converted, and the last eight bits are the CRC result. This result is accessed via an extra read command.

In software mode, enabling the CRC function involves setting either the CRCEN or STATUSEN bit within the configuration register to 1 (refer to the corresponding section for details).

If the CRC function is enabled, a CRC is calculated on the conversion results for Channel VxA and Channel VxB. This CRC is then transferred on the serial or parallel interface following the transmission of the conversion results, depending on the device configuration. The Hamming distance, which indicates the minimum number of bit changes required to change one valid code into another, varies based on the number of bits in the conversion result. For conversions with 119 or fewer bits, the Hamming distance is 4, ensuring robust error detection. For conversions with more than 119 bits, the Hamming distance is 1, which guarantees that any single-bit error will be detected.

The following is a pseudocode description of how the CRC is implemented in the TPAFE51760:

crc = 8'b0;

i = 0;

x = number of conversion channel pairs;

for (i=0, i<x, i++) begin

crc1 = crc_out(An,Crc);

crc = crc_out(Bn,Crc1);

i = i +1;

end

where the function crc_out(data, crc) is

crc_out[0] = data[14] ^ data[12] ^ data[8] ^ data[7] ^ data[6] ^ data[0] ^ crc[0] ^ crc[4] ^ crc[6];

crc_out[1] = data[15] ^ data[14] ^ data[13] ^ data[12] ^ data[9] ^ data[6] ^ data[1] ^ data[0] ^ crc[1] ^ crc[4] ^ crc[5] ^ crc[6] ^ crc[7];

crc_out[2] = data[15] ^ data[13] ^ data[12] ^ data[10] ^ data[8] ^ data[6] ^ data[2] ^ data[1] ^ data[0] ^ crc[0] ^ crc[2] ^ crc[4] ^ crc[5] ^ crc[7];

crc_out[3] = data[14] ^ data[13] ^ data[11] ^ data[9] ^ data[7] ^ data[3] ^ data[2] ^ data[1] ^ crc[1] ^ crc[3] ^ crc[5] ^ crc[6];

crc_out[4] = data[15] ^ data[14] ^ data[12] ^ data[10] ^ data[8] ^ data[4] ^ data[3] ^ data[2] ^ crc[0] ^ crc[2] ^ crc[4] ^ crc[6] ^ crc[7];

crc_out[5] = data[15] ^ data[13] ^ data[11] ^ data[9] ^ data[5] ^ data[4] ^ data[3] ^ crc[1] ^ crc[3] ^ crc[5] ^ crc[7];

crc_out[6] = data[14] ^ data[12] ^ data[10] ^ data[6] ^ data[5] ^ data[4] ^ crc[2] ^ crc[4] ^ crc[6];

crc_out[7] = data[15] ^ data[13] ^ data[11] ^ data[7] ^ data[6] ^ data[5] ^ crc[3] ^ crc[5] ^ crc[7];

The initial CRC word used by the TPAFE51760 is an 8-bit word set to zero. To calculate the CRC word for a conversion result (A_N), an XOR operation is performed as described earlier. This CRC word (crc1) is then used as the initial value for calculating the CRC word (CRC) for the next conversion result (B_N). This process is repeated cyclically for each pair of converted channels.

Depending on the mode of operation of the TPAFE51760, the status register value is appended to the conversion data and can be read out via an extra read command over the serial or parallel interface. To verify data integrity, the user can repeat the XOR calculation described in the preceding code for the received conversion results and compare the calculated CRC word with the received CRC word. For detailed information on how the CRC word is appended to the data in each mode of operation, refer to the figure below.

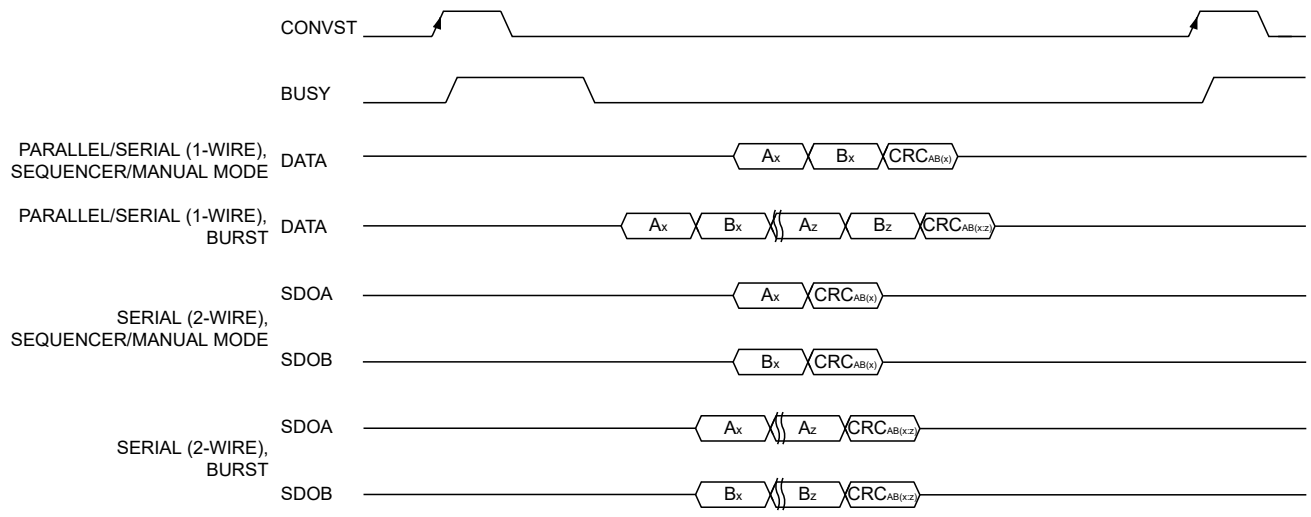


Figure 37. CRC Readback for All Modes

Register Summary

The TPAFE51760 provides a total of six read/write registers for configuring the device in software mode. Additionally, it offers 32 sequencer stack registers for programming the highly configurable on-chip sequencer, along with a read-only status register. The status register contains information about the previously converted channel pair and the CRC result.

Table 15. Register Summary

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x02	Configuration register	[15:8]	Addressing							Reserved	0x0000	R/W
		[7:0]	SDEF	BURSTEN	SEQEN	OS			STATUSEN	CRCEN		
0x03	Channel register	[15:8]	Addressing							Reserved	0x0000	R/W
		[7:0]	CHB				CHA					
0x04	Input Range Register A1	[15:8]	Addressing							Reserved	0x00FF	R/W
		[7:0]	V3A		V2A		V1A		V0A			
0x05	Input Range Register A2	[15:8]	Addressing							Reserved	0x00FF	R/W
		[7:0]	V7A		V6A		V5A		V4A			
0x06	Input Range Register B1	[15:8]	Addressing							Reserved	0x00FF	R/W
		[7:0]	V3B		V2B		VB1		V0B			
0x07	Input Range Register B2	[15:8]	Addressing							Reserved	0x00FF	R/W
		[7:0]	V7B		V6B		VB5		V4B			
0x20 to 0x3F	Sequencer Stack Registers[0:31]	[15:8]	Addressing							SSRENx	0x0000[1]	R/W
		[7:0]	BSELx				ASELx					
N/A	Status register	[15:8]	A[3:0]				B[3:0]				N/A	R
		[7:0]	CRC[7:0]									

(1) After a full or partial rest is issued, the sequencer stack register is reinitialized to cycle through Channel V0A and Channel V0B to Channel V7A and Channel V7B. The remaining 24 layers of the stack are reinitialized to 0x0.

Addressing Registers

The seven most significant bits (MSBs) sent to the device are used to decode the selected register. These MSBs consist of the register address (REGADDR) represented by Bits[5:0], along with the read/write bit. The register address bits specify which on-chip register is being accessed, while the read/write bit determines whether the remaining nine bits of data on the DB10/SDI lines will be written to the selected register. If the read/write bit is set to 1, the nine bits of data will be loaded into the register identified by the register select bits. Conversely, if the read/write bit is set to 0, the command is interpreted as a read request, and the data from the addressed register will be available for reading during the subsequent read operation.

Table 16. Addressing Register

Bits	Mnemonic	Description
D15	W/R	If a 1 is written to this bit, Bits[D8:D0] of this register is written to the register specified by REGADDR[5:0]. Alternatively, if a 0 is written, the next operation is a read from the designated register.
D14	REGADDR[5]	If a 1 is written to this bit, the contents of REGADDR[4:0] specifies the 32 sequencer stack registers. Alternatively, if a 0 is written to this bit, a register is selected as defined by REGADDR[4:0].
[D13:D9]	REGADDR[4:0]	When W/R =1, the contents of REGADDR[4:0] determine the register for selection as follows: 00001: reserved. 00010: selects the configuration register. 00011: selects the channel register. 00100: selects Input Range Register A1. 00101: selects Input Range Register A2. 00110: selects Input Range Register B1. 00111: selects Input Range Register B2. 01000: selects the status register When W/R = 0, and REGADDR[4:0] contains 00000, the conversion codes are read.
[D8:D0]	DATA[8:0]	These bits are written into the corresponding register specified by Bits REGADDR[5:0]. See the following sections for detailed descriptions of each register.

Configuration Register

The configuration register is used in software mode, the user could configure it to customize the ADC's main functions, like the sequencer, burst mode, oversampling, and CRC options.

Address: 0x02, Reset: 0x0000, Name: Configuration Register

Table 17. Bit Descriptions for the Configuration Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Addressing	0	Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	RW
8	RESERVED		Reserved.	0x0	R/W
7	SDEF	0	Self-detector error flag. Test passed. The TPAFE51760 has configured itself successfully after power-up.	N/A	R
		1	Test failed. An issue was detected during the device configuration. A reset is required.		
6	BURSTEN	0	Burst mode enable. Burst mode is disabled. Each channel pair to be converted requires a CNVST pulse.	0x0	RW
		1	A single CNVST pulse converts every channel pair programmed in the 32-layer sequencer stack registers up to and including the layer defined by the SSRENx bit. See the Software Mode Sequencer section and the Software Mode Burst section for further details.		
5	SEQEN	0	Channel sequencer enabled. The channel sequencer is disabled.	0x0	RW
		1	The channel sequencer is enabled.		
[4:2]	OS		Oversampling (OS) ratio, samples per channel.	0x0	RW
		000	Oversampling disabled.		
		001	Oversampling enabled, OSR = 2.		
		010	Oversampling enabled, OSR = 4.		
		011	Oversampling enabled, OSR = 8.		
		100	Oversampling enabled, OSR = 16.		
		101	Oversampling enabled, OSR = 32.		
		110	Oversampling enabled, OSR = 64.		
		111	Oversampling enabled, OSR = 128.		
1	STATUSEN	0	Status register output enables. The status register is not read out when reading the conversion result.	0x0	RW
		1	The status register is read out at the end of all the conversion words (including the self-test channel if enabled in sequencer mode) if all the selected channels are read out. The CRC result is included in the last eight bits.		
0	CRCEN		CRC enable. The STATUSEN and CRCEN bits have identical functionality.	0x0	RW

Channel Register

In software manual mode, the channel register selects the input channel or self-test channel for the next conversion.

Address: 0x03, Reset: 0x0000, Name: Channel Register

Table 18. Bit Descriptions for the Channel Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
8	RESERVED		Reserved.	0x0	R/W
[7:4]	CHB		Channel selection bits for ADC B channels.	0x0	R/W
		0000	V0A/V0B.		
		0001	V1A/V1B.		
		0010	V2A/V2B.		
		0011	V3A/V3B.		
		0100	V4A/V4B.		
		0101	V5A/V5B.		
		0110	V6A/V6B.		
		0111	V7A/V7B.		
		1000	V_{CC}.		
		1001	ALDO.		
		1010	Reserved.		
		1011	Set the dedicated bits for digital interface communication self test function. When conversion codes are read, Code 0xAAAA is read out as the conversion code of Channel A, and Code 0x5555 is output as the conversion code of Channel B.		
		1100	Reserved.		
[3:0]	CHA		Channel selection bits for ADC A Channels. Settings are the same as for ADC B.	0x0	R/W

Input Range Registers

The Input Range Register A1 and Input Range Register A2 allow user to choose one of three available input ranges (±10 V, ±5 V, or ±2.5 V) for analog input channels V0A to V7A. Similarly, the Input Range Register B1 and Input Range Register B2 enable the selection of one of the three possible input ranges (±10 V, ±5 V, or ±2.5 V) for analog input channels V0B to V7B.

Input Range Register A1

Address: 0x04, Reset: 0x00FF, Name: Input Range Register A1

Table 19. Bit Descriptions for Input Range Register A1

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
8	RESERVED		Reserved.	0x0	R/W
[7:6]	V3A		V3A voltage range selection.	0x3	R/W
		00	V3A ± 10 V.		
		01	V3A ± 2.5 V.		
		10	V3A ± 5 V.		
		11	V3A ± 10 V.		
[5:4]	V2A		V2A voltage range selection.	0x3	R/W
		00	V2A ± 10 V.		
		01	V2A ± 2.5 V.		
		10	V2A ± 5 V.		
		11	V2A ± 10 V.		
[3:2]	V1A		V1A voltage range selection.	0x3	R/W
		00	V1A ± 10 V.		
		01	V1A ± 2.5 V.		
		10	V1A ± 5 V.		
		11	V1A ± 10 V.		
[1:0]	V0A		V0A voltage range selection.	0x3	R/W
		00	V0A ± 10 V.		
		01	V0A ± 2.5 V.		
		10	V0A ± 5 V.		
		11	V0A ± 10 V.		

Input Range Register A2

Address: 0x05, Reset: 0x00FF, Name: Input Range Register A2

Table 20. Bit Descriptions for Input Range Register A2

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
8	RESERVED		Reserved.	0x0	R/W
[7:6]	V7A		V7A voltage range selection.	0x3	R/W
		00	V7A ± 10 V.		
		01	V7A ± 2.5 V.		
		10	V7A ± 5 V.		
		11	V7A ± 10 V.		
[5:4]	V6A		V6A voltage range selection.	0x3	R/W
		00	V6A ± 10 V.		
		01	V6A ± 2.5 V.		
		10	V6A ± 5 V.		
		11	V6A ± 10 V.		
[3:2]	V5A		V5A voltage range selection.	0x3	R/W
		00	V5A ± 10 V.		
		01	V5A ± 2.5 V.		
		10	V5A ± 5 V.		
		11	V5A ± 10 V.		
[1:0]	V4A		V4A voltage range selection.	0x3	R/W
		00	V4A ± 10 V.		
		01	V4A ± 2.5 V.		
		10	V4A ± 5 V.		
		11	V4A ± 10 V.		

Input Range Register B1

Address: 0x06, Reset: 0x00FF, Name: Input Range Register B1

Table 21. Bit Descriptions for Input Range Register B1

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
8	RESERVED		Reserved.	0x0	R/W
[7:6]	V3B		V3B voltage range selection.	0x3	R/W
		00	V3B ± 10 V.		
		01	V3B ± 2.5 V.		
		10	V3B ± 5 V.		
		11	V3B ± 10 V.		
[5:4]	V2B		V2B voltage range selection.	0x3	R/W
		00	V2B ± 10 V.		
		01	V2B ± 2.5 V.		
		10	V2B ± 5 V.		
		11	V2B ± 10 V.		
[3:2]	V1B		V1B voltage range selection.	0x3	R/W
		00	V1B ± 10 V.		
		01	V1B ± 2.5 V.		
		10	V1B ± 5 V.		
		11	V1B ± 10 V.		
[1:0]	V0B		V0B voltage range selection.	0x3	R/W
		00	V0B ± 10 V.		
		01	V0B ± 2.5 V.		
		10	V0B ± 5 V.		
		11	V0B ± 10 V.		

Input Range Register B2

Address: 0x07, Reset: 0x00FF, Name: Input Range Register B2

Table 22. Bit Descriptions for Input Range Register B2

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
8	RESERVED		Reserved.	0x0	R/W
[7:6]	V7B		V7B voltage range selection.	0x3	R/W
		00	V7B ± 10 V.		
		01	V7B ± 2.5 V.		
		10	V7B ± 5 V.		
		11	V7B ± 10 V.		
[5:4]	V6B		V6B voltage range selection.	0x3	R/W
		00	V6B ± 10 V.		
		01	V6B ± 2.5 V.		
		10	V6B ± 5 V.		
		11	V6B ± 10 V.		
[3:2]	V5B		V5B voltage range selection.	0x3	R/W
		00	V5B ± 10 V.		
		01	V5B ± 2.5 V.		
		10	V5B ± 5 V.		
		11	V5B ± 10 V.		
[1:0]	V4B		V4B voltage range selection.	0x3	R/W
		00	V4B ± 10 V.		
		01	V4B ± 2.5 V.		
		10	V4B ± 5 V.		
		11	V4B ± 10 V.		

Sequencer Stack Registers

The channel register determines the next channel to be converted, whether it's a diagnostic channel or a pair of analog input channels. However, for sampling multiple analog input channels efficiently, the TPAFE51760 provides 32 sequencer stack registers as a practical solution. When the REGADDR5 bit register is set to 1, REGADDR[4:0] specifies one of these 32 sequencer stack registers. Within each sequencer stack register, the user can configure a pair of analog inputs to be sampled simultaneously.

The sequence structure is organized as a stack, with each row representing two channels that are converted simultaneously. The sequence starts with Sequencer Stack Register 1 and progresses through to Sequencer Stack Register 32. If Bit D8, which is the enable bit (SSRENx), is set to 1 within a sequencer stack register, the sequence concludes with the pair of analog inputs defined by that register. It then returns to the first sequencer stack register and begins the cycle again. By default, the sequencer stack registers are configured to cycle through Channel V0A and Channel V0B to Channel V7A and Channel V7B. Following a full or partial reset, the sequencer stack registers reset and resume cycling through Channel V0A and Channel V0B to Channel V7A and Channel V7B.

Address: 0x20 to 0x3F, Reset: 0x0000, Name: Sequencer Stack Registers[0:31]

Table 23. Bit Descriptions for Sequencer Stack Registers[0:31]

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
8	SSREN[0:31]		Setting this bit to 0 instructs the ADC to move to the next layer of the sequencer stack after converting the present channel pair. Setting this bit to 1 defines that layer of the sequencer stack as the final layer in the sequence. Thereafter, the sequencer loops back to the first layer of the stack.	0x0	R/W
[7:4]	BSEL[0:31]		Channel selection bits for ADC B channels	0x0[1]	R/W
		0000	V0B.		
		0001	V1B.		
		0010	V2B.		
		0011	V3B.		
		0100	V4B.		
		0101	V5B.		
		0110	V6B.		
		0111	V7B.		
		1000	V_{CC}.		
		1001	ALDO.		
		1010	Reserved.		
		1011	Set the dedicated bits for the digital interface communication self-test function. When conversion codes are read, Code 0xAAAA is read out as the conversion code of Channel A, and Code 0x5555 is output as the conversion code of Channel B.		
		1100	Reserved.		
[3:0]	ASEL[0:31]		Channel selection bits for ADC A channels. Settings are the same as for ADC B.	0x0[1]	R/W

(1) After a full or partial reset is issued, the sequencer stack register is reinitialized to cycle through Channel V0A and Channel V0B to Channel V7A and Channel V7B. The remaining 24 layers of the stack are reinitialized to 0x0.

Status Register

The status register is a 16-bit register that can only be read and not written to. If either the STATUSEN bit or the CRCEN bit in the configuration register is set to Logic 1, the status register is read out after all conversion words for the chosen channels. This includes the self-test channel if it is enabled in sequencer mode.

Table 24. Status Register

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A[3:0]				B[3:0]				CRC[7:0]							

Table 25. Bit Descriptions for Status Register

Bit	Bit Name	Settings	Description	Reset	Access
[D15:D12]	A[3:0]		Channel index for previous conversion result on Channel A.	N/A	R
[D11:D8]	B[3:0]		Channel index for previous conversion result on Channel B.	N/A	R
[D7:D0]	CRC[7:0]		CRC calculation for the previous conversion result(s). Refer to the CRC section for further details.	N/A	R

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

Functionality Overview

The TPAFE51760 offers two primary modes of operation: hardware mode and software mode. Furthermore, these modes can be complemented with either a serial or parallel communications interface. Depending on the chosen mode of operation and interface, certain functionalities may be limited or restricted. While both software serial and software parallel modes provide full functionality, hardware serial and hardware parallel modes offer more limited functionality.

Functionality	Operation Mode			
	Software Mode, HW_RNGSELx = 00		Hardware Mode, HW_RNGSELx ≠ 00	
	Serial, SER/$\overline{\text{PAR}}$ = 1	Serial, SER/$\overline{\text{PAR}}$ = 0	Serial, SER/$\overline{\text{PAR}}$ = 1	Serial, SER/$\overline{\text{PAR}}$ = 0
Internal/External Reference	Yes	Yes	Yes	Yes
Selectable Analog Input Ranges				
Individual Channel Configuration	Yes	Yes	No	No
Common Channel Configuration	No	No	Yes	Yes
Sequential Sequencer	Yes	Yes	Yes	Yes
Fully Configurable Sequencer	Yes	Yes	No	No
Burst Mode	Yes	Yes	Yes	Yes
On-Chip Oversampling	Yes	Yes	Yes	No
CRC	Yes	Yes	Yes	No
Diagnostic Channel Conversion	Yes	Yes	No	No
Hardware Reset	Yes	Yes	Yes	Yes
Serial 1-Wire Mode	Yes	No	Yes	No
Serial 2-Wire Mode	Yes	No	Yes	No
Register Access	Yes	Yes	No	No

Typical Connection

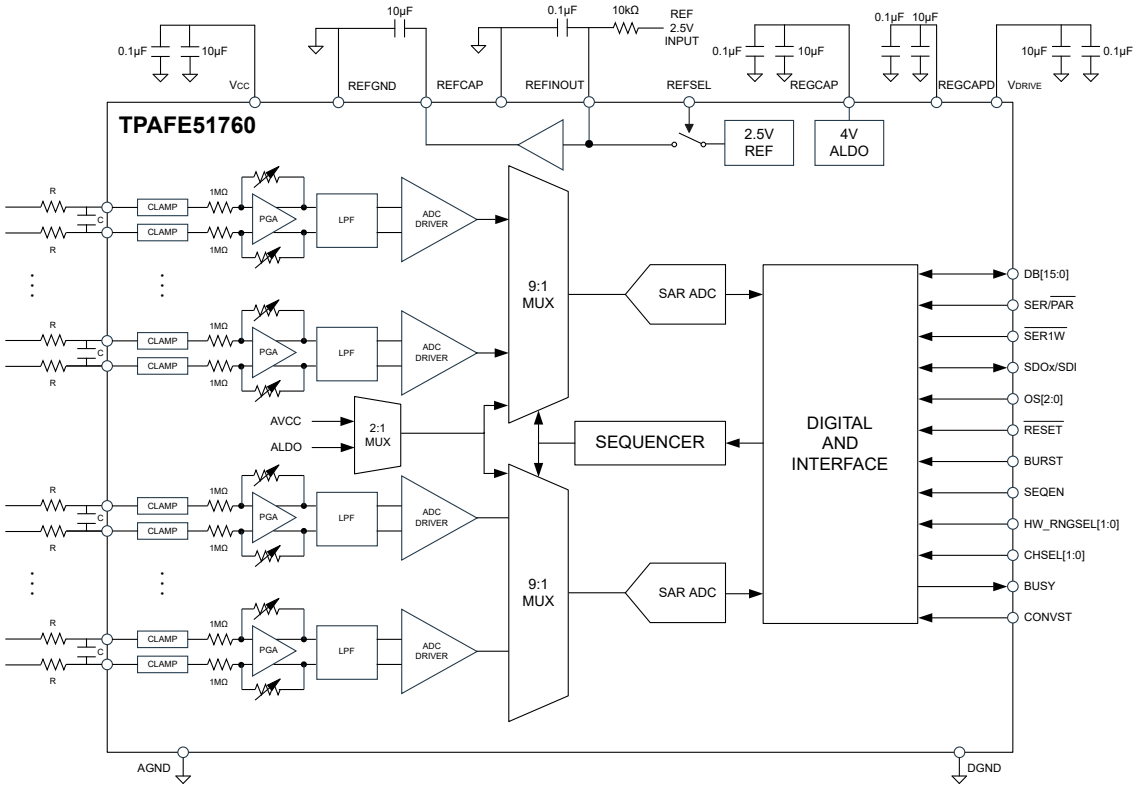


Figure 38. Typical External Connections

Layout

Layout Example

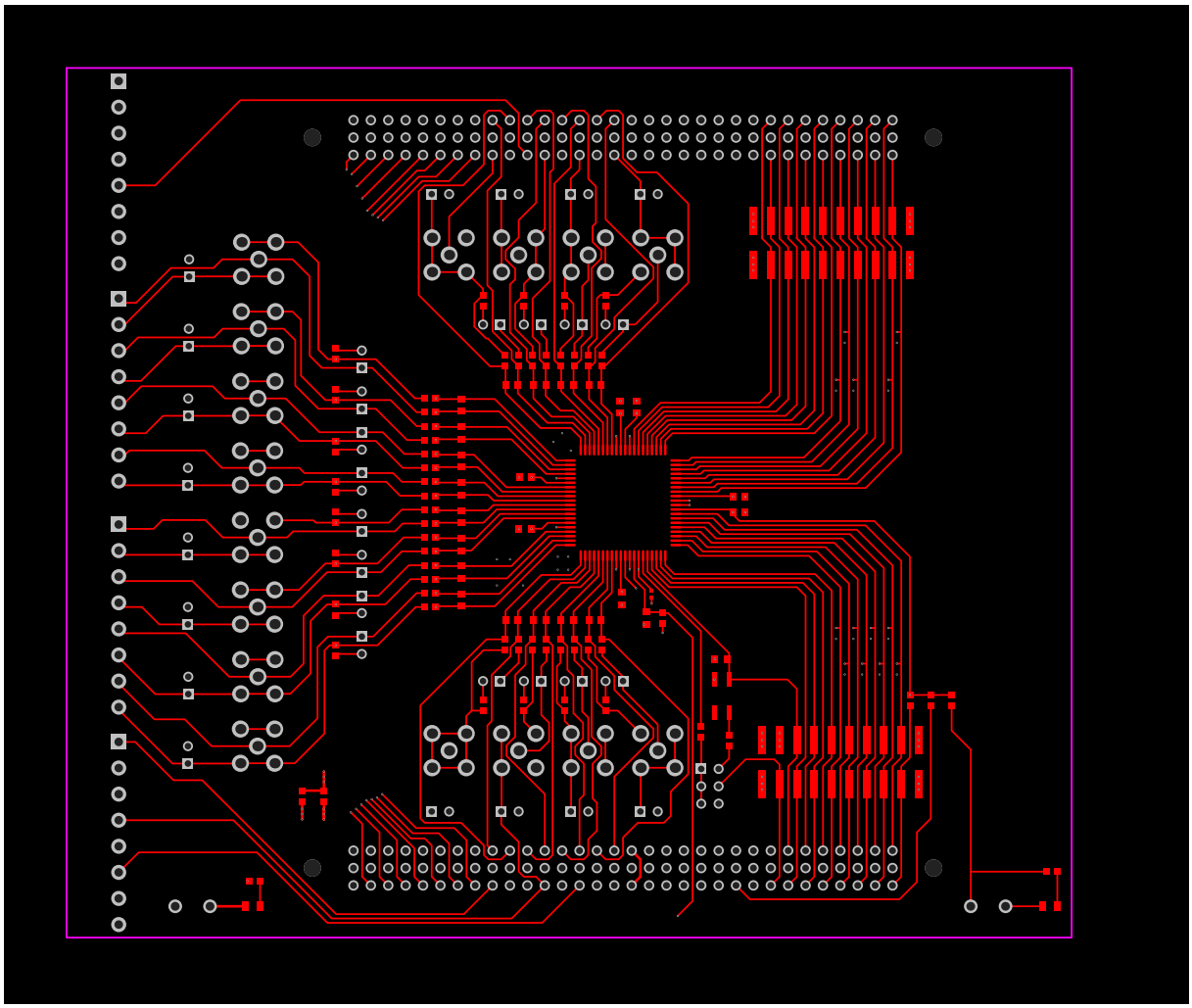


Figure 39. Top Layer Layout Example

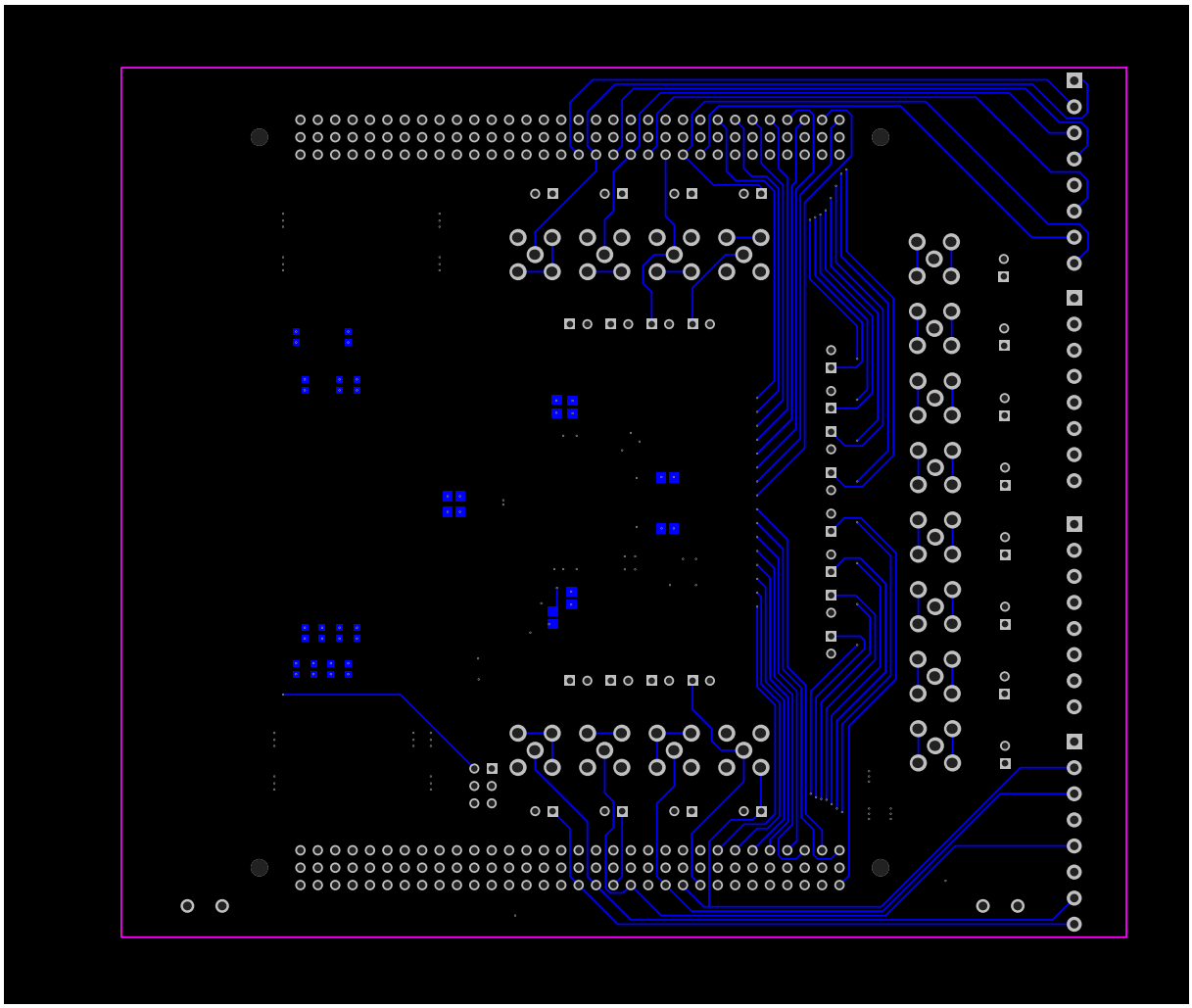
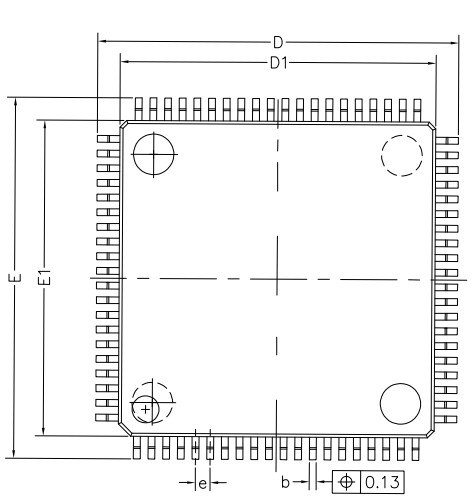


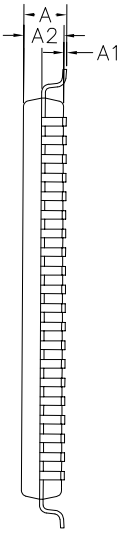
Figure 40. Bottom Layer Layout Example

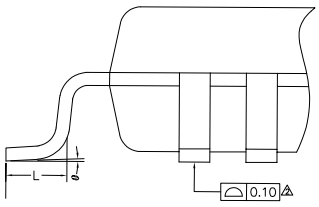
Package Outline Dimensions

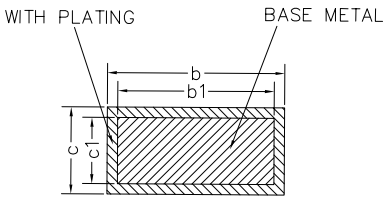
LQFP14X14-80

Package Outline Dimensions QL6(LQFP14X14-80-A)









Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	---	1.600	—	0.063
A1	0.050	0.150	0.002	0.006
A2	1.350	1.450	0.053	0.057
b	0.260	0.380	0.010	0.015
c	0.130	0.180	0.005	0.007
D	15.800	16.200	0.622	0.638
D1	13.900	14.100	0.547	0.555
E	15.800	16.200	0.622	0.638
E1	13.900	14.100	0.547	0.555
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	7°	0	7°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPAFE51760-QL6T	−40 to 125°C	LQFP14X14-80	51760	3	Tray, 900	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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