16-bit, 500-kSPS, 4-channel, Bipolar Input ADC

Features

- 16-bit, 4-channel ADC with Integrated Analog Front-end
- Sampling with 500 KSPS throughput Rate
- Independently Programmable Channel Inputs
  - True Bipolar Single-ended: ±12.288 V, ±10.24 V, ±6.144 V, ±5.12 V, ±3.072 V, ±2.56 V
  - Unipolar Single-ended: 0 V - 12.288 V, 0 V - 10.24 V, 0 V - 6.144 V, 0 V - 5.12 V
  - True Bipolar Fully-differential: ±12.288 V, ±10.24 V, ±6.144 V, ±5.12 V
  - Configurable Analog Bandwidth: 15 kHz or 35 kHz
- Power Supply
  - Single Analog Supply: 5 V
  - Digital Supply: 1.71 V to 5 V
- Highly Integrated Analog Front-end
  - 1-MΩ Analog Input Impedance
  - Programmable Gain Amplifier
  - Analog Low-pass Filter
  - Internal Accurate Reference and Reference Buffer
  - ±30 V Analog Input Overvoltage Clamp Protection with 8-kV ESD
- Flexible Digital and Interface
  - Serial Interface Compatible with SPI
  - Daisy-chain Function
  - Channel Sequencer
- Integrated Diagnostic Function
  - Analog Input Open Detect with Manual or Auto Mode
  - Optional Cyclic Redundancy Check (CRC) Error Checking
  - AUX Input with Direct Connection to ADC Inputs
- Typical Performance
  - DNL: ±0.5 LSB
  - INL: ±1 LSB
  - SNR: 90.5 dB
  - SINAD: 90 dB
  - THD: −103 dB
- Package: TSSOP38 Package
- Wide Operating Temperature Range: −40°C to +125°C

Applications

- Analog Input Modules
- Relay Protection
- Multi-channel Data Acquisition

Description

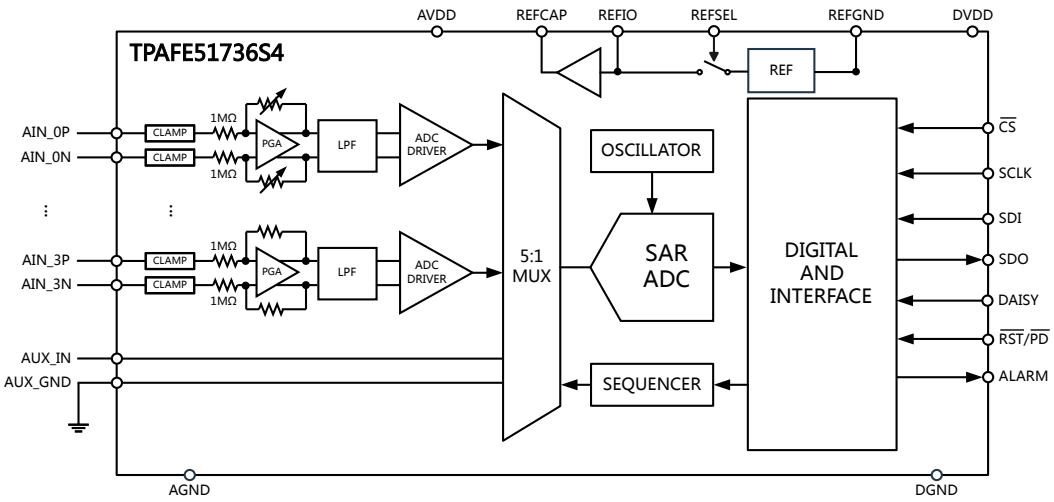
The TPAFE51736S4 is a 4-channel, 16-bit, 500 kSPS sampling system based on a successive approximation register (SAR) analog-to-digital converter (ADC). The TPAFE51736S4 is highly integrated with an analog front-end for each channel, including an input overvoltage clamp, 1 MΩ input impedance, programmable gain amplifier (PGA), active low-pass filter, and ADC driver. Internal precision and low-drift reference with buffer make the device feasible for a compact data acquisition solution. The digital interface supports communication with various host controllers with SPI-compatible serial and daisy-chaining of multiple devices.

The TPAFE51736S4 can process true bipolar single-ended ±12.288 V, ±10.24 V, ±6.144 V, ±5.12 V, ±3.072 V, ±2.56 V, unipolar single-ended 0 V - 12.288 V, 0 V - 10.24 V, 0 V - 6.144 V, 0 V - 5.12 V, and true bipolar fully-differential ±12.288 V, ±10.24 V, ±6.144 V, ±5.12 V input signals, with single 5 V analog power supply. The 1 MΩ high input impedance simplified analog input design, and the device can be connected directly to sensors. The analog input overvoltage can protect the device up to ±30 V. The device offers a simple SPI-compatible serial interface and also supports daisy-chaining of multiple devices.

The device integrates various diagnostic functions to improve system robustness, like analog input open detection and CRC error checking on read and write data and registers.

The TPAFE51736S4 is available in the 38-lead TSSOP 9.7 mm x 4.4 mm package and operates from −40°C to +125°C.

Functional Block Diagram



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Product Family Table

Order Number	Channels	Resolution	Throughput	Package
TPAFE51736S4-TS7R	4	16 Bits	500 kSPS	TSSOP38

Revision History

Date	Revision	Notes
2024-12-26	Rev.A.0	Initial released version

Pin Configuration and Functions

TPAFE51736S4
TSSOP38 Package
Top View

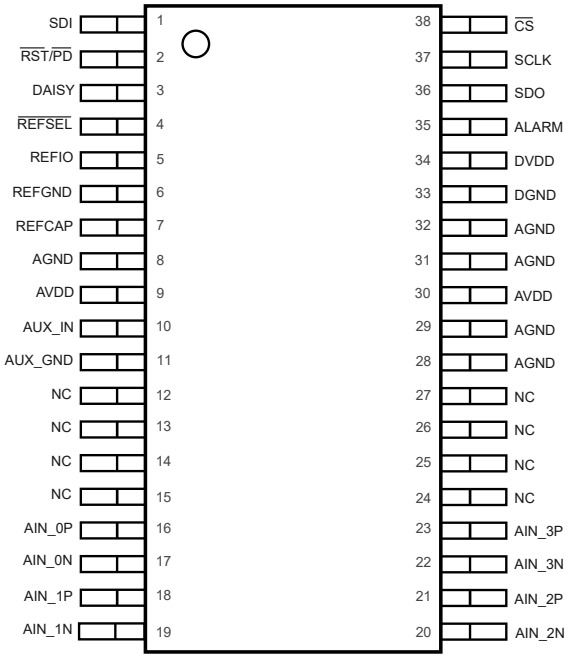


Table 1. Pin Functions: TPAFE51736S4

Pin		Type (1)	Description
No.	Name		
1	SDI	DI	Data input of the SPI interface
2	$\overline{\text{RST}}/\overline{\text{PD}}$	DI	Hardware $\overline{\text{RST}}/\overline{\text{PD}}$ with low logic input active. This pin can perform a reset or power-down function depending on the low input duration.
3	DAISY	DI	Chain the data input during daisy-chain mode
4	$\overline{\text{REFSEL}}$	DI	Active low logic input to enable the internal reference. When this pin is low, the internal reference is enabled and REFIO acts as an output pin. When this pin is high, the internal reference is enabled and REFIO acts as an input pin to apply the external input REF.
5	REFIO	AIO	External reference input pin and internal reference output pin
6	REFGND	P	Reference ground pin. Connect this pin to AGND.
7	REFCAP	AO	Reference buffer output pin. Decouple this pin to AGND using capacitor. The voltage on this pin is typically 4.096 V.
8,28,29, 31,32	AGND	P	Analog ground pins.
9, 30	AVDD	P	Analog supply pins.

Pin		Type (1)	Description
No.	Name		
10	AUX_INP	AI	Auxiliary input channel: positive input.
11	AUX_GND	AI	Auxiliary input channel: negative input.
12	NC	AI	Leave this pin floating or connected to AGND.
13	NC	AI	Leave this pin floating or connected to AGND.
14	NC	AI	Leave this pin floating or connected to AGND.
15	NC	AI	Leave this pin floating or connected to AGND.
16	AIN_0P	AI	Positive analog input for channel 0.
17	AIN_0N	AI	Negative analog input for channel 0.
18	AIN_1P	AI	Positive analog input for channel 1.
19	AIN_1N	AI	Negative analog input for channel 1.
20	AIN_2N	AI	Negative analog input for channel 2.
21	AIN_2P	AI	Positive analog input for channel 2.
22	AIN_3N	AI	Negative analog input for channel 3.
23	AIN_3P	AI	Positive analog input for channel 3.
24	NC	AI	Leave this pin floating or connected to AGND.
25	NC	AI	Leave this pin floating or connected to AGND.
26	NC	AI	Leave this pin floating or connected to AGND.
27	NC	AI	Leave this pin floating or connected to AGND.
34	DVDD	P	Digital supply pins.
35	ALARM	DO	ALARM function output. This pin can be float if alarm function is disabled.
36	SDO	DO	This pin outputs serial conversion data.
37	SCLK	DI	This pin acts as the serial clock input for data transfers.
38	$\overline{CS}$	DI	Active low logic input; chip-select signal

(1) AI is analog input, GND is ground, P is power supply, REF is reference input/output, DI is digital input, DO is digital output, and CAP is decoupling capacitor pin.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Analog Voltage	Analog Input Voltage (AINxP or AINxN) to GND	−30	+30	V
	AUX_IN to GND	−0.3	AVDD + 0.3 V	V
	REFCAP or REFIO to REFGND	−0.3	AVDD + 0.3 V	V
Digital Voltage	Digital Input Voltage to GND	−0.3	DVDD + 0.3 V	V
	Digital Output Voltage to GND	−0.3	DVDD + 0.3 V	V
Supply Voltage	AVDD to GND	−0.3	7	V
	DVDD to GND	−0.3	AVDD + 0.3 V	V
T_J	Maximum Junction Temperature		150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	Analog input pins	ANSI/ESDA/JEDEC JS-001 (1)	±8	kV
		All other pins		±4	kV
CDM	Charged Device Model ESD		ANSI/ESDA/JEDEC JS-002 (2)	±1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
AVDD	Analog Supply Voltage	4.75	5	5.25	V
DVDD	Digital Supply Voltage	1.71	3.3	AVDD	V

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
TSSOP38	68.8	19.9	°C/W

Electrical Characteristics

All test conditions: AVDD = 5 V, V_{REF} = 4.096 V (internal), DVDD = 3 V, f_{SAMPLE} = 500 kSPS, T_A = −40 °C to 125 °C, unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Unit
Analog Inputs					
Input V_{IN} Voltage Ranges (1) V_{IN} = AINxP - AINxN	Input range = ±3 × V_{REF}	−3 × V_{REF}		3 × V_{REF}	V
	Input range = ±2.5 × V_{REF}	−2.5 × V_{REF}		2.5 × V_{REF}	
	Input range = ±1.5 × V_{REF}	−1.5 × V_{REF}		1.5 × V_{REF}	
	Input range = ±1.25 × V_{REF}	−1.25 × V_{REF}		1.25 × V_{REF}	
	Input range = ±0.75 × V_{REF}	−0.75 × V_{REF}		0.75 × V_{REF}	
	Input range = ±0.625 × V_{REF}	−0.625 × V_{REF}		0.625 × V_{REF}	
	Input range = 3 × V_{REF}	0		3 × V_{REF}	
	Input range = 2.5 × V_{REF}	0		2.5 × V_{REF}	
	Input range = 1.5 × V_{REF}	0		1.5 × V_{REF}	
	Input range = 1.25 × V_{REF}	0		1.25 × V_{REF}	
AIN_xP Operating Input Range, Positive Input (1)	Input range = ±3 × V_{REF}	−3 × V_{REF}		3 × V_{REF}	V
	Input range = ±2.5 × V_{REF}	−2.5 × V_{REF}		2.5 × V_{REF}	
	Input range = ±1.5 × V_{REF}	−1.5 × V_{REF}		1.5 × V_{REF}	
	Input range = ±1.25 × V_{REF}	−1.25 × V_{REF}		1.25 × V_{REF}	
	Input range = ±0.75 × V_{REF}	−0.75 × V_{REF}		0.75 × V_{REF}	
	Input range = ±0.625 × V_{REF}	−0.625 × V_{REF}		0.625 × V_{REF}	
	Input range = 3 × V_{REF}	0		3 × V_{REF}	
	Input range = 2.5 × V_{REF}	0		2.5 × V_{REF}	
	Input range = 1.5 × V_{REF}	0		1.5 × V_{REF}	
	Input range = 1.25 × V_{REF}	0		1.25 × V_{REF}	
AIN_xN Operating Input Range, Negative Input (1)	Input range = ±3 × V_{REF}	−3 × V_{REF}		3 × V_{REF}	V
	Input range = ±2.5 × V_{REF}	−2.5 × V_{REF}		2.5 × V_{REF}	
	Input range = ±1.5 × V_{REF}	−1.5 × V_{REF}		1.5 × V_{REF}	
	Input range = ±1.25 × V_{REF}	−1.25 × V_{REF}		1.25 × V_{REF}	
	Input range = ±0.75 × V_{REF}	−0.75 × V_{REF}		0.75 × V_{REF}	
	Input range = ±0.625 × V_{REF}	−0.625 × V_{REF}		0.625 × V_{REF}	
	Input range = 3 × V_{REF}	−0.1		0.1	
	Input range = 2.5 × V_{REF}	−0.1		0.1	
	Input range = 1.5 × V_{REF}	−0.1		0.1	
	Input range = 1.25 × V_{REF}	−0.1		0.1	

Parameter		Test Conditions	Min	Typ	Max	Unit
Fully Differential Input Range (1) V_{IN} = AINxP - AINxN		Input range = ±3 × V_{REF}	−3 × V_{REF}		3 × V_{REF}	V
		Input range = ±2.5 × V_{REF}	−2.5 × V_{REF}		2.5 × V_{REF}	
		Input range = ±1.5 × V_{REF}	−1.5 × V_{REF}		1.5 × V_{REF}	
		Input range = ±1.25 × V_{REF}	−1.25 × V_{REF}		1.25 × V_{REF}	
		Input range = ±0.75 × V_{REF}	−0.75 × V_{REF}		0.75 × V_{REF}	
		Input range = ±0.625 × V_{REF}	−0.625 × V_{REF}		0.625 × V_{REF}	
Fully Differential Input Common-Mode Input Range (1)		Input range = ±3 × V_{REF}	−6.8		6.5	V
		Input range = ±2.5 × V_{REF}	−6.8		6.5	
		Input range = ±1.5 × V_{REF}	−3.4		4.9	
		Input range = ±1.25 × V_{REF}	−3.4		4.9	
		Input range = ±0.75 × V_{REF}	−1.7		4.1	
		Input range = ±0.625 × V_{REF}	−1.7		4.1	
Z_{IN}	Input Impedance	All input ranges, T_A = 25°C	0.85	1	1.17	Mohm
	Input Impedance Temperature Drift	All input ranges		7		ppm/°C
Analog Input Current	Input Leakage Current	Input range = ±2.5 × V_{REF}		8.8		µA
		Input range = ±1.25 × V_{REF}		3.3		
		Input range = ±0.625 × V_{REF}		1.1		
		Input range = 2.5 × V_{REF}		9.2		
		Input range = 1.25 × V_{REF}		4.3		
Input Overvoltage Protection (1)						
Analog Input Clamp	Overvoltage Protection Voltage	All input ranges	−30		30	V
Analog Input Filter						
−3 dB BW	Analog Input LPF Bandwidth −3 dB	Low bandwidth		15		kHz
		High bandwidth		35		
−0.1 dB BW	Analog Input LPF Bandwidth −0.1 dB	Low bandwidth		2.5		kHz
		High bandwidth		5.5		
System Performance						
Resolution			16			Bits
NMC	No Missing Codes		16			Bits
DNL	Differential Nonlinearity	All input ranges	–0.99	±0.5	1	LSB
INL	Integral Nonlinearity	All input ranges	–2	±1	2	LSB
E_G	Positive Full-scale Error	At T_A = 25°C, all normal input ranges		±0.02	±0.05	%FSR
		At T_A = 25°C, all overrange input ranges		±0.02	±0.12	%FSR

Parameter		Test Conditions	Min	Typ	Max	Unit
	Positive Full-scale Error Matching (1) All Input Ranges (channel-to-channel)	At T_A = 25°C, all normal input ranges		±0.02	±0.05	%FSR
		At T_A = 25°C, all overrange input ranges		±0.02	±0.12	%FSR
	Positive Full-scale Error Temperature Drift (1)	All input ranges	−5	1	5	ppm/°C
E_O	Offset Error At T_A = 25°C,	Input range = ±3 × V_{REF}		±0.375	±2.63	mV
		Input range = ±2.5 × V_{REF}		±0.32	±1.25	
		Input range = ±1.5 × V_{REF}		±0.56	±1.69	
		Input range = ±1.25 × V_{REF}		±0.47	±0.95	
		Input range = ±0.75 × V_{REF}		±0.375	±1.41	
		Input range = ±0.625 × V_{REF}		±0.32	±0.8	
		Input range = 3 × V_{REF}		±0.375	±4.59	
		Input range = 2.5 × V_{REF}		±0.32	±2.2	
		Input range = 1.5 × V_{REF}		±0.47	±4.69	
		Input range = 1.25 × V_{REF}		±0.39	±1.8	
	Offset Error Matching (1) (channel to channel At T_A = 25°C)	Input range = ±3 × V_{REF}		±0.375	±2.63	mV
		Input range = ±2.5 × V_{REF}		±0.32	±1.25	
		Input range = ±1.5 × V_{REF}		±0.56	±1.69	
		Input range = ±1.25 × V_{REF}		±0.47	±0.95	
		Input range = ±0.75 × V_{REF}		±0.375	±1.41	
		Input range = ±0.625 × V_{REF}		±0.32	±0.8	
		Input range = 3 × V_{REF}		±0.375	±4.59	
		Input range = 2.5 × V_{REF}		±0.32	±2.2	
		Input range = 1.5 × V_{REF}		±0.47	±4.69	
		Input range = 1.25 × V_{REF}		±0.39	±1.8	
	Offset Error Temperature Drift (1)	All input ranges	−4	1	4	ppm/°C
Sampling Dynamics (1)						
t_{CONV}	Conversion Time				880	ns
t_{ACQ}	Acquisition Time		1120			ns
f_S	Maximum Throughput Rate without Latency			500		kSPS
Dynamic Characteristics						
SNR	Low Bandwidth –0.5 dBFS 1 kHz Input	Input range = ±3 × V_{REF}	87.2	90.5		dB
		Input range = ±2.5 × V_{REF}	86.9	89.9		
		Input range = ±1.5 × V_{REF}	87	90		

Parameter		Test Conditions	Min	Typ	Max	Unit
		Input range = ±1.25 × V_{REF}	86.5	89.4		
		Input range = ±0.75 × V_{REF}	86.2	88.9		
		Input range = ±0.625 × V_{REF}	85.5	88.3		
		Input range = 3 × V_{REF}	86.9	89.8		
		Input range = 2.5 × V_{REF}	86.3	89		
		Input range = 1.5 × V_{REF}	85.6	88.2		
		Input range = 1.25 × V_{REF}	84.8	87.1		
	High Bandwidth –0.5 dBFS 1 kHz Input	Input range = ±3 × V_{REF}		90		dB
		Input range = ±2.5 × V_{REF}		90		
		Input range = ±1.5 × V_{REF}		90		
		Input range = ±1.25 × V_{REF}		89		
		Input range = ±0.75 × V_{REF}		89		
		Input range = ±0.625 × V_{REF}		88		
		Input range = 3 × V_{REF}		88		
		Input range = 2.5 × V_{REF}		88		
		Input range = 1.5 × V_{REF}		86		
		Input range = 1.25 × V_{REF}		85		
THD	Low Bandwidth –0.5 dBFS 1 kHz Input	Input range = ±3 × V_{REF}		–103		dB
		Input range = ±2.5 × V_{REF}		–103		
		Input range = ±1.5 × V_{REF}		–103		
		Input range = ±1.25 × V_{REF}		–103		
		Input range = ±0.75 × V_{REF}		–103		
		Input range = ±0.625 × V_{REF}		–103		
		Input range = 3 × V_{REF}		–103		
		Input range = 2.5 × V_{REF}		–103		
		Input range = 1.5 × V_{REF}		–103		
		Input range = 1.25 × V_{REF}		–103		
	High Bandwidth –0.5 dBFS 1 kHz Input	Input range = ±3 × V_{REF}		–100		dB
		Input range = ±2.5 × V_{REF}		–100		
		Input range = ±1.5 × V_{REF}		–100		
		Input range = ±1.25 × V_{REF}		–100		
		Input range = ±0.75 × V_{REF}		–100		
		Input range = ±0.625 × V_{REF}		–100		
		Input range = 3 × V_{REF}		–100		
		Input range = 2.5 × V_{REF}		–100		
		Input range = 1.5 × V_{REF}		–100		
		Input range = 1.25 × V_{REF}		–100		

Parameter		Test Conditions	Min	Typ	Max	Unit
SINAD	Low Bandwidth –0.5 dBFS 1 kHz Input	Input range = ±3 × V_{REF}	86.6	90		dB
		Input range = ±2.5 × V_{REF}	86.7	89.7		
		Input range = ±1.5 × V_{REF}	86.6	89.8		
		Input range = ±1.25 × V_{REF}	86.3	89.2		
		Input range = ±0.75 × V_{REF}	85.5	88.8		
		Input range = ±0.625 × V_{REF}	84.6	88.2		
		Input range = 3 × V_{REF}	86.3	89.6		
		Input range = 2.5 × V_{REF}	85.7	88.8		
		Input range = 1.5 × V_{REF}	85.2	88.1		
		Input range = 1.25 × V_{REF}	84.4	87		
	High Bandwidth –0.5 dBFS 1 kHz Input	Input range = ±3 × V_{REF}		89		dB
		Input range = ±2.5 × V_{REF}		89		
		Input range = ±1.5 × V_{REF}		89		
		Input range = ±1.25 × V_{REF}		89		
		Input range = ±0.75 × V_{REF}		88		
		Input range = ±0.625 × V_{REF}		88		
		Input range = 3 × V_{REF}		89		
		Input range = 2.5 × V_{REF}		89		
		Input range = 1.5 × V_{REF}		87		
		Input range = 1.25 × V_{REF}		86		
Crosstalk Isolation		Interfere channel input overdriven to 2 x maximum input voltage		120		dB
Crosstalk Memory		Interfere channel input overdriven to 2 x maximum input voltage		90		dB
Auxiliary Channel						
Resolution			16			Bits
V_{AUX_IN}	AUX_IN Voltage Range (1)	(AUX_IN – AUX_GND)	0		V_{REF}	V
	Operating Input Range (1)	AUX_IN	0		V_{REF}	V
		AUX_GND		0		V
C_{IN}	Input Capacitance	During sampling		35		pF
		During conversion		5		pF
Analog input current	Input Leakage Current			100		nA
DNL	Differential Nonlinearity	All input ranges	–0.99	±0.5	1	LSB
INL	Integral Nonlinearity	All input ranges	–2.2	±1	2.2	LSB

Parameter		Test Conditions	Min	Typ	Max	Unit
$E_{G(AUX)}$	Gain Error	At T_A = 25°C		±0.01	±0.018	%FSR
$E_{O(AUX)}$	Offset Error	At T_A = 25°C		±0.5	±1.05	mV
SNR	Signal-to-noise Ratio	V_{AUX_IN} = –0.5 dBFS at 1 kHz	85.4	89		dB
THD	Total Harmonic Distortion	V_{AUX_IN} = –0.5 dBFS at 1 kHz		−104		dB
SINAD	Signal-to-noise Distortion Ratio	V_{AUX_IN} = –0.5 dBFS at 1 kHz	85	88.8		dB
SFDR	Spurious-free Dynamic Range	V_{AUX_IN} = –0.5 dBFS at 1 kHz		104		dB
Internal Reference Output						
V_{REFIO_INT}	REFIO Voltage	Voltage on REFIO pin (configured as output) T_A= 25°C	4.086	4.096	4.106	V
	Reference Temperature Drift (1)			5	10	ppm/°C
C_{OUT_REFIO}	Decoupling Capacitor on REFIO			0.1		µF
V_{REFCAP}	Reference Voltage	Reference voltage to ADC (on REFCAP pin) T_A= 25°C	4.086	4.096	4.106	V
	Reference Buffer Output Impedance			0.5		Ω
	Reference Buffer Temperature Drift			1		ppm/°C
C_{OUT_REFCAP}	Decoupling Capacitor on REFIO			10		µF
t_{ON}	Reference Turn-on Time	C_{OUT_REFIO} = 0.1 µF C_{OUT_REFCAP} = 10 µF		10		ms
External Reference Input						
V_{REFIO_EXT}	External Reference	External reference voltage on REFIO (configured as input)	4.046	4.096	4.146	V
Power-Supply Requirements						
AVDD (1)	Analog Power-supply Voltage	Analog supply	4.75	5	5.25	V
DVDD (1)	Digital Power-supply Voltage	Digital supply range	1.65	3.3	AVDD	V
		Digital supply range for specified performance	2.7	3.3	5.25	V
I_{AVDD_DYN}	AVDD Dynamic	AVDD = 5 V, f_S = maximum and internal reference		18	22	mA

Parameter		Test Conditions	Min	Typ	Max	Unit
I_{AVDD_STC}	AVDD Static	Device not converting and internal reference		15	20	mA
I_{STDBY}	Standby	At AVDD = 5 V, device in STDBY mode and internal reference		6	8	mA
I_{PWR_DN}	Power-down	At AVDD = 5 V, device in PWR_DN		12		µA
I_{DVDD_DYN}	Digital Supply Current	At DVDD = 3.3 V, output = 0000		0.5		mA
Digital Inputs (CMOS)						
V_{IH}	Digital Input Logic Levels	DVDD > 2.1 V	0.7 x DVDD		DVDD + 0.3	V
V_{IL}			–0.3		0.3 x DVDD	V
V_{IH}	Digital Input Logic Levels	DVDD ≤ 2.1 V	0.8 x DVDD		DVDD + 0.3	V
V_{IL}			–0.3		0.2 x DVDD	V
Input Leakage Current				100		nA
Input Capacitance				5		pF
Digital Outputs (CMOS)						
V_{OH}	Digital Output Logic Levels	I_O= 500-µA source	0.8 x DVDD		DVDD	V
V_{OL}		I_O= 500-µA sink	0		0.2 x DVDD	V
Floating State Leakage Current		Only for SDO		1		µA
Internal Pin Capacitance				5		pF
Temperature Range (1)						
T_A	Operating Free-air Temperature		-40		125	°C

(1) These specifications are not production tested but are supported by characterization data at the initial product release.

Timing Requirements (1)

Universal Serial Timing Specifications

AVDD = 5 V, DVDD = 5 V, V_{REF} = 4.096 V internal reference, f_{SAMPLE} = 500 kSPS, T_A = −40°C to +125°C, interface timing tested using a load capacitance of 20 pF, unless otherwise noted.

Table 2. Serial Interface Timing Specifications

Parameter		Min	Typ	Max	Unit
Timing Specifications					
f_S	Sampling frequency (f_{CLK}= max)			500	kSPS
t_S	ADC cycle time period (f_{CLK}= max)	2			µs
f_{SCLK}	Serial clock frequency (f_S= max) DVDD ≥ 3V			17	MHz
t_{SCLK}	Serial clock time period (f_S= max) DVDD ≥ 3V	59			ns
t_{CONV}	Conversion time			880	ns
t_{DZ_CSDO}	Delay time: $\overline{CS}$ falling to data enable			10	ns
t_{D_CKCS}	Delay time: last SCLK falling to $\overline{CS}$ rising	10			ns
t_{DZ_CSDO}	Delay time: $\overline{CS}$ rising to SDO going to 3-state	10			ns
Timing Requirements					
t_{ACQ}	Acquisition time	1120			ns
t_{PH_CK}	Clock high time	0.4		0.6	t_{SCLK}
t_{PL_CK}	Clock low time	0.4		0.6	t_{SCLK}
t_{PH_CS}	$\overline{CS}$ high time	30			ns
t_{SU_CSCK}	Setup time: $\overline{CS}$ falling to SCLK falling	15			ns
t_{HT_CKDO}	Hold time: SCLK falling to (previous) data valid on SDO	5			ns
t_{SU_DOCK}	Setup time: SDO data valid to SCLK falling	25			ns
t_{SU_DICK}	Setup time: SDI data valid to SCLK falling	5			ns
t_{HT_CKDI}	Hold time: SCLK falling to (previous) data valid on SDI	5			ns
t_{SU_DSYCK}	Setup time: DAISY data valid to SCLK falling	5			ns
t_{HT_CKDSY}	Hold time: SCLK falling to (previous) data valid on DAISY	5			ns

(1) Parameters are provided by the design simulation.

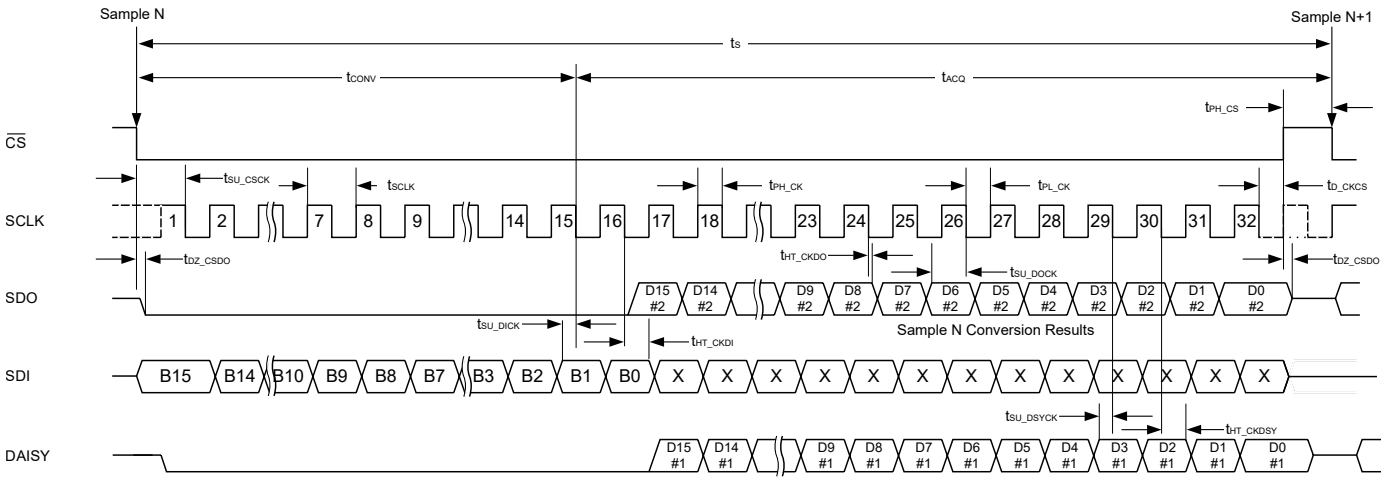
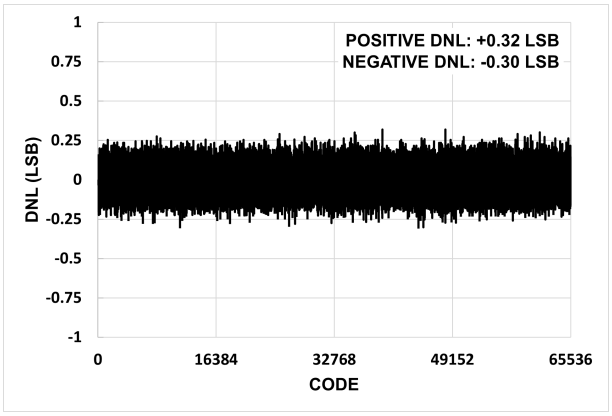


Figure 1. Universal Timing Diagram Across All Interfaces

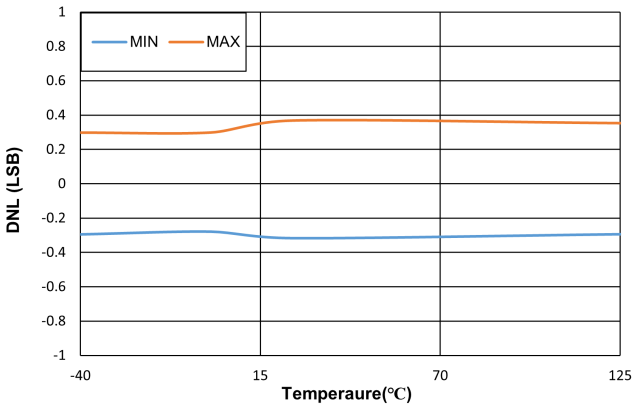
Typical Performance Characteristics

All test conditions: T_A = 25°C, AVDD = 5 V, DVDD = 5 V, internal reference V_{REF} = 4.096 V, and f_{SAMPLE} = 500 kSPS, unless otherwise noted.



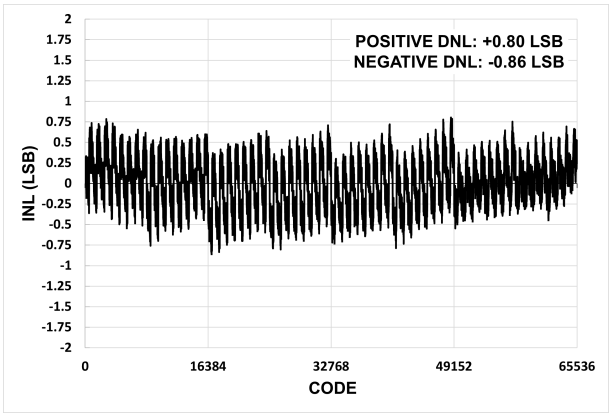
All input ranges

Figure 2. Typical DNL for All Codes



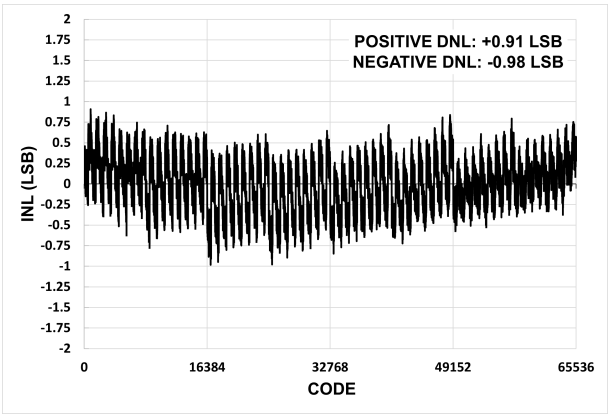
All input ranges

Figure 3. DNL vs. Temperature



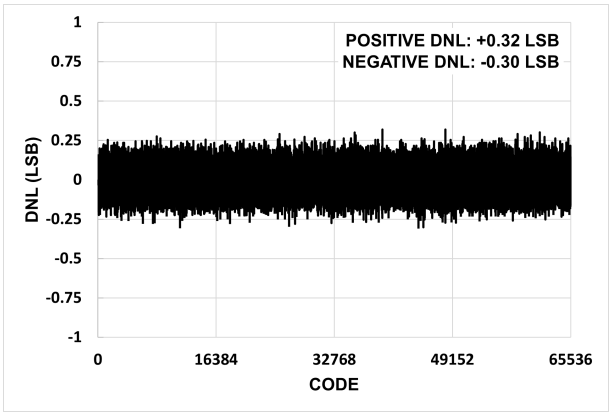
Range = ±1.25 × V_{REF}

Figure 4. Typical INL for All Codes



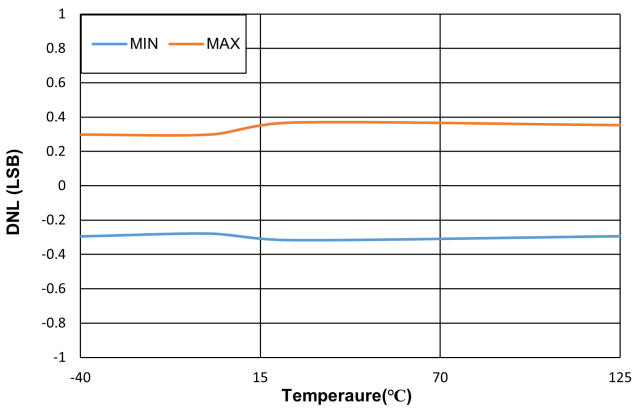
Range = ±0.625 × V_{REF}

Figure 5. Typical INL for All Codes



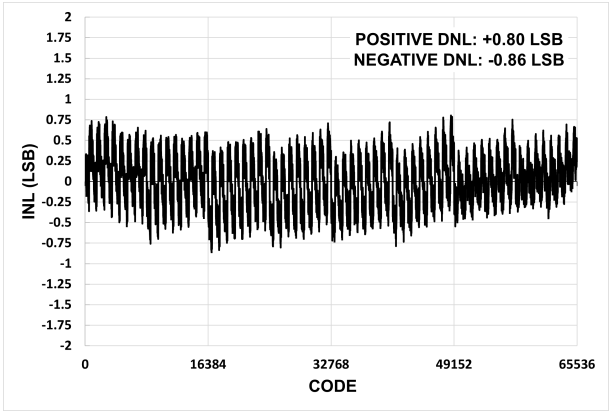
All input ranges

Figure 6. Typical DNL for All Codes



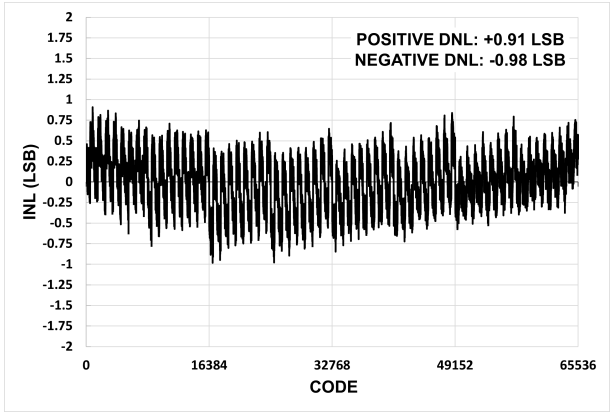
All input ranges

Figure 7. DNL vs. Temperature



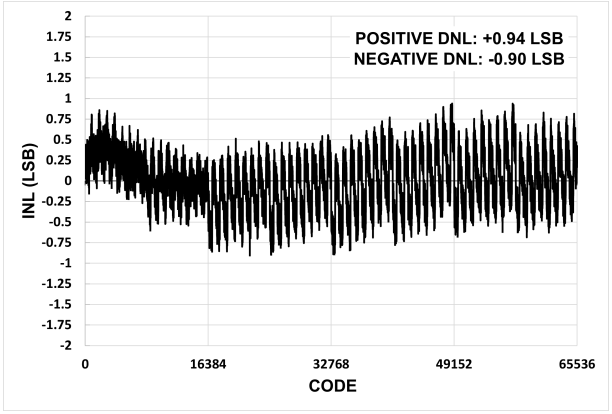
Range = ±1.25 × V_{REF}

Figure 8. Typical INL for All Codes



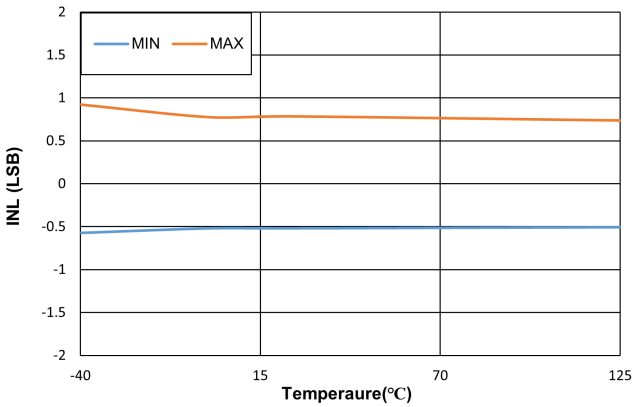
Range = ±0.625 × V_{REF}

Figure 9. Typical INL for All Codes



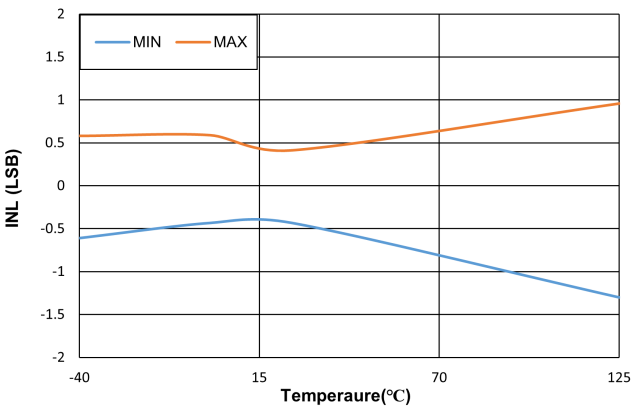
Range = 1.25 × V_{REF}

Figure 10. Typical INL for All Codes



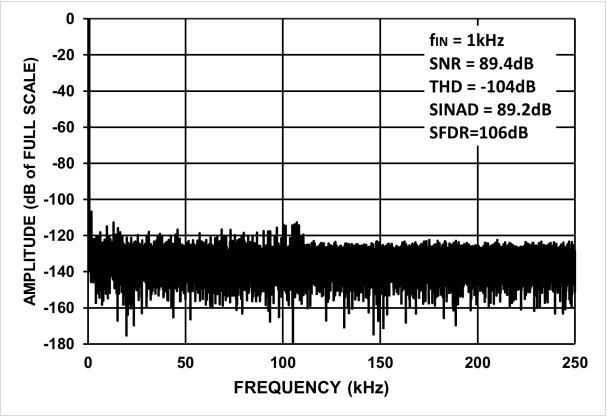
Bipolar input ranges

Figure 11. INL vs. Temperature



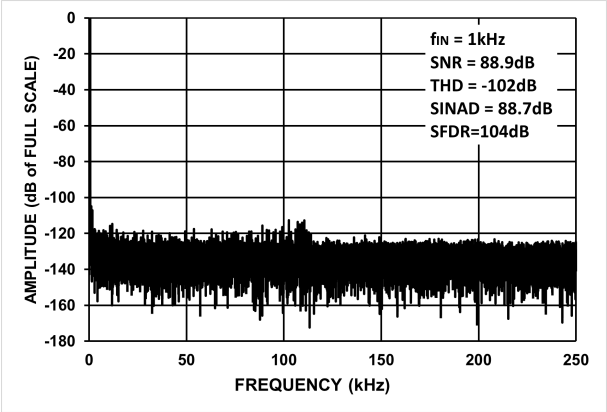
Unipolar input ranges

Figure 12. INL vs. Temperature



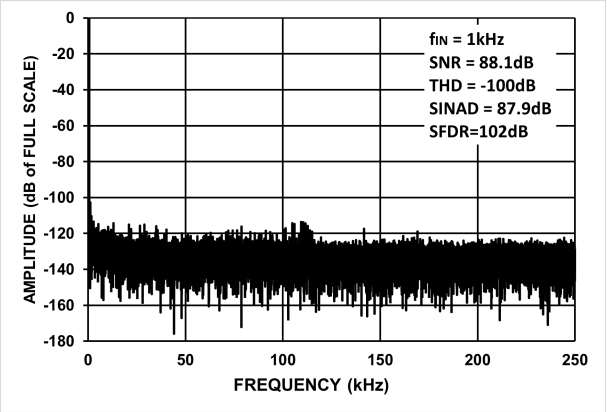
Range = ±2.5 × V_{REF}

Figure 13. Typical FFT Plot



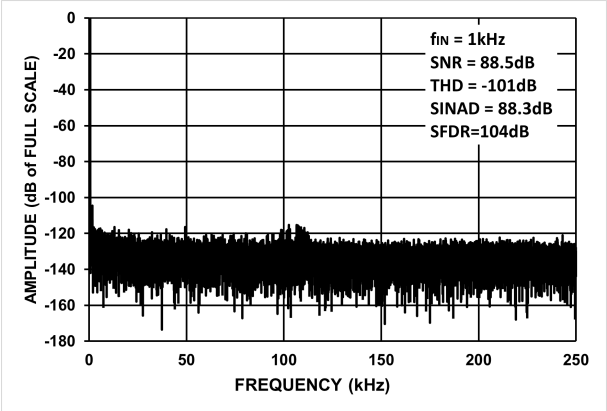
Range = ±1.25 × V_{REF}

Figure 14. Typical FFT Plot



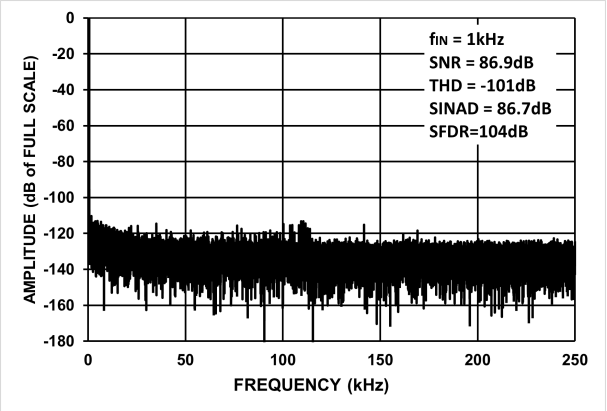
Range = ±0.625 × V_{REF}

Figure 15. Typical FFT Plot



Range = 2.5 × V_{REF}

Figure 16. Typical FFT Plot



Range = 1.25 × V_{REF}

Figure 17. Typical FFT Plot

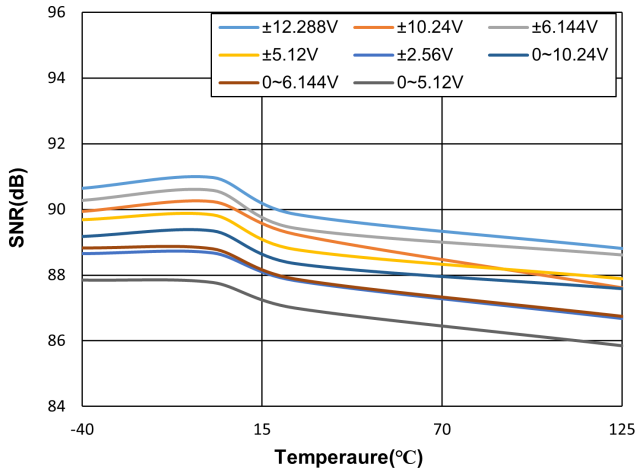


Figure 18. SNR vs. Temperature

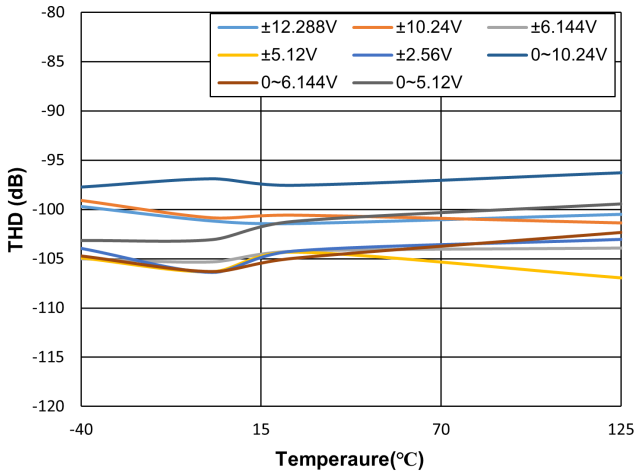


Figure 19. THD vs. Temperature

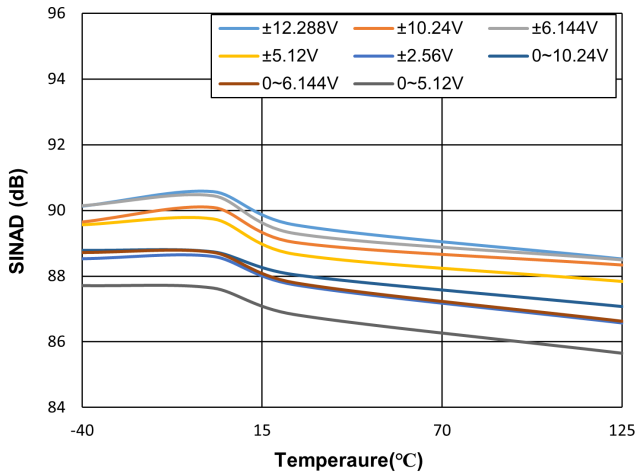


Figure 20. SNDR vs. Temperature

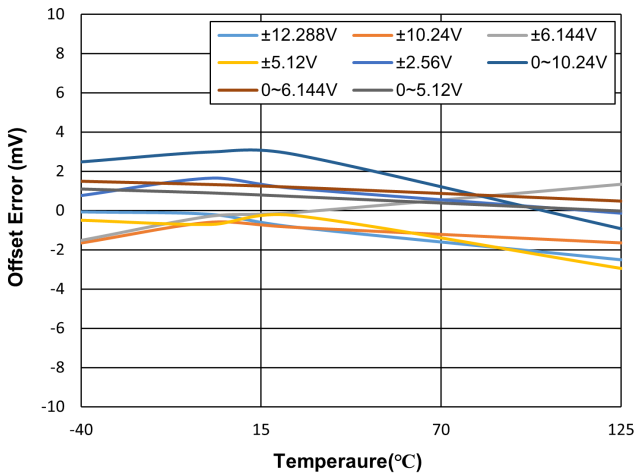


Figure 21. Offset vs. Temperature

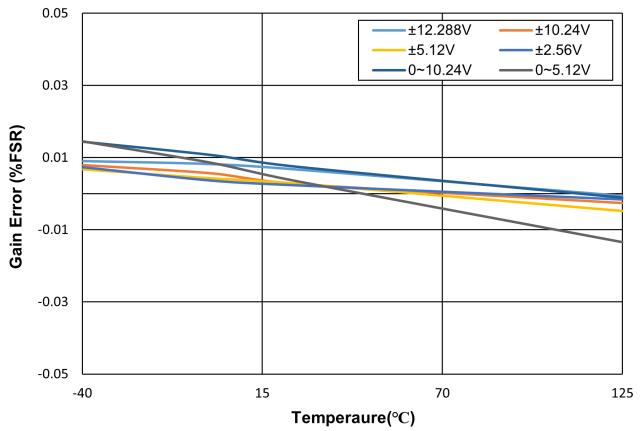


Figure 22. Gain Error vs. Temperature

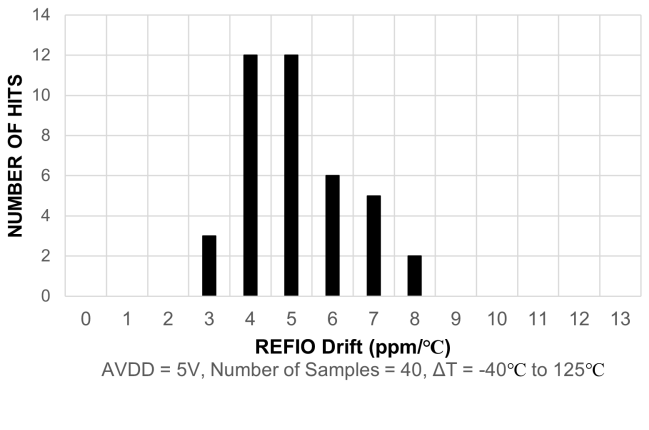


Figure 23. Internal Reference Temperature Drift Histogram

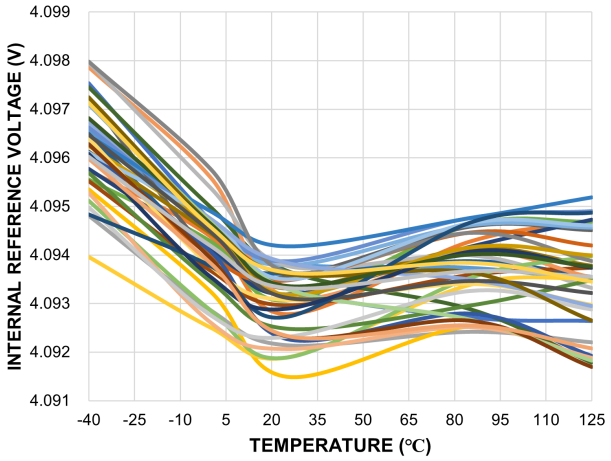


Figure 24. Internal Reference vs. Temperature

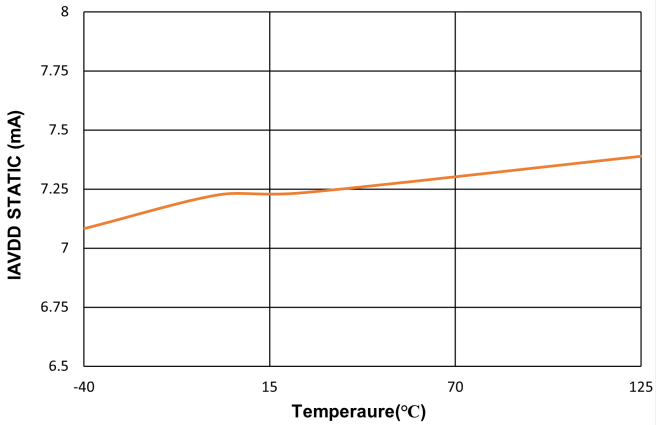


Figure 25. AVDD Current vs. Temperature for the TPAFE51736S8 (STANDBY)

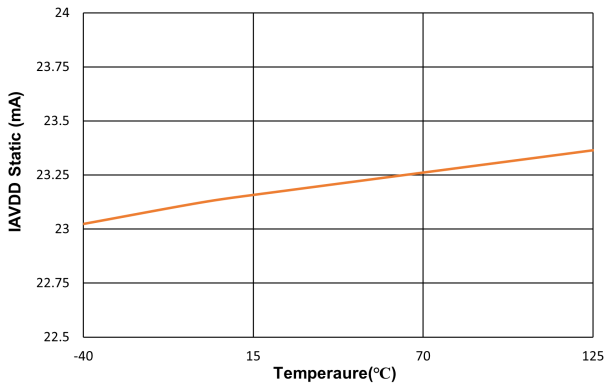


Figure 26. AVDD Current vs. Temperature for the TPAFE51736S8 (Static)

Detailed Description

Overview

The TPAFE51736S4 is a 16-bit data acquisition system with 4 analog input channels. Each input channel includes input protection circuitry, a programmable gain amplifier (PGA), an analog low-pass filter, and an analog-to-digital converter (ADC) driver. These channels feed into a 4-channel analog multiplexer (MUX) with an ADC operating at a 500 KSPS throughput rate. The device incorporates a 4.096-V internal reference with a fast-settling buffer and a flexible channel sequencer. It also provides high-speed serial interfaces for communication with the daisy-chain function, making it suitable for a wide range of data acquisition applications.

The device operates with a single 5-V analog supply and can process true bipolar input signals. It provides a programmable analog signal range, including options for true bipolar single-ended ±12.288 V, ±10.24 V, ±6.144 V, ±5.12 V, ±3.072 V, ±2.56 V, unipolar single-ended 0 V - 12.288 V, 0 V - 10.24 V, 0 V - 6.144 V, 0 V - 5.12 V, and true bipolar fully-differential ±12.288 V, ±10.24 V, ±6.144 V, ±5.12 V input signals. The input clamp protection circuitry can protect the device from being damaged by voltages as high as ±30 V. The device features a constant 1MΩ resistive input impedance.

Functional Block Diagram

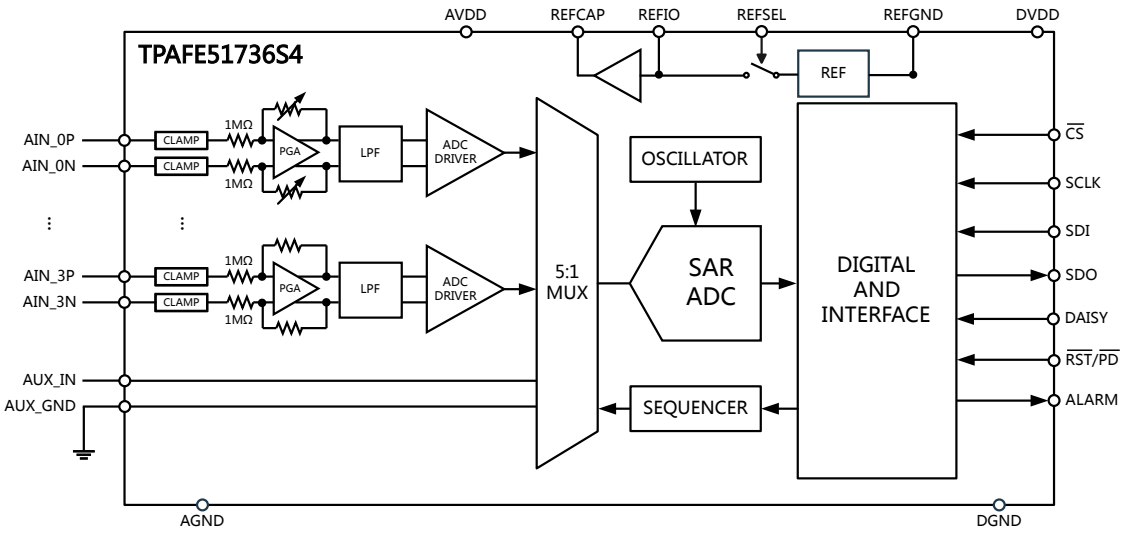


Figure 27. TPAFE51736S4 Block Diagram

Feature Description

Analog Inputs

The TPAFE51736 incorporates a 16-bit successive approximation register (SAR) analog-to-digital converter (ADC). The ADC is linked up to 8 analog input channels through a multiplexer. The device comprises a total of eight analog input pairs. The ADC is responsible for converting the voltage difference between the analog input pairs AINxP – AINxN. The simplified circuit schematic for each analog input channel is shown in the function block diagram, encompassing the input clamp protection circuit, PGA, low-pass filter, multiplexer, high-speed ADC driver, and a precision 16-bit SAR ADC.

Analog Input Ranges

The TPAFE51736 can handle true bipolar differential, bipolar single-ended, and unipolar single-ended input voltages. It is possible to configure an individual analog input range per channel from the range select registers.

The devices sample the voltage difference (AIN_xP – AIN_xN) between the selected analog input pairs. They allow a ±0.1 V range on the AIN_nGND pin for all analog input channels. This feature is beneficial in modular systems where the sensor or signal-conditioning block is located at a distance from the ADC on the board. It proves particularly useful when there might be a difference in the ground potential between the sensor or signal conditioner and the ADC ground. In such cases, it is recommended to run separate wires from the AIN_xN pin of the device to the sensor or signal-conditioning ground.

In single-ended mode, the AINxN pins are typically connected to analog ground and allow a ±0.1 V range referred to ground.

In differential mode, the AINxP and AINxN typically sense the fully differential input signals within a certain input common mode range. Also, this feature is beneficial in modular systems where the sensor or signal-conditioning block is located at a distance from the ADC on the board. It proves particularly useful when there might be a difference in the ground potential between the sensor or signal conditioner and the ADC ground. In such cases, it is recommended to run separate wires from the AIN_xN pin of the device to the sensor or signal-conditioning ground.

Analog Input Impedance

The TPAFE51736 features a fixed high analog input impedance of 1 MΩ, which is nearly constant at different sampling frequencies. It eliminates the need for an external driver amplifier, allowing direct connection to the source or sensor.

Analog Input Clamp Protection

The TPAFE51736 incorporates an internal clamp protection circuit on each of the analog input channels. This protection circuit allows each analog input voltage to swing up to ±30 V. Beyond this threshold, the input clamp circuit activates while still operating from a single 5 V supply.

To ensure that the input current stays within safe limits (±10 mA) for input voltages above the clamp threshold, it is advisable to use a series resistor with the analog inputs. This resistor can serve the dual purpose of limiting input current and providing an antialiasing low-pass filter (LPF) when combined with a capacitor. Matching the external source impedance on the AINxP and AINxN pins helps cancel any additional offset error. However, it's advisable to avoid prolonged activation of the clamp protection circuitry during normal or power-down conditions for optimal device performance.

Programmable Gain Amplifier (PGA)

The TPAFE51736 includes a PGA at each analog input channel, providing support for both unipolar/bipolar single-ended and bipolar differential inputs. The supported analog input ranges are listed below. Each channel's analog input range can be configured independently using the range select register fields located at addresses 0x5 to 0xC and 0xD for range expanding.

Table 3. Analog Input Ranges

Analog Input Mode	Analog Input Range	CHn_OVER_RANGE	RANGE_CHn[3:0]		
			BIT 2	BIT 1	BIT 0
Single-ended	±3 x V_{REF}	1	0	0	0
Single-ended	±2.5 x V_{REF}	0	0	0	0
Single-ended	±1.5 x V_{REF}	1	0	0	1
Single-ended	±1.25 x V_{REF}	0	0	0	1
Single-ended	±0.75 x V_{REF}	1	0	1	0
Single-ended	±0.625 x V_{REF}	0	0	1	0
Differential	±3 x V_{REF}	1	0	1	1
Differential	±2.5 x V_{REF}	0	0	1	1
Differential	±1.5 x V_{REF}	1	1	0	0
Differential	±1.25 x V_{REF}	0	1	0	0
Differential	±0.75 x V_{REF}	1	1	1	1
Differential	±0.625 x V_{REF}	0	1	1	1
Single-ended	0 to 3 x V_{REF}	1	1	0	1
Single-ended	0 to 2.5 x V_{REF}	0	1	0	1
Single-ended	0 to 1.5 x V_{REF}	1	1	1	0
Single-ended	0 to 1.25 x V_{REF}	0	1	1	0

Low-Pass Filter (LPF)

Every analog input channel on the TPAFE51736 is equipped with an antialiasing low-pass filter (LPF) situated at the PGA output. The following table outlines the programmable LPF options associated with the analog input range in the device. The analog input bandwidth for all eight channels can be chosen using the LPF_CONFIG[1:0] bits found in address 0xE.

Table 4. Low-Pass Filter Corner Frequency

LPF	Analog Input Range	Typical –3 dB Bandwidth
Low-bandwidth	All input ranges	15 kHz
High-bandwidth	All input ranges	35 kHz

Multiplexer (MUX)

The TPAFE51736 includes an integrated multi-channel analog multiplexer. Each analog input channel is processed of the voltage difference between the positive analog input AIN_xP and the negative ground input AIN_xN through the analog front-end circuitry before entering the multiplexer. The ADC directly samples the output of the multiplexer. The multiplexer can scan these analog inputs in either manual or auto-scan mode, as detailed in the Channel Sequencing Modes section.In manual mode (MAN_Ch_n), the channel is selected for every sample through a register write. In auto-scan mode (AUTO_RST), the channel number increments automatically on every $\overline{CS}$ falling edge after the current channel is sampled. The analog inputs can be chosen for an auto-scan with register settings (refer to the Auto-Scan Sequencing Control Registers section). The devices automatically scan only the selected analog inputs in ascending order.

Reference

The TPAFE51736 can operate with either an internal voltage reference or an external voltage reference, utilizing the internal buffer. The configuration between internal and external reference is controlled by an external $\overline{\text{REFSEL}}$ pin. The devices incorporate a built-in buffer amplifier designed to drive the reference input of the internal ADC core, optimizing overall performance.

Internal Reference

The TPAFE51736 includes an on-chip 4.096 V reference which can be accessed through the REFIO pin. The SAR ADC utilizes this internally generated and buffered 4.096 V reference for its conversions. To select the internal reference, connect the $\overline{\text{REFSEL}}$ pin to AGND or tie it low. In this configuration, the REFIO pin serves as an output pin, providing the internal reference value. It is recommended to place a 0.1 µF decoupling capacitor between the REFIO pin and REFGND, and a larger capacitor requires longer settling time. Place the capacitor as close to the REFIO pin as possible.The capacitors act as decoupling components and form a low-pass filter with the output impedance of the internal band-gap circuit, limiting the noise of the reference. Avoid using the REFIO pin to drive external loads, as REFIO has limited current output capability. If needed as a source, it can be followed by an operational amplifier buffer.

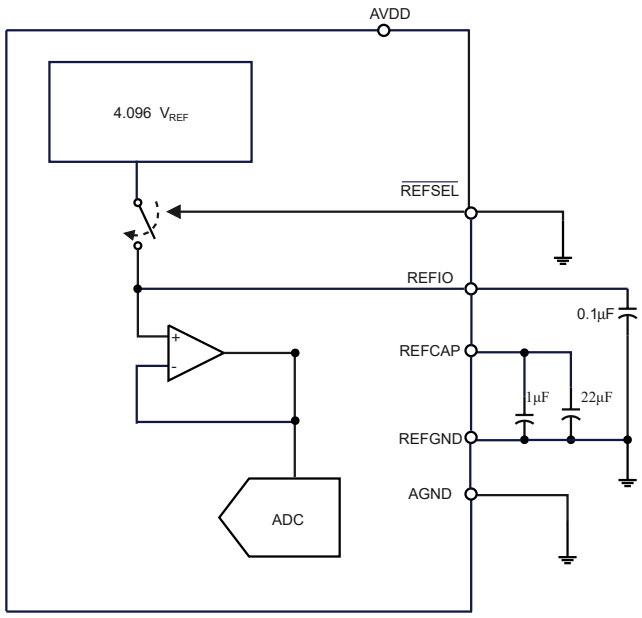


Figure 28. Device Connections for Using an Internal 4.096-V Reference

External Reference

Alternatively, the TPAFE51736 can accept an external reference voltage applied to the REFIO pin. When an external 4.096 V reference is provided, the device internally amplifies it to create the 4.096 V buffered reference used by the SAR ADC. To select external reference mode, either tie the $\overline{\text{REFSEL}}$ pin high or connect it to the DVDD supply. In this mode, an external 4.096-V reference should be applied at REFIO, which becomes an input pin. Users can use any external reference in this mode. The internal buffer is designed to handle dynamic loading on the REFCAP pin, which is internally connected to the ADC reference input. When using an external reference, it's important to appropriately filter the reference output to minimize its impact on system performance.

The output of the internal reference buffer is present at the REFCAP pin. To ensure proper operation, decoupling capacitors of 22 µF and 1 µF must be connected between REFCAP and REFGND. It's important not to use the internal buffer to drive any external loads due to the limited current output capability of this buffer.

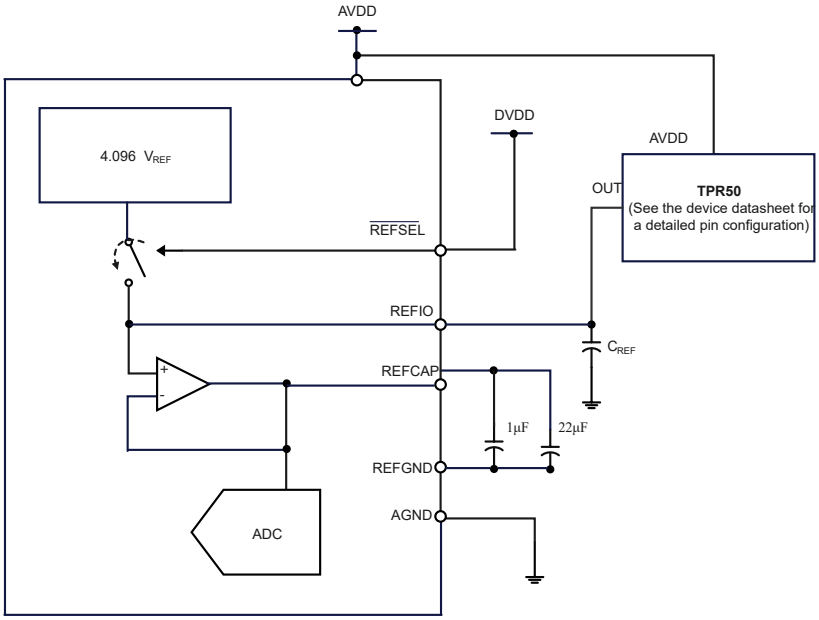


Figure 29. Device Connections for Using an External 4.096-V Reference

Auxiliary Channel

The TPAFE51736 incorporates a single-ended auxiliary input channel (AUX_IN and AUX_GND). The AUX channel facilitates a direct interface with an internal, high-precision, 16-bit ADC through the multiplexer, excluding the front-end analog signal conditioning found in other analog input channels. The AUX channel supports a unipolar input range of 0 V to V_{REF}, as no front-end PGA on the auxiliary channel. The AUX_IN pin can accept input signals ranging from 0 V to V_{REF}, while the AUX_GND pin should be connected to GND.

During a conversion, the voltage between these pins is directly sampled on an internal sampling capacitor. The input current required to charge the sampling capacitor depends on factors such as the sampling rate, input frequency, and source impedance. For slow applications with a low-impedance source, the inputs of the AUX channel can be directly driven. However, as the throughput, input frequency, or source impedance increases, a driving amplifier is recommended at the input to achieve optimal AC performance from the AUX channel.

ADC Transfer Function

The TPAFE51736 outputs 16 bits of conversion data in straight binary format for all ranges and all modes (unipolar/bipolar). The full-scale range (FSR) for each input signal is determined by the difference between the positive full-scale (PFS) input voltage and the negative full-scale (NFS) input voltage. The size of the least significant bit (LSB) is calculated as FSR / 2^16 = FSR / 65536 for the 16-bit resolution of the ADC. In the case of a reference voltage (V_{REF}) set to 4.096 V, the LSB values for various input ranges are as follows:

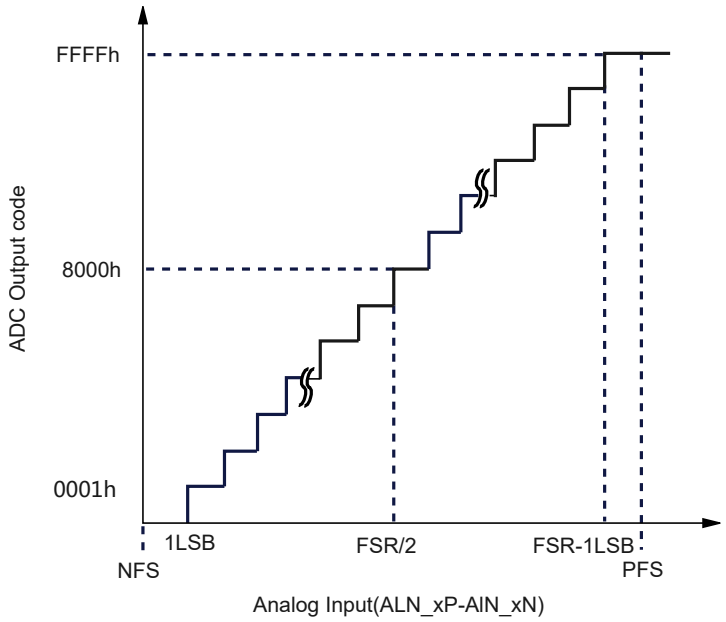


Figure 30. 16-Bit ADC Transfer Function (Straight-Binary Format)

Table 5. Transfer Characteristics

Input Range	NFS (V)	PFS (V)	FSR (V)	LSB (μV)
±3 x V_{REF}	−12.288	12.288	24.576	375
±2.5 x V_{REF}	−10.24	10.24	20.48	312.5
±1.5 x V_{REF}	−6.144	6.144	12.288	187.5
±1.25 x V_{REF}	−5.12	5.12	10.24	156.25
±0.75 x V_{REF}	−3.072	3.072	6.144	93.75
±0.625 x V_{REF}	−2.56	2.56	5.12	78.125
0 to 3 x V_{REF}	0	12.288	12.288	187.5
0 to 2.5 x V_{REF}	0	10.24	10.24	156.25
0 to 1.5 x V_{REF}	0	6.144	6.144	93.75
0 to 1.25 x V_{REF}	0	5.12	5.12	78.125

Alarm Feature

The TPAFE51736 features an active-high ALARM output. The ALARM signal is synchronous with a state change on the 16th falling edge of the SCLK signal. A high level on ALARM indicates that the alarm flag has been triggered on one or more channels of the device. This pin can be connected to interrupt the host input. Upon receiving an ALARM interrupt, the alarm flag registers are examined to identify which channels have an alarm condition. Each channel on the devices supports two independently programmable alarms – a low alarm and a high alarm – with separate hysteresis settings for each alarm threshold. If the alarm feature is disabled, the ALARM pin can be left floating.

The TPAFE51736 features programmable high/low alarm thresholds with hysteresis (H) for robust out-of-range detection: a high alarm triggers when the digital output exceeds the upper limit (T+H) and resets only when the value falls to or below (T-H-2), while a low alarm activates below the lower limit (T-H-1) and clears upon reaching (T+H+1), with the asymmetric reset thresholds (±1 LSB offset) preventing noise-induced false triggers. These alarms support interrupt-driven monitoring for critical applications like overvoltage protection, with thresholds configurable via SPI.

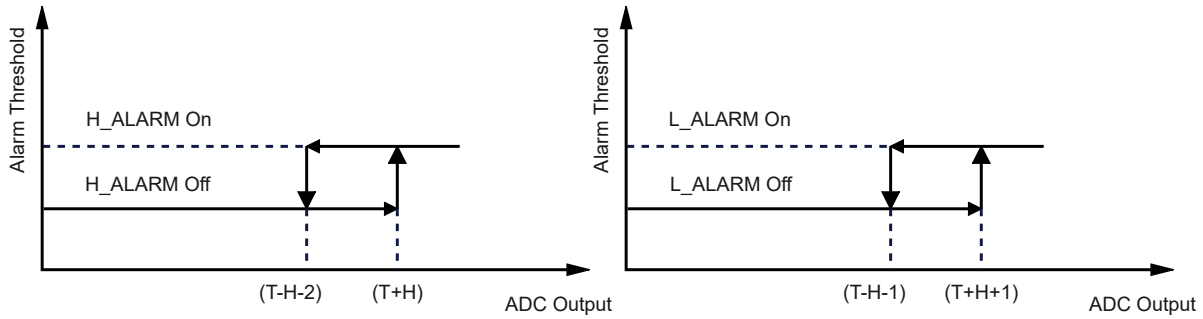
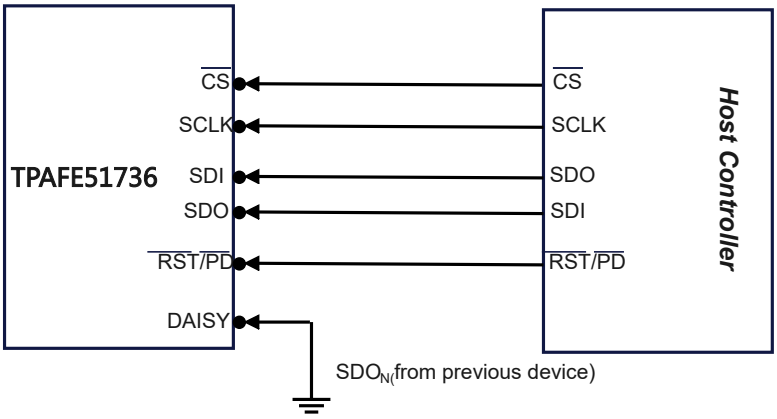


Figure 31. High-ALARM and Low-ALARM Hysteresis

Device Functional Modes

Device Interface
Digital Pin Description



- $\overline{CS}$ (input)
  The $\overline{CS}$ signal serves as an active-low, chip-select signal. It also functions as a control signal to initiate a conversion on the falling edge. Each data frame starts with the falling edge of the $\overline{CS}$ signal. In the previous frame, the analog input channel slated for conversion is configured. As the $\overline{CS}$ signal falls, the devices sample the input signal from the designated channel, and a conversion is triggered using the internal clock. Throughout this conversion process, the settings for the subsequent data frame can be input. When the $\overline{CS}$ signal is in a high state, the ADC is in an idle state.
- $\overline{SCLK}$ (input)
  This pin serves as the external clock input for the data interface. All synchronous interactions with the device are synchronized to the falling edges of the SCLK signal.
- $\overline{SDI}$ (input)
  SDI (Serial Data Input) is the input line for serial data. It is employed by the host processor to set the internal device registers for configuring the device. During the beginning of each data frame, the $\overline{CS}$ (Chip Select) signal becomes low, and the data on the SDI line is read by the device at each falling edge of the SCLK (Serial Clock) signal for the ensuing 16 SCLK cycles. Any modifications made to the device configuration in a specific data frame take effect on the device upon the subsequent falling edge of the $\overline{CS}$ signal.
- SDO (output)
  SDO (Serial Data Output) is the output line for serial data. The device utilizes SDO to transmit conversion data. The size of the data output frame varies depending on the register setting for the SDO format. When $\overline{CS}$ (Chip Select) is at a low level, it releases the SDO pin from the Hi-Z (High Impedance) state. SDO stays low for the first 15 falling edges of SCLK (Serial Clock). The Most Significant Bit (MSB) of the output data stream is clocked out on SDO during the 16th falling edge of SCLK, followed by the subsequent data bits on each falling edge thereafter. The SDO line returns to a low state after the complete data frame is output and goes back to a Hi-Z state when $\overline{CS}$ goes high.
- DAISY (Input)
  The DAISY pin serves as a serial input in daisy-chain mode. In scenarios where multiple devices are connected in a daisy-chain configuration, the DAISY pin of the initial device in the chain is linked to GND. Subsequently, the DAISY pin of each successive device is connected to the SDO (Serial Data Output) pin of the preceding device. The SDO output of the last device in the chain is then connected to the SDI (Serial Data Input) of the host processor. In stand-alone device applications, the DAISY pin is simply connected to GND.

- $\overline{RST}$ /$\overline{PD}$ (input)
  $\overline{RST}$ /$\overline{PD}$ is a dual-function pin. It can be utilized to put the device into power-down mode or to reset the program registers to their default values.
  To enter power-down mode, this pin should be pulled low for at least 600 ns. This action is asynchronous to the clock, allowing it to be triggered at any time. In power-down mode, the device ignores any activity on the digital input pins, except for the $\overline{RST}$ /$\overline{PD}$ pin.
  To perform a reset (RST) of the program registers, the $\overline{RST}$ /$\overline{PD}$ pin needs to be pulled low for no more than 200 ns. Similar to the power-down mode, this action is asynchronous to the clock. Once the pin is pulled back to a logic high state, the devices enter normal mode with the program registers reset to their default values.
  Upon returning to a logic high level, the devices wake up in a default state, and to configure the device, a valid write operation on the program register is necessary, followed by an appropriate command (AUTO_RST or MAN) to initiate conversions.

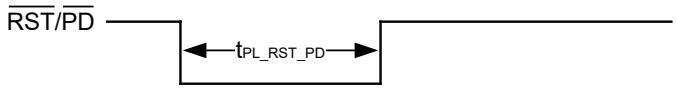


Figure 32. $\overline{RST}$/$\overline{PD}$ Pin Timing

Table 6. $\overline{RST}$/$\overline{PD}$ Pin Functionality

Condition	Device Mode
120 ns < $t_{PL\_RST\_PD}$ ≤ 200 ns	The device is in RST mode and does not enter PWR_DN mode.
200 ns < $t_{PL\_RST\_PD}$ < 600 ns	The device is in RST mode and may or may not enter PWR_DN mode. NOTE: This setting is not recommended.
$t_{PL\_RST\_PD}$ ≥ 600 ns	The device enters PWR_DN mode and the program registers are reset to the default value.

Data Acquisition Example

An example of how a host processor can utilize the device interface to set up the internal registers, perform configuration, and acquire data for sampling a specific input channel is shown below:

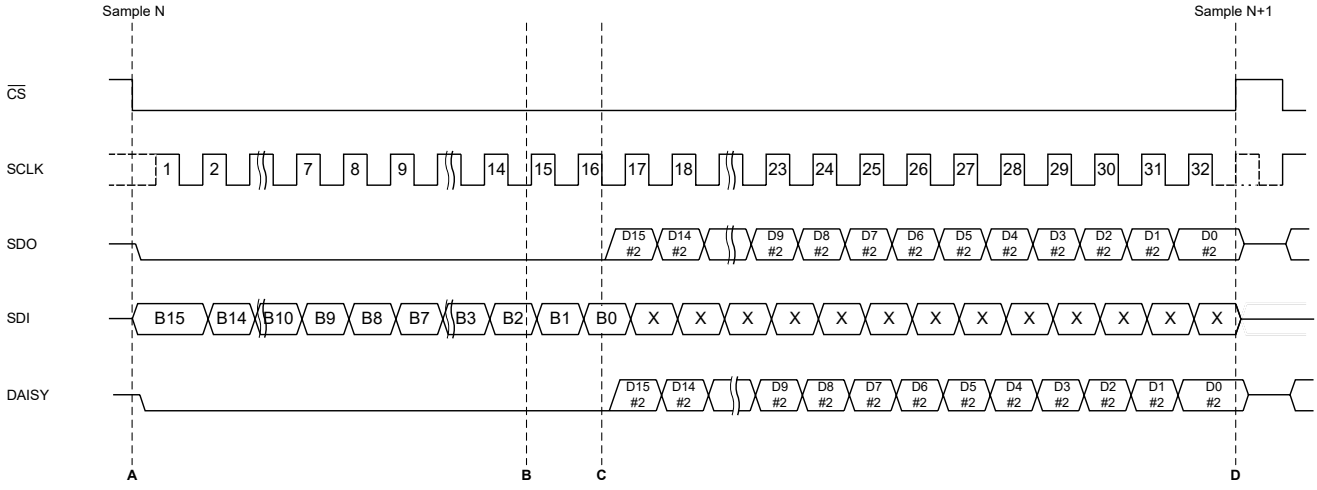


Figure 33. Device Operation Using the Serial Interface Timing Diagram

- **Phase A:** During the data conversion frame initiation, triggered by a falling edge of the $\overline{CS}$ signal, the host instructs the device to sample the analog input signal. This sampled signal is then converted by the ADC using an internal oscillator clock. The specific analog input channel for conversion in this frame is determined by the selection made in the previous data frame. Simultaneously, the host can configure the device for the next conversion by providing input through the SDI and SCLK inputs. The data on the SDI line is latched into the device at each falling edge of the SCLK signal for the next 16 SCLK cycles. Throughout these initial cycles, the SDO line remains low as the device doesn't output internal conversion data during this period.
- **Phase B:** Within the initial 16 SCLK cycles, the internal conversion process is completed, and the data within the converter is now available. However, the device withholds the output of data bits on the SDO line until the 16th falling edge is detected on the SCLK input. It is crucial that the 16th SCLK falling edge occurs after the internal conversion is finished to ensure accurate data output from the device. Consequently, the SCLK frequency is limited to a maximum value, as specified in the timing specifications to maintain proper functioning.
- **Phase C:** At the 16th falling edge of the SCLK signal, the device retrieves the LSB of the input word from the SDI line. No further readings are taken from the SDI line for the remainder of the data frame. Simultaneously, on the same edge, the MSB of the conversion data is transmitted on the SDO line, ready to be read by the host processor during the subsequent falling edge of the SCLK signal. For a 16-bit output data sequence, the LSB can be accessed on the 32nd SCLK falling edge. The SDO maintains a 0 output on subsequent SCLK falling edges until the initiation of the next conversion.
- **Phase D:**After receiving the internal data from the device, the host ends the data frame by setting the $\overline{CS}$ signal to a high state. Subsequently, the SDO output enters a high-impedance (Hi-Z) state until the start of the next data frame.

Host-to-Device Connection Topologies

The TPAFE51736 features a highly configurable digital interface, enabling flexible communication with host controllers via SPI. The figure below shows a standard single-device connection, systems often require multi-ADC configurations under constrained microcontroller GPIO resources. To address this, both daisy-chain and star topologies are supported by this device.

Daisy-Chain Topology

The TPAFE51736 supports a daisy-chain mode where multiple devices share common $\overline{CS}$ and SCLK lines while cascading data through their DAISY_IN/SDO connections - the DAISY_IN of the first ADC is grounded, each subsequent ADC's SDO drives the DAISY_IN of the next device, and the SDO of the final ADC returns to the host controller, creating a simple shift-register topology without requiring special configuration. This approach minimizes host GPIO requirements but introduces timing constraints: designers must account for cumulative propagation delays through the chain and maintain clean clock distribution to ensure reliable data capture at the host, particularly important in systems where conversion results must be synchronized across multiple ADCs.

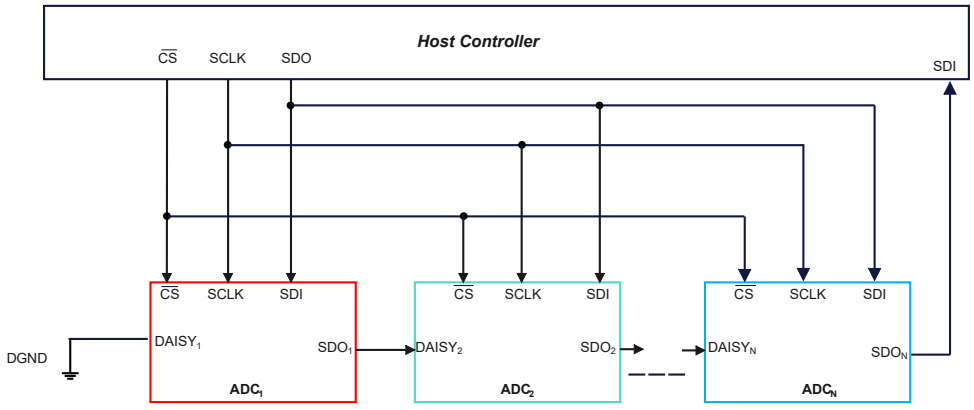


Figure 34. Daisy-Chain Connection Schematic

A typical timing diagram for three devices connected in daisy-chain mode is shown below.

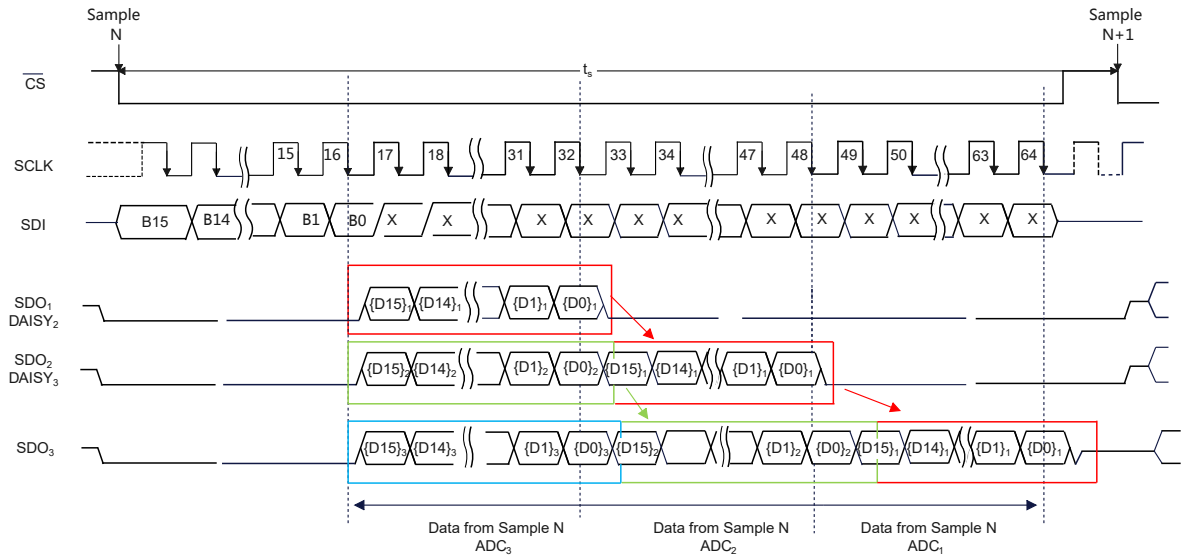


Figure 35. Three Devices Connected in Daisy-Chain Mode Timing Diagram

On the falling edge of $\overline{CS}$, all ADCs simultaneously sample their analog inputs and begin conversion. During the first 16 SCLK cycles, the host can configure the next conversion by writing register settings via the shared SDI line while all SDO outputs remain low. Post-conversion, each ADC loads its 16-bit result into an internal shift register. At the 16th SCLK falling edge, the MSB is output on each ADC's SDO, with subsequent bits shifted out on later edges—each ADC simultaneously shifts in data from its DAISY_IN while shifting out its own result. This creates a pipelined output stream where the host receives data in reverse order . For N devices, 16×N SCLK cycles are needed to read all results, plus 16 cycles for the next configuration, totaling 16×(N+1) cycles (e.g., 64 cycles for 3 ADCs). Throughput scales inversely with chain length, making this topology ideal for GPIO-limited systems where latency is secondary to channel density.

The following points must be noted about the daisy-chain configuration illustrated below.

- Since all SDI pins are tied together, every ADC in the chain receives the same configuration data. To enable per-device settings, additional host GPIOs must independently control each ADC's SDI, increasing system complexity.
- Beyond the four devices, excessive capacitive loading on shared $\overline{CS}$, SCLK, and SDO lines can introduce signal integrity issues (rise/fall time degradation, clock skew). To mitigate this, insert digital buffers (e.g., CMOS level shifters) on host-driven signals (CS/SCLK) to maintain robust timing margins. Ensure proper impedance matching and minimize trace lengths to reduce reflections.

Star Topology

The star topology configuration (Figure 94) connects all ADC devices' SDI and SCLK lines in parallel to the host controller's corresponding outputs, while their SDO outputs are wire-OR'd together to the host's SDI input. Each ADC maintains an independent chip select ($\overline{CS}$) line from the controller, enabling individual device addressing. This architecture provides simultaneous configuration capability through the shared SDI/SCLK bus while allowing selective data retrieval, avoiding the daisy-chain's cumulative latency penalty. However, the wire-OR SDO connection requires careful attention to bus contention risks and proper tri-state management during $\overline{CS}$ desertion, making robust pull-up resistors and clean signal timing essential for reliable operation in multi-device systems.

The star topology maintains the same timing as standalone operation, with each ADC's data frame controlled by its dedicated $\overline{CS}$ line while sharing common SDI and SCLK lines with other devices. The host must strictly enforce single-device activation

(only one $\overline{CS}$ low at a time) to prevent bus contention on the shared, wire-OR'd SDO line, as deselected devices enter Hi-Z state when $\overline{CS}$ is high. This architecture enables parallel configuration and random-access polling without daisy-chain latency, but requires N+2 GPIOs (for N ADCs) and careful $\overline{CS}$ sequencing to maintain signal integrity, making it ideal for systems needing low-latency access to individual converters despite increased GPIO overhead. The shared SDO line's capacitive loading (typically limiting SCLK to <20MHz for N>4 devices) must be properly managed with appropriate pull-ups and layout considerations.

Restricting the star configuration to four devices maximum due to increasing capacitive loading on shared SDO and SCLK lines is recommended, which can degrade signal integrity and cause timing violations. For this case, insert digital buffers on both SCLK (host output) and SDO (shared bus).

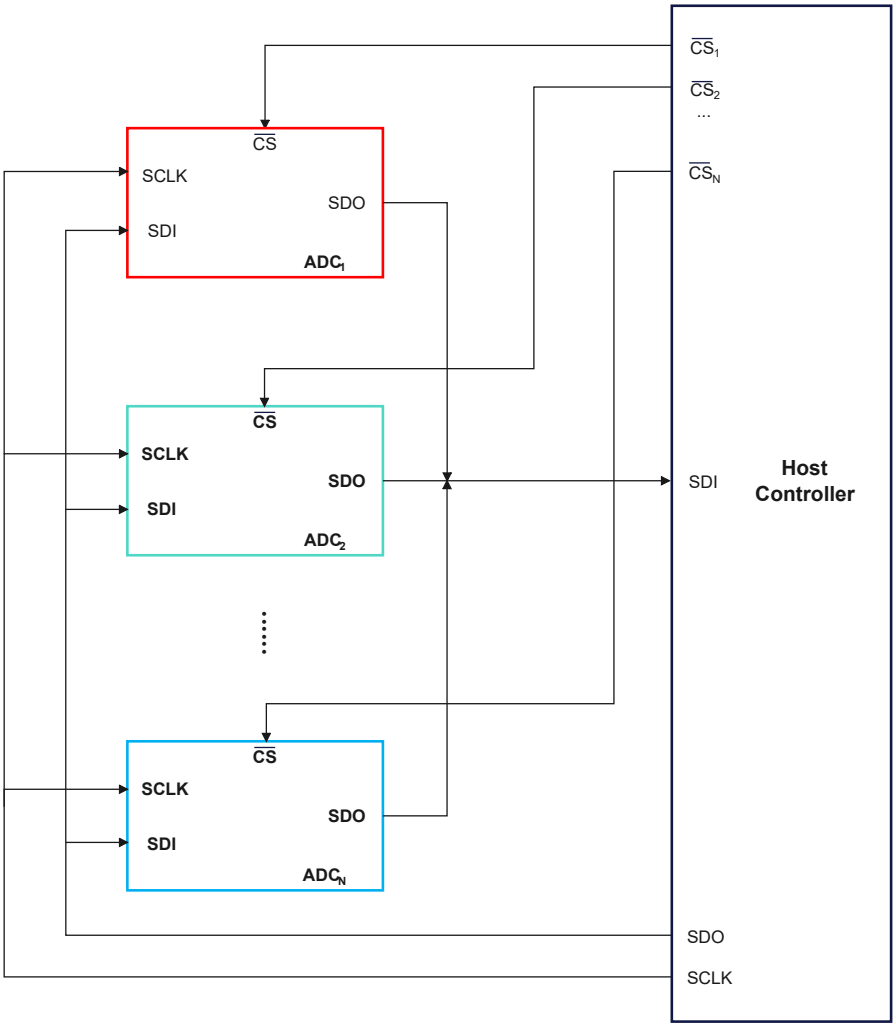
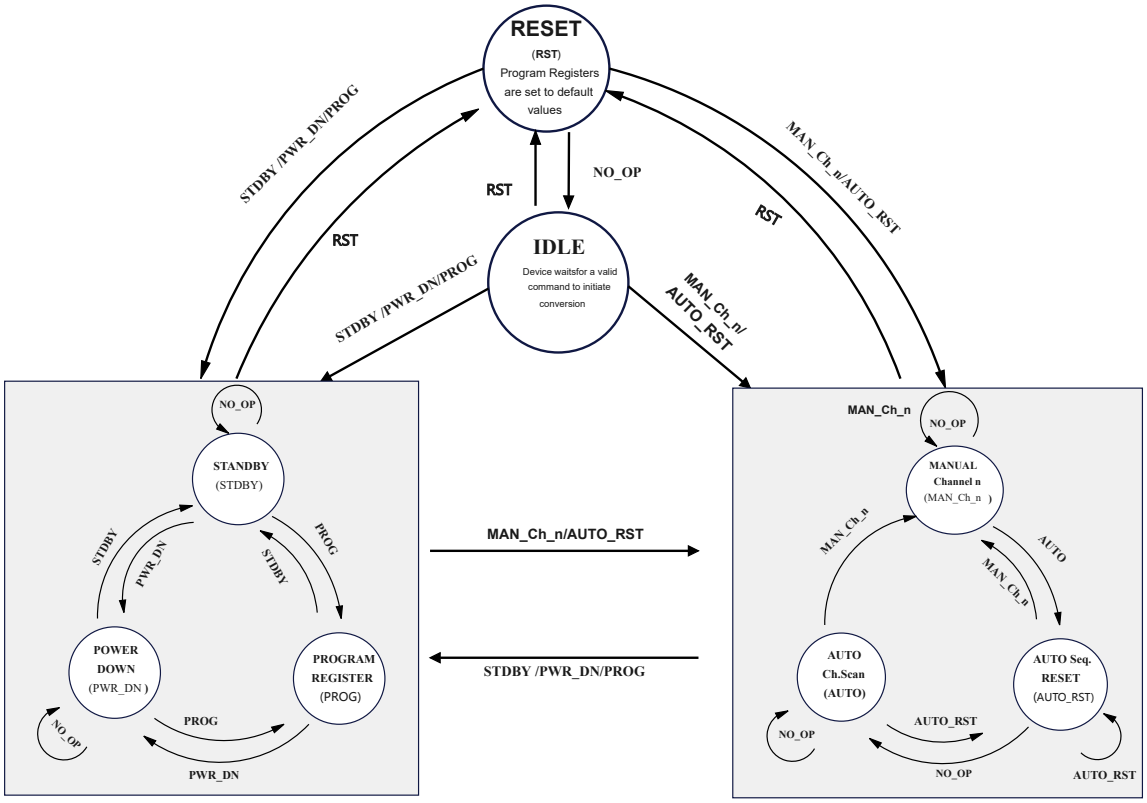


Figure 36. Star Connection Schematic

Device Modes

The TPAFE51736 offers various software-programmable modes of operation. Upon power-up, the device enters idle mode, where it remains inactive until receiving a command from the user. All commands to transition between different modes are listed in the command register. Following power-up, the program registers are initialized with default values, necessitating proper configuration settings before initiating any conversions.



Continued Operation in the Selected Mode (NO_OP)

Continuously holding the SDI line low, equivalent to writing zeros to all 16 bits, while the device is operational maintains the device in the last selected mode (STDBY, PWR_DN, AUTO_RST, or MAN_Ch_n). In this mode, the device holds the settings already configured in the program registers.

In the event of a NO_OP condition during a read or write operation in the program register (PROG mode), the device retains the current settings of the program registers. Subsequently, the device returns to IDLE mode, awaiting the user to issue a proper command for executing program register read or write configurations.

Frame Abort Condition (FRAME_ABORT)

As described in the Data Acquisition Example section, the digital interface of the device is structured so that each data frame begins with a falling edge of the $\overline{CS}$ signal. Within the first 16 SCLK cycles, the device reads the 16-bit command word on the SDI line. The device postpones the execution of the command until the reception of the last bit of the command, which is captured on the 16th SCLK falling edge. Throughout this process, the $\overline{CS}$ signal must remain low. If, for any reason, the $\overline{CS}$ signal transitions to a high state before the data transmission concludes, the device enters an INVALID state, awaiting a

proper command. This state is referred to as the FRAME_ABORT condition. While operating in the INVALID mode, any read operation on the device returns invalid data on the SDO line. The output of the ALARM pin continues to reflect the status of the input signal on the previously selected channel.

STANDBY Mode (STDBY)

The TPAFE51736 features a low-power standby mode (STDBY) where a portion of the circuit is powered down. Notably, the internal reference and buffer remain active, enabling the devices to fast power up within 10 µs upon exiting the STDBY mode. When transitioning out of STDBY mode, the program registers are not reset to their default values.

To activate the STDBY mode, perform a valid write operation to the command register with the STDBY command set to 8200h. This command is executed, and the device enters STDBY mode on the subsequent rising edge of the $\overline{CS}$ signal following the write operation. The device remains in STDBY mode if no valid conversion command (AUTO_RST or MAN_Ch_n) is executed and SDI remains low during the subsequent data frames. In STDBY mode, the program register settings can be modified (as detailed in the Program Register Read/Write Operation section) using 16 SCLK cycles. However, if 32 complete SCLK cycles are provided, the device outputs invalid data on the SDO line since there is no ongoing conversion in STDBY mode. Nonetheless, the program register read operation can proceed normally during this mode.

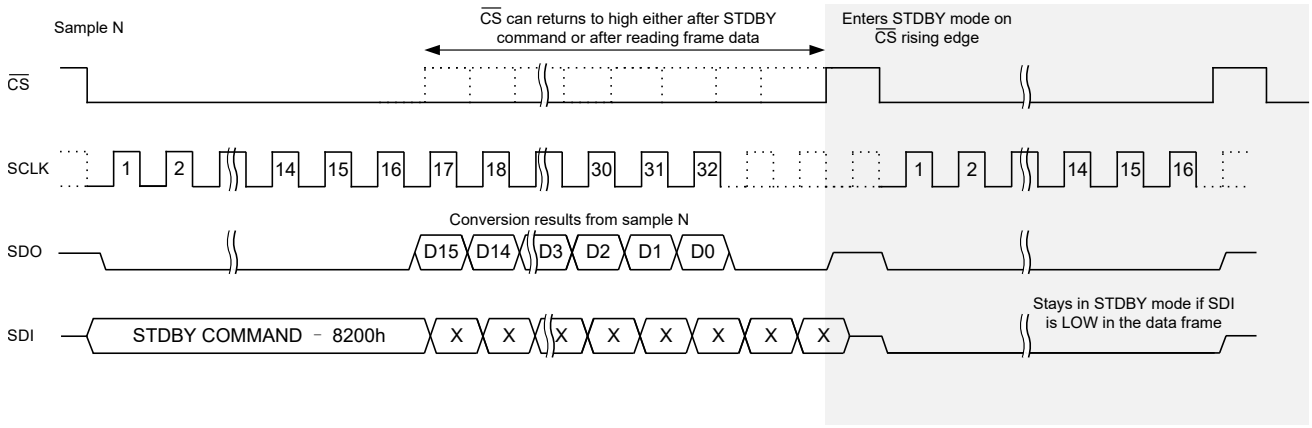


Figure 37. Enter and Remain in STDBY Mode Timing Diagram

To exit STDBY mode, execute a valid 16-bit write command to enter either the auto (AUTO_RST) or manual (MAN_CH_n) scan mode. The device initiates the exit from STDBY mode at the following rising edge of the signal. Upon the subsequent falling edge of $\overline{CS}$, the device captures the analog input from the channel specified by the MAN_CH_n command or the initial channel in the AUTO_RST mode sequence. To ensure accurate sampling of the input signal, maintain the $\overline{CS}$ signal width at a minimum of 10 µs after exiting STDBY mode. This duration allows the internal circuitry of the device to be fully powered up and properly biased before the sample is taken. The data output for the selected channel can be read within the same data frame.

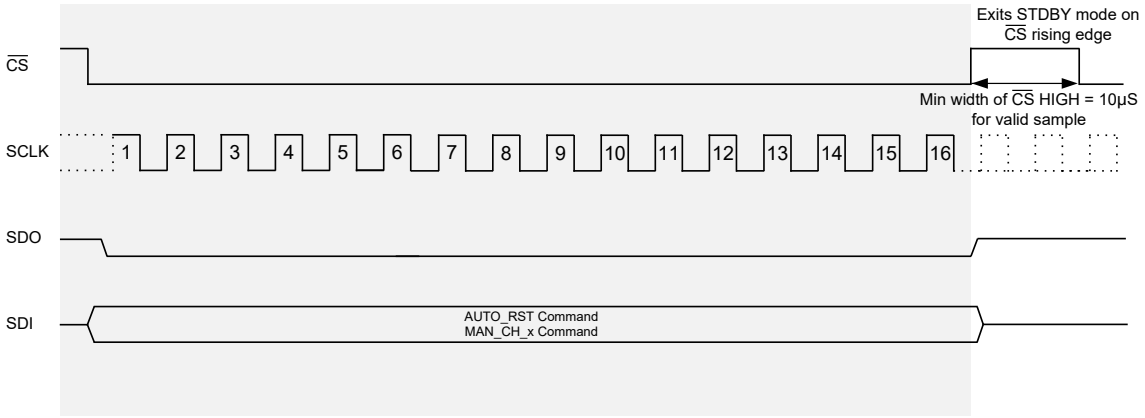


Figure 38. Exit STDBY Mode Timing Diagram

Power-Down Mode (PWR_DN)

The TPAFE51736 offers both hardware and software power-down modes (PWR_DN), during which all internal circuitry, including the internal reference and buffer, is powered down. Upon exiting PWR_DN mode, a minimum of 10 ms is required for the device to power up and convert the selected analog input channel, provided the device is operating in the internal reference mode ($\overline{REFSEL}$ = 0). The hardware power mode is detailed in the $\overline{RST}$/$\overline{PD}$ (Input) section. The primary distinction between the hardware and software power-down modes is that the program registers are reset to default values when the devices wake up from hardware power-down, whereas the previous settings of the program registers are retained when waking up from software power-down.

To initiate PWR_DN mode through software, perform a valid write operation on the command register with a software PWR_DN command of 8300h. The command is executed, causing the device to enter PWR_DN mode on the subsequent$\overline{CS}$ rising edge. The device remains in PWR_DN mode if no valid conversion command (AUTO_RST or MAN_Ch_n) is executed and SDI remains low during the subsequent data frames. When operating in PWR_DN mode, the program register settings can be updated using 16 SCLK cycles. However, if 32 complete SCLK cycles are provided, the device returns invalid data on the SDO line because there is no ongoing conversion in PWR_DN mode. The program register read operation can still take place normally during this mode.

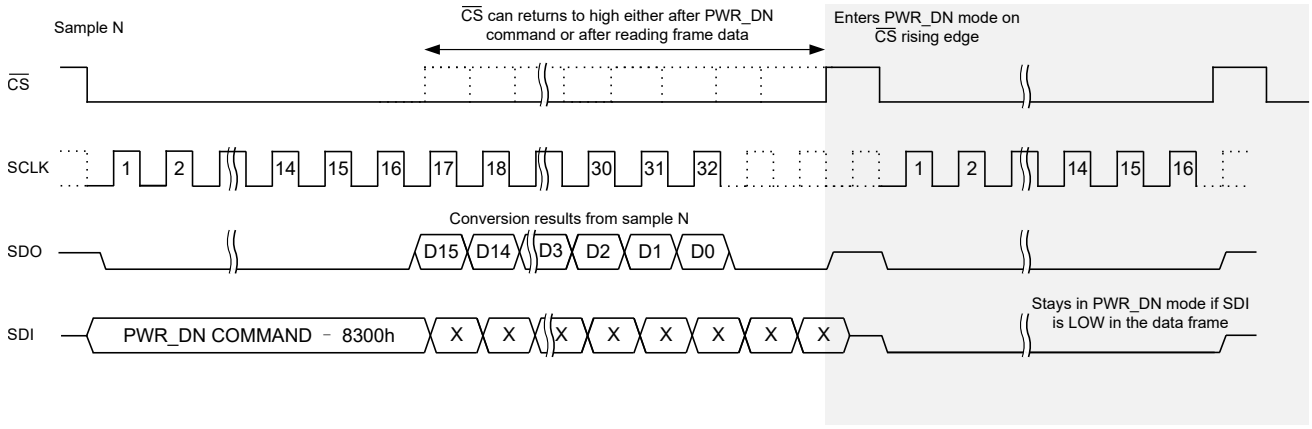


Figure 39. Enter and Remain in PWR_DN Mode Timing Diagram

To exit PWR_DN mode, execute a valid 16-bit write command. The device transitions out of PWR_DN mode on the following $\overline{CS}$ rising edge. When operating in internal reference mode ($\overline{REFSEL}$ = 0), it takes approximately 10 ms for the device to power up the reference and other internal circuits, reaching the necessary accuracy before valid conversion data is output for the selected input channel.

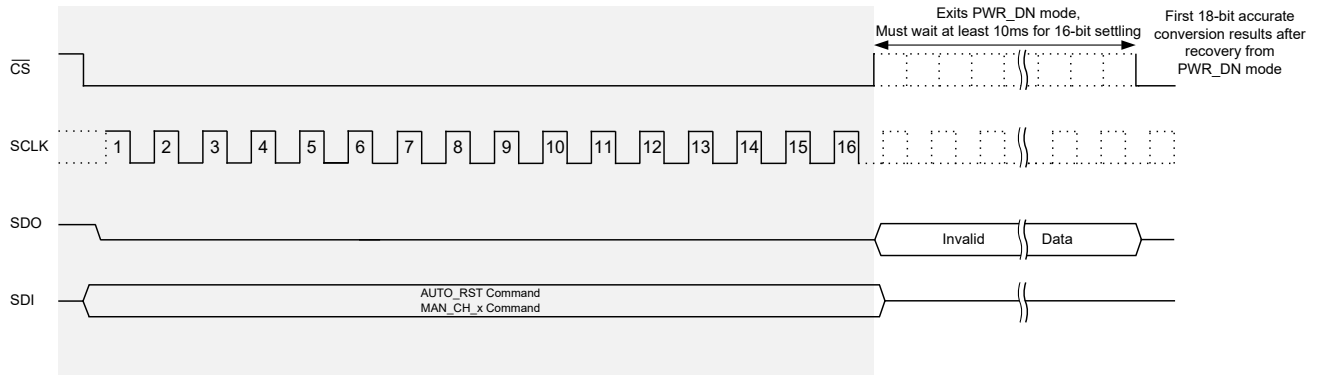


Figure 40. Exit PWR_DN Mode Timing Diagram

Auto Channel Enable with Reset (AUTO_RST)

The TPAFE51736 can be configured to automatically scan the input signal on all analog channels by issuing a valid auto channel sequence with a reset (AUTO_RST, A000h) command in the command register, as illustrated in. In this process, the $\overline{CS}$ signal can be raised high immediately after the AUTO_RST command or after reading the output data of the frame. However, to ensure accurate acquisition and conversion of the input signal on the first selected channel in the next data frame, the command frame must be a complete frame of 32 SCLK cycles.

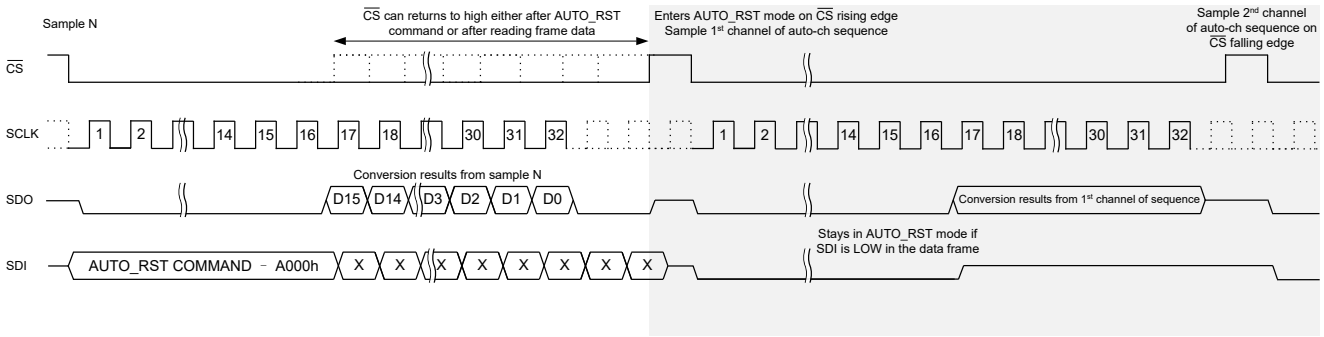


Figure 41. Enter AUTO_RST Mode Timing Diagram

The devices continues operating in AUTO_RST mode if no other valid command is executed and SDI is kept low, during subsequent data frames. If the AUTO_RST command is executed again at any time during this mode, the sequence of the scanned channels is reset. The devices return to the lowest count channel of the auto-scan sequence in the program register and repeat the sequence. The timing diagram below illustrates this behavior using an example where channels 0 to 2 are selected in the auto sequence.

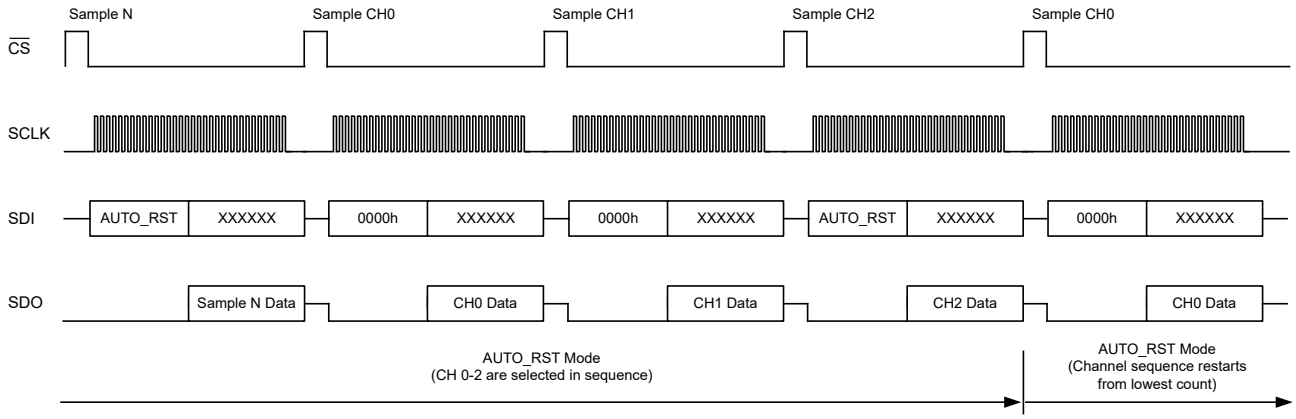


Figure 42. Device Operation Example in AUTO_RST Mode

Manual Channel n Select (MAN_Ch_n)

The TPAFE51736 can be configured to convert a specific analog input channel by operating in manual channel n scan mode (MAN_Ch_n). This configuration is achieved by writing a valid manual channel n select command (MAN_Ch_n) in the command register. In the below timing diagram, the $\overline{CS}$ signal can be pulled high immediately after the MAN_Ch_n command or after reading the output data of the frame. However, for accurate acquisition and conversion of the input signal on the next channel, the command frame must be a complete frame of 32 SCLK cycles.

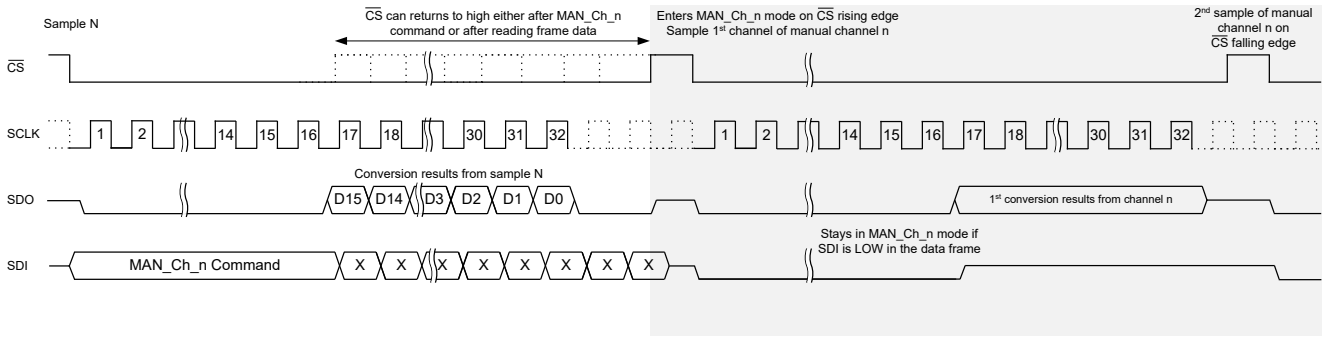


Figure 43. Enter MAN_Ch_n Scan Mode Timing Diagram

Upon executing the manual channel n select command (MAN_Ch_n), the devices sample the analog input on the specified channel during the $\overline{CS}$ falling edge of the subsequent data frame. The input voltage range for each channel in the MAN_Ch_n mode can be configured by setting the related program registers. If no other valid command is executed and SDI is kept low during subsequent data frames, the device continues to sample the analog input on the same channel. The timing diagram below illustrates this behavior, using channel 1 as an example in the manual sequencing mode.

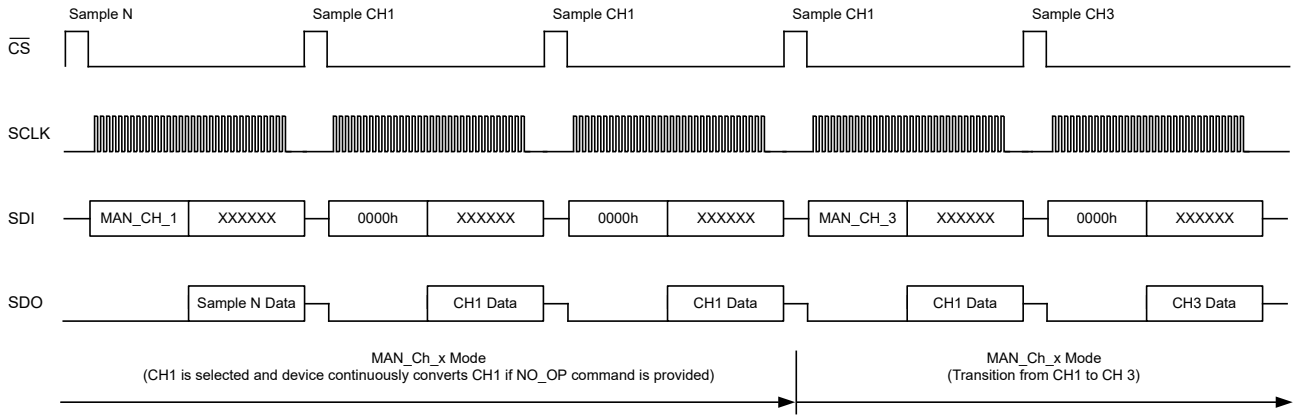


Figure 44. Device Operation in MAN_Ch_n Mode

Channel Sequencing Modes

The TPAFE51736 provides two channel sequencing modes: AUTO_RST and MAN_Ch_n.

In AUTO_RST mode, the channel number automatically increments in every subsequent frame. As explained in the Auto-Scan Sequencing Control Registers section, the analog inputs can be selected for an automatic scan with a register setting. The device automatically scans only the selected analog inputs in ascending order. The unselected analog input channels can also be powered down to optimize power consumption in this mode of operation. The auto-mode sequence can be reset at any time during an automatic scan using the AUTO_RST command. When the reset command is received, the ongoing auto-mode sequence is reset and restarted from the lowest selected channel in the sequence.

In MAN_Ch_n mode, the same input channel is selected during every data conversion frame. The input command words to select individual analog channels in MAN_Ch_n mode are listed in the Command Register Map. If a particular input channel is selected during a data frame, then the analog inputs on the same channel are sampled during the next data frame. The figure below illustrates the SDI command sequence for transitions from AUTO_RST to MAN_Ch_n mode.

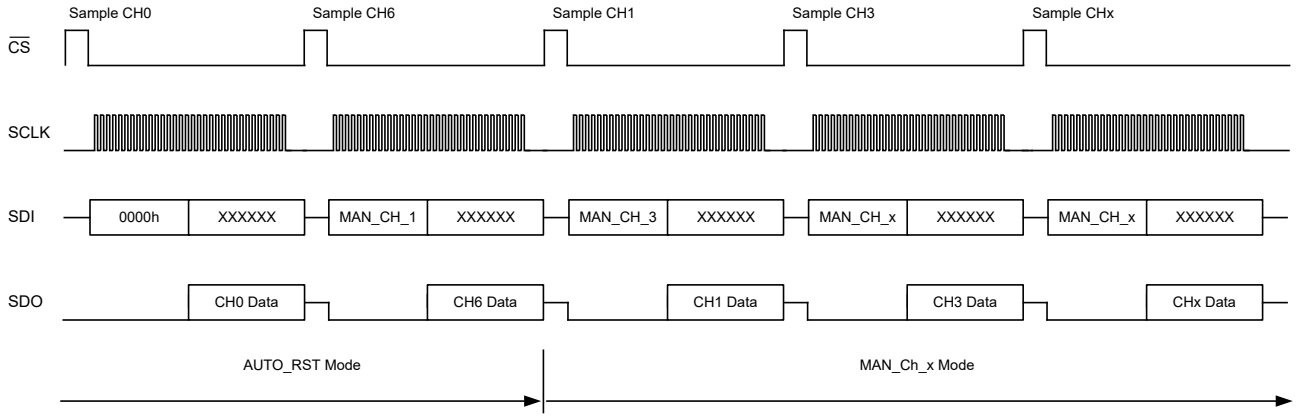


Figure 45. Transitioning from AUTO_RST to MAN_Ch_n Mode (Channels 0 and 6 are Selected for Auto Sequence)

The following figure illustrates the SDI command sequence for transitions from MAN_Ch_n to AUTO_RST mode. It's important to note that each SDI command is executed on the next $\overline{CS}$ falling edge. Additionally, an RST command can

be issued at any instant during any channel sequencing mode, and upon execution, the device is placed into a default power-up state in the next data frame.

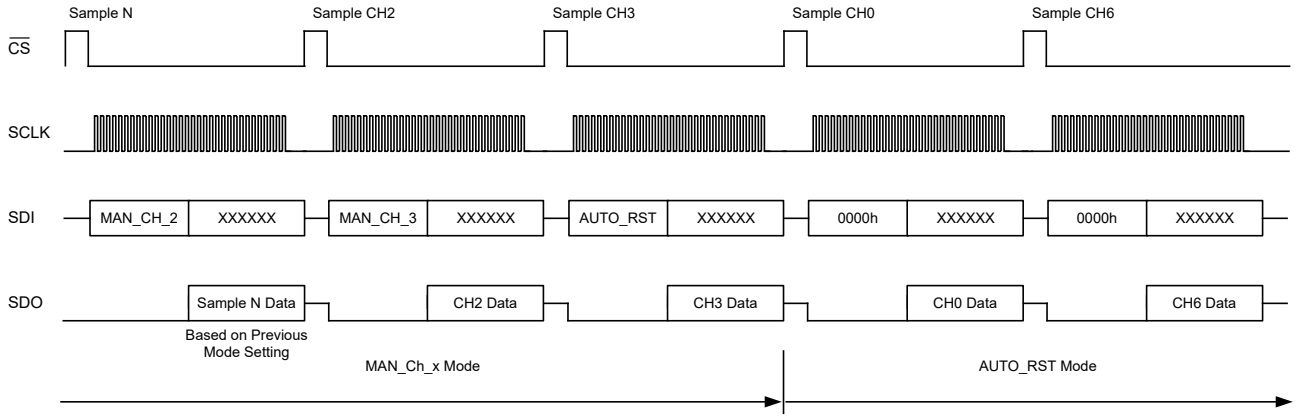


Figure 46. Transitioning from MAN_Ch_n to AUTO_RST Mode (Channels 0 and 6 are Selected for Auto Sequence)

Reset Program Registers (RST)

The TPAFE51736 offers both hardware and software reset (RST) modes, resetting all program registers to their default values. The hardware reset is achieved through a dedicated pin $\overline{RST}/\overline{PD}$ (Input).

For a software reset, the program registers can be reset during any data frame by executing a valid write operation on the command register with an RST command of 8500h. The device remains in RST mode if no valid conversion command (AUTO_RST or MAN_Ch_n) is executed, and SDI remains low during subsequent data frames. In RST mode, the program register settings can be updated using 16 SCLK cycles. However, providing 32 complete SCLK cycles results in invalid data on the SDO line, as there is no ongoing conversion in RST mode. During this mode, program register values can be read normally. To initiate a conversion on a specific analog channel using default program register settings, a valid AUTO_RST or MAN_CH_n channel selection command must be executed.

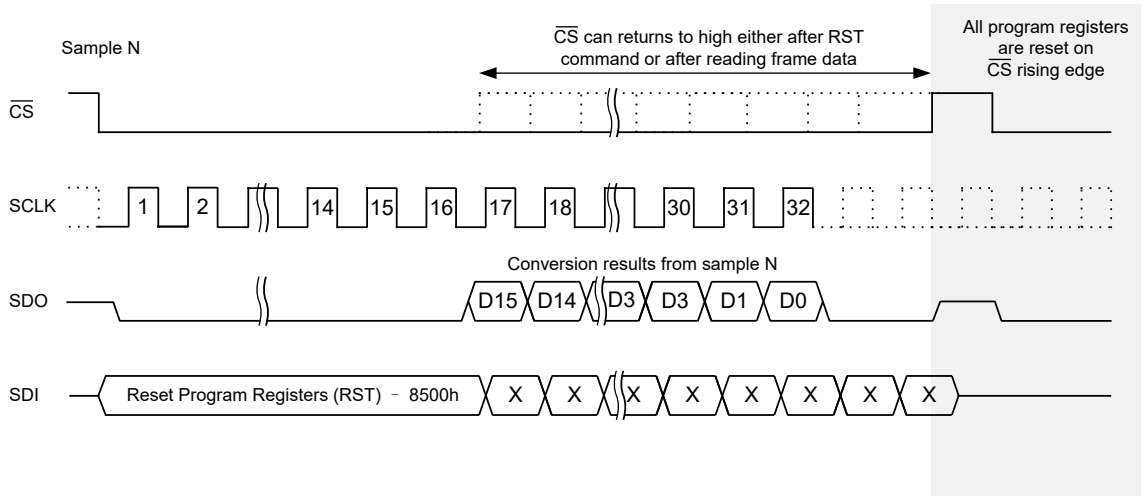


Figure 47. Reset Program Registers (RST) Timing Diagram

Register Maps

The TPAFE51736 provides two main categories: command registers and program registers.

The command registers are utilized for selecting the channel sequencing mode (AUTO_RST or MAN_Ch_n), configuring the device in standby (STDBY) or power-down (PWR_DN) mode, and performing a reset (RST) to initialize program registers to their default values.

The program registers serve various purposes, including selecting the sequence of channels for AUTO_RST mode, specifying the SDO output format, controlling input range settings for individual channels, managing the ALARM feature, reading alarm flags, and programming alarm thresholds for each channel. The program registers provide a range of configuration options for customizing the device behavior to specific requirements.

Command Registers

The command register, a write-only 16-bit register, plays a crucial role in configuring the operating modes of TPAFE51736. This register is responsible for selecting the channel sequencing mode (AUTO_RST or MAN_Ch_n), configuring the device in standby (STDBY) or power-down (PWR_DN) mode, and resetting (RST) the program registers to their default values. The table below provides a comprehensive list of all the command settings available in this register. Upon power-up or reset, the command register initializes with all bits set to 0, and the device remains in a standby state, awaiting a command to be written before entering any operational mode. The universal timing figure illustrates a typical timing diagram for writing a 16-bit command into the device. The execution of the command takes place at the conclusion of the specific data frame when the $\overline{CS}$ signal transitions to a high state.

Table 7. Command Register Map

Register	MSB Byte								LSB Byte	Command (Hex)	Operation in the Next Frame
	B15	B14	B13	B12	B11	B10	B9	B8	B[7:0]		
Continued Operation (NO_OP)	0	0	0	0	0	0	0	0	0000 0000	0000h	Continue operation in the previous mode
Standby (STDBY)	1	0	0	0	0	0	1	0	0000 0000	8200h	Device is placed into standby mode
Power Down (PWR_DN)	1	0	0	0	0	0	1	1	0000 0000	8300h	Device is powered down
Reset program registers (RST)	1	0	0	0	0	1	0	1	0000 0000	8500h	Program register is reset to default
Auto Ch. Sequence with Reset (AUTO_RST)	1	0	1	0	0	0	0	0	0000 0000	A000h	Auto mode enabled following a reset
Manual Ch 0 Selection (MAN_Ch_0)	1	1	0	0	0	0	0	0	0000 0000	C000h	Channel 0 input is selected
Manual Ch 1 Selection (MAN_Ch_1)	1	1	0	0	0	1	0	0	0000 0000	C400h	Channel 1 input is selected

Register	MSB Byte								LSB Byte	Command (Hex)	Operation in the Next Frame
	B15	B14	B13	B12	B11	B10	B9	B8	B[7:0]		
Manual Ch 2 Selection (MAN_Ch_2)	1	1	0	0	1	0	0	0	0000 0000	C800h	Channel 2 input is selected
Manual Ch 3 Selection (MAN_Ch_3)	1	1	0	0	1	1	0	0	0000 0000	CC00h	Channel 3 input is selected
Manual Ch 4 Selection (MAN_Ch_4)(1)	1	1	0	1	0	0	0	0	0000 0000	D000h	Channel 4 input is selected
Manual Ch 5 Selection (MAN_Ch_5)	1	1	0	1	0	1	0	0	0000 0000	D400h	Channel 5 input is selected
Manual Ch 6 Selection (MAN_Ch_6)	1	1	0	1	1	0	0	0	0000 0000	D800h	Channel 6 input is selected
Manual Ch 7 Selection (MAN_Ch_7)	1	1	0	1	1	1	0	0	0000 0000	DC00h	Channel 7 input is selected
Manual AUX Selection (MAN_AUX)	1	1	1	0	0	0	0	0	0000 0000	E000h	AUX channel input is selected

(1) Shading registers are not available for 4-channel version devices.

Program Registers

Program Registers

The program register, a 16-bit register, is instrumental in configuring the operating modes of the TPAFE51736. This setting of the register configures the selection of the channel sequence for AUTO_RST mode, configuration of the device ID in daisy-chain mode, choice of the SDO output format, control of input range settings for individual channels, management of the ALARM feature, reading the alarm flags, and programming the alarm thresholds for each channel. The table below provides a comprehensive list of all the program settings available in this register.Upon power-up or reset, the various program registers within the device initialize with their default values. The device remains in a standby state, waiting for a command to be written before entering any operational mode.

Program Register Read/Write Operation

The program register serves as a 16-bit read or write register in the TPAFE51736. To initiate any read or write operation to the program registers, a minimum of 24 SCLKs is required after the falling edge of $\overline{CS}$. When $\overline{CS}$ is pulled low, the SDO line also transitions low. The device interprets the command, with the first seven bits (bits 15-9) indicating the register address and the eighth bit (bit 8) specifying the write or read instruction.

During a write cycle, the next eight bits (bits 7-0) on SDI represent the desired data for the addressed register. Over the subsequent eight SCLK cycles, the device outputs this 8-bit data, confirming that it has been successfully written into the register. This readback of data provides a means of verification to ensure the accuracy of the entered data. The figure below illustrates a typical timing diagram for a program register write cycle.

Table 8. Write Cycle Command Word

Pin	Register Address (Bits 15-9)	WR/$\overline{RD}$ (Bit 8)	Data (Bits 7-0)
SDI	ADDR [6:0]	1	DIN [7:0]

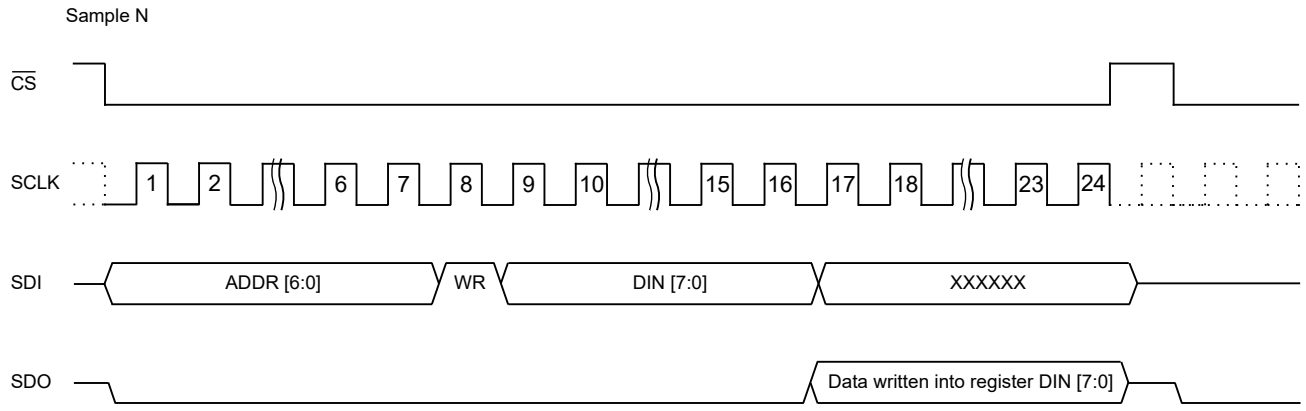


Figure 48. Program Register Write Cycle Timing Diagram

During a read cycle, the next eight bits (bits 7-0) on SDI are considered as don't care bits, and SDO remains low. Starting from the 16th SCLK falling edge and onward, SDO outputs the 8-bit data from the addressed register during the subsequent eight clocks, following an MSB-first format. The figure below presents a typical timing diagram for a program register read cycle.

Table 9. Read Cycle Command Word

Pin	Register Address (Bits 15-9)	WR/$\overline{RD}$ (Bit 8)	Data (Bits 7-0)
SDI	ADDR [6:0]	0	XXXXXXXX
SDO	0000 000	0	DOUT [7:0]

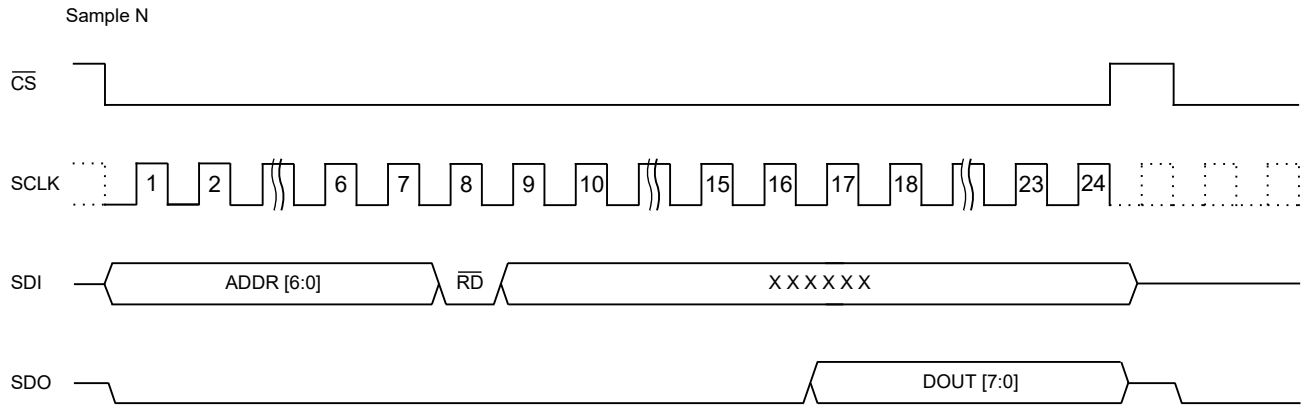


Figure 49. Program Register Read Cycle Timing Diagram

Program Registers Map

Table 10. Program Registers Map

Register	Register Address BITS[15:9]	Default Value (1)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Auto Scan Sequencing Control										
AUTO_SEQ_EN	01h	FFh	CH7_EN(2)	CH6_EN	CH5_EN	CH4_EN	CH3_EN	CH2_EN	CH1_EN	CH0_EN
Channel Power Down	02h	00h	CH7_PD	CH6_PD	CH5_PD	CH4_PD	CH3_PD	CH2_PD	CH1_PD	CH0_PD
Device Feature Selection Control										
Feature Select	03h	00h	DEV[1:0]		0	ALARM_EN0	0	SDO [2:0]		
Range Select Registers										
Channel 0 Input Range	05h	00h	0	0	0	0	Range Select Channel 0[3:0]			
Channel 1 Input Range	06h	00h	0	0	0	0	Range Select Channel 1[3:0]			
Channel 2 Input Range	07h	00h	0	0	0	0	Range Select Channel 2[3:0]			
Channel 3 Input Range	08h	00h	0	0	0	0	Range Select Channel 3[3:0]			
Channel 4 Input Range	09h	00h	0	0	0	0	Range Select Channel 4[3:0]			
Channel 5 Input Range	0Ah	00h	0	0	0	0	Range Select Channel 5[3:0]			

Channel 6 Input Range	0Bh	00h	0	0	0	0	Range Select Channel 6[3:0]			
Channel 7 Input Range	0Ch	00h	0	0	0	0	Range Select Channel 7[3:0]			
Over-range Select Registers										
Channel Overrange	0Dh	00h	CH7_OVER_RANGE_EN	CH6_OVER_RANGE_EN	CH5_OVER_RANGE_EN	CH4_OVER_RANGE_EN	CH3_OVER_RANGE_EN	CH2_OVER_RANGE_EN	CH1_OVER_RANGE_EN	CH0_OVER_RANGE_EN
LPF Bandwidth Configuration Registers										
LPF Bandwidth Configuration	0Eh	01h	0	0	0	0	0	0	Bandwidth Select [1:0]	
CRC Configure Registers										
CRC Configure	0Fh	00h	CRC Error	0	0	0	0	0	0	CRC_EN
Alarm Flag Registers (Read-only)										
ALARM Overview Tripped-Flag	10h	00h	Tripped Alarm Flag Ch7	Tripped Alarm Flag Ch6	Tripped Alarm Flag Ch5	Tripped Alarm Flag Ch4	Tripped Alarm Flag Ch3	Tripped Alarm Flag Ch2	Tripped Alarm Flag Ch1	Tripped Alarm Flag Ch0
ALARM Ch 0-3 Tripped-Flag	11h	00h	Tripped Alarm Flag Ch0 Low	Tripped Alarm Flag Ch0 High	Tripped Alarm Flag Ch1 Low	Tripped Alarm Flag Ch1 High	Tripped Alarm Flag Ch2 Low	Tripped Alarm Flag Ch2 High	Tripped Alarm Flag Ch3 Low	Tripped Alarm Flag Ch3 High
ALARM Ch 0-3 Active-Flag	12h	00h	Active Alarm Flag Ch0 Low	Active Alarm Flag Ch0 High	Active Alarm Flag Ch1 Low	Active Alarm Flag Ch1 High	Active Alarm Flag Ch2 Low	Active Alarm Flag Ch2 High	Active Alarm Flag Ch3 Low	Active Alarm Flag Ch3 High
ALARM Ch 4-7 Tripped-Flag	13h	00h	Tripped Alarm Flag Ch4 Low	Tripped Alarm Flag Ch4 High	Tripped Alarm Flag Ch5 Low	Tripped Alarm Flag Ch5 High	Tripped Alarm Flag Ch6 Low	Tripped Alarm Flag Ch6 High	Tripped Alarm Flag Ch7 Low	Tripped Alarm Flag Ch7 High
ALARM Ch 4-7 Active-Flag	14h	00h	Active Alarm Flag Ch4 Low	Active Alarm Flag Ch4 High	Active Alarm Flag Ch5 Low	Active Alarm Flag Ch5 High	Active Alarm Flag Ch6 Low	Active Alarm Flag Ch6 High	Active Alarm Flag Ch7 Low	Active Alarm Flag Ch7 High
Alarm Threshold Registers										

Ch 0 Hysteresis	15h	00h	CH0_HYST[7:0]
Ch 0 High Threshold MSB	16h	FFh	CH0_HT[15:8]
Ch 0 High Threshold LSB	17h	FFh	CH0_HT[7:0]
Ch 0 Low Threshold MSB	18h	00h	CH0_LT[15:8]
Ch 0 Low Threshold LSB	19h	00h	CH0_LT[7:0]
…	…	…	… See the *Alarm Threshold Setting Registers*for details regarding the ALARM threshold settings registers. …
Ch 7 Hysteresis	38h	00h	CH7_HYST[7:0]
Ch 7 High Threshold MSB	39h	FFh	CH7_HT[15:8]
Ch 7 High Threshold LSB	3Ah	FFh	CH7_HT[7:0]
Ch 7 Low Threshold MSB	3Bh	00h	CH7_LT[15:8]
Ch 7 Low Threshold LSB	3Ch	00h	CH7_LT[7:0]
Command Read Back (Read-only)			
Command Read Back	3Fh	00h	COMMAND_WORD[7:0]
Open Detection Enable			

Open Detection Configure	78h	00h	CH7_OPEN_DETECTION_EN	CH6_OPEN_DETECTION_EN	CH5_OPEN_DETECTION_EN	CH4_OPEN_DETECTION_EN	CH3_OPEN_DETECTION_EN	CH2_OPEN_DETECTION_EN	CH1_OPEN_DETECTION_EN	CH0_OPEN_DETECTION_EN
Open Detected (Read-only)										
Open Detected	79h	00h	CH7_OPEN	CH6_OPEN	CH5_OPEN	CH4_OPEN	CH3_OPEN	CH2_OPEN	CH1_OPEN	CH0_OPEN
Open Detection Mode										
Open Detection Mode	7Ah	00h	Open Detection Mode[7:0]							
Open Detected Threshold										
Open Detect Threshold	7Bh	00h	0	0	Open Detect Threshold[5:0]					
Status										
Status	7Dh	00h	0	0	0	0	0	Open Detected	ALARM Overview Tripped-Flag	CRE Error Detected

(1) Shading registers are not available for 4-channel version devices.

Auto-Scan Sequence Enable Register (address = 01h)

In AUTO_RST mode, the device automatically scans the preselected channels in ascending order, with a new channel chosen for every conversion. Each specific channel can be selectively included in the auto-channel sequencing. For channels not selected for auto-sequencing, the analog front-end circuitry can be individually powered down.

This register selects individual channels for sequencing in AUTO_RST mode. The default value for this register is FFh, implying that, in the default condition, all channels are included in the auto-scan sequence. If no channels are included in the auto sequence (i.e., the value for this register is 00h), then channel 0 is selected for conversion by default.

Table 11. AUTO_SEQ_EN Register

Bit	Field	Type	Reset	Description
7	CH7_EN	R/W	1h	Channel 7 enable. 0 = Channel 7 is not selected for sequencing in AUTO_RST mode 1 = Channel 7 is selected for sequencing in AUTO_RST mode
6	CH6_EN	R/W	1h	Channel 6 enable. 0 = Channel 6 is not selected for sequencing in AUTO_RST mode 1 = Channel 6 is selected for sequencing in AUTO_RST mode
5	CH5_EN	R/W	1h	Channel 5 enable. 0 = Channel 5 is not selected for sequencing in AUTO_RST mode 1 = Channel 5 is selected for sequencing in AUTO_RST mode
4	CH4_EN	R/W	1h	Channel 4 enable. 0 = Channel 4 is not selected for sequencing in AUTO_RST mode 1 = Channel 4 is selected for sequencing in AUTO_RST mode
3	CH3_EN	R/W	1h	Channel 3 enable. 0 = Channel 3 is not selected for sequencing in AUTO_RST mode 1 = Channel 3 is selected for sequencing in AUTO_RST mode
2	CH2_EN	R/W	1h	Channel 2 enable. 0 = Channel 2 is not selected for sequencing in AUTO_RST mode 1 = Channel 2 is selected for sequencing in AUTO_RST mode
1	CH1_EN	R/W	1h	Channel 1 enable. 0 = Channel 1 is not selected for sequencing in AUTO_RST mode 1 = Channel 1 is selected for sequencing in AUTO_RST mode
0	CH0_EN	R/W	1h	Channel 0 enable. 0 = Channel 0 is not selected for sequencing in AUTO_RST mode 1 = Channel 0 is selected for sequencing in AUTO_RST mode

(1) Shading registers are not available for 4-channel version devices.

Channel Power Down Register (address = 02h)

This register powers down individual channels that are not included for sequencing in AUTO_RST mode. The default value for this register is 00h, which implies that, in the default condition, all channels are powered up. If all channels are powered down (i.e., the value for this register is FFh), then the analog front-end circuits for all channels are powered down, and the output of the ADC contains invalid data. If the device is in MAN-Ch_n mode and the selected channel is powered down, then the device yields invalid output, which can also trigger a false alarm condition.

Table 12. Channel Power Down Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH7_PD	R/W	0h	Channel 7 power-down. 0 = The analog front-end on channel 7 is powered up and channel 7 can be included in the AUTO_RST sequence 1 = The analog front-end on channel 7 is powered down and channel 7 cannot be included in the AUTO_RST sequence
6	CH6_PD	R/W	0h	Channel 6 power-down. 0 = The analog front-end on channel 6 is powered up and channel 6 can be included in the AUTO_RST sequence 1 = The analog front-end on channel 6 is powered down and channel 6 cannot be included in the AUTO_RST sequence
5	CH5_PD	R/W	0h	Channel 5 power-down. 0 = The analog front-end on channel 5 is powered up and channel 5 can be included in the AUTO_RST sequence 1 = The analog front-end on channel 5 is powered down and channel 5 cannot be included in the AUTO_RST sequence
4	CH4_PD	R/W	0h	Channel 4 power-down. 0 = The analog front-end on channel 4 is powered up and channel 4 can be included in the AUTO_RST sequence 1 = The analog front-end on channel 4 is powered down and channel 4 cannot be included in the AUTO_RST sequence
3	CH3_PD	R/W	0h	Channel 3 power-down. 0 = The analog front-end on channel 3 is powered up and channel 3 can be included in the AUTO_RST sequence 1 = The analog front end on channel 3 is powered down and channel 3 cannot be included in the AUTO_RST sequence
2	CH2_PD	R/W	0h	Channel 2 power-down. 0 = The analog front end on channel 2 is powered up and channel 2 can be included in the AUTO_RST sequence 1 = The analog front end on channel 2 is powered down and channel 2 cannot be included in the AUTO_RST sequence
1	CH1_PD	R/W	0h	Channel 1 power-down. 0 = The analog front end on channel 1 is powered up and channel 1 can be included in the AUTO_RST sequence 1 = The analog front end on channel 1 is powered down and channel 1 cannot be included in the AUTO_RST sequence

Bit	Field	Type	Reset	Description
0	CH0_PD	R/W	0h	Channel 0 power-down. 0 = The analog front end on channel 0 is powered up and channel 0 can be included in the AUTO_RST sequence 1 = The analog front end on channel 0 is powered down and channel 0 cannot be included in the AUTO_RST sequence

(1) Shading registers are not available for 4-channel version devices.

Device Features Selection Control Register (address = 03h)

The bits in this register can be used to configure the device ID for daisy-chain operation, enable the ALARM feature, and configure the output bit format on SDO.

Table 13. Feature Select Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DEV[1:0]	R/W	0h	Device ID bits 00 = ID for device 0 in daisy-chain mode 01 = ID for device 1 in daisy-chain mode 10 = ID for device 2 in daisy-chain mode 11 = ID for device 3 in daisy-chain mode
5	0	R	0h	Must always be set to 0
4	0	R/W	0h	ALARM feature enable 0 = ALARM feature is disabled 1 = ALARM feature is enabled
3	0	R	0h	Must always be set to 0
2-0	SDO[2:0]	R/W	0h	SDO data format bits

Table 14. Description of Program Register Bits for SDO Data Format

SDO Format SDO[2:0]	Begining of the Output Bit Stream	Output Format			
		Bits 24-9	Bits 8-5	Bits 4-3	Bits 2-0
000	16th SCLK falling edge, no latency	Conversion result for selected channel (MSB-first)	SDO pulled low		
001	16th SCLK falling edge, no latency	Conversion result for selected channel (MSB-first)	Channel address(1)	SDO pulled low	
010	16th SCLK falling edge, no latency	Conversion result for selected channel (MSB-first)	Channel address(1)	Device address(1)	SDO pulled low
011	16th SCLK falling edge, no latency	Conversion result for selected channel (MSB-first)	Channel address(1)	Device address(1)	Input range(1)

(1) The table below lists the bit descriptions for these channel addresses, device addresses, and input range.

Table 15. Bit Description for the SDO Data

Bit	Bit Description
24-9	16 bits of conversion result for the channel represented in MSB-first format
8-5	Four bits of channel address. 0000 = Channel 0 0001 = Channel 1 0010 = Channel 2

Bit	Bit Description
	0011 = Channel 3 0100 = Channel 4 (valid only for the 8-channel version device) 0101 = Channel 5 (valid only for the 8-channel version device) 0110 = Channel 6 (valid only for the 8-channel version device) 0111 = Channel 7 (valid only for the 8-channel version device)
4-3	Two bits of device address (mainly useful in daisy-chain mode)
2-0	Three LSB bits of input voltage range (Refer to the Range Select Registers)

Range Select Registers (addresses 05h-0Ch)

Address 05h corresponds to channel 0, address 06h corresponds to channel 1, address 07h corresponds to channel 2, address 08h corresponds to channel 3, address 09h corresponds to channel 4, address 0Ah corresponds to channel 5, address 0Bh corresponds to channel 6, and address 0Ch corresponds to channel 7. These registers allow the selection of input ranges for all individual channels (n = 0 to 3 for the 4-channel version device and n = 0 to 7 for the 8-channel version device). The default value for these registers is 00h

Table 16. Channel n Input Range Registers Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R	0h	Must always be set to 0
3-0	Range_CHn[3:0]	R/W	0	Input range selection bits for channel n (n = 0 to 3 for the 4-channel version and n = 0 to 7 for the 8-channel version devices) 0000 = Input range is set to ±2.5 x V_{REF} (Single-ended) 0001 = Input range is set to ±1.25 x V_{REF}(Single-ended) 0010 = Input range is set to ±0.625 x V_{REF}(Single-ended) 0011 = Input range is set to ±2.5 x V_{REF} (Differential) 0100 = Input range is set to ±1.25 x V_{REF}(Differential) 0101 = Input range is set to 0 to 2.5 x V_{REF} 0110 = Input range is set to 0 to 1.25 x V_{REF}

Over Range Setting Registers (address 0Dh)

The channel input range can be expanded to 20% of the range set in Range Select Registers. Also, the over range can be configured individually for each channel.

Table 17. Over Range Setting Registers Field Descriptions

Bit	Field	Type	Reset	Description
7	Over_Range_CH 7	R/W	0	Channel 7 over range control. 0b = Channel 7 range as programmed in register 0Ch 1b = Enable 20% Overrange for Channel 7 range set as programmed in register 0Ch
6	Over_Range_CH 6	R/W	0	Channel 6 over range control. 0b = Channel 6 range as programmed in register 0Bh 1b = Enable 20% Overrange for Channel 6 range set as programmed in register 0Bh
5	Over_Range_CH 5	R/W	0	Channel 5 over range control. 0b = Channel 5 range as programmed in register 0Ah 1b = Enable 20% Overrange for Channel 5 range set as programmed in register 0Ah
4	Over_Range_CH 4	R/W	0	Channel 4 over range control. 0b = Channel 4 range as programmed in register 09h 1b = Enable 20% Overrange for Channel 4 range set as programmed in register 09h
3	Over_Range_CH 3	R/W	0	Channel 3 over range control. 0b = Channel 3 range as programmed in register 08h 1b = Enable 20% Overrange for Channel 3 range set as programmed in register 08h
2	Over_Range_CH 2	R/W	0	Channel 2 over range control. 0b = Channel 2 range as programmed in register 07h 1b = Enable 20% Overrange for Channel 2 range set as programmed in register 07h
1	Over_Range_CH 1	R/W	0	Channel 1 over range control. 0b = Channel 1 range as programmed in register 06h 1b = Enable 20% Overrange for Channel 1 range set as programmed in register 06h
0	Over_Range_CH 0	R/W	0	Channel 0 over range control. 0b = Channel 0 range as programmed in register 09h 1b = Enable 20% Overrange for Channel 0 range set as programmed in register 05h

(1) Shading registers are not available for 4-channel version devices.

LPF Bandwidth Configuration Registers (address 0Eh)

The AFE LPF -3dB bandwidth is configurable for all channels simultaneously, which can cover more application scenarios.

Table 18. LPF Bandwidth Configuration Registers Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	R	0h	Must always be set to 0
1-0	LPF_CONFIG [1:0]	R/W	01h	00 = LPF -3dB bandwidth is 35 kHz 01 = LPF -3dB bandwidth is 15 kHz 10 = Not available 11 = Not available

CRC Configure Register (address = 0Fh)

These registers store alarm conditions related to individual channels, and their flags can be read when an alarm interrupt is received on the ALARM pin. Each alarm has two flags: active and tripped. The active flag is set to 1 during the alarm condition, persisting as long as the alarm condition exists. The tripped flag also activates during an alarm condition but remains set until it is read. This feature eliminates the need for the device to continuously track the alarm.

The ALARM overview tripper-flags register compiles the logical OR of high or low tripped alarm flags for all eight channels.

Table 19. CRC Configure Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CRC_Error	R	0h	Receive command CRC error status. 0 = CRC error 1 = CRC pass
6-1	0	R	0h	Must always be set to 0
0	Enables interface CRC check	R/W	0h	0 = Interface CRC check disabled 1 = Interface CRC check enabled

Alarm Overview Tripped-flag Register (address = 10h)

These registers store alarm conditions related to individual channels, and their flags can be read when an alarm interrupt is received on the ALARM pin. Each alarm has two flags: active and tripped. The active flag is set to 1 during the alarm condition, persisting as long as the alarm condition exists. The tripped flag also activates during an alarm condition but remains set until it is read. This feature eliminates the need for the device to continuously track the alarm.

The ALARM overview tripper-flags register compiles the logical OR of high or low tripped alarm flags for all eight channels.

Table 20. Alarm Overview Tripped-flag Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Tripped Alarm Flag Ch7	R	0h	Tripped alarm flag for all analog channels at a glance. Each individual bit indicates a tripped alarm flag status for each channel, as per the alarm flags register for channels 7 to 0, respectively. 0 = No alarm detected 1 = Alarm detected
6	Tripped Alarm Flag Ch6	R	0h	
5	Tripped Alarm Flag Ch5	R	0h	
4	Tripped Alarm Flag Ch4	R	0h	
3	Tripped Alarm Flag Ch3	R	0h	
2	Tripped Alarm Flag Ch2	R	0h	
1	Tripped Alarm Flag Ch1	R	0h	
0	Tripped Alarm Flag Ch0	R	0h	

(1) Shading registers are not available for 4-channel version devices.

Alarm Flag Registers: Tripped and Active (address = 11h-14h)

Each channel has two alarm thresholds (high and low), and each threshold has two associated flags. An active alarm flag is activated when an alarm is triggered (i.e., when data crosses the alarm threshold) and stays active as long as the alarm condition persists. On the other hand, a tripped alarm flag is activated in a similar manner to the active alarm flag but remains latched until it is read. Registers 11h to 14h in the program registers store both the active and tripped alarm flags for all eight individual channels.

Table 21. Alarm Ch0-3 Tripped-flag Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Tripped Alarm Flag Ch n Low or High (n = 0 to 3)	R	0h	Tripped alarm flag high, low for channel n (n = 0 to 3) Each individual bit indicates an active high or low alarm flag status for each channel, as per the alarm flags register for channels 0 to 7. 0 = No alarm detected 1 = Alarm detected

Table 22. Alarm Ch0-3 Active-flag Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Active Alarm Flag Ch n Low or High (n = 0 to 3)	R	0h	Active alarm flag high, low for channel n (n = 0 to 3) Each individual bit indicates an active high or low alarm flag status for each channel, as per the alarm flags register for channels 0 to 7. 0 = No alarm detected 1 = Alarm detected

Table 23. Alarm Ch4-7 Tripped-flag Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Tripped Alarm Flag Ch n Low or High (n = 4 to 7)	R	0h	Tripped alarm flag high, low for channel n (n = 4 to 7) Each individual bit indicates an active high or low alarm flag status for each channel, as per the alarm flags register for channels 0 to 7. 0 = No alarm detected 1 = Alarm detected

Table 24. Alarm Ch4-7 Active-flag Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Active Alarm Flag Ch n Low or High (n = 4 to 7)	R	0h	Active alarm flag high, low for channel n (n = 4 to 7) Each individual bit indicates an active high or low alarm flag status for each channel, as per the alarm flags register for channels 0 to 7. 0 = No alarm detected 1 = Alarm detected

Alarm Threshold Setting Registers (addresses = 15h-3Ch)

The TPAFE51736 is equipped with separate high and low alarm threshold settings for each channel. Each alarm threshold is 16 bits wide and includes an 8-bit hysteresis value, which is consistent for both high and low threshold settings. This 40-bit configuration is achieved through five 8-bit registers linked to each high and low alarm.

Table 25. Alarm Threshold Setting Registers

Name	ADDR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	BIT 0
Ch 0 Hysteresis	15h	CH0_HYST[7:0]							
Ch 0 High Threshold MSB	16h	CH0_HT[15:8]							
Ch 0 High Threshold LSB	17h	CH0_HT[7:0]							
Ch 0 Low Threshold MSB	18h	CH0_LT[15:8]							
Ch 0 Low Threshold LSB	19h	CH0_LT[7:0]							
Ch 1 Hysteresis	1Ah	CH1_HYST[7:0]							
Ch 1 High Threshold MSB	1Bh	CH1_HT[15:8]							
Ch 1 High Threshold LSB	1Ch	CH1_HT[7:0]							
Ch 1 Low Threshold MSB	1Dh	CH1_LT[15:8]							
Ch 1 Low Threshold LSB	1Eh	CH1_LT[7:0]							
Ch 2 Hysteresis	1Fh	CH2_HYST[7:0]							
Ch 2 High Threshold MSB	20h	CH2_HT[15:8]							
Ch 2 High Threshold LSB	21h	CH2_HT[7:0]							
Ch 2 Low Threshold MSB	22h	CH2_LT[15:8]							
Ch 2 Low Threshold LSB	23h	CH2_LT[7:0]							
Ch 3 Hysteresis	24h	CH3_HYST[7:0]							
Ch 3 High Threshold MSB	25h	CH3_HT[15:8]							
Ch 3 High Threshold LSB	26h	CH3_HT[7:0]							
Ch 3 Low Threshold MSB	27h	CH3_LT[15:8]							
Ch 3 Low Threshold LSB	28h	CH3_LT[7:0]							
Ch 4 Hysteresis(1)	29h	CH4_HYST[7:0]							
Ch 4 High Threshold MSB	2Ah	CH4_HT[15:8]							
Ch 4 High Threshold LSB	2Bh	CH4_HT[7:0]							
Ch 4 Low Threshold MSB	2Ch	CH4_LT[15:8]							
Ch 4 Low Threshold LSB	2Dh	CH4_LT[7:0]							
Ch 5 Hysteresis	2Eh	CH5_HYST[7:0]							
Ch 5 High Threshold MSB	2Fh	CH5_HT[15:8]							
Ch 5 High Threshold LSB	30h	CH5_HT[7:0]							
Ch 5 Low Threshold MSB	31h	CH5_LT[15:8]							
Ch 5 Low Threshold LSB	32h	CH5_LT[7:0]							
Ch 6 Hysteresis	33h	CH6_HYST[7:0]							
Ch 6 High Threshold MSB	34h	CH6_HT[15:8]							

Name	ADDR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	BIT 0
Ch 6 High Threshold LSB	35h	CH6_HT[7:0]							
Ch 6 Low Threshold MSB	36h	CH6_LT[15:8]							
Ch 6 Low Threshold LSB	37h	CH6_LT[7:0]							
Ch 7 Hysteresis	38h	CH7_HYST[7:0]							
Ch 7 High Threshold MSB	39h	CH7_HT[15:8]							
Ch 7 High Threshold LSB	3Ah	CH7_HT[7:0]							
Ch 7 Low Threshold MSB	3Bh	CH7_LT[15:8]							
Ch 7 Low Threshold LSB	3Ch	CH7_LT[7:0]							

(1) Shading registers are not available for 4-channel version devices.

Table 26. Channel n Hysteresis Register Field Descriptions

Bit	Field	Type	Reset	Description

7-0	CH n Hysteresis[7-0]	R/W	0h	These bits set the channel high and low alarm hysteresis for channel n.
				n = 0 to 7 for the 8-channel version devices;
				n = 0 to 3 for the 4-channel version devices;
				For example, bits 7-0 of the channel 0 register (address 15h) set the channel 0 alarm hysteresis.
				00000000 = No hysteresis
				00000001 = ±1-LSB hysteresis
				00000010 to 11111110 = ±2-LSB to ±254-LSB hysteresis
				11111111 = ±255-LSB hysteresis

Table 27. Channel n High Threshold MSB Register Field Descriptions

Bit	Field	Type	Reset	Description

7-0	CHn_HT[15:8]	R/W	1h	These bits set the MSB byte for the 16-bit channel n high alarm.
				n = 0 to 7 for the 8-channel version devices;
				n = 0 to 3 for the 4-channel version devices;
				For example, bits 7-0 of the channel 0 register (address 16h) set the MSB byte for the channel 0 high alarm threshold. The channel 0 high alarm threshold is AAFFh when bits 7-0 of the ch 0 high threshold MSB register (address 16h) are set to AAh and bits 7-0 of the ch 0 high threshold LSB register (address 17h) are set to FFh.
				0000 0000 = MSB byte is 00h
				0000 0001 = MSB byte is 01h
				0000 0010 to 1110 1111 = MSB byte is 02h to FEh
				1111 1111 = MSB byte is FFh

Table 28. Channel n High Threshold LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CHn_HT[7:0]	R/W	1h	These bits set the LSB byte for the 16-bit channel n high alarm.

Bit	Field	Type	Reset	Description

				n = 0 to 7 for the 8-channel version devices;
				n = 0 to 3 for the 4-channel version devices;
				For example, bits 7-0 of the channel 0 register (address 17h) set the LSB for the channel 0 high alarm threshold. The channel 0 high alarm threshold is AAFFh when bits 7-0 of the ch 0 high threshold MSB register (address 16h) are set to AAh and bits 7- 0 of the ch 0 high threshold LSB register (address 17h) are set to FFh.
				0000 0000 = LSB byte is 00h
				0000 0001 = LSB byte is 01h
				0000 0010 to 1110 1111 = LSB byte is 02h to FEh
				1111 1111 = LSB byte is FFh

Table 29. Channel n Low Threshold MSB Register Field Descriptions

Bit	Field	Type	Reset	Description

7-0	CHn_LT[15:8]	R/W	0h	These bits set the MSB byte for the 16-bit channel n low alarm.
				n = 0 to 7 for the 8-channel version devices;
				n = 0 to 3 for the 4-channel version devices;
				For example, bits 7-0 of the channel 0 register (address 18h) set the MSB byte for the channel 0 low alarm threshold. The channel 0 low alarm threshold is AAFFh when bits 7-0 of the ch 0 low threshold MSB register (address 18h) are set to AAh and bits 7-0 of the ch 0 low threshold LSB register (address 19h) are set to FFh.
				0000 0000 = MSB byte is 00h
				0000 0001 = MSB byte is 01h
				0000 0010 to 1110 1111 = MSB byte is 02h to FEh
				1111 1111 = MSB byte is FFh

Table 30. Channel n Low Threshold LSB Register Field Descriptions

Bit	Field	Type	Reset	Description

7-0	CHn_LT[7:0]	R/W	0h	These bits set the LSB byte for the 16-bit channel n low alarm.
				n = 0 to 7 for the 8-channel version devices;
				n = 0 to 3 for the 4-channel version devices;
				For example, bits 7-0 of the channel 0 register (address 19h) set the LSB for the channel 0 low alarm threshold. The channel 0 low alarm threshold is AAFFh when bits 7-0 of the ch 0 low threshold MSB register (address 18h) are set to AAh and bits 7- 0 of the ch 0 low threshold LSB register (address 19h) are set to FFh.
				0000 0000 = LSB byte is 00h
				0000 0001 = LSB byte is 01h
				0000 0010 to 1110 1111 = LSB byte is 02h to FEh
				1111 1111 = LSB byte is FFh

Command Read-Back Register (address = 3Fh)

This register allows the device mode of operation to be read. On execution of this command, the device outputs the command word executed in the previous data frame. The output of the command register appears on SDO from the 16th falling edge onwards in an MSB-first format. All information regarding the command register is contained in the first eight bits and the last eight bits are 0 (see Table 6), thus the command read-back operation can be stopped after the 24th SCLK cycle.

Table 31. ALARM Overview Tripped-Flag Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	COMMAND_WORD[15:8]	R	0h	Command executed in the previous data frame.

Open Detect Enable Register (address = 78h)

These registers configure the open detect feature, the open circuit detection operates in manual mode or in automatic mode.

Table 32. Open Detect Enable Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Ch7 Open Detect Enable	R/W	0h	In automatic mode, enables analog input open circuit detection for Channel 7. In manual mode, sets the open detection.
6	Ch6 Open Detect Enable	R/W	0h	In automatic mode, enables analog input open circuit detection for Channel 6. In manual mode, sets the open detection.
5	Ch5 Open Detect Enable	R/W	0h	In automatic mode, enables analog input open circuit detection for Channel 5. In manual mode, sets the open detection.
4	Ch4 Open Detect Enable	R/W	0h	In automatic mode, enables analog input open circuit detection for Channel 4. In manual mode, sets the open detection.
3	Ch3 Open Detect Enable	R/W	0h	In automatic mode, enables analog input open circuit detection for Channel 3. In manual mode, sets the open detection.
2	Ch2 Open Detect Enable	R/W	0h	In automatic mode, enables analog input open circuit detection for Channel 2. In manual mode, sets the open detection.
1	Ch1 Open Detect Enable	R/W	0h	In automatic mode, enables analog input open circuit detection for Channel 1. In manual mode, sets the open detection.
0	Ch0 Open Detect Enable	R/W	0h	In automatic mode, enables analog input open circuit detection for Channel 0. In manual mode, sets the open detection.

(1) Shading registers are not available for 4-channel version devices.

Open Detected Register (address = 79h)

Table 33. Open Detected Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Ch7 Open Detected	R/W	0h	0 = Analog Input 7 Open Circuit Not Detected 1 = Analog Input 7 Open Circuit Detected
6	Ch6 Open Detected	R/W	0h	0 = Analog Input 6 Open Circuit Not Detected 1 =Analog Input 6 Open Circuit Detected
5	Ch5 Open Detected	R/W	0h	0 = Analog Input 5 Open Circuit Not Detected 1 =Analog Input 5 Open Circuit Detected
4	Ch4 Open Detected	R/W	0h	0 = Analog Input 4 Open Circuit Not Detected 1 =Analog Input 4 Open Circuit Detected
3	Ch3 Open Detected	R/W	0h	0 = Analog Input 3 Open Circuit Not Detected 1 =Analog Input 3 Open Circuit Detected
2	Ch2 Open Detected	R/W	0h	0 = Analog Input 2 Open Circuit Not Detected 1 =Analog Input 2 Open Circuit Detected
1	Ch1 Open Detected	R/W	0h	0 = Analog Input 1 Open Circuit Not Detected 1 =Analog Input 1 Open Circuit Detected
0	Ch0 Open Detected	R/W	0h	0 = Analog Input 0 Open Circuit Not Detected 1 =Analog Input 0 Open Circuit Detected

(1) Shading registers are not available for 4-channel version devices.

Open Detect Mode Register (address = 7Ah)

Table 34. Open Detect Mode Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Open Detect Mode	R/W	0h	Open detect mode configuration. 0 = Open detect is disabled 1 = Manual mode open detect Others = Automatic mode open detect

Open Detect Threshold Register (address = 7Bh)

These registers configure the open detect threshold, which triggers automatic open detect mode.

Table 35. Open Detect Threshold Register Field Descriptions

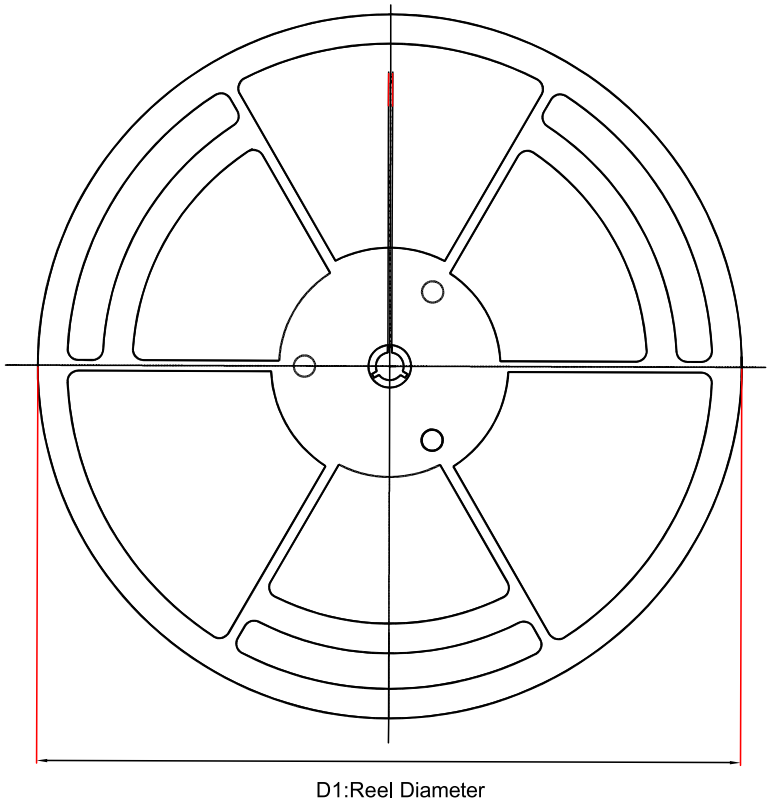
Bit	Field	Type	Reset	Description
7-6	0	R	0h	Must always be set to 0
5-0	Open Detect Threshold	R/W	0h	0 = Default open detect threshold is 350 LSB Others = Open detect threshold = Open detect threshold * 256 For example,when set to 6'h2, Open detect threshold = 16'h = 0200, thus 2*256=512 LSB.

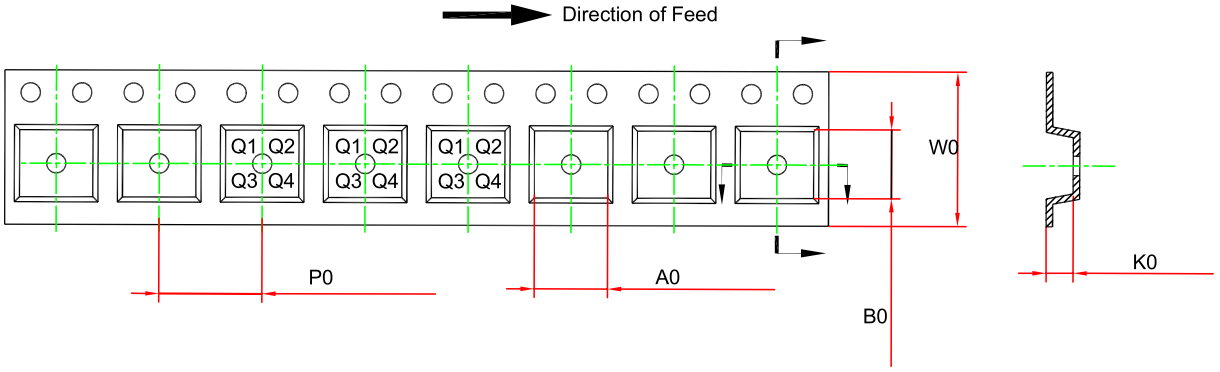
Status Register (address = 7Dh)

Table 36. Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	R	0h	Must always be set to 0
2	Open Detected	R	0h	0 = Normal status 1 = Open detected. Check the Open Detected Register to check which channel is detected.
1	ALARM Overview Tripped-Flag	R	0h	0 = Normal status 1 = Alarm detected. Check the ALARM Overview Tripped-Flag Register to check which channel is detected.
0	CRE Error Detected	R	0h	0 = Normal status 1 = CRC Error. CRC error flag, the same as Bit 7 in CRC Configure Register.

Tape and Reel Information



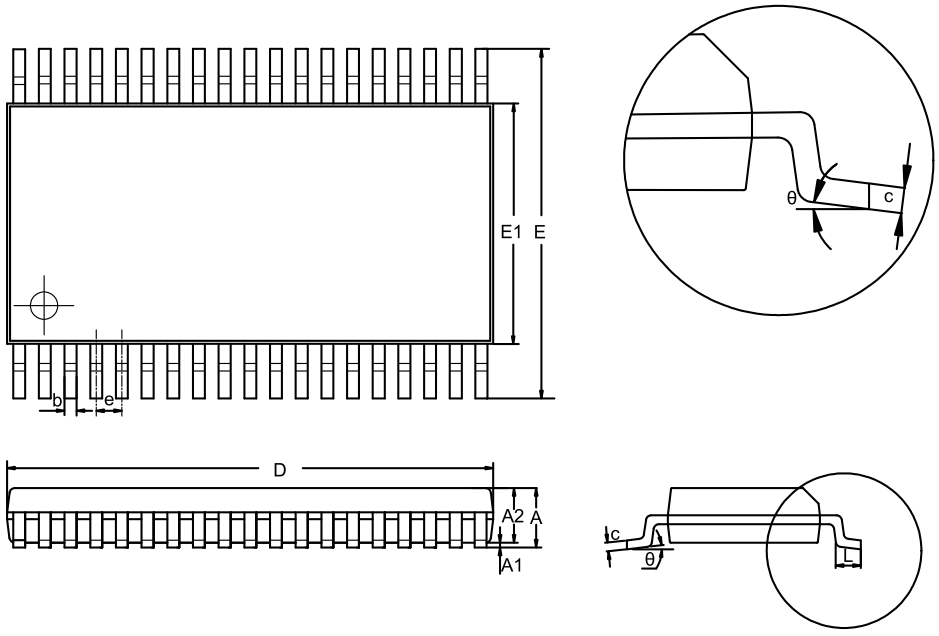


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPAFE51736S4-TS7R	TSSOP38	330	21.6	6.8	10.25	1.6	8	16	Q1

Package Outline Dimensions

TSSOP38

Package Outline Dimensions TS7(TSSOP-38-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	—	1.200	—	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.170	0.270	0.007	0.011
c	0.090	0.200	0.004	0.008
D	9.600	9.800	0.378	0.386
E	6.250	6.550	0.246	0.258
E1	4.300	4.500	0.169	0.177
e	0.500 BSC		0.020 BSC	
L	0.500	0.700	0.020	0.028
θ	1°	7°	1°	7°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPAFE51736S4-TS7R	−40 to 125°C	TSSOP38	51736S4	2	Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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