16-Bit, 100-kSPS, Bipolar Input ADC

Features

- 16-Bit, Single-Channel ADC with Integrated Analog Front-End
- Sampling with 100 kSPS throughput Rate
- Independently Programmable Channel Inputs
  - True Bipolar Single-ended: ±12.288 V, ±10.24 V, ±6.144 V, ±5.12 V, ±3.072 V, ±2.56 V
  - Unipolar Single-ended: 0 V - 12.288 V, 0 V - 10.24 V, 0 V - 6.144 V, 0 V - 5.12 V
  - True Bipolar Fully-differential: ±12.288 V, ±10.24 V, ±6.144 V, ±5.12 V
  - Configurable Analog Bandwidth: 15 kHz or 35 kHz
- Power Supply
  - Single Analog Supply: 5 V
  - Digital Supply: 1.71 V to 5 V
- Highly Integrated Analog Front-End
  - 1-MΩ Analog Input Impedance
  - Programmable Gain Amplifier
  - Analog Low-Pass Filter
  - Internal Accurate Reference and Reference Buffer
  - ±30 V Analog Input Overvoltage Clamp Protection with ±7-kV ESD
- Flexible Digital and Interface
  - Serial Interface Compatible with SPI
  - Daisy-Chain Function
- Integrated Diagnostic Function
  - Analog Input Open Detect with Manual or Auto Mode
  - Optional Cyclic Redundancy Check (CRC) Error Checking
  - ALARM
- Typical Performance
  - DNL: ±0.5 LSB
  - INL: ±1 LSB
  - SNR: 90 dB
  - SINAD: 90 dB
  - THD: −103 dB
- Package: TSSOP16 Package
- Wide Operating Temperature Range: −40°C to +125°C

Applications

- Analog Input Modules
- Servo
- Channel-to-Channel Isolated Data Acquisition

Description

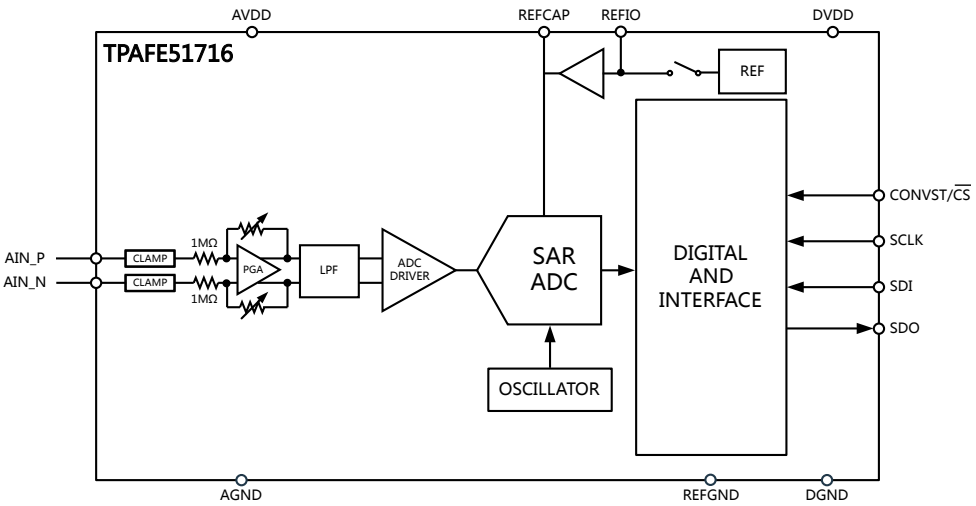
The TPAFE51716S is a single-channel, 16-bit, 100 kSPS sampling system based on a successive approximation register (SAR) analog-to-digital converter (ADC). The TPAFE51716S is highly integrated with analog front-end for each channel, including input overvoltage clamp, 1 MΩ input impedance, programmable gain amplifier (PGA), active low-pass filter, and ADC driver. Internal precision and low-drift reference with buffer makes the device feasible for a compact data acquisition solution. The digital interface supports communication with various host controllers with SPI-compatible serial and daisy-chaining of multiple devices.

The TPAFE51716S can process true bipolar single-ended ±12.288 V, ±10.24 V, ±6.144 V, ±5.12 V, ±3.072 V, ±2.56 V, unipolar single-ended 0 V - 12.288 V, 0 V - 10.24 V, 0 V - 6.144 V, 0 V - 5.12 V, and true bipolar fully-differential ±12.288 V, ±10.24 V, ±6.144 V, ±5.12 Vinput signals, with a single 5 V analog power supply. The 1 MΩ high input impedance simplified analog input design, and the device can be connected directly to sensors. The analog input overvoltage could protect the device up to ±30 V. The device offers a simple SPI-compatible serial interface and also supports daisy-chaining of multiple devices.

The device integrates various diagnostic functions to improve system robustness, like analog input open detection, alarm, and CRC error checking on read and write data and registers.

The TPAFE51716S is available in the TSSOP 5x4.4-16 package and operates from −40°C to +125°C.

Functional Block Diagram



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Product Family Table

Order Number	Channels	Resolution	Throughput	Package
TPAFE51716S-TS3R	1	16 Bits	100 kSPS	TSSOP16

Revision History

Date	Revision	Notes
2025-01-17	Rev.A.0	Initial release.

Pin Configuration and Functions

TPAFE51716S
TSSOP16 Package
Top View

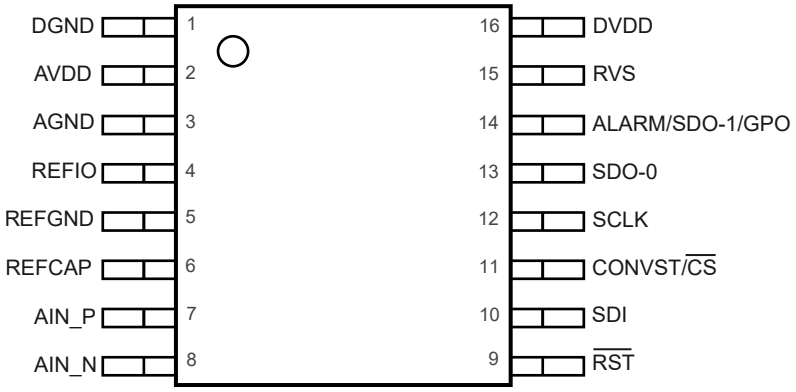


Table 1. Pin Functions: TPAFE51716S

Pin		Type (1)	Description
No.	Name		
3	AGND	P	Analog ground pins.
8	AIN_N	AI	Negative analog input.
7	AIN_P	AI	Positive analog input
14	ALARM/ SDO-1/GPO	DO	Multifunction output pin. Active high alarm. Data output 1 for serial communication. General-purpose output pin.
2	AVDD	P	Analog supply pins.
11	CONVST/$\overline{CS}$	DI	Dual-functionality pin. Active high logic: conversion start input pin; a CONVST rising edge brings the device from the acquisition phase to the conversion phase. Active low logic: chip-select input pin; the device takes control of the data bus when $\overline{CS}$ is low; the SDO-x pins go to tri-state when $\overline{CS}$ is high.
1	DGND	P	Digital ground pins.
16	DVDD	P	Digital supply pins.
6	REFCAP	AO	Reference buffer output pin. Decouple this pin to AGND using a capacitor. The voltage on this pin is typically 4.096 V.
5	REFGND	P	Reference ground pin. Connect this pin to AGND.
4	REFIO	AIO	External reference input pin and internal reference output pin
9	RST	DI	Hardware RST with low logic input active.
15	RVS	DO	Multifunction output pin for serial interface. With $\overline{CS}$ held high, RVS reflects the status of the internal ADCST signal With $\overline{CS}$ low, the status of RVS depends on the output protocol selection.
12	SCLK	DI	This pin acts as the serial clock input for data transfers.

Pin		Type (1)	Description
No.	Name		
10	SDI	DI	Data input of the SPI interface
13	SDO-0	DO	This pin outputs serial data 0.

(1) AI is analog input, GND is ground, P is power supply, REF is reference input/output, DI is digital input, DO is digital output, and CAP is decoupling capacitor pin.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Analog Voltage	Analog Input Voltage (AINxP or AINxN) to GND	−30	+30	V
	AUX_IN to GND	−0.3	AVDD + 0.3 V	V
	REFCAP or REFIO to REFGND	−0.3	AVDD + 0.3 V	V
Digital Voltage	Digital Input Voltage to GND	−0.3	DVDD + 0.3 V	V
	Digital Output Voltage to GND	−0.3	DVDD + 0.3 V	V
Supply Voltage	AVDD to GND	−0.3	7	V
	DVDD to GND	−0.3	AVDD + 0.3 V	V
T_J	Maximum Junction Temperature		150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	Analog input pins	ANSI/ESDA/JEDEC JS-001 (1)	±7	kV
		All other pins		±2	kV
CDM	Charged Device Model ESD		ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
AVDD	Analog Supply Voltage	4.75	5	5.25	V
DVDD	Digital Supply Voltage	1.71	3.3	AVDD	V

Thermal Information

Package Type	θ_{JA}	$\theta_{JC(TOP)}$	θ_{JB}	Unit
TSSOP16	104.93	23.04	73.46	°C/W

Electrical Characteristics

All test conditions: AVDD = 5 V, V_{REF} = 4.096 V (internal), DVDD = 3.3 V, f_{SAMPLE} = 100 kSPS,

T_A = −40 °C to 125 °C, unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Unit
Analog Inputs					
Input V_{IN} Voltage Ranges V_{IN} = AIN_P - AIN_N	Input range = ±3 × V_{REF}	−3 × V_{REF}		3 × V_{REF}	V
	Input range = ±2.5 × V_{REF}	−2.5 × V_{REF}		2.5 × V_{REF}	
	Input range = ±1.5 × V_{REF}	−1.5 × V_{REF}		1.5 × V_{REF}	
	Input range = ±1.25 × V_{REF}	−1.25 × V_{REF}		1.25 × V_{REF}	
	Input range = ±0.75 × V_{REF}	−0.75 × V_{REF}		0.75 × V_{REF}	
	Input range = ±0.625 × V_{REF}	−0.625 × V_{REF}		0.625 × V_{REF}	
	Input range = 3 × V_{REF}	0		3 × V_{REF}	
	Input range = 2.5 × V_{REF}	0		2.5 × V_{REF}	
	Input range = 1.5 × V_{REF}	0		1.5 × V_{REF}	
	Input range = 1.25 × V_{REF}	0		1.25 × V_{REF}	
AIN_P Operating Input Range, Positive Input	Input range = ±3 × V_{REF}	−3 × V_{REF}		3 × V_{REF}	V
	Input range = ±2.5 × V_{REF}	−2.5 × V_{REF}		2.5 × V_{REF}	
	Input range = ±1.5 × V_{REF}	−1.5 × V_{REF}		1.5 × V_{REF}	
	Input range = ±1.25 × V_{REF}	−1.25 × V_{REF}		1.25 × V_{REF}	
	Input range = ±0.75 × V_{REF}	−0.75 × V_{REF}		0.75 × V_{REF}	
	Input range = ±0.625 × V_{REF}	−0.625 × V_{REF}		0.625 × V_{REF}	
	Input range = 3 × V_{REF}	0		3 × V_{REF}	
	Input range = 2.5 × V_{REF}	0		2.5 × V_{REF}	
	Input range = 1.5 × V_{REF}	0		1.5 × V_{REF}	
	Input range = 1.25 × V_{REF}	0		1.25 × V_{REF}	
AIN_N Operating Input Range, Negative Input	Input range = ±3 × V_{REF}	−3 × V_{REF}		3 × V_{REF}	V
	Input range = ±2.5 × V_{REF}	−2.5 × V_{REF}		2.5 × V_{REF}	
	Input range = ±1.5 × V_{REF}	−1.5 × V_{REF}		1.5 × V_{REF}	
	Input range = ±1.25 × V_{REF}	−1.25 × V_{REF}		1.25 × V_{REF}	
	Input range = ±0.75 × V_{REF}	−0.75 × V_{REF}		0.75 × V_{REF}	
	Input range = ±0.625 × V_{REF}	−0.625 × V_{REF}		0.625 × V_{REF}	
	Input range = 3 × V_{REF} (1)	−0.1		0.1	
	Input range = 2.5 × V_{REF} (1)	−0.1		0.1	
	Input range = 1.5 × V_{REF} (1)	−0.1		0.1	
	Input range = 1.25 × V_{REF} (1)	−0.1		0.1	
Fully Differential Input Range (1) V_{IN} = AIN_P - AIN_N	Input range = ±3 × V_{REF}	−3 × V_{REF}		3 × V_{REF}	V
	Input range = ±2.5 × V_{REF}	−2.5 × V_{REF}		2.5 × V_{REF}	

Parameter		Test Conditions	Min	Typ	Max	Unit
		Input range = ±1.5 × V_{REF}	−1.5 × V_{REF}		1.5 × V_{REF}	
		Input range = ±1.25 × V_{REF}	−1.25 × V_{REF}		1.25 × V_{REF}	
		Input range = ±0.75 × V_{REF}	−0.75 × V_{REF}		0.75 × V_{REF}	
		Input range = ±0.625 × V_{REF}	−0.625 × V_{REF}		0.625 × V_{REF}	
Fully Differential Input Common-Mode Input Range (1)		Input range = ±3 × V_{REF}	−6.8		6.5	V
		Input range = ±2.5 × V_{REF}	−6.8		6.5	
		Input range = ±1.5 × V_{REF}	−3.4		4.9	
		Input range = ±1.25 × V_{REF}	−3.4		4.9	
		Input range = ±0.75 × V_{REF}	−1.7		4.1	
		Input range = ±0.625 × V_{REF}	−1.7		4.1	
Z_{IN}	Input Impedance	All input ranges, T_A = 25°C	0.86	1	1.17	Mohm
	Input Impedance Temperature Drift	All input ranges		7		ppm/°C
Analog Input Current	Input Leakage Current	Input range = ±2.5 × V_{REF}		8.8		µA
		Input range = ±1.25 × V_{REF}		3.3		
		Input range = ±0.625 × V_{REF}		1.1		
		Input range = 2.5 × V_{REF}		9.2		
		Input range = 1.25 × V_{REF}		4.3		
Input Overvoltage Protection (1)						
Analog Input Clamp	Overvoltage Protection Voltage	All input ranges	−30		30	V
Analog Input Filter						
−3 dB BW	Analog Input LPF Bandwidth −3 dB	Low bandwidth		15		kHz
		High bandwidth		35		
−0.1 dB BW	Analog Input LPF Bandwidth −0.1 dB	Low bandwidth		2.5		kHz
		High bandwidth		5.5		
System Performance						
Resolution			16			Bits
NMC	No Missing Codes		16			Bits
DNL	Differential Nonlinearity	All input ranges	−0.99	±0.5	1	LSB
INL	Integral Nonlinearity	All input ranges	−2	±1	2	LSB
E_G	Gain Error At T_A = 25°C	Input range = ±3 × V_{REF}	−0.02		0.02	%FSR
		Input range = ±2.5 × V_{REF}	−0.02		0.02	
		Input range = ±1.5 × V_{REF}	−0.18		0.18	
		Input range = ±1.25 × V_{REF}	−0.02		0.02	
		Input range = ±0.75 × V_{REF}	−0.18		0.18	
		Input range = ±0.625 × V_{REF}	−0.02		0.02	

Parameter		Test Conditions	Min	Typ	Max	Unit
		Input range = 3 × V_{REF}	−0.2		0.16	
		Input range = 2.5 × V_{REF}	−0.045		0.045	
		Input range = 1.5 × V_{REF}	−0.2		0.16	
		Input range = 1.25 × V_{REF}	−0.06		0.06	
	Gain Error Temperature Drift (1)	All input ranges	−5	1	5	ppm/°C
E_O	Offset Error At T_A = 25°C,	Input range = ±3 × V_{REF}	−2.9	±0.375	2.9	mV
		Input range = ±2.5 × V_{REF}	−1.25	±0.32	1.25	
		Input range = ±1.5 × V_{REF}	−2.1	±0.56	2.1	
		Input range = ±1.25 × V_{REF}	−1.1	±0.47	1.1	
		Input range = ±0.75 × V_{REF}	−1.5	±0.375	1.5	
		Input range = ±0.625 × V_{REF}	−0.8	±0.32	0.8	
		Input range = 3 × V_{REF}	−6.4	±0.375	5.3	
		Input range = 2.5 × V_{REF}	−0.5	±0.32	0.5	
		Input range = 1.5 × V_{REF}	−6.2	±0.47	5	
		Input range = 1.25 × V_{REF}	−1.2	±0.39	1.2	
	Offset Error Temperature Drift (1)	All input ranges	−4	1	4	ppm/°C
Sampling Dynamics						
t_{CONV}	Conversion Time				5	µs
t_{ACQ}	Acquisition Time		5			µs
f_S	Maximum Throughput Rate without Latency			100		kSPS
Dynamic Characteristics						
SNR	Low Bandwidth –0.5 dBFS 1 kHz Input	Input range = ±3 × V_{REF}	88.5	90.5		dB
		Input range = ±2.5 × V_{REF}	88.2	89.9		
		Input range = ±1.5 × V_{REF}	87.8	90		
		Input range = ±1.25 × V_{REF}	87.4	89.4		
		Input range = ±0.75 × V_{REF}	86.6	88.9		
		Input range = ±0.625 × V_{REF}	85.8	88.3		
		Input range = 3 × V_{REF}	87.4	89.8		
		Input range = 2.5 × V_{REF}	86.9	89		
		Input range = 1.5 × V_{REF}	85.7	88.2		
		Input range = 1.25 × V_{REF}	85.0	87.1		
	High Bandwidth –0.5 dBFS 1 kHz Input	Input range = ±3 × V_{REF}		90		dB
		Input range = ±2.5 × V_{REF}		90		
		Input range = ±1.5 × V_{REF}		90		

Parameter		Test Conditions	Min	Typ	Max	Unit
		Input range = ±1.25 × V_{REF}		89		
		Input range = ±0.75 × V_{REF}		89		
		Input range = ±0.625 × V_{REF}		88		
		Input range = 3 × V_{REF}		88		
		Input range = 2.5 × V_{REF}		88		
		Input range = 1.5 × V_{REF}		86		
		Input range = 1.25 × V_{REF}		85		
THD	Low Bandwidth –0.5 dBFS 1 kHz Input	Input range = ±3 × V_{REF}		–103		dB
		Input range = ±2.5 × V_{REF}		–103		
		Input range = ±1.5 × V_{REF}		–103		
		Input range = ±1.25 × V_{REF}		–103		
		Input range = ±0.75 × V_{REF}		–103		
		Input range = ±0.625 × V_{REF}		–103		
		Input range = 3 × V_{REF}		–103		
		Input range = 2.5 × V_{REF}		–103		
		Input range = 1.5 × V_{REF}		–103		
		Input range = 1.25 × V_{REF}		–103		
	High Bandwidth –0.5 dBFS 1 kHz Input	Input range = ±3 × V_{REF}		–100		dB
		Input range = ±2.5 × V_{REF}		–100		
		Input range = ±1.5 × V_{REF}		–100		
		Input range = ±1.25 × V_{REF}		–100		
		Input range = ±0.75 × V_{REF}		–100		
		Input range = ±0.625 × V_{REF}		–100		
		Input range = 3 × V_{REF}		–100		
		Input range = 2.5 × V_{REF}		–100		
		Input range = 1.5 × V_{REF}		–100		
		Input range = 1.25 × V_{REF}		–100		
SINAD	Low Bandwidth –0.5 dBFS 1 kHz Input	Input range = ±3 × V_{REF}	86.3	90		dB
		Input range = ±2.5 × V_{REF}	85.9	89.7		
		Input range = ±1.5 × V_{REF}	86.1	89.8		
		Input range = ±1.25 × V_{REF}	85.5	89.2		
		Input range = ±0.75 × V_{REF}	84.6	88.8		
		Input range = ±0.625 × V_{REF}	83.9	88.2		
		Input range = 3 × V_{REF}	85.5	89.6		
		Input range = 2.5 × V_{REF}	85.2	88.8		
		Input range = 1.5 × V_{REF}	84.0	88.1		
		Input range = 1.25 × V_{REF}	82.7	87		

Parameter		Test Conditions	Min	Typ	Max	Unit
	High Bandwidth –0.5 dBFS 1 kHz Input	Input range = ±3 × V_{REF}		89		dB
		Input range = ±2.5 × V_{REF}		89		
		Input range = ±1.5 × V_{REF}		89		
		Input range = ±1.25 × V_{REF}		89		
		Input range = ±0.75 × V_{REF}		88		
		Input range = ±0.625 × V_{REF}		88		
		Input range = 3 × V_{REF}		89		
		Input range = 2.5 × V_{REF}		89		
		Input range = 1.5 × V_{REF}		87		
		Input range = 1.25 × V_{REF}		86		
Internal Reference Output						
V_{REFIO_INT}	REFIO Voltage	Voltage on REFIO pin (configured as output) T_A= 25°C	4.088	4.096	4.104	V
	Reference Temperature Drift (1)			5	10	ppm/°C
C_{OUT_REFIO}	Decoupling Capacitor on REFIO			0.1		µF
V_{REFCAP}	Reference Voltage	Reference voltage to ADC (on REFCAP pin) T_A= 25°C	4.091	4.096	4.101	V
	Reference Buffer Output Impedance			0.5		Ω
	Reference Buffer Temperature Drift			1		ppm/°C
C_{OUT_REFCAP}	Decoupling Capacitor on REFIO			10		µF
t_{ON}	Reference Turn-on Time	C_{OUT_REFIO} = 0.1µF C_{OUT_REFCAP} = 10µF		10		ms
External Reference Input						
V_{REFIO_EXT}	External Reference	External reference voltage on REFIO (configured as input)	4.046	4.096	4.146	V
Power-supply Requirements						
AVDD	Analog Power-supply Voltage	Analog supply	4.75	5	5.25	V
DVDD	Digital Power-supply Voltage	Digital supply range	1.65	3.3	AVDD	V
		Digital supply range for specified performance	2.7	3.3	5.25	V

Parameter		Test Conditions	Min	Typ	Max	Unit
I_{AVDD_DYN}	AVDD Dynamic	AVDD = 5 V, f_S = maximum and internal reference		9	9.5	mA
I_{AVDD_STC}	AVDD Static	Device not converting and internal reference		8.5	9.3	mA
I_{STDBY}	Standby	At AVDD = 5 V, device in STDBY mode and internal reference		7		mA
I_{PWR_DN}	Power-down	At AVDD = 5 V, device in PWR_DN		2.8	200	µA
I_{DVDD_DYN}	Digital Supply Current	At DVDD = 3.3 V, output = 0000		0.1		mA
Digital Inputs (CMOS)						
V_{IH}	Digital Input Logic Levels	DVDD > 2.1 V	0.7 x DVDD		DVDD + 0.3	V
V_{IL}			–0.3		0.3 x DVDD	V
V_{IH}	Digital Input Logic Levels	DVDD ≤ 2.1 V	0.8 x DVDD		DVDD + 0.3	V
V_{IL}			–0.3		0.2 x DVDD	V
Input Leakage Current				100		nA
Input Capacitance				5		pF
Digital Outputs (CMOS)						
V_{OH}	Digital Output Logic Levels	I_O= 500-µA source	0.8 x DVDD		DVDD	V
V_{OL}		I_O= 500-µA sink	0		0.2 x DVDD	V
Floating State Leakage Current		Only for SDO		1		µA
Internal Pin Capacitance				5		pF
Temperature Range						
T_A	Operating Free-air Temperature		-40		125	°C

(1) These specifications are not production tested but are supported by characterization data at the initial product release.

Timing Requirements (1)

Conversion Cycle Timing Specifications

AVDD = 5 V, DVDD = 5 V, V_{REF} = 4.096 V internal reference, f_{SAMPLE} = 100 kSPS, T_A = 25°C, unless otherwise noted.

Parameter		Min	Typ	Max	Unit
Timing Specifications					
f_{cycle}	Sampling frequency			100	kSPS
t_{cycle}	ADC cycle time period	$1/f_{cycle}$			µs
f_{acq}	Acquisition time	5			µs
t_{CONV}	Conversion time			5	µs

Asynchronous Reset Timing Specifications

AVDD = 5 V, DVDD = 5 V, V_{REF} = 4.096 V internal reference, f_{SAMPLE} = 100 kSPS, T_A = −40°C to +125°C, unless otherwise noted.

Parameter		Min	Typ	Max	Unit
Timing Specifications					
t_{wl_RST}	Pulse duration: $\overline{RST}$ low	100			ns
$t_{D\_RST\_POR}$	Delay time for POR reset: $\overline{RST}$ rising to RVS rising		20		ms
$t_{D\_RST\_APP}$	Delay time for application reset: $\overline{RST}$ rising to CONVST/$\overline{CS}$ rising			1	µs
t_{NAP_WKUP}	Wake-up time: NAP mode			20	µs
t_{PWRUP}	Power-up time: PD mode		20		ms

SPI-Compatible Serial Interface Timing Specifications

AVDD = 5 V, DVDD = 5 V, V_{REF} = 4.096 V internal reference, f_{SAMPLE} = 100 kSPS, T_A = −40°C to +125°C, unless otherwise noted.

Parameter		Min	Typ	Max	Unit
Timing Specifications					
f_{CLK}	Serial clock frequency			66.67	MHz
t_{CLK}	Serial clock time period	$1/f_{cycle}$			
t_{PH_CK}	SCLK high time	0.45		0.55	t_{CLK}
t_{PL_CK}	SCLK low time	0.45		0.55	t_{CLK}
t_{SU_CSCK}	Setup time: CONVST/$\overline{CS}$ falling to first SCLK capture edge	7.5			ns
t_{SU_CKDI}	Setup time: SDI data valid to SCLK capture edge	7.5			ns
t_{HT_CKDI}	Hold time: SCLK capture edge to (previous) data valid on SDI	7.5			ns
t_{HT_CKCS}	Delay time: last SCLK capture edge to CONVST/$\overline{CS}$ rising	7.5			ns
t_{DEN_CSDO}	Delay time: CONVST/$\overline{CS}$ falling edge to data enable			9.5	ns
t_{DZ_CSDO}	Delay time: CONVST/$\overline{CS}$ rising to SDO-x going to 3-state			10	ns

Parameter		Min	Typ	Max	Unit
t_{D_CKDO}	Delay time: SCLK launch edge to (next) data valid on SDO-x			12	ns
t_{D_CSRVS}	Delay time: CONVST/$\overline{CS}$ rising edge to RVS falling			14	ns

Timing Requirements: Source-Synchronous Serial Interface (External Clock)

AVDD = 5 V, DVDD = 5 V, V_{REF} = 4.096 V internal reference, f_{SAMPLE} = 100 kSPS, T_A = −40°C to +125°C, unless otherwise noted.

Parameter		Min	Typ	Max	Unit
Timing Specifications					
f_{CLK}	Serial clock frequency			66.67	MHz
t_{CLK}	Serial clock time period	$1/f_{cycle}$			
t_{PH_CK}	SCLK high time	0.45		0.55	t_{CLK}
t_{PL_CK}	SCLK low time	0.45		0.55	t_{CLK}
t_{DEN_CSDO}	Delay time: CONVST/$\overline{CS}$ falling edge to data enable			9.5	ns
t_{DZ_CSDO}	Delay time: CONVST/$\overline{CS}$ rising to SDO-x going to 3-state			10	ns
$t_{D\_CKRVS\_r}$	Delay time: SCLK rising edge to RVS rising			14	ns
$t_{D\_CKRVS\_f}$	Delay time: SCLK falling edge to RVS falling			14	ns
t_{D_RVSDO}	Delay time: RVS rising to (next) data valid on SDO-x			2.5	ns
t_{D_CSRVS}	Delay time: CONVST/$\overline{CS}$ rising edge to RVS displaying internal device state			15	ns

Timing Requirements: Source-Synchronous Serial Interface (Internal Clock)

AVDD = 5 V, DVDD = 5 V, V_{REF} = 4.096 V internal reference, f_{SAMPLE} = 100 kSPS, T_A = −40°C to +125°C, unless otherwise noted.

Parameter		Min	Typ	Max	Unit
Timing Specifications					
t_{DEN_CSDO}	Delay time: CONVST/$\overline{CS}$ falling edge to data enable			9.5	ns
t_{DZ_CSDO}	Delay time: CONVST/$\overline{CS}$ rising to SDO-x going to 3-state			10	ns
t_{DEN_CSRVS}	Delay time: CONVST/$\overline{CS}$ falling edge to first rising edge on RVS			50	ns
t_{D_RVSDO}	Delay time: RVS rising to (next) data valid on SDO-x			2.5	ns
t_{INTCLK}	Time period: internal clock	15			
t_{CYC_RVS}	Time period: RVS signal	15		15	ns
t_{WH_RVS}	RVS high time	0.4		0.6	t_{INTCLK}
t_{WL_RVS}	RVS low time	0.4		0.6	t_{INTCLK}
t_{D_CSRVS}	Delay time: CONVST/$\overline{CS}$ rising edge to RVS displaying internal device state			15	ns

(1) Parameters are preliminary and provided by design simulation.

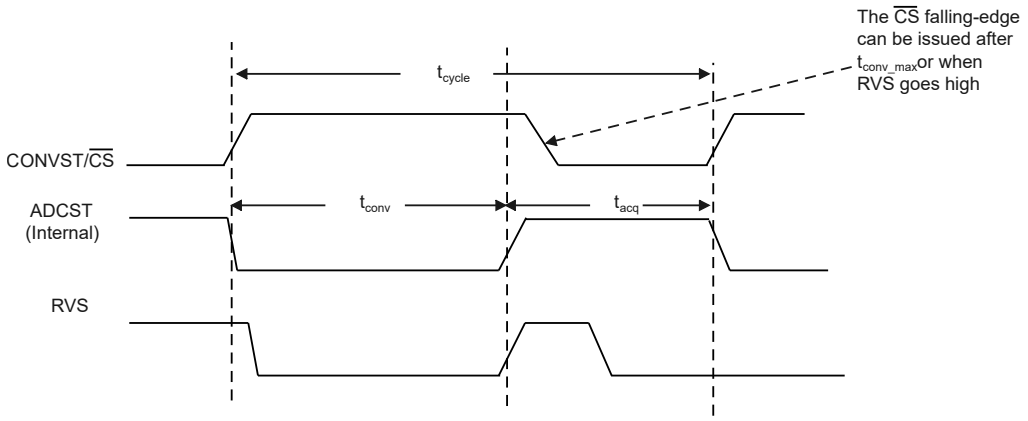


Figure 1. Conversion Cycle Timing Diagram

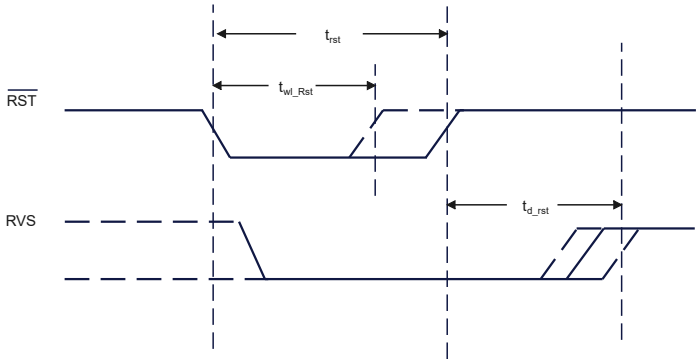


Figure 2. Asynchronous Reset Timing Diagram

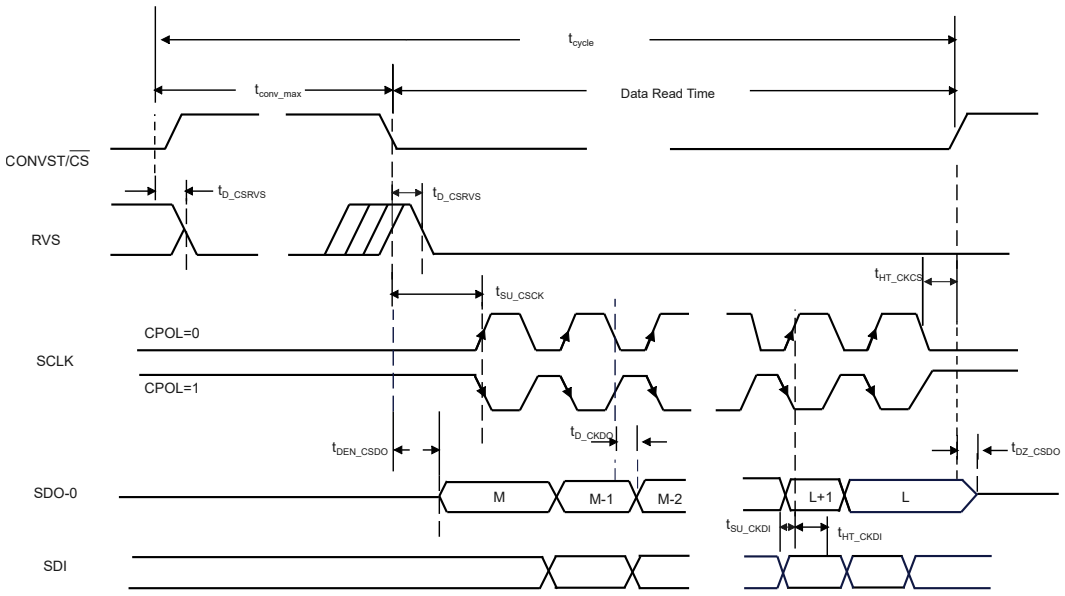


Figure 3. Standard SPI Interface Timing Diagram for CPHA = 0

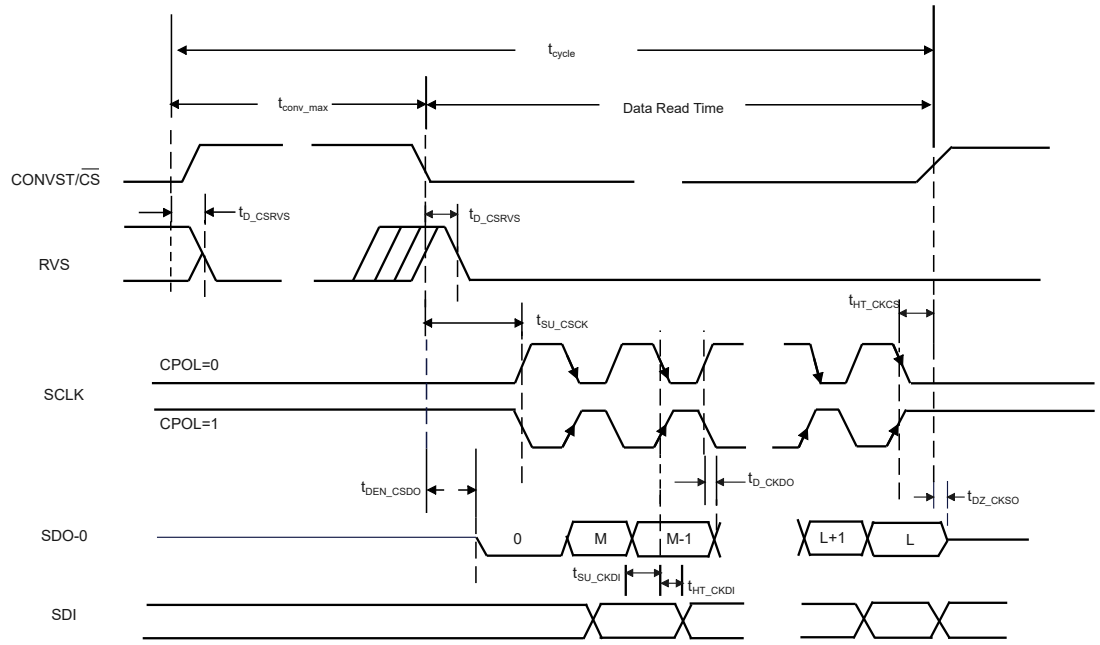


Figure 4. Standard SPI Interface Timing Diagram for CPHA = 1

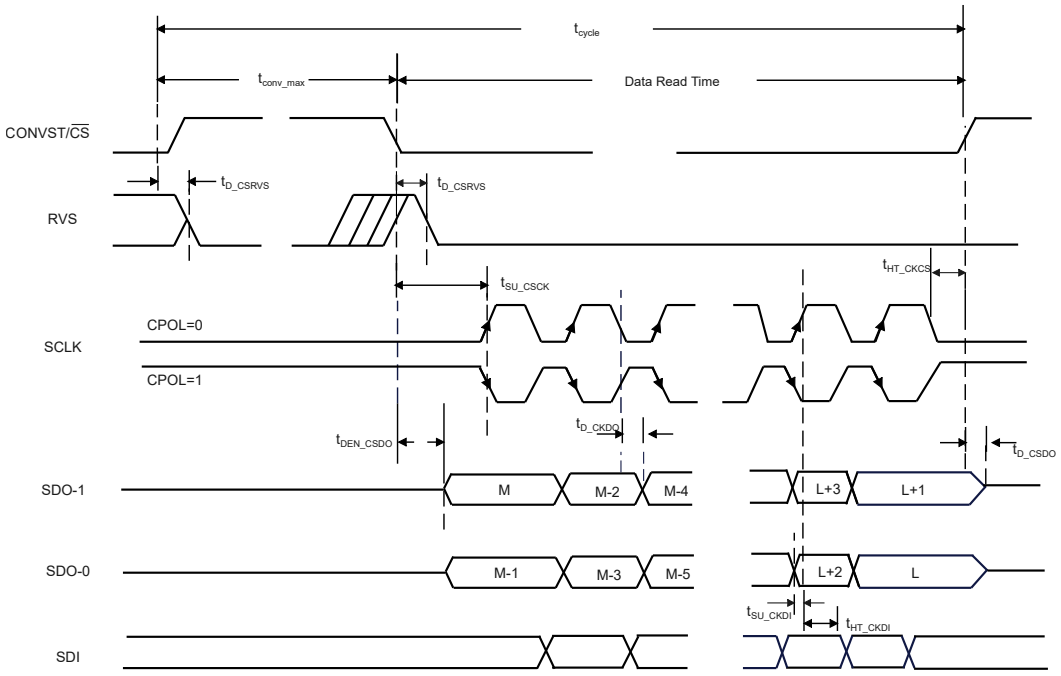


Figure 5. MultiSPI Interface Timing Diagram for Dual SDO-x and CPHA = 0

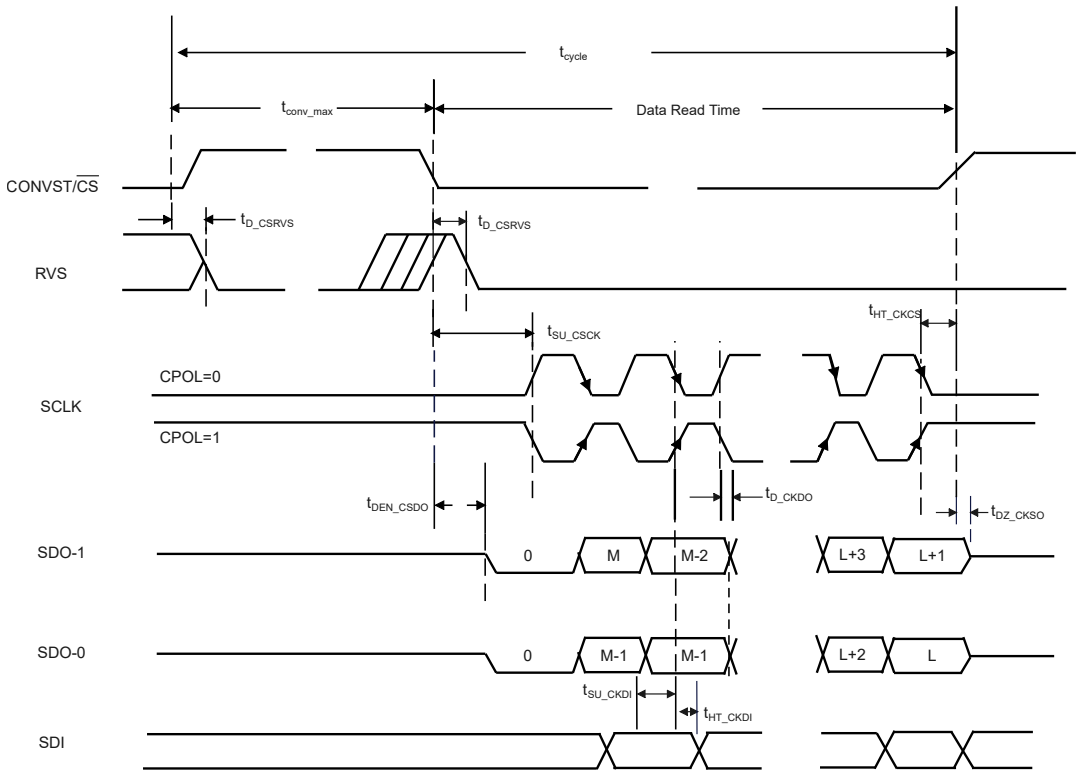


Figure 6. MultiSPI Interface Timing Diagram for Dual SDO-x and CPHA = 1

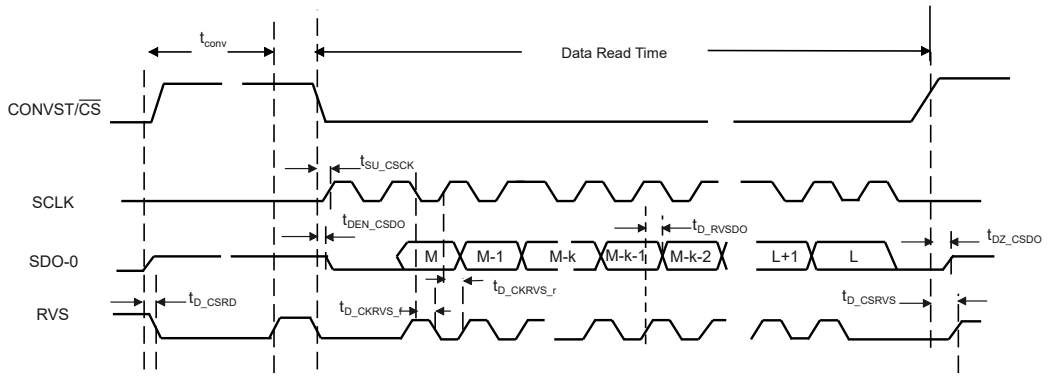


Figure 7. MultiSPI Source-Synchronous External Clock Serial Interface Timing Diagram

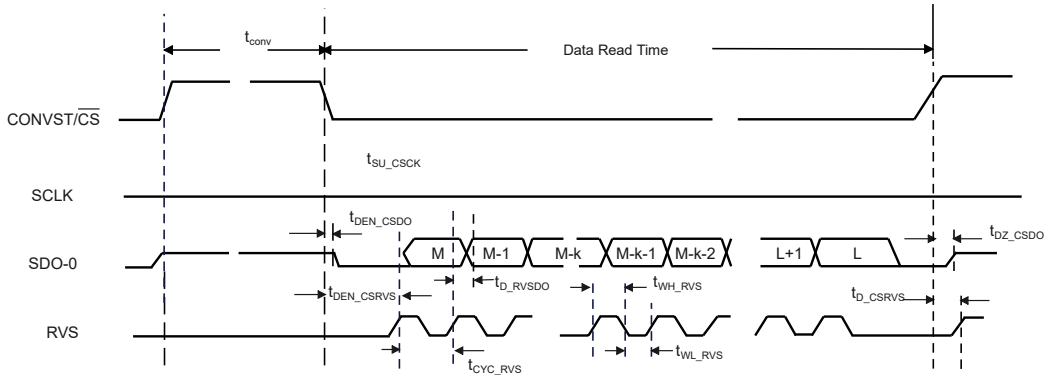


Figure 8. MultiSPI Source-Synchronous Internal Clock Serial Interface Timing Diagram

Typical Performance Characteristics

All test conditions: at T_A = 25°C, AVDD = 5 V, DVDD = 5 V, VREF = 4.096 V (internal), and maximum throughput (unless otherwise noted).

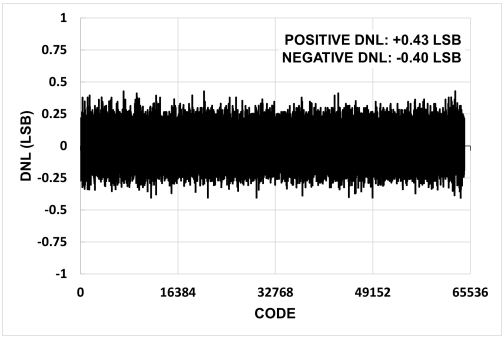


Figure 9. DNL

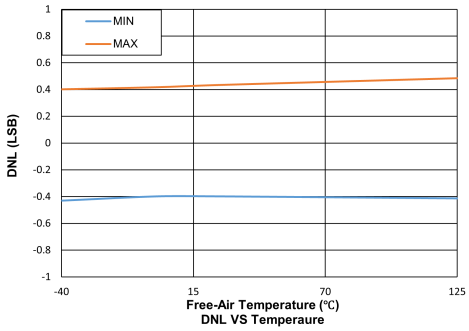


Figure 10. DNL vs. Temperature

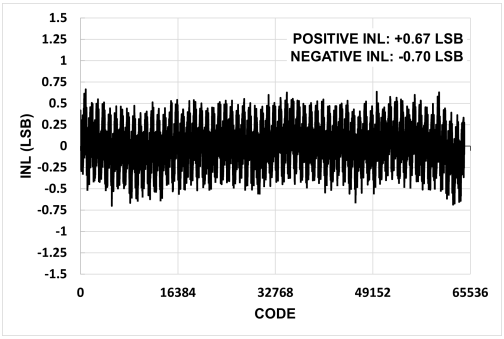


Figure 11. INL (Bipolar Ranges)

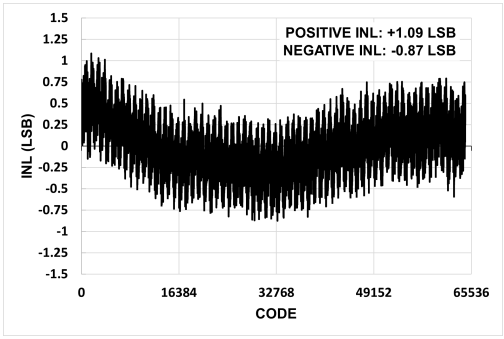


Figure 12. INL (Unipolar Ranges)

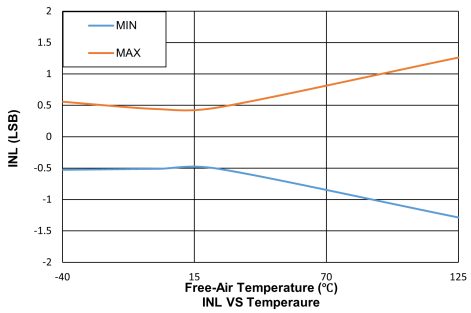


Figure 13. INL vs. Temperature (Bipolar Ranges)

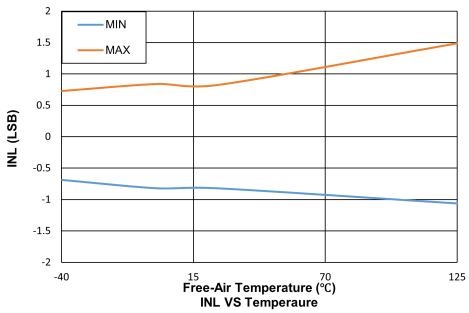


Figure 14. INL vs. Temperature (Unipolar Ranges)

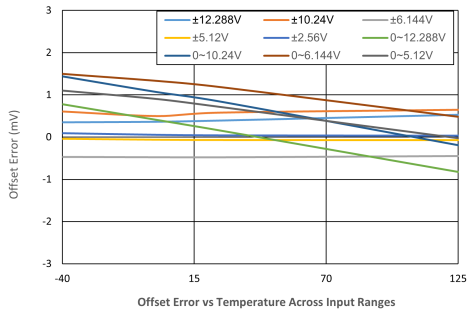


Figure 15. Offset vs. Temperature

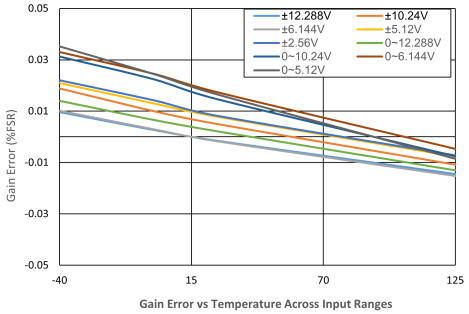


Figure 16. Gain Error vs. Temperature

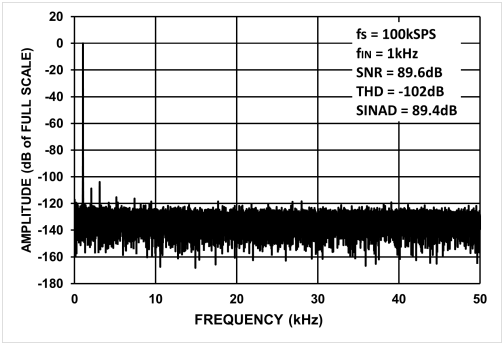


Figure 17. FFT Plot

Detailed Description

Overview

The TPAFE51716S is a 16-bit data acquisition system with single analog input channels. Each input channel includes input protection circuitry, a programmable gain amplifier (PGA), an analog low-pass filter, and an analog-to-digital converter (ADC) driver with ADC operating on 100 KSPS throughput rate. The device incorporates a 4.096V internal reference with a fast-settling buffer. It also provides high-speed serial interfaces for communication with a daisy-chain function, making it suitable for a wide range of data acquisition applications.

The device operates with a single 5-V analog supply and can process true bipolar input signals. It provides a programmable analog signal range, including options for true bipolar single-ended ±12.288 V, ±10.24 V, ±6.144 V, ±5.12 V, ±3.072 V, ±2.56 V, unipolar single-ended 0 V - 12.288 V, 0 V - 10.24 V, 0 V - 6.144 V, 0 V - 5.12 V, and true bipolar fully-differential ±12.288 V, ±10.24 V, ±6.144 V, ±5.12 Vinput signals. The input clamp protection circuitry can protect the device from being damaged by voltages as high as ±30 V. The device features a constant 1-MΩ resistive input impedance.

Functional Block Diagram

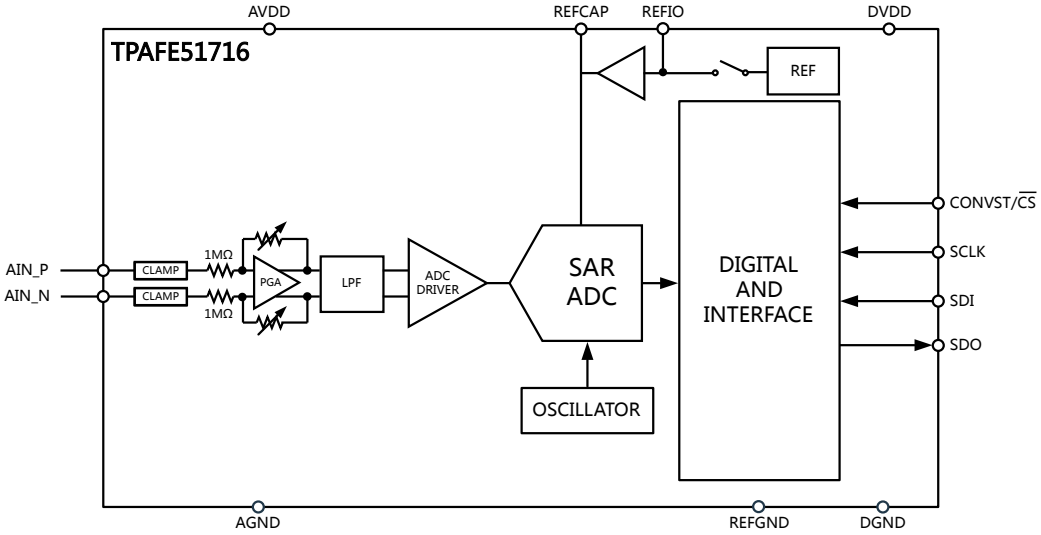


Figure 18. TPAFE51716S Block Diagram

Feature Description

Analog Inputs

The TPAFE51716 incorporates a 16-bit successive approximation register (SAR) analog-to-digital converter (ADC). The device comprises one analog input pairs. The ADC is responsible for converting the voltage difference between the analog input pair AIN_P – AIN_N. The simplified circuit schematic for each analog input channel is shown in a function block diagram, encompassing the input clamp protection circuit, PGA, low-pass filter, high-speed ADC driver, and a precision 16-bit SAR ADC.

Analog Input Ranges

The TPAFE51716 can handle true bipolar differential, bipolar single-ended, and unipolar single-ended input voltages. It is possible to configure an individual analog input range per channel, from the range select registers.

The devices sample the voltage difference (AIN_P – AIN_N) between the selected analog input pairs. This feature is beneficial in modular systems where the sensor or signal-conditioning block is located at a distance from the ADC on the board. It proves particularly useful when there might be a difference in the ground potential between the sensor or signal conditioner and the ADC ground. In such cases, it is recommended to run separate wires from the AIN_N pin of the device to the sensor or signal-conditioning ground.

In single-ended mode, the AIN_N pins are typically connected to analog ground and allow a ±0.1 V range referred to ground.

In differential mode, the AIN_P and AIN_N typically sense the fully differential input signals within a certain input common mode range. Also, this feature is beneficial in modular systems where the sensor or signal-conditioning block is located at a distance from the ADC on the board. It proves particularly useful when there might be a difference in the ground potential between the sensor or signal conditioner and the ADC ground. In such cases, it is recommended to run separate wires from the AIN_N pin of the device to the sensor or signal-conditioning ground.

Analog Input Impedance

The TPAFE51716 features a fixed high analog input impedance of 1 MΩ, which is nearly constant at different sampling frequencies. It eliminates the need for an external driver amplifier, allowing direct connection to the source or sensor.

Analog Input Clamp Protection

The TPAFE51716 incorporates an internal clamp protection circuit on each of the analog input channels. This protection circuit allows each analog input voltage to swing up to ±30 V. Beyond this threshold, the input clamp circuit activates while still operating from a single 5 V supply.

To ensure that the input current stays within safe limits (±10 mA) for input voltages above the clamp threshold, it is advisable to use a series resistor with the analog inputs. This resistor can serve the dual purpose of limiting input current and providing an antialiasing low-pass filter (LPF) when combined with a capacitor. Matching the external source impedance on the AIN_P and AIN_N pins helps cancel any additional offset error. However, it's advisable to avoid prolonged activation of the clamp protection circuitry during normal or power-down conditions for optimal device performance.

Programmable Gain Amplifier (PGA)

The TPAFE51716 includes a PGA at each analog input channel, providing support for both unipolar/bipolar single-ended and bipolar differential inputs. The supported analog input ranges are listed below. The input range is set by the RANGE_SEL[3:0] bits in the configuration register.

Table 2. Analog Input Ranges

Analog Input Mode	Analog Input Range	RANGE_SEL[3:0]			
		BIT 3	BIT 2	BIT 1	BIT 0
Single-ended	±3 x V_{REF}	0	0	0	0
Single-ended	±2.5 x V_{REF}	0	0	0	1
Single-ended	±1.5 x V_{REF}	0	0	1	0
Single-ended	±1.25 x V_{REF}	0	0	1	1
Single-ended	±0.625 x V_{REF}	0	1	0	0
Single-ended	±0.75 x V_{REF}	0	1	0	1
Differential	±3 x V_{REF}	0	1	1	0
Differential	±2.5 x V_{REF}	0	1	1	1
Single-ended	0 to 3 x V_{REF}	1	0	0	0
Single-ended	0 to 2.5 x V_{REF}	1	0	0	1
Single-ended	0 to 1.5 x V_{REF}	1	0	1	0
Single-ended	0 to 1.25 x V_{REF}	1	0	1	1
Differential	±1.5 x V_{REF}	1	1	0	0
Differential	±1.25 x V_{REF}	1	1	0	1
Differential	±0.75 x V_{REF}	1	1	1	0
Differential	±0.625 x V_{REF}	1	1	1	1

The analog input channel on the TPAFE51716 is equipped with an antialiasing low-pass filter (LPF) situated at the PGA output. The following table outlines the programmable LPF options associated with the analog input range in the device. The analog input bandwidth for all eight channels can be chosen using the LPF_CONFIG[1:0] bits found in address 0x34.

Table 3. Low-Pass Filter Corner Frequency

LPF	Analog Input Range	Typical −3 dB Bandwidth
Low-bandwidth	All input ranges	15 kHz
High-bandwidth	All input ranges	35 kHz

Reference

The TPAFE51716 can operate with either an internal voltage reference or an external voltage reference, utilizing the internal buffer. The configuration between internal and external reference is controlled by programming the INTREF_DIS bit of the RANGE_SEL_REG register. The devices incorporate a built-in buffer amplifier designed to drive the reference input of the internal ADC core, optimizing overall performance.

Internal Reference

The TPAFE51716 includes an on-chip 4.096 V reference, which can be accessed through the REFIO pin. The SAR ADC utilizes this internally generated and buffered 4.096 V reference for its conversions. To select the internal reference, program the INTREF_DIS bit of the RANGE_SEL_REG register. The internal reference is enabled (INTREF_DIS = 0) by default after reset or powering up. The INTREF_DIS bit must be set to 1 to disable the internal reference source if an external reference source is used. In this configuration, the REFIO pin serves as an output pin, providing the internal reference value. It is recommended to place a 10 µF and a 0.1 µF decoupling capacitor between the REFIO pin and REFGND. Place the capacitor

as close to the REFIO pin as possible.The capacitors act as decoupling components and form a low-pass filter with the output impedance of the internal band-gap circuit, limiting the noise of the reference. Avoid using the REFIO pin to drive external loads, as REFIO has limited current output capability. If needed as a source, it can be followed by an operational amplifier buffer.

External Reference

Alternatively, the TPAFE51716 can accept an external reference voltage applied to the REFIO pin. When an external 4.096 V reference is provided, the device internally amplifies it to create the 4.096 V buffered reference used by the SAR ADC. To select external reference mode, , the INTREF_DIS bit of the RANGE_SEL_REG register must be set to 1. In this mode, an external 4.096-V reference should be applied at REFIO, which becomes an input pin. The user can use any external reference in this mode. The internal buffer is designed to handle dynamic loading on the REFCAP pin, which is internally connected to the ADC reference input. When using an external reference, it's important to appropriately filter the reference output to minimize its impact on system performance.

The output of the internal reference buffer is present at the REFCAP pin. To ensure proper operation, decoupling capacitors of 22 µF and 0.1 µF must be connected between REFCAP and REFGND. It's important not to use the internal buffer to drive any external loads due to the limited current output capability of this buffer.

ADC Transfer Function

The TPAFE51716 outputs 16 bits of conversion data in straight binary format for all ranges and all modes (unipolar/bipolar). The full-scale range (FSR) for each input signal is determined by the difference between the positive full-scale (PFS) input voltage and the negative full-scale (NFS) input voltage. The size of the least significant bit (LSB) is calculated as FSR / 2^16 = FSR / 65536 for the 16-bit resolution of the ADC. In the case of a reference voltage (V_{REF}) set to 4.096 V, the LSB values for various input ranges are as follows:

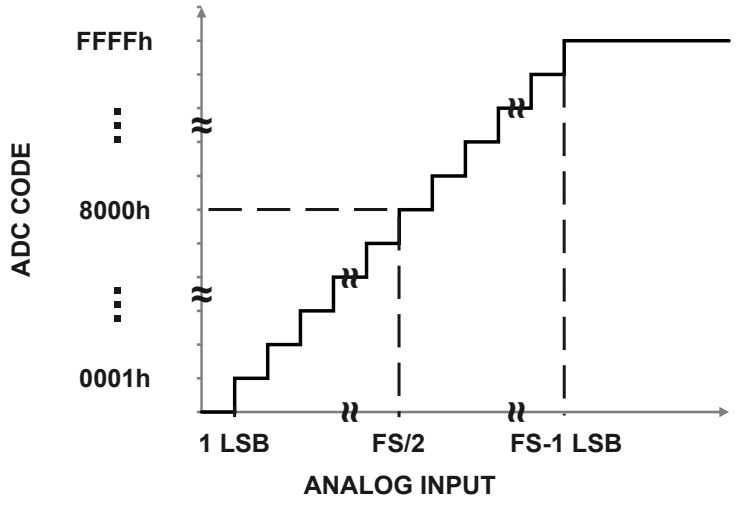


Figure 19. Device Transfer Function (Straight-Binary Format)

Table 4. Transfer Characteristics

Input Range	NFS (V)	PFS (V)	FSR (V)	LSB (µV)
±3 x V_{REF}	-12.288	12.288	24.576	375
±2.5 x V_{REF}	-10.24	10.24	20.48	312.5
±1.5 x V_{REF}	-6.144	6.144	12.288	187.5

Input Range	NFS (V)	PFS (V)	FSR (V)	LSB (µV)
±1.25 x V_{REF}	-5.12	5.12	10.24	156.25
±0.75 x V_{REF}	-3.072	3.072	6.144	93.75
±0.625 x V_{REF}	-2.56	2.56	5.12	78.125
0 to 3 x V_{REF}	0	12.288	12.288	187.5
0 to 2.5 x V_{REF}	0	10.24	10.24	156.25
0 to 1.5 x V_{REF}	0	6.144	6.144	93.75
0 to 1.25 x V_{REF}	0	5.12	5.12	78.125

Alarm Feature

The device includes an active-high alarm output on the ALARM/SDO-1/GPO pin when configured for alarm functionality. To enable the ALARM output on this multifunction pin, set the SDO1_CONFIG[1:0] bits in the SDO_CTL_REG register to 01b.

The device supports two alarm functions: an input alarm and an AVDD alarm.

- The input alarm monitors the ADC input voltage and compares it to user-programmable high and low thresholds. An active-high alarm output is triggered if the value of the input signal exceeds these thresholds.
- The AVDD alarm monitors the ADC's analog supply voltage and compares it to programmed low and high thresholds. An active-high alarm output is triggered if AVDD crosses either threshold in any direction.

When the alarm functionality is turned on, both the input and AVDD alarm functions are enabled by default. These alarm functions can be selectively disabled by programming the IN_AL_DIS and VDD_AL_DIS bits(respectively) of the RST_PWRCTL_REG register

Each alarm, whether input or AVDD, has two associated flags: the active alarm flag and the tripped alarm flag, both readable in the ALARM_REG register. When an alarm is triggered, both flags are set. The active alarm flag clears at the end of the current ADC conversion unless the alarm condition persists, while the tripped flag remains set until ALARM_REG is read.

The ALARM output flags update internally at the end of each conversion and can be read during any data frame initiated by pulling the CONVST/$\overline{CS}$ signal low.

The ALARM output flags can be accessed through the ALARM output pin, by reading the internal ALARM registers, or by appending the ALARM flags to the data output.

- A high level on the ALARM pin signals an over- or undervoltage condition on AVDD or an analog input channel. This pin can be used to interrupt the host input.
- The internal ALARM flag bits in the ALARM_REG register update at the end of each conversion. After an ALARM interrupt is received on the output pin, reading the internal alarm flag registers provides details on the conditions that triggered the alarm.
- The alarm output flags can be optionally included in the data output bit stream, allowing the user to monitor alarm conditions alongside conversion data.

Input Alarm

The device includes both high and low alarms for the analog input. These alarms have independently programmable threshold values, which can be adjusted through the ALARM_H_TH_REG and ALARM_L_TH_REG registers. A common hysteresis setting is applied to both alarms to prevent rapid toggling due to minor signal fluctuations.

The device triggers an input high alarm when the digital output exceeds the [high alarm threshold (T)]. The alarm is cleared when the digital output falls below or equals the high alarm lower limit [high alarm (T) – H – 1].

Similarly, the input low alarm is activated when the digital output drops below the low alarm threshold [low alarm threshold (T)]. The alarm is reset when the digital output rises above or equals the low alarm higher limit [low alarm (T) + H + 1].

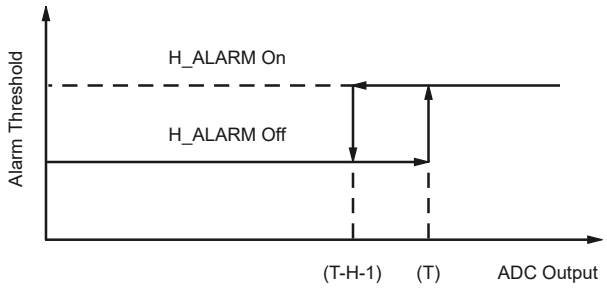


Figure 20. High ALARM Hysteresis

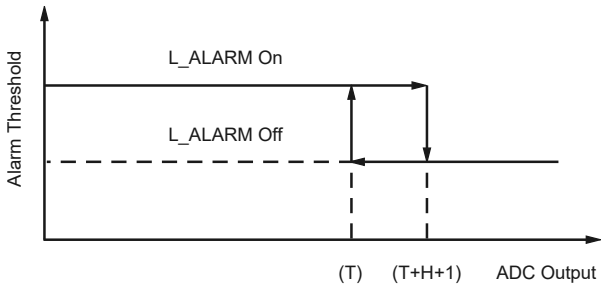


Figure 21. Low ALARM Hysteresis

AVDD Alarm

The device includes high and low alarms for monitoring the analog voltage supply, AVDD. These alarms are triggered by fixed trip points, designed to alert when the AVDD supply voltage exceeds or falls below specified thresholds. The high alarm is triggered if AVDD exceeds a typical value of 5.3 V or 5.5 V. The low alarm is asserted if AVDD drops below 4.7 V. This feature is particularly useful for identifying issues such as glitches or brown-out conditions on the analog AVDD supply, which could lead to unexpected device behavior.

Device Functional Modes

Device Modes

The device features a multiSPI digital interface that facilitates communication and data transfer between the device and the host controller. This interface supports multiple data transfer protocols, enabling the host to exchange both data and commands with the device. The host can transfer data into the device using one of the standard SPI modes. The device can be configured to output data in various ways, allowing flexibility in terms of throughput and latency requirements. The control of data output can either be managed by the host or the device, and the timing of data exchange can be either system synchronous or source synchronous.

The digital interface module of the device consists of several main components, which include shift registers (both input and output), configuration registers, and a protocol unit. These components work together to handle data transfer between the device and the host. In any given data frame, data are transferred both into and out of the device. As a result, the host perceives the device as a 32-bit input-output shift register, providing a continuous exchange of data. This structure ensures that the communication between the device and the host is efficient and flexible, allowing for seamless operation.

Host-to-Device Connection Topologies

The multiSPI interface allows for various configurations of data exchange between the host and the device. By configuring the appropriate device registers, the host can choose the optimal communication method to suit the specific system requirements, such as throughput, latency, and the number of connected devices. The flexibility of the multiSPI interface enables the user to adapt the data transfer protocol to different topologies, making it easier to integrate the device into various system architectures.

Single Device: All multiSPI Options

The figure below shows the pin connection between a host controller and a stand-alone device to exercise all options provided by the multiSPI interface.

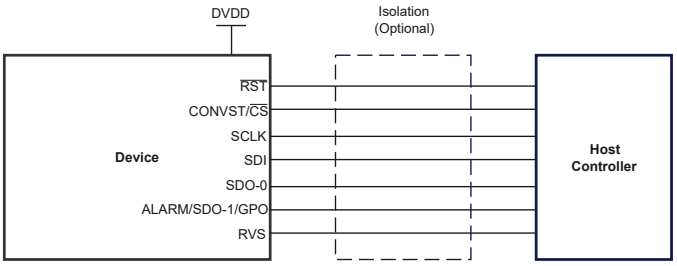


Figure 22. All MultiSPI Protocols Pin Configuration

Single Device: Standard SPI Interface

The figure below shows the minimum pin interface for applications using a standard SPI protocol.

The CONVST/$\overline{CS}$, SCLK, SDI, and SDO-0 pins constitute a standard SPI port of the host controller. The $\overline{RST}$ pin can be tied to DVDD. The RVS pin can be monitored for timing benefits. The ALARM/SDO-1/GPO pin may not have any external connection.

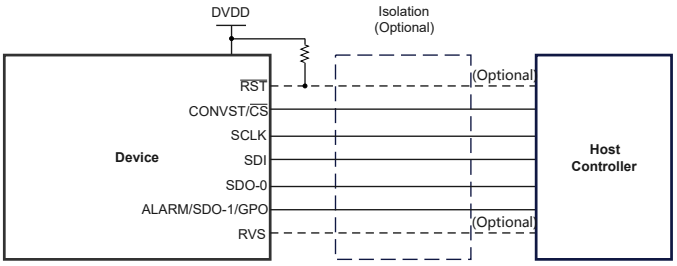


Figure 23. Standard SPI Protocol Pin Configuration

Multiple Devices: Daisy-Chain Topology

A typical connection diagram showing multiple devices in a daisy-chain topology is shown below.

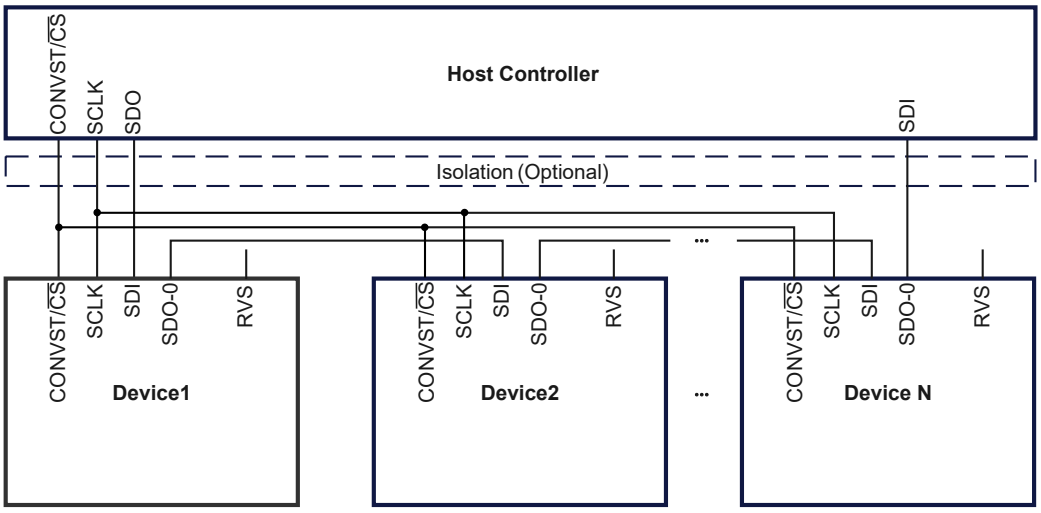


Figure 24. Standard SPI Protocol Pin Configuration

In this configuration, multiple devices are chained together, allowing the host controller to communicate with each device sequentially. The CONVST/$\overline{CS}$ and SCLK signals are shared across all devices, with the SDI input of the first device connected to the host's SDO-x output. The output from each device is then passed to the next device in the chain, with the final device's output connecting back to the host's SDI pin. This arrangement enables the host to send and receive data from multiple devices over a single SPI interface.

To set up multiple devices in a daisy-chain configuration, the host controller must ensure that each device is programmed with the same configuration register values. This ensures that the devices work together using a shared SDO-0 output. The data transfer between devices should occur with the external clock, and the devices should follow one of the legacy, SPI-compatible protocols for data reading and writing.

In a daisy-chain configuration, all devices in the chain sample their analog input signals on the rising edge of the CONVST/$\overline{CS}$ signal. The data transfer frame begins when CONVST/$\overline{CS}$ transitions to a falling edge. At each rising edge of the SCLK signal, every device in the chain shifts out the most significant bit (MSB) to the SDO-0 pin. On each subsequent falling edge of SCLK, the devices shift in the data received on the SDI pin, adding it as the least significant bit (LSB) of the unified shift register. This setup results in a data stream where the host controller receives data in the following order: first from device N, then device N-1, and so on, with the most significant bit sent first (MSB-first). When the CONVST/$\overline{CS}$ signal rises again, each device decodes the data in the unified shift register and takes the appropriate action based on the received information. This allows for efficient data transfer and synchronization in the daisy-chain topology.

In a daisy-chain topology with N devices, the data transfer frame must consist of 32 × N SCLK capture edges to ensure proper data transmission and device configuration. This ensures that each device in the chain receives its complete set of data. If the data transfer frame is shorter than 32 × N SCLK capture edges, it can lead to incorrect or incomplete configurations for the devices, causing erroneous operation. Therefore, it's important to ensure the frame is of the correct length. If the data transfer frame exceeds 32 × N SCLK capture edges, the host controller must carefully align the configuration data for each device before bringing the CONVST/$\overline{CS}$ signal high. This alignment ensures that the data is correctly distributed across all devices in the chain.

In a daisy-chain topology, the overall system throughput decreases as the number of devices in the chain increases. This is because the data transfer frame needs to accommodate data for each device, and the time it takes to shift data through the chain grows with the number of devices. For N devices in the chain, the data must be shifted out sequentially for each device, which increases the total number of clock cycles required for each transfer. Therefore, the more devices in the chain, the longer it takes to complete a full data transfer, resulting in reduced throughput. A typical timing diagram for three devices connected in a daisy-chain topology and using the SPI-00-S protocol is shown below.

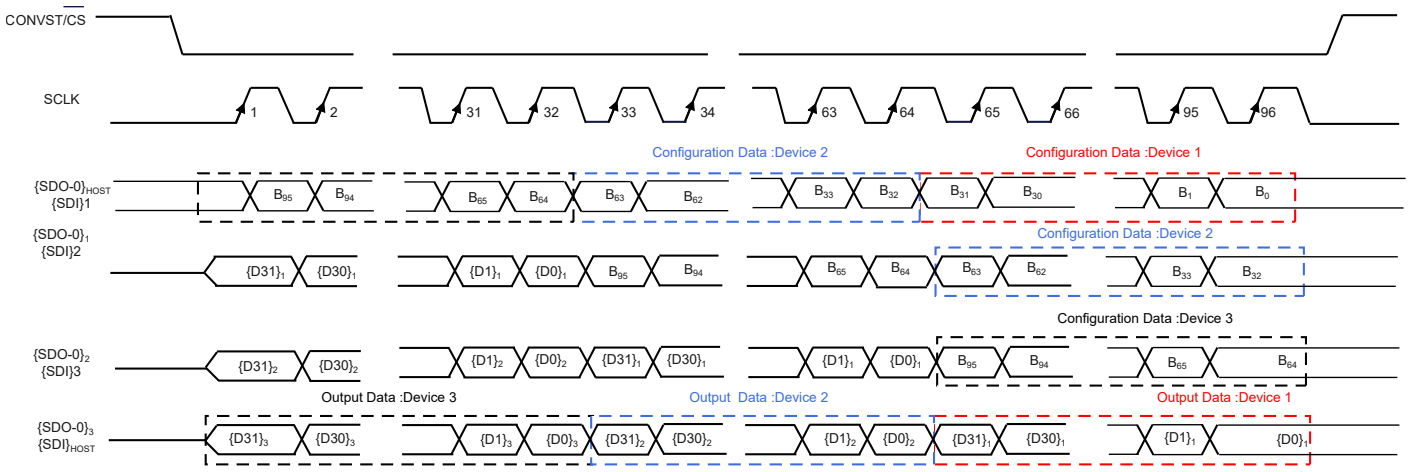


Figure 25. Three Devices in Daisy-Chain Mode Timing Diagram

Device Operational Modes

The TPAFE51716 offers various modes of operation: RESET, ACQ, and CONV, which are configured by CONVST/$\overline{CS}$ and $\overline{RST}$ signals.

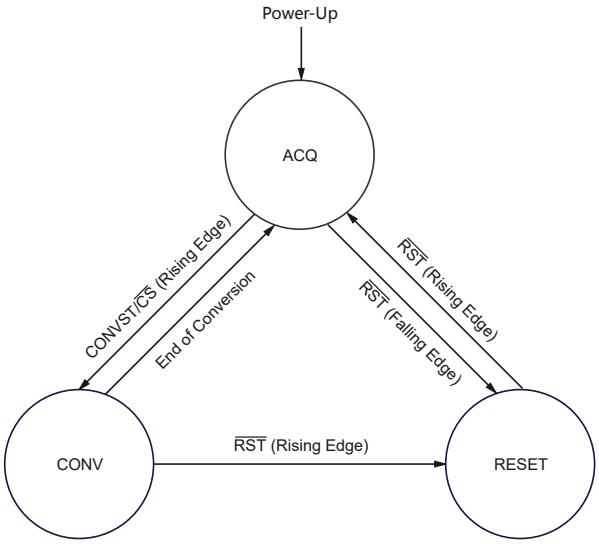


Figure 26. Device Functional States

RESET State

To initiate a RESET state, the device provides an active-low $\overline{RST}$ pin, which functions as an asynchronous digital input. To trigger the RESET, the $\overline{RST}$ pin needs to be pulled low and maintained at a low state for the duration specified in the Timing Requirements: Asynchronous Reset table, typically referred to as the t_{wl_RST} duration.

The device consists of two different types of reset functions: an application reset or a power-on reset (POR). The functionality of the RST pin is determined by the state of the RSTn_APP bit in the RST_PWRCTL_REG register.

To enable the $\overline{RST}$ pin for initiating an application reset, the RSTn_APP bit within the RST_PWRCTL_REG register needs to be set to 1b. When in this RESET state, all configuration registers are reset to their default values, the RVS pins remain at a low state, and the SDO-x pins enter a tri-state mode.

By default, the $\overline{RST}$ pin is configured to trigger a power-on reset (POR) when pulled low, with the RSTn_APP bit set to 0b. During a POR, all internal components of the device, such as the PGA, ADC driver, and voltage reference, undergo a reset. After exiting the POR state, it's essential to allow the specified duration of $t_{D\_RST\_POR}$ for the internal circuitry to stabilize accurately.

To exit any of the RESET states, the $\overline{RST}$ pin needs to be pulled high while keeping CONVST/$\overline{CS}$ and SCLK held low. Following a delay specified by either $t_{D\_RST\_POR}$ or $t_{D\_RST\_APP}$, the device transitions to the ACQ state, and the RVS pin transitions to a high state.

To operate the device in either the ACQ or CONV states, the $\overline{RST}$ pin should be maintained at a high level. In this configuration, transitions occurring on the CONVST/$\overline{CS}$ pin dictate the functional state of the device.

ACQ State

During the ACQ state, the device initiates the acquisition of the analog input signal. This state is entered upon power-up, following any asynchronous reset, or upon completion of each conversion process.

Transitioning from the ACQ state to the RESET state occurs on the falling edge of the $\overline{RST}$ signal, while transitioning to the CONV state happens on the rising edge of the CONVST/$\overline{CS}$ signal.

Additionally, the device features a low-power NAP mode to minimize power consumption during the ACQ state.

CONV State

Upon the rising edge of the CONVST/$\overline{CS}$ signal, the device transitions from the ACQ state to the CONV state. During the conversion process, the device utilizes an internal clock, disregarding any subsequent transitions on the CONVST/$\overline{CS}$ signal until the ongoing conversion concludes, typically within the time interval denoted as t_{conv}.

To activate the STDBY mode, perform a valid write operation to the command register with the STDBY command set to 8200h. This command is executed, and the device enters STDBY mode on the subsequent rising edge of the $\overline{CS}$ signal following the write operation. The device will remain in STDBY mode if no valid conversion command (AUTO_RST or MAN_Ch_n) is executed and SDI remains low during the subsequent data frames. In STDBY mode, the program register settings can be modified (as detailed in the Program Register Read/Write Operation section) using 16 SCLK cycles. However, if 32 complete SCLK cycles are provided, the device will output invalid data on the SDO line since there is no ongoing conversion in STDBY mode. Nonetheless, the program register read operation can proceed normally during this mode.

At the end of the conversion process, the device reverts to the ACQ state. The cycle time for the device is determined by:

$t_{cycle\text{-}min} = t_{conv} + t_{acq\text{-}min}$

Programming

The device consists of configuration registers, detailed in the Register Maps section, which facilitate two primary types of data transfer operations: data writes, where the host configures the device, and data reads, where the host retrieves data from the device.

Data Transfer Frame

A data transfer frame between the device and the host controller starts at the falling edge of the CONVST/$\overline{CS}$ pin and concludes when the device begins conversion at the subsequent rising edge. The host controller can trigger a data transfer frame by lowering the CONVST/$\overline{CS}$ signal, typically after the CONV phase ends, as outlined in the CONV State section.

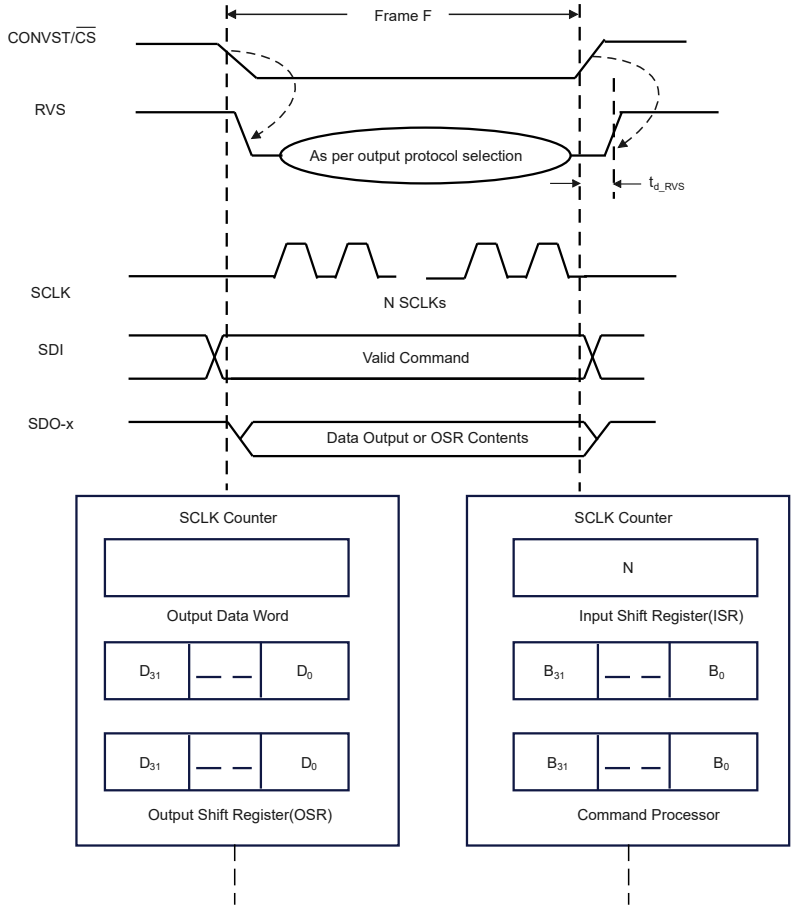


Figure 27. Data Transfer Frame

For a typical data transfer frame F:

1. The host controller initiates the frame by pulling CONVST/$\overline{CS}$ low. Upon the falling edge of CONVST/$\overline{CS}$:

- RVS signal goes low, marking the start of the frame.
- The internal SCLK counter resets to 0.
- The device takes control of the data bus, loading the output data word into the 32-bit output shift register (OSR).
- The internal configuration register resets to 0000h, equivalent to a NOP command.

2. During the frame, the host controller provides clocks on the SCLK pin:

- On each SCLK capture edge, the SCLK counter increments, and the data bit received on SDI is shifted into the LSB of the input shift register.
- On each launch edge of the output clock (SCLK), the MSB of the output shift register data is shifted out on the selected SDO-x pins.
- The RVS pin status depends on the output protocol selection.

3. The host controller ends the frame by pulling CONVST/$\overline{CS}$ high. Upon the rising edge of CONVST/$\overline{CS}$:

- The SDO-x pins go to tri-state.
- The contents of the input shift register transfer to the command processor for decoding.

- RVS output goes low, marking the start of conversion.

After pulling CONVST/$\overline{CS}$ high, the host controller must monitor for a low-to-high transition on the RVS pin or wait for the tconv_max time before initiating a new frame.

At the end of the frame:

- If the SCLK counter = 32, the frame is treated as an optimal data transfer frame, and its contents are considered a valid command word.
- If the SCLK counter is < 32, it's considered a short data transfer frame, where the data write operation is invalid, but the output data bits on SDO-x pins are still valid.
- If the SCLK counter is > 32, it's considered a long data transfer frame. There's no restriction on the maximum number of clocks within any frame, but the last 32 bits before the CONVST/$\overline{CS}$ rising edge must constitute the desired command.

Input Command Word and Register Write Operation

Any data write operation to the device synchronizes with the external clock provided on the SCLK pin. The device allows either one byte or two bytes (equivalent to half a word) to be read or written during any device programming operation. The table below lists the input commands supported by the device, where commands associated with reading or writing two bytes in a single operation are suffixed as HWORD.

For any HWORD command, the LSB of the 9-bit address is always ignored and considered as 0b. For instance, regardless of whether address 04h or 05h is specified for any particular HWORD command, the device always executes the command on address 04h.

Table 5. List of Input Commands

OPCODE B[31:0]	COMMAND ACRONYM	COMMAND DESCRIPTION
00000000_000000000_ 00000000_00000000	NOP	No operation
11000_xx_<9-bit address>_ <16-bit data> (1)	CLEAR_HWORD	• Command used to clear any (or a group of) bits of a register. • Any bit marked 1 in the data field results in that particular bit of the specified register being reset to 0, leaving the other bits unchanged. • Half-word command (that is, the command functions on 16 bits at a time). • LSB of the 9-bit address is always ignored and considered as 0b.(2)
11001_xx_<9-bit address>_ 00000000_00000000	READ_HWORD	• Command used to perform a 16-bit read operation. • Half-word command (that is, the device outputs 16 bits of register data at a time). • LSB of the 9-bit address is always ignored and considered as 0b. • Upon receiving this command, the device sends out 16 bits of the register in the next frame.
01001_xx_<9-bit address>_ 00000000_00000000	READ	• Same as the READ_HWORD except that only eight bits of the register (byte read) are returned in the next frame.
11010_00_<9-bit address>_ <16-bit data>	WRITE	• Half-word write command (two bytes of input data are written into the specified address). • LSB of the 9-bit address is always ignored and considered as 0b.
11010_01_<9-bit address>_ <16-bit data>		• Half-word write command.

OPCODE B[31:0]	COMMAND ACRONYM	COMMAND DESCRIPTION
		• LSB of the 9-bit address is always ignored and considered as 0b. • With this command, only the MS byte of the 16-bit data word is written at the specified register address. The LS byte is ignored.
11010_10_<9-bit address>_ <16-bit data>		• Half-word write command. • LSB of the 9-bit address is always ignored and considered as 0b. • With this command, only the LS byte of the 16-bit data word is written at the specified register address. The MS byte is ignored.
11011_xx_<9-bit address>_ <16-bit data>	SET_HWORD	• Command used to set any (or a group of) bits of a register. • Any bit marked 1 in the data field results in that particular bit of the specified register being set to 1, leaving the other bits unchanged. • Half-word command (that is, the command functions on 16 bits at a time). • LSB of the 9-bit address is always ignored and considered as 0b.
All other input command combinations	NOP	No operation

(1) <9-bit address> is realized by adding a 0 at the MSB location followed by an 8-bit register address. The <9-bit address> for register 0x04h is 0x0-0000-0100b.

(2) An HWORD command operates on a set of 16 bits in the register map that is usually identified as two registers of eight bits each. For example, the command 11000_xx_<0_0000_0101><16-bit data> is treated the same as the command 11000_xx_<0_0000_0100><16- bit data> for bits 15:0 of the RST_PWRCTL_REG register.

All input commands listed in the table, including CLEAR_HWORD, WRITE, and SET_HWORD commands used to configure internal registers, must be 32 bits long. When provided in a particular data frame F, these commands get executed at the rising edge of the CONVST/$\overline{CS}$ signal.

Output Data Word

During any data transfer frame, the data read from the device can be synchronized either to the external clock on the SCLK pin or to an internal clock of the device, depending on the configuration of the internal registers.

In each data transfer frame, the contents of the internal output shift register are shifted out on the SDO-x pins. The output data for the subsequent frame (F+1) depends on the command issued in the current frame (F) and the status of the DATA_VAL[2:0] bits as follows:

- If the DATA_VAL[2:0] bits in the DATAOUT_CTL_REG register are set to 1xxb, the output data word for frame (F+1) contains a fixed data pattern specified in the DATAOUT_CTL_REG register.
- If a valid READ command is issued in frame F, the output data word for frame (F+1) contains 8-bit register data followed by 0's.
- If a valid READ_HWORD command is issued in frame F, the output data word for frame (F+1) contains 16-bit register data followed by 0's.
- For all other combinations, the output data word for frame (F+1) contains the latest 16-bit conversion result. Program the DATAOUT_CTL_REG register to append various data flags to the conversion result in the following sequence:
  1. Append DEVICE_ADDR[3:0] bits if the DEVICE_ADDR_INCL bit is set to 1.
  2. Append ADC INPUT RANGE FLAGS if the RANGE_INCL bit is set to 1.
  3. Append AVDD ALARM FLAGS if the VDD_ACTIVE_ALARM_INCL bit is set to 1.
  4. Append INPUT ALARM FLAGS if the IN_ACTIVE_ALARM_INCL bit is set to 1.
  5. Append PARITY bits if the PAR_EN bit is set to 1.
  6. Set all remaining bits in the 32-bit output data word to 0.

Table 6. Output Data Word with All Data Flags Enabled

DEVICE_ADDR_INCL = 1b, VDD_ACTIVE_ALARM_INCL = 1b, IN_ACTIVE_ALARM_INCL = 1b, RANGE_INCL = 1b, and PAR_EN = 1b						
D[31:16]	D[15:12]	D[11:8]	D[7:6]	D[5:4]	D[3:2]	D[1:0]
Conversion result	Device address	ADC input range	AVDD alarm flags	Input alarm flags	Parity bits	00b

Table 7. Output Data Word with Only Some Data Flags Enabled

DEVICE_ADDR_INCL = 0b, VDD_ACTIVE_ALARM_INCL = 1b, IN_ACTIVE_ALARM_INCL = 0b, RANGE_INCL = 1b, and PAR_EN = 1b				
D[31:16]	D[15:12]	D[11:10]	D[9:8]	D[7:0]
Conversion result	ADC input range	AVDD alarm flags	Parity bits	00000000b

Data Transfer Protocols

The multiSPI interface of the device is designed to offer greater flexibility by allowing the host controller to operate at slower SCLK speeds while still maintaining the required cycle time for operations.

- For any data write operation, the host controller can use any of the four legacy SPI-compatible protocols to configure the device. These protocols provide flexibility in how the host communicates with the device, allowing for compatibility with various existing SPI setups.
- For any data read operation from the device, the multiSPI interface module offers the following options:
  - Legacy, SPI-compatible protocol with a single SDO-x
  - Legacy, SPI-compatible protocol with dual SDO-x
  - ADC controller clock or source-synchronous (SRC) protocol for data transfer

Protocols for Configuring the Device

As described in the table below, the host controller can use any of the four legacy, SPI-compatible protocols (SPI-00-S, SPI-01-S, SPI-10-S, or SPI-11-S) to write data into the device.

PROTOCOL	SCLK POLARITY (At $\overline{CS}$ Falling Edge)	SCLK PHASE (Capture Edge)	SDI_CTL_REG	SDO_CTL_REG	DIAGRAM
SPI-00-S	Low	Rising	00h	00h	Figure 28
SPI-01-S	Low	Falling	01h	00h	Figure 28
SPI-10-S	High	Falling	02h	00h	Figure 28
SPI-11-S	High	Rising	03h	00h	Figure 28

On power-up or after coming out of any asynchronous reset, the device defaults to using the SPI-00-S protocol for both data read and data write operations. To select a different SPI-compatible protocol, the host controller must program the SDI_MODE[1:0] bits in the SDI_CNTL_REG register. However, the first write operation after power-up or reset must be performed using the SPI-00-S protocol. Once the first operation has been completed, any subsequent data transfer frames can follow the newly selected SPI protocol, as determined by the configuration of the SDI_MODE[1:0] bits. The selected protocol applies to both read and write operations.

The figures below show the details of four protocols using an optimal data frame. It should be noted that a valid write operation to the device requires a minimum of 32 SCLKs to be provided within a data transfer frame.

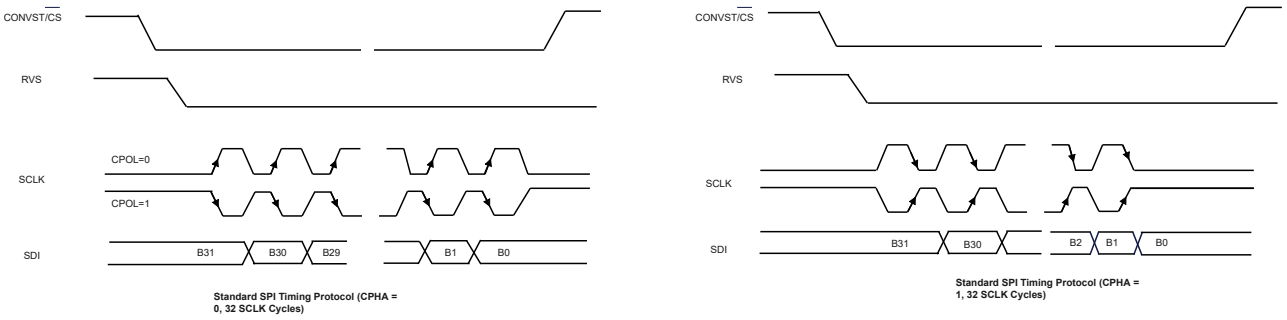


Figure 28. Standard SPI Timing Protocol

Protocols for Reading from the Device

The protocols for the data read operation can be broadly classified into three categories:

- Legacy, SPI-compatible protocols with a single SDO-x
- Legacy, SPI-compatible protocols with dual SDO-x
- ADC controller clock or source-synchronous (SRC) protocol for data transfer

Legacy, SPI-Compatible (SYS-xy-S) Protocols with a Single SDO-x

The host controller can use any of the four legacy, SPI-compatible protocols (SPI-00-S, SPI-01-S, SPI-10-S, or SPI-11-S) to read data from the device.

PROTOCOL	SCLK POLARITY (At $\overline{CS}$ Falling Edge)	SCLK PHASE (Capture Edge)	MSB BIT LAUNCH EDGE	SDI_CTL_REG	SDO_CTL_REG	DIAGRAM
SPI-00-S	Low	Rising	$\overline{CS}$ falling	00h	00h	Figure 29
SPI-01-S	Low	Falling	1st SCLK rising	01h	00h	Figure 29
SPI-10-S	High	Falling	$\overline{CS}$ falling	02h	00h	Figure 29
SPI-11-S	High	Rising	1st SCLK falling	03h	00h	Figure 29

To select a different SPI-compatible protocol for both data read and write operations, the device defaults to the SPI-00-S protocol on power-up or after an asynchronous reset. To change the protocol, configure the SDI_MODE[1:0] bits in the SDI_CNTL_REG register. The first data transfer operation must use the SPI-00-S protocol. After this first write operation, the selected protocol takes effect, and subsequent data transfer frames will follow the newly selected protocol. The protocol configuration applies to both data read and write operations.

- Program the SDI_MODE[1:0] bits in the SDI_CTL_REG register. The first write operation must adhere to the SPI-00-S protocol. Any subsequent data transfer frames must adhere to the newly selected protocol.
- Set the SDO_MODE[1:0] bits = 00b in the SDO_CTL_REG register.

When using any of the SPI-compatible protocols, the RVS output remains low throughout the data transfer frame. Figures below shows the details of the four protocols. The host controller can choose a short data transfer frame to optimize the communication with the device. By using a short frame, the host can read only the required number of MSBs (Most Significant Bits) from the 32-bit output data word.

When the host controller uses a long data transfer frame with SDO_CNTL_REG[7:0] = 00h, the device operates in daisy-chain mode.

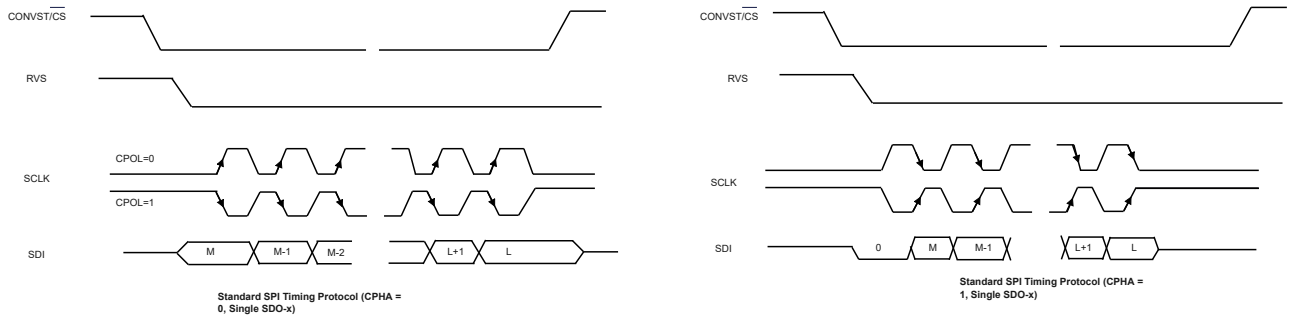


Figure 29. Standard SPI Timing Protocol with a Single SDO-x

Legacy, SPI-Compatible (SYS-xy-S) Protocols with Dual SDO-x

The device allows for increasing the SDO-x bus width from one bit to two bits in dual SDO mode, activated by setting the SDO1_CONFIG[1:0] bits in the SDO_CTL_REG register to 11b, with the ALARM/SDO-1/GPO pin functioning as SDO-1.

Figure below shows that in dual SDO mode, two bits of data are launched on the two SDO-x pins (SDO-0 and SDO-1) on every SCLK launch edge.

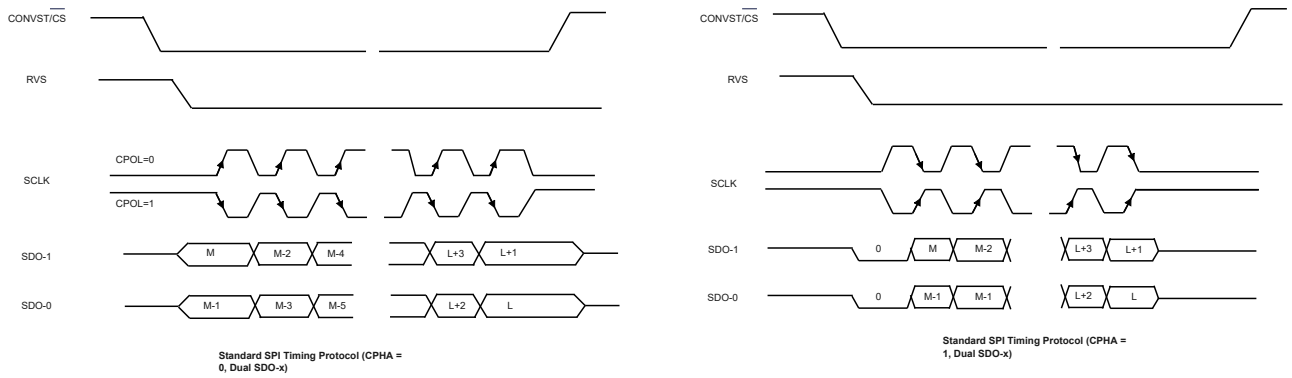


Figure 30. Standard SPI Timing Protocol with Dual SDO-x

Source-Synchronous (SRC) Protocols

The multiSPI interface supports an ADC controller clock or source-synchronous mode, where the device provides an output clock synchronized with the output data, and the host controller can select the output clock source and data bus width; in all SRC modes, the RVS pin outputs the clock synchronized with the data.

The SRC protocol enables configuration of the clock source (internal or external) and the output bus width, similar to the SPI protocols.

Output Clock Source Options

The device allows the output clock on the RVS pin to be synchronous to either the external clock provided on the SCLK pin or the internal clock, which is selected via the SSYNC_CLK bit in the SDO_CTL_REG register. Timing diagrams and specifications for both external and internal clock modes in the SRC protocol are provided in the relevant figures and tables.

Output Bus Width Options

The device can increase the SDO-x bus width from one bit (default) to two bits (dual SDO-x) when using SRC protocols. To enable dual SDO mode, the SDO1_CONFIG[1:0] bits in the SDO_CTL_REG register must be set to 11b, and in this mode, the ALARM/SDO-1/GPO pin will function as SDO-1.

CRC on Data Interface

The TPAFE51716S features a cyclic redundancy check (CRC) module for checking the integrity of the data bits exchanged over the SPI interface. The CRC module is bidirectional, which appends an 8-bit CRC to every byte read from the device and also evaluates the CRC of every incoming byte over the SPI interface. The CRC module uses the CRC-8-CCITT polynomial ($x^8 + x^2 + x + 1$) for CRC computation.

To enable the CRC module, set the CRC_EN bit in the CRC_CFG register. When the TPAFE51716S detects a CRC error on the SPI interface, the CRC_ERROR bit is set.

The device appends an 8-bit CRC to the output data packet when the CRC module is enabled.

The host must compute and append the appropriate 8-bit CRC to the command string in the same SPI frame. When implementing the CRC calculation, the initial value of CRC8 is set to 0. Using the polynomial mentioned above, perform the CRC calculation sequentially on valid command[31:24], valid command[23:16], valid command[15:8], and valid command[7:0]. The result of each CRC calculation is used as the initial value for the next CRC calculation. After four rounds of CRC calculation, the final CRC checksum is obtained. The CRC checker will compare this checksum with the 8-bit CRC received from the SDI.

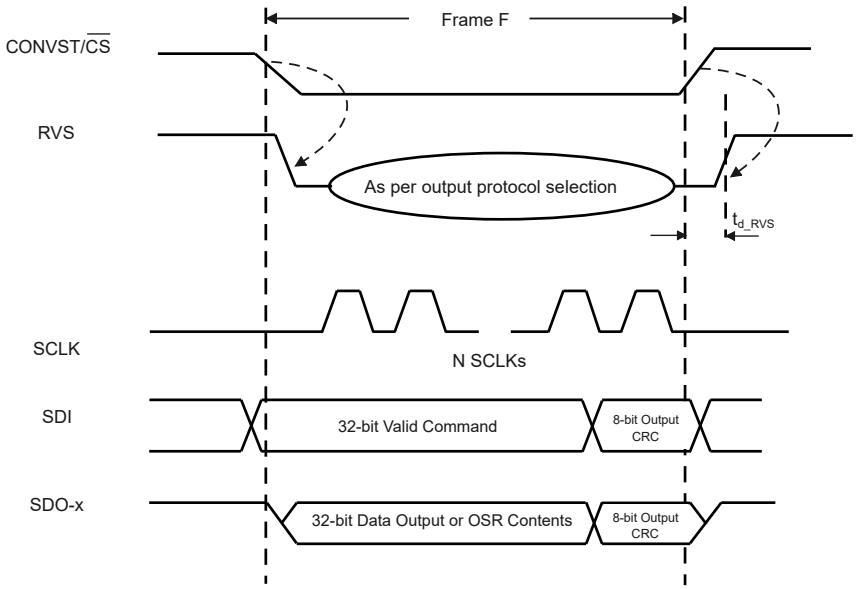


Figure 31. Data Transfer Frame with CRC Enabled

Register Maps

Device Configuration and Register Maps

Device Configuration and Register Maps

The configuration registers of the device are mapped as described below. Each configuration register is comprised of four registers, each containing a data byte.

Table 8. Configuration Registers Mapping

Address	Register Name	Register Functions
00h	DEVICE_ID_REG	Device ID register
04h	RST_PWRCTL_REG	Reset and power control register
08h	SDI_CTL_REG	SDI data input control register
0Ch	SDO_CTL_REG	SDO-x data input control register
10h	DATAOUT_CTL_REG	Output data control register
14h	RANGE_SEL_REG	Input range selection control register
20h	ALARM_REG	ALARM output register
24h	ALARM_H_TH_REG	ALARM high threshold and hysteresis register
26h	ALARM_HYST_REG	Hystersis control register
28h	ALARM_L_TH_REG	ALARM low threshold register
30h	OPEN_DETECT	Open circuit detection register
32h	OPEN_DETECT_ADC_CODE	Open detection ADC code register
34h	BW_CTRL	PGA bandwidth control register
38h	CRC_CFG	CRC register

DEVICE_ID_REG Register

DEVICE_ID_REG Register (address = 00h)

This register stores the unique identification numbers assigned to a device when it is part of a daisy-chain configuration involving multiple devices.

Address for bits 7-0 = 00h Address for bits 15-8 = 01h Address for bits 23-16 = 02h Address for bits 31-24 = 03h

Table 9. DEVICE_ID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Reserved	R	00h	Reserved. Reads return 00h.
23-20	Reserved	R	0000b	Reserved. Reads return 0000b.
19-16	DEVICE_ADDR[3:0]	R/W	0000b	These bits can be used to identify up to 16 different devices in a system.
15-0	Reserved	R	0000h	Reserved. Reads return 0000h.

RST_PWRCTL_REG Register

RST_PWRCTL_REG Register (address = 04h)

This register manages the reset and power-down functionalities provided by the converter. Before performing any write operation to the RST_PWRCTL_REG register, a preceding write operation must be executed with the register address set to 05h and the register data set to 69h.

Address for bits 7-0 = 04h Address for bits 15-8 = 05h Address for bits 23-16 = 06h Address for bits 31-24 = 07h

Table 10. RST_PWRCTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0000h	Reserved. Reads return 0000h.
15-8	WKEY[7:0]	R/W	00h	This value functions as a protection key to enable writes to bits 5-0. Bits are written only if WKEY is set to 69h first.
7-6	Reserved	R	00b	Reserved. Reads return 00b
5	VDD_AL_DIS	R/W	0b	0b = VDD alarm is enabled 1b = VDD alarm is disabled
4	IN_AL_DIS	R/W	0b	0b = Input alarm is enabled 1b = Input alarm is disabled
3	Reserved	R	0b	Reserved. Reads return 0h.
2	RSTn_APP (1)	R/W	0b	0b = RST pin functions as a POR class reset (causes full device initialization) 1b = RST pin functions as an application reset (only user-programmed modes are cleared)
1	NAP_EN (2)	R/W	0b	0b = Disables the NAP mode of the converter 1b = Enables the converter to enter NAP mode if CONVST/$\overline{CS}$ is held high after the current conversion completes
0	PWRDN (2)	R/W	0b	0b = Puts the converter into active mode 1b = Puts the converter into power-down mode

(1) Setting this bit forces the $\overline{RST}$ pin to function as an application reset until the next power cycle.
(2) See the electrical characteristic table for details on the latency encountered when entering and exiting the associated low-power mode.

SDI_CTL_REG Register

SDI_CTL_REG Register (address = 08h)

This register configures the protocol used for writing data to the device.

Address for bits 7-0 = 08h Address for bits 15-8 = 09h Address for bits 23-16 = 0Ah Address for bits 31-24 = 0Bh

Table 11. SDI_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0000h	Reserved. Reads return 0000h.
15-8	Reserved	R	00h	Reserved. Reads return 00h.
7-2	Reserved	R	000000b	Reserved. Reads return 000000b.
1-0	SDI_MODE[1:0]	R/W	00b	These bits select the protocol for reading from or writing to the device. 00b = Standard SPI with CPOL = 0 and CPHASE = 0 01b = Standard SPI with CPOL = 0 and CPHASE = 1 10b = Standard SPI with CPOL = 1 and CPHASE = 0 11b = Standard SPI with CPOL = 1 and CPHASE = 1

SDO_CTL_REG Register

SDO_CTL_REG Register (address = 0Ch)

This register controls the data protocol used to transmit data out from the SDO-x pins of the device.

Address for bits 7-0 = 0Ch Address for bits 15-8 = 0Dh Address for bits 23-16 = 0Eh Address for bits 31-24 = 0Fh

Table 12. SDO_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0000h	Reserved. Reads return 0h.
15-13	Reserved	R	000b	Reserved. Reads return 000b.
12	GPO_VAL	R/W	0b	1-bit value for the output on the GPO pin.
11-10	Reserved	R	00b	Reserved. Reads return 00b.
9-8	SDO1_CONFIG[1:0]	R/W	00b	Two bits are used to configure ALARM/SDO-1/GPO: 00b = SDO-1 is always tri-stated; 1-bit SDO mode 01b = SDO-1 functions as ALARM; 1-bit SDO mode 10b = SDO-1 functions as GPO; 1-bit SDO mode 11b = SDO-1 combined with SDO-0 offers a 2-bit SDO mode
7	Reserved	R	0b	Reserved. Reads return 0b.
6	SSYNC_CLK (1)	R/W	0b	This bit controls the source of the clock selected for source-synchronous transmission. 0b = External SCLK (no division) 1b = Internal clock (no division)
5-2	Reserved	R	0000b	Reserved. Reads return 0000b.
1-0	SDO_MODE[1:0]	R/W	00b	These bits control the data output modes of the device. 0xb = SDO mode follows the same SPI protocol as that used for SDI; see the SDI_CTL_REG register 10b = Invalid configuration 11b = SDO mode follows the ADC controller clock or source-synchronous protocol

(1) This bit takes effect only in the ADC controller clock or source-synchronous mode of operation.

DATAOUT_CTL_REG Register

DATAOUT_CTL_REG Register (address = 10h)

This register controls the data output by the device.

Address for bits 7-0 = 10h Address for bits 15-8 = 11h Address for bits 23-16 = 12h Address for bits 31-24 = 13h

Table 13. DATAOUT_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0000h	Reserved. Reads return 0000h.
15	Reserved	R	0b	Reserved. Reads return 0b.
14	DEVICE_ADDR_INCL	R/W	0b	Control to include the 4-bit DEVICE_ADDR register value in the SDO-x output bit stream. 0b = Do not include the register value 1b = Include the register value
13-12	VDD_ACTIVE_ALARM_INCL[1:0]	R/W	00b	Control to include the active VDD ALARM flags in the SDO-x output bit stream. 00b = Do not include 01b = Include ACTIVE_VDD_H_FLAG 10b = Include ACTIVE_VDD_L_FLAG s 11b = Include both flag
11-10	IN_ACTIVE_ALARM_INCL[1:0]	R/W	00b	Control to include the active input ALARM flags in the SDO-x output bit stream. 00b = Do not include 01b = Include ACTIVE_IN_H_FLAG 10b = Include ACTIVE_IN_L_FLAG s 11b = Include both flag
9	Reserved	R	0b	Reserved. Reads return 0h.
8	RANGE_INCL	R/W	0b	Control to include the 4-bit input range setting in the SDO-x output bit stream. 0b = Do not include the range configuration register value

Bit	Field	Type	Reset	Description
				1b = Include the range configuration register value
7-4	Reserved	R	0000b	Reserved. Reads return 0000b.
3	PAR_EN (1)	R/W	0b	0b = Output data does not contain parity information 1b = Two parity bits (ADC output and output data frame) are appended to the LSBs of the output data. The ADC output parity bit reflects an even parity for the ADC output bits only. The output data frame parity bit reflects an even parity signature for the entire output data frame, including the ADC output bits and any internal flags or register settings. The ADC output parity bit is not included in the frame parity bit computation.

(1) Setting this bit increases the length of the output data by two bits.

RANGE_SEL_REG Register

RANGE_SEL_REG Register (address = 14h)

This register controls the configuration of the internal reference and input voltage ranges for the converter.

Address for bits 7-0 = 14h Address for bits 15-8 = 15h Address for bits 23-16 = 16h Address for bits 31-24 = 17h

Table 14. RANGE_SEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0000h	Reserved. Reads return 0000h.
15-8	Reserved	R	00h	Reserved. Reads return 00h.
7	Reserved	R	0b	Reserved. Reads return 0b.
6	INTREF_DIS	R/W	0b	Control to disable the ADC internal reference. 0b = Internal reference is enabled 1b = Internal reference is disabled
5-4	Reserved	R	00b	Reserved. Reads return 00b.
3-0	RANGE_SEL[3:0]	R/W	0000b	These bits comprise the 4-bit register that selects the nine input ranges of the ADC. 0000b = ±3 × V_{REF} 0001b = ±2.5 × V_{REF} 0010b = ±1.5 × V_{REF} 0011b = ±1.25 × V_{REF} 0100b = ±0.625 × V_{REF} 0101b = ±0.75 × V_{REF} 0110b = Differential ±3 × V_{REF} 0111b = Differential ±2.5 × V_{REF} 1000b = 3 × V_{REF} 1001b = 2.5 × V_{REF}

Bit	Field	Type	Reset	Description
				1010b = 1.5 × V_{REF} 1011b = 1.25 × V_{REF} 1100b = Differential ±1.5 × V_{REF} 1101b = Differential ±1.25 × V_{REF} 1110b = Differential ±0.75 × V_{REF} 1111b = Differential ±0.625 × V_{REF}

ALARM_REG Register

ALARM_REG Register (address = 20h)

This register contains the output alarm flags (active and tripped) for the input and AVDD alarm.

Address for bits 7-0 = 20h Address for bits 15-8 = 21h Address for bits 23-16 = 22h Address for bits 31-24 = 23h

Table 15. ALARM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0000h	Reserved. Reads return 0000h.
15	ACTIVE_VDD_L_FLAG	R	0b	Active ALARM output flag for low AVDD voltage. 0b = No ALARM condition 1b = ALARM condition exists
14	ACTIVE_VDD_H_FLAG	R	0b	Active ALARM output flag for high AVDD voltage. 0b = No ALARM condition 1b = ALARM condition exists
13-12	Reserved	R	00b	Reserved. Reads return 00b.
11	ACTIVE_IN_L_FLAG	R	0b	Active ALARM output flag for low input voltage. 0b = No ALARM condition 1b = ALARM condition exists
10	ACTIVE_IN_H_FLAG	R	0b	Active ALARM output flag for high input voltage. 0b = No ALARM condition 1b = ALARM condition exists
9-8	Reserved	R	00b	Reserved. Reads return 00b.
7	TRP_VDD_L_FLAG	R	0b	Tripped ALARM output flag for low AVDD voltage. 0b = No ALARM condition 1b = ALARM condition exists

Bit	Field	Type	Reset	Description
6	TRP_VDD_H_FLAG	R	0b	Tripped ALARM output flag for high AVDD voltage. 0b = No ALARM condition 1b = ALARM condition exists
5	TRP_IN_L_FLAG	R	0b	Tripped ALARM output flag for low input voltage. 0b = No ALARM condition 1b = ALARM condition exists
4	TRP_IN_H_FLAG	R	0b	Tripped ALARM output flag for high input voltage. 0b = No ALARM condition 1b = ALARM condition exists
3-1	Reserved	R	000b	Reserved. Reads return 000b.
0	OVW_ALARM	R	0b	Logical OR outputs all tripped ALARM flags. 0b = No ALARM condition 1b = ALARM condition exists

ALARM_H_TH_REG Register

ALARM_H_TH_REG Register (address = 24h)

This register controls hysteresis and a high threshold for the input alarm and AVDD alarm.

Address for bits 7-0 = 24h Address for bits 15-8 = 25h Address for bits 23-16 = 26h Address for bits 31-24 = 27h

Table 16. ALARM_H_TH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	INP_ALRM_HYST[7:0]	R/W	00h	INP_ALRM_HYST[7:2]: 6-bit hysteresis value for the input ALARM. INP_ALRM_HYST[1:0] must be set to 00b.
23-16	AVDD_H_ALARM_TH[7:0]	R/W	00h	AVDD high alarm threshold. x0h = 5.3 V x1h = 5.5 V
15-0	INP_ALRM_HIGH_TH[15:0]	R/W	FFFFh	Threshold for comparison is INP_ALRM_HIGH_TH[15:0].

ALARM_L_TH_REG Register

ALARM_L_TH_REG Register (address = 28h)

This register controls the low threshold for the input alarm.

Address for bits 7-0 = 28h Address for bits 15-8 = 29h Address for bits 23-16 = 2Ah Address for bits 31-24 = 2Bh

Table 17. ALARM_L_TH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
32-16	Reserved	R	0000h	Reserved. Reads return 0000h.
15-0	INP_ALRM_LOW_TH[15:0]	R/W	0000h	Threshold for comparison is INP_ALRM_LOW_TH[15:0].

OPEN_DETECT Register

OPEN_DETECT Register (address = 30h)

This register configures open detection parameters.

Address for bits 7-0 = 30h Address for bits 15-8 = 31h

Table 18. OPEN_DETECT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	OPEN_DETECT_QUEUE	R/W	00h	Open detection queue. When set to 0, open detect is disabled. When set to 1, open detect is configured in manual mode. When set to >1, open detect operates in automatic mode and the value set in this register specifies the number of conversions when there is no change in output code before the PGA common mode is switched.
7-6	Reserved	R	0h	Reserved
5	OPEN_STS	R	0b	0b = No open circuit detected 1b = Open circuit detected
4	Reserved	R	0h	Reserved
3-1	OPEN_DETECT_H_VCM_SEL	R/W	6h	Select the VCM high voltage of open circuit detection 000b = VCM is 2.5V 001b = VCM is 2.6V 010b = VCM is 2.7V 011b = VCM is 2.8V 100b = VCM is 2.9V 101b = VCM is 3.0V 110b = VCM is 3.1V 111b = VCM is 3.3V
0	OPEN_DETECT_EN	R/W	0b	0b = Open detection is disabled 1b = in automatic mode, enable analog input open circuit detection. in manual mode, set the PGA common mode to high

OPEN_DETECT_ADC_CODE Register

OPEN_DETECT_ADC_CODE Register (address = 32h)

Automatic open detection mode open detection monitoring threshold.

Address for bits 7-0 = 32h Address for bits 15-8 = 33h

Table 19. ALARM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	Reserved	R	000h	Reserved. Reads return 000h.
5-0	OPEN_DETECT_ADC_CODE	R/W	00h	Open detection in automatic mode threshold. 0b = ADC code threshold is 350 LSB When set to other codes，threshold is [OPEN_DETECT_ADC_CODE, 00000000] = OPEN_DETECT_ADC_CODE*256. For example, when set to 6'h2, ADC_CODE=16'h=0200, that is 2*256=512 LSB.

BW_CTRL Register

BW_CTRL Register (address = 34h)

This register configures the analog bandwidth of PGA.

Address for bits 7-0 = 34h Address for bits 15-8 = 35h

Table 20. BW_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	Reserved	R	0000h	Reserved. Reads return 0000h.
1-0	BW_SEL	R/W	01b	PGA −3dB analog bandwidth. 00b = 33 kHz

Bit	Field	Type	Reset	Description
				01b = 16 kHz 10b = 376 kHz 11b = Reserved

CRC_CFG Register

CRC_CFG Register (address = 38h)

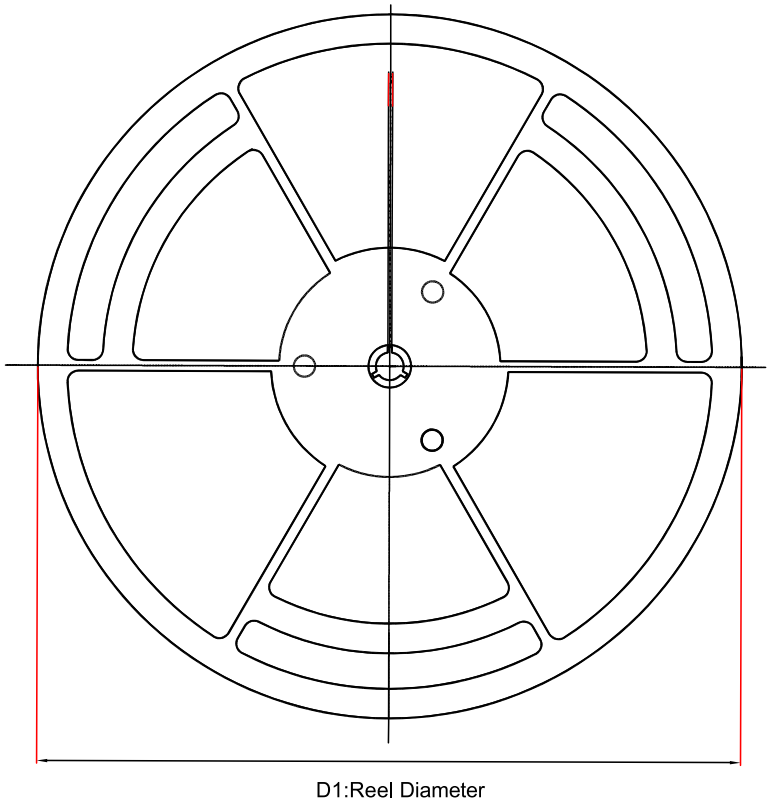
This register configures the CRC function.

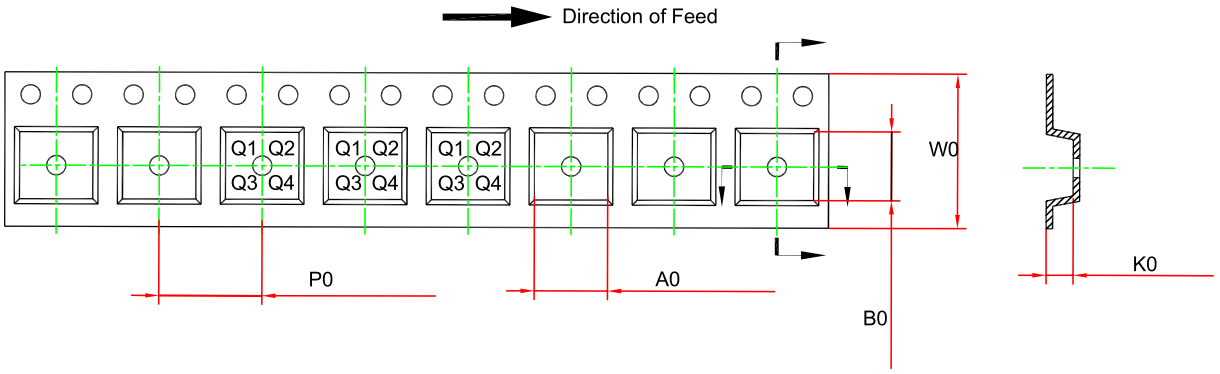
Address for bits 7-0 = 38h Address for bits 15-8 = 39h

Table 21. CRC_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	Reserved	R	00h	Reserved. Reads return 00h.
7	CRC_ERROR	R/W	0b	CRC error status. 0b = CRC pass 1b = CRC error detected
6-1	Reserved	R	00h	Reserved. Reads return 00h.
0	CRC_EN	R/W	00b	CRC function enable. 0b = CRC disabled 1b = CRC enabled

Tape and Reel Information



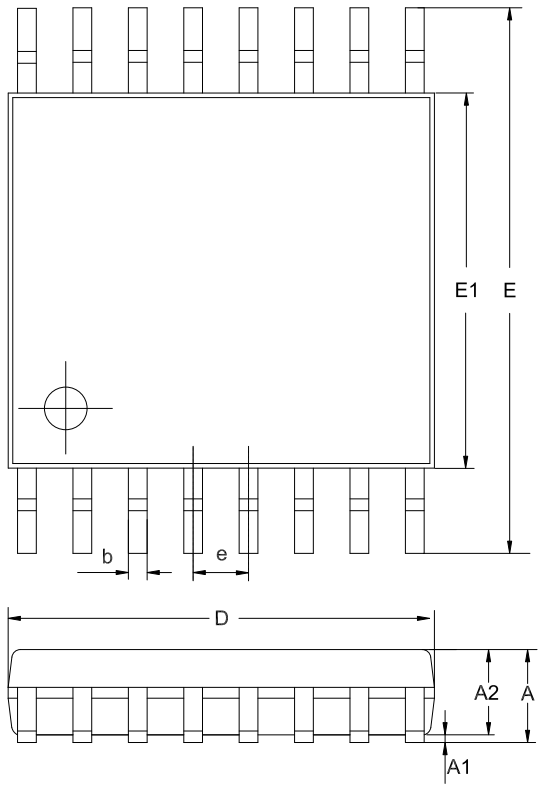


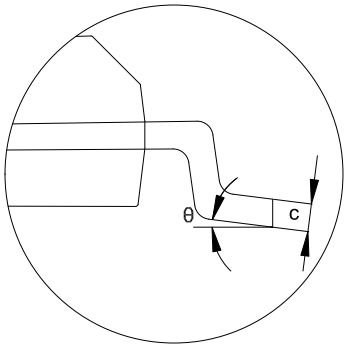
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPAFE51716S-TS3R	TSSOP16	330	17.6	6.8	5.5	1.5	8	12	Q1

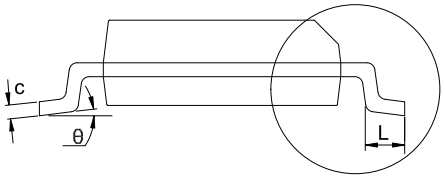
Package Outline Dimensions

TSSOP16

Package Outline Dimensions TS3(TSSOP-16-A)







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPAFE51716S-TS3R	−40 to 125°C	TSSOP16	51716S	3	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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